U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
1[a] A structure, comprising a	To the extent the preamble is limiting, the Samsung Accused Devices comprise structures. Broadly speaking, the Samsung Accused Devices are processors, such as the Exynos 7420, the Snapdragon 820,

[1] Discovery in this case is ongoing. Accordingly, Plaintiff expects that these contentions may be subject to supplementation and/or amendment after further discovery and disclosure of Defendants' non-infringement positions in order to focus the issues in this case. For example, Plaintiff may supplement these contentions in response to information learned during discovery to rebut allegations of non-infringement either literally or under the doctrine of equivalents. Additionally, Plaintiff expects that these contentions may be subject to amendment or supplementation to identify and accuse additional devices released, developed, or made available after the date on which these contentions are served.

[2] As described in more detail herein, the limitations recited in this chart are all met by processors (and the transistors thereon) that Samsung manufactures according to Samsung's 14 nm FinFET process technology, including Samsung's 14LPE and 14LPP processes. Samsung makes, uses, sells, offers for sale, imports, advertises, and/or markets these infringing processors. The infringing processors include Samsung Exynos processors (and the transistors thereon) manufactured by Samsung according to Samsung's 14 nm FinFET process technology, including the Samsung Exynos 7420, Samsung Exynos 7570, Samsung Exynos 7870, Samsung Exynos 7880, Samsung Exynos 7872, Samsung Exynos 7874, Samsung Exynos 7885, Samsung Exynos 8890, Samsung Exynos 7904, and Samsung Exynos 7270 processors. The infringing processors also include third-party processors (and the transistors thereon) manufactured by Samsung according to Samsung's 14 nm FinFET process technology, including A9 processors. The infringing processors, in turn, are incorporated into a wide range of Samsung and third party devices, including the Samsung Galaxy A40, Samsung Galaxy A30, Samsung Galaxy M30, Samsung Galaxy M20, Samsung Galaxy M10, Samsung Galaxy J2 Core, Samsung Galaxy On6, Samsung Galaxy J6, Samsung Galaxy J4, Samsung Galaxy A6, Samsung Galaxy On7 Prime, Samsung Galaxy A8, Samsung Galaxy A8+, Samsung Galaxy J7, Samsung Galaxy J5, Samsung Galaxy J3, Samsung Galaxy Xcover 4, Samsung Galaxy A7, Samsung Galaxy A5, Samsung Galaxy A3, Samsung Galaxy A8, Samsung Galaxy J7, Samsung Galaxy S7 Edge, Samsung Galaxy S7, Samsung Galaxy Note5, Samsung Galaxy S6 Edge+, Samsung Galaxy S6 Edge, Samsung Galaxy S6, Samsung Galaxy S6 Active, Samsung Galaxy Tab A10.1, Samsung Galaxy Tab Active 2, Samsung Galaxy J7 Duo, Samsung Galaxy Gear Sport, Samsung Galaxy Gear S3 Frontier, Samsung Galaxy Gear S3 Classic, Apple iPhone 6s, Apple iPhone 6s Plus, Xiaomi Mi 5, Alcatel Idol 4S Windows 10 mobile(6071W), ASUS ZenFone 3 Deluxe, Blackberry DTEK60, Gree Phone 2, Gree Phone 2 mini, HP Elite X3, HTC 10, Light L 16, LeEco (leTv) Le Max 2 X820, LeEco (LeTv) LeMax Pro X910, LeEco (LeTv) Le Pro 3 Elite, LeEco (LeTv) Max 3 X920, Lenovo ZUK Z2, Lenovo ZUK Z2 Pro, LG G5, LG Q8, LG V20, Moto Z, Moto Z Force, OnePlus 3, Qiku 360 Q5 Plus, Samsung Galaxy S7 Active, Samsung Galaxy Note 7, Samsung Galaxy Tab S3, Sharp Aquos Zeta SH-04H, Sharp Aquos XX3, Sony Xperia X Performance, Sony Xperia XZ, Sony Xperia XZS, TCL 950, Vertu Constellation, Vivo Xplay 5 Elite, Vivo Xplay 6, 8848 M4, Xiaomi Mi 5 Prime/Pro, ZTE Axon 7, ZTE Nubia Z11, Google Pixel, Google Pixel XL, Xiaomi Mi 5s, HTC U Ultra, ASUS ZenFone 3 Deluxe, Asus Zenfone AR, Asus Zenfone Ares,

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
semiconductor region in a substrate, a metal electrical contact to said semiconductor region, a metal oxide layer, and a passivating dielectric tunnel barrier layer between said semiconductor region and said metal electrical contact,	and the Apple A9, which are devices that use electrical energy to operate, and electronic devices incorporating those processors, such as the Galaxy S6, the LG G5, and the iPhone 6s. The below pictures depict, as an example, a teardown of a Galaxy S6 to reveal the Exynos 7420 processor therein, outlined in red.

Xiaomi Mi 5s Plus, Xiaomi Mi Note 2, Xiaomi Mi Mix, LeEco Le Pro 3, LeEco Cool Changer S1, Smartisan M1, Smartisan M1L, OnePlus 3T, Lenovo ZUK Edge, LG G6, LG G6+, LG G7 Fit, ZTE Axon 7s, ZTE Axon M, and Samsung Galaxy Note FE. The foregoing processors and devices incorporating those processors are the "Samsung Accused Devices."

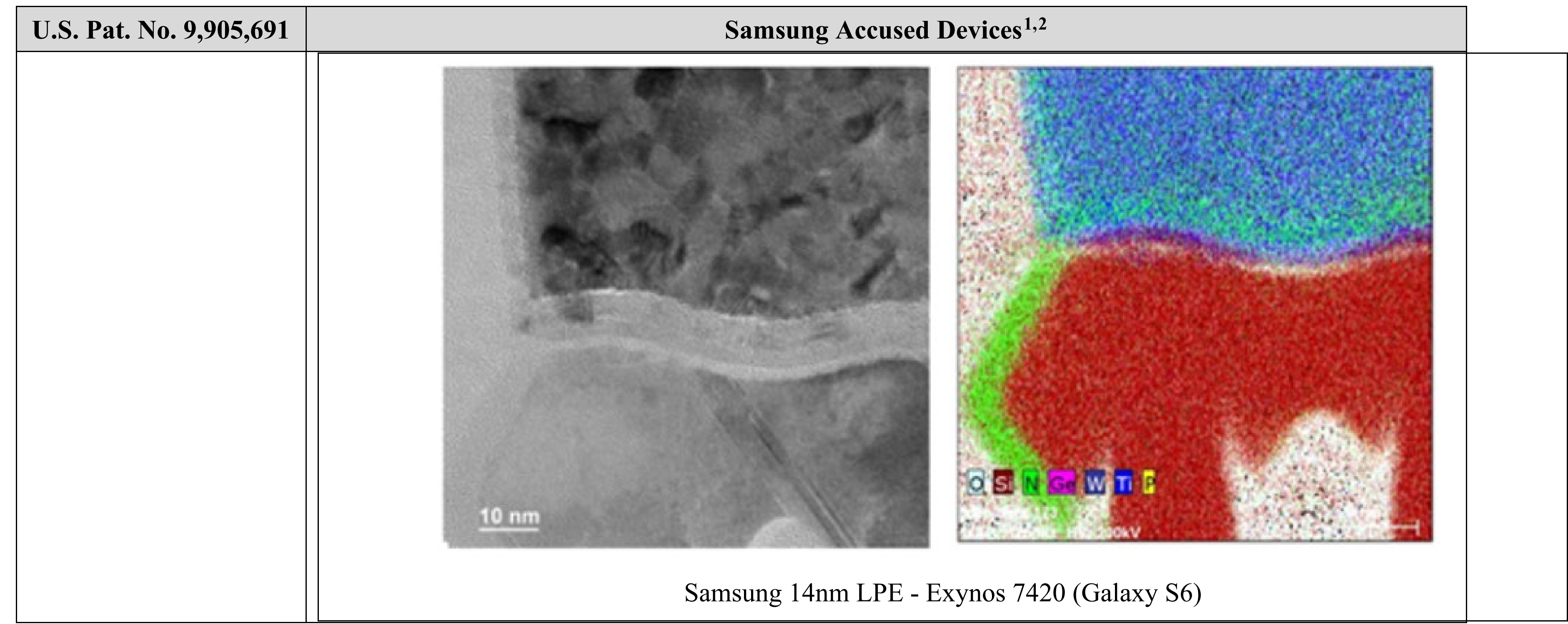
U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]

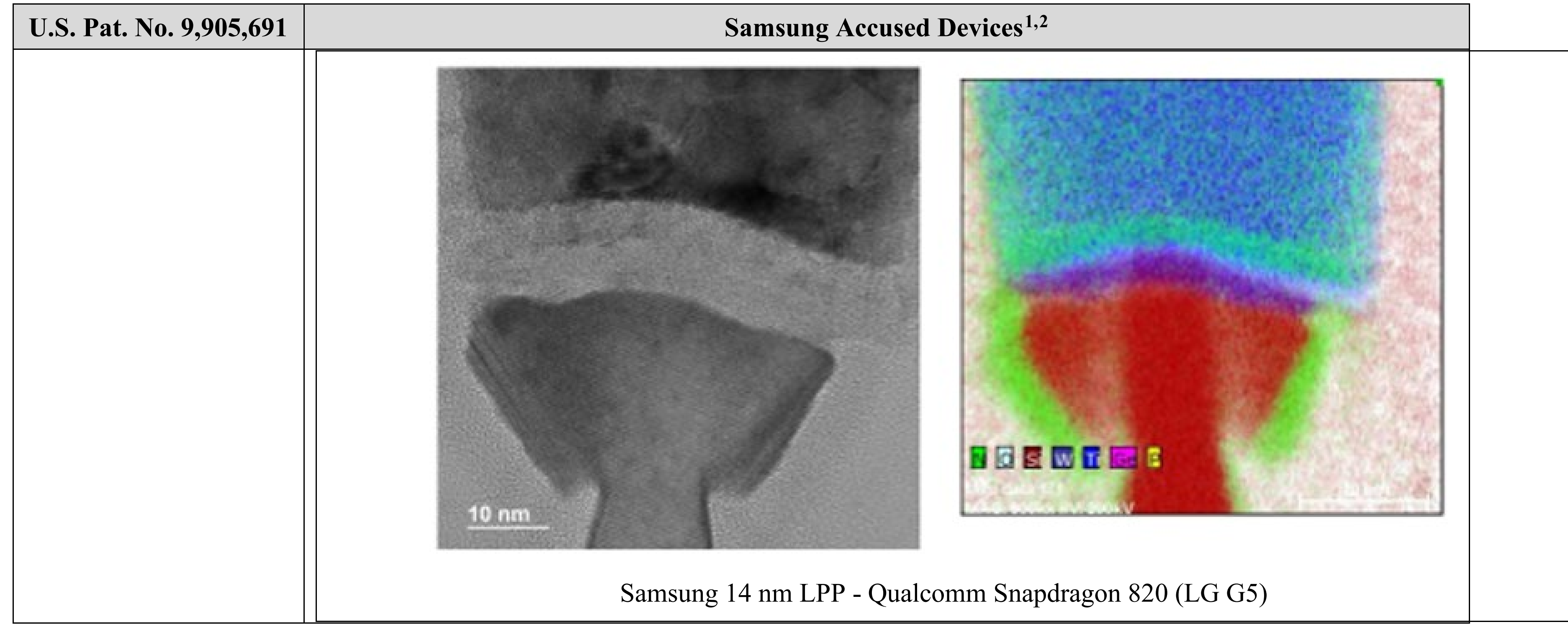
U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]

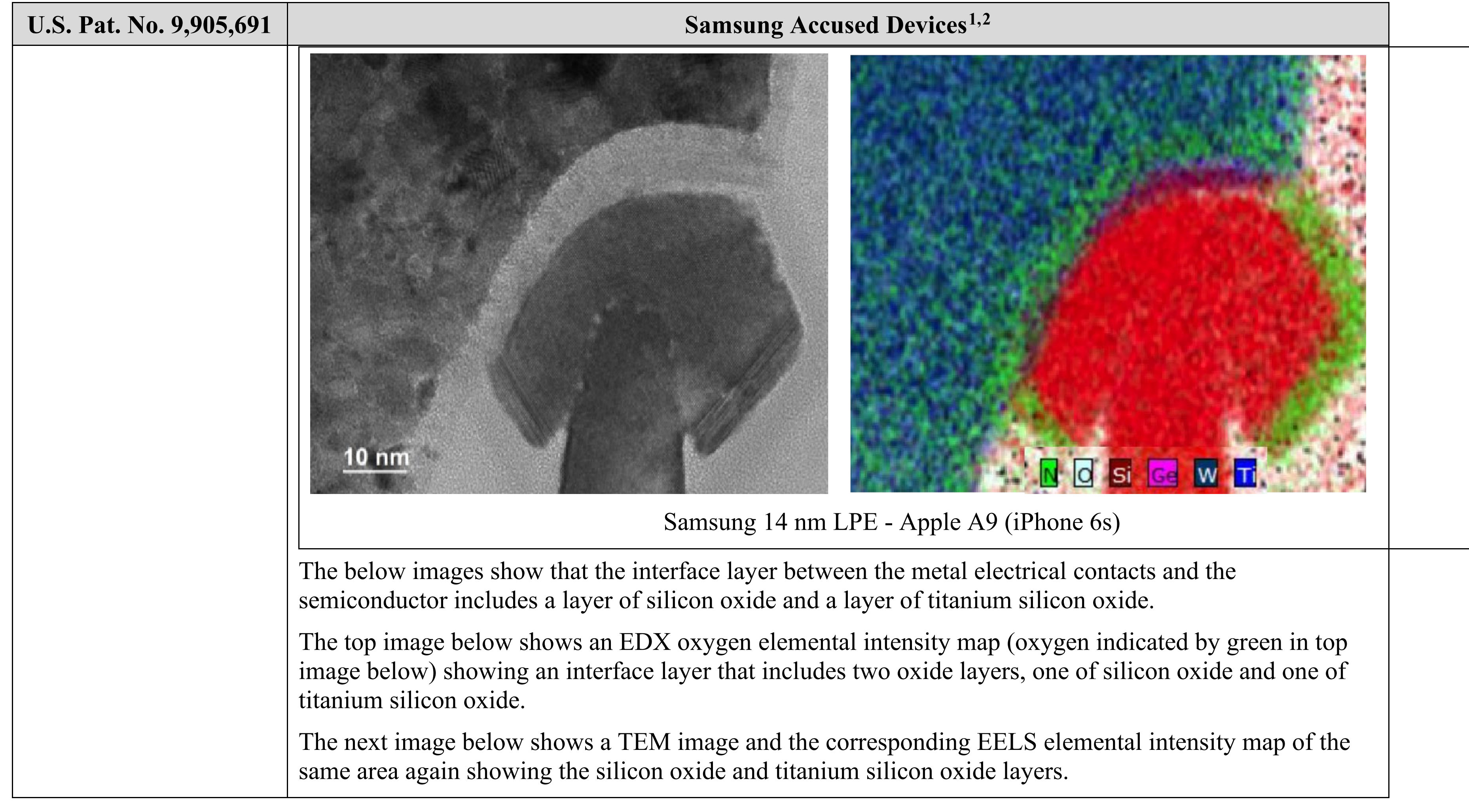
U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	See https://www.ifixit.com/Teardown/Samsung+Galaxy+S6+Teardown/39174 (last visited February 28, 2020). The Samsung Accused Devices include billions of FinFET transistors packed closely together and corresponding contacts, with junctions between the semiconductor of the transistors and the contacts that constitute junctions between a silicon-based semiconductor (at the source/drain region of the FinFET transistor) and a conductor (the corresponding metal electrical contact). Taking a random cross section from one Samsung accused processor reveals the following transmission electron microscope (TEM) image, which depicts the source/drain semiconductor region of two FinFET transistors (each of the transistors having four fins), their corresponding metal electrical contacts, and the junctions between them.

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	100 nm Samsung 14nm LPE - Exynos 7420 (Galaxy S6) The source/drain region of the FinFET transistor shown in the above image comprises a silicon-based semiconductor region in a silicon substrate. The corresponding metal contacts (including tungsten and titanium nitride) comprise metal electrical contacts to said semiconductor region. The interface between them includes layers of silicon oxide and titanium silicon oxide. The titanium silicon oxide layer comprises a metal oxide layer. The silicon oxide layer comprises a passivating dielectric tunnel barrier layer between said semiconductor region and said metal electrical contact. Silicon oxide (SiO) is a passivating material, as described by the specification and other sources. *See, e.g.,* '691 Patent, 8:54-58 ("the ***present inventors propose techniques for providing non-insulating, passivated semiconductor surfaces using*** materials other than nitrogen; ***for example, oxides,*** hydrides, arsenides and/or fluorides"); 9:63-10:2 ("Different passivation materials are contemplated. According to one embodiment, the interface layer 520 is formed using … oxygen (O) … (that is, the interface layer 520 may include … an oxide …)."), 10:8-10 ("***passivation layers made using*** N and/or ***O*** may not require distinct separation layers, as these elements ***may form a layer of a compound with Si*** …"); Kherani & Chowdhury, U.S. Patent Application 20130298984, para. 7

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	(silicon oxide (SiOx) is a passivating material). In addition, silicon oxide forms a dielectric tunnel barrier layer between the metal contact and the semiconductor. *See, e.g.,* '691 Patent, 17:41-52 ("both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide semiconductor junction) permit tunneling currents"; "The tunnel barrier presented by [conventional junctions] may be an order of magnitude thicker than ***the dielectric tunnel barrier in the present invention***."); Crafts & Schultz-Wittmann, U.S. Patent No. 9,966,481, Abstract & 9:12-13 ("The ***passivating dielectric layer*** is intentionally modified to allow direct contact, or ***tunnel barrier*** contact, with the substrate."; "122: Electrically passivating interface layer; Examples: silicon oxide"). The above elements, taken together, comprise a structure. The images below are zoomed-in TEM images of the junction between a FinFET source/drain region and the corresponding contact in various exemplary Samsung Accused Devices. The images on the left are close-up TEM images. The color images on the right are EDX elemental intensity maps showing that the source/drain is made of a silicon-based semiconductor and the contact area includes two conductors, tungsten (W) and titanium nitride (TiN).

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	 Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

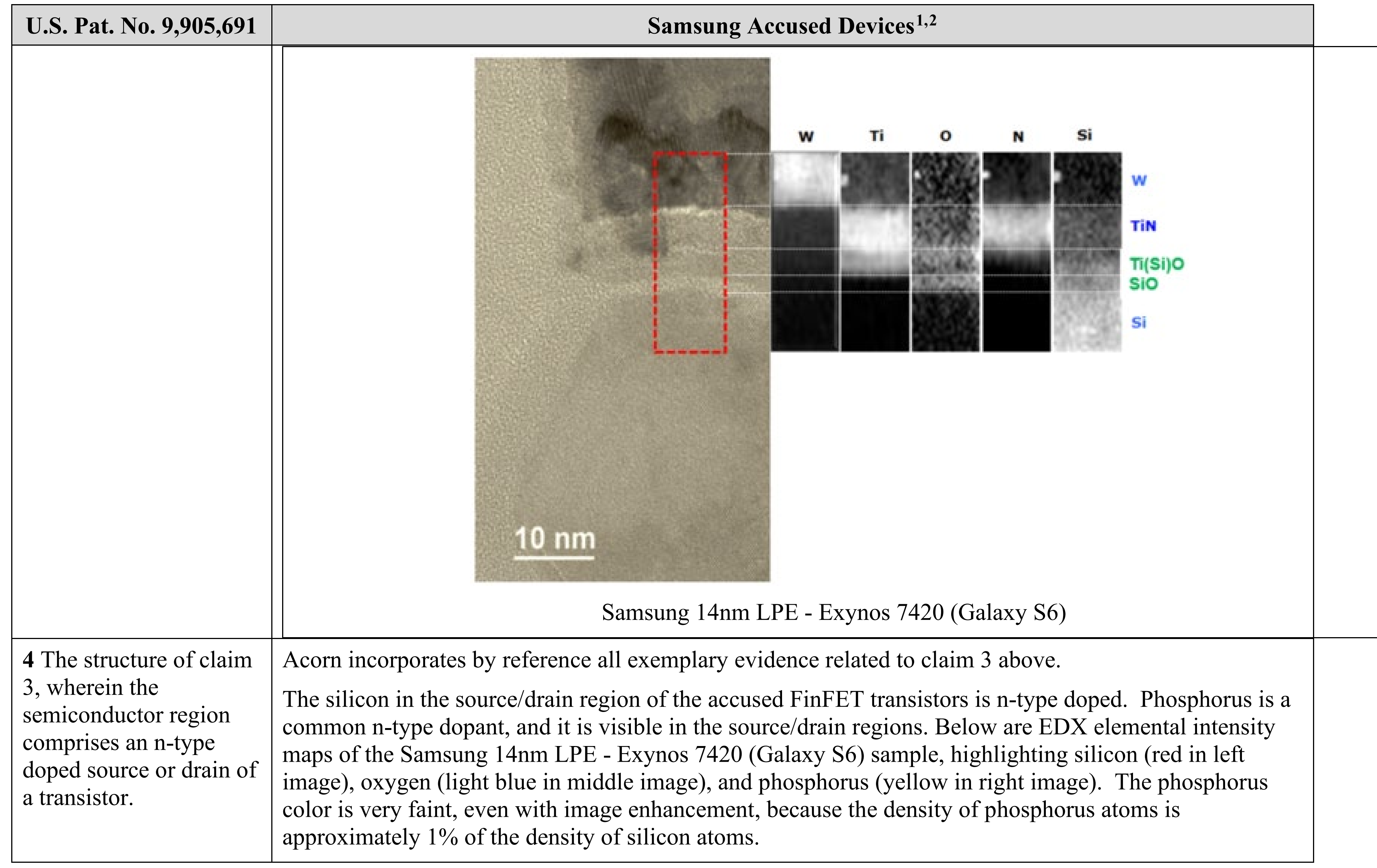
U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	 Samsung 14 nm LPP - Qualcomm Snapdragon 820 (LG G5)

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	 Samsung 14 nm LPE - Apple A9 (iPhone 6s) The below images show that the interface layer between the metal electrical contacts and the semiconductor includes a layer of silicon oxide and a layer of titanium silicon oxide. The top image below shows an EDX oxygen elemental intensity map (oxygen indicated by green in top image below) showing an interface layer that includes two oxide layers, one of silicon oxide and one of titanium silicon oxide. The next image below shows a TEM image and the corresponding EELS elemental intensity map of the same area again showing the silicon oxide and titanium silicon oxide layers.

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	Metal (tungsten) Silicon oxide Titanium silicon oxide Silicon (S/D) fin O 20 nm MAG: 1250kx HV: 200kV Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	Samsung 14nm LPE - Exynos 7420 (Galaxy S6)
1[b] said semiconductor region being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer and said metal oxide layer,	As shown and described above with respect to claim limitation 1[a], the accused semiconductor region is electrically connected to the accused metal electrical contact through the accused passivating dielectric tunnel barrier layer (of silicon oxide) and the accused metal oxide layer (of titanium silicon oxide). During operation of the Accused Samsung Devices, when the FinFET is turned on, an electrical current passes from the source contact through the layers to the semiconductor region and from the semiconductor region through the layers to the drain contact.

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
1[c] wherein said passivating dielectric tunnel barrier layer comprises a semiconductor oxide.	As shown and described above with respect to claim limitation 1[a], the accused passivating tunnel barrier layer comprises silicon oxide, a semiconductor oxide.
2 The structure of claim 1, wherein the semiconductor oxide comprises an oxide of the semiconductor region.	Acorn incorporates by reference all exemplary evidence related to claim 1 above. As shown and described above with respect to claim limitation 1[a], the accused semiconductor oxide layer, the passivating dielectric tunnel barrier layer, is made of silicon oxide, which is an oxide of the semiconductor region, which comprises silicon.
3 The structure of claim 1, wherein the semiconductor oxide of the dielectric tunnel barrier layer has a thickness of approximately 0.1 nm to 5 nm.	Acorn incorporates by reference all exemplary evidence related to claim 1 above. The TEM image and corresponding EELS elemental intensity map of the same area reproduced below show that the semiconductor oxide of the dielectric tunnel barrier layer (made of silicon oxide) has a thickness of approximately 2 nm, which is between 0.1 nm and 5 nm.

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	 Samsung 14nm LPE - Exynos 7420 (Galaxy S6)
4 The structure of claim 3, wherein the semiconductor region comprises an n-type doped source or drain of a transistor.	Acorn incorporates by reference all exemplary evidence related to claim 3 above. The silicon in the source/drain region of the accused FinFET transistors is n-type doped. Phosphorus is a common n-type dopant, and it is visible in the source/drain regions. Below are EDX elemental intensity maps of the Samsung 14nm LPE - Exynos 7420 (Galaxy S6) sample, highlighting silicon (red in left image), oxygen (light blue in middle image), and phosphorus (yellow in right image). The phosphorus color is very faint, even with image enhancement, because the density of phosphorus atoms is approximately 1% of the density of silicon atoms.

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	Si Map data 173 MAG: 1250kx HV: 200kV 20 nm O Map data 173 MAG: 1250kx HV: 200kV 20 nm P Map data 173 MAG: 1250kx HV: 200kV 20 nm
6 The structure of claim 3, wherein the metal oxide layer comprises an oxide of titanium.	Acorn incorporates by reference all exemplary evidence related to claim 3 above. As shown and described above with respect to claim limitation 1[a], the accused metal oxide layer comprises titanium silicon oxide, which comprises an oxide of titanium.
8 The structure of claim 6, wherein the semiconductor region comprises an n-type doped source or drain of a transistor.	Acorn incorporates by reference all exemplary evidence related to claim 6 above. Acorn incorporates herein its arguments made with respect to claim 4 above.
10 The structure of claim 6, wherein the semiconductor oxide comprises an oxide of silicon.	Acorn incorporates by reference all exemplary evidence related to claim 6 above. Acorn incorporates herein its arguments made with respect to claim 2 above.
11 The structure of claim 6, wherein the	Acorn incorporates by reference all exemplary evidence related to claim 6 above.

5364176

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
semiconductor oxide of the dielectric tunnel barrier layer is adjacent the semiconductor region.	The semiconductor oxide of the dielectric tunnel barrier layer, the silicon oxide layer, is adjacent the silicon semiconductor region. The top image below shows an EDX oxygen elemental intensity map (oxygen indicated by green in top image below) showing the silicon oxide layer adjacent the silicon region. The next image below shows a TEM image and the corresponding EELS elemental intensity map of the same area again showing the silicon oxide layer adjacent the silicon region. Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	Samsung 14nm LPE - Exynos 7420 (Galaxy S6)
12 The structure of claim 6, wherein the metal electric contact comprises titanium.	Acorn incorporates by reference all exemplary evidence related to claim 6 above. As shown and described above with respect to claim limitation 1[a] the metal electric contact includes tungsten and titanium nitride, and thus comprises titanium.
13 The structure of claim 3, wherein the semiconductor oxide comprises an oxide of silicon.	Acorn incorporates by reference all exemplary evidence related to claim 3 above. Acorn incorporates herein its arguments made with respect to claim 2 above.

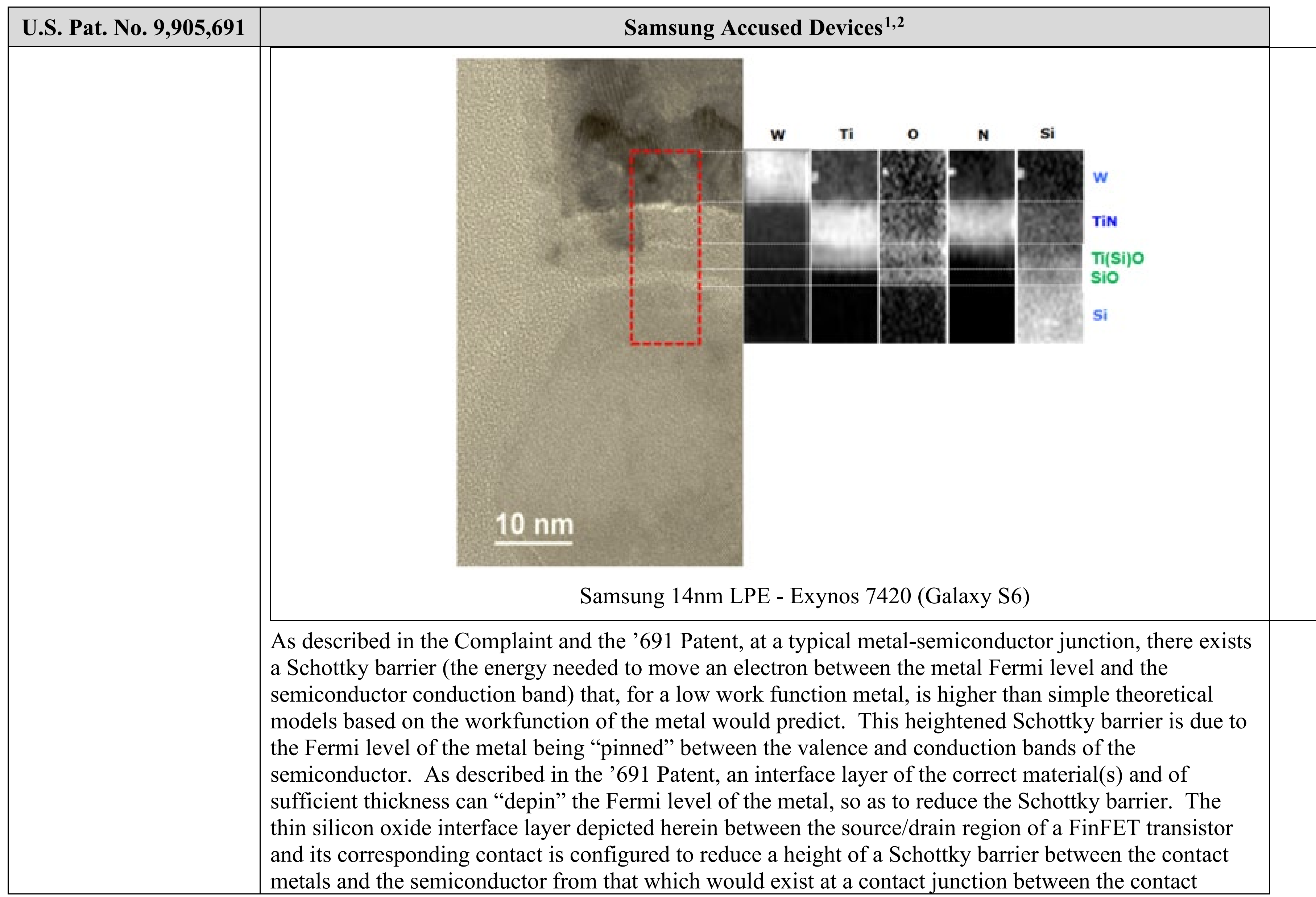
<table>
<tr><th>U.S. Pat. No. 9,905,691</th><th>Samsung Accused Devices[1,2]</th></tr>
<tr><td>15 The structure of claim 13, wherein the metal oxide layer comprises an oxide of titanium.</td><td>Acorn incorporates by reference all exemplary evidence related to claim 13 above.
Acorn incorporates herein its arguments made with respect to claim 6 above.</td></tr>
<tr><td>16 The structure of claim 15, wherein the metal electrical contact comprises titanium.</td><td>Acorn incorporates by reference all exemplary evidence related to claim 15 above.
Acorn incorporates herein its arguments made with respect to claim 12 above.</td></tr>
<tr><td>17 The structure of claim 15, wherein the semiconductor comprises an n-type doped source or drain of a transistor.</td><td>Acorn incorporates by reference all exemplary evidence related to claim 15 above.
Acorn incorporates herein its arguments made with respect to claim 4 above.</td></tr>
<tr><td>18 The structure of claim 17, wherein a specific contact resistivity between the n-type doped source or n-type doped source or drain and the metal electrical contact is less than 1 $\Omega\cdot\mu m^2$.</td><td>Acorn incorporates by reference all exemplary evidence related to claim 17 above.
The interface layer of the accused electrical junctions is configured to provide a specific contact resistivity between the metal electrical contact and the n-type dope source or drain of less than 1 $\Omega\cdot\mu m^2$. This is shown by the 2013 International Technology Roadmap for Semiconductors, which makes clear that doping process technology requirements for these devices have required specific contact resistances of less than 1 Ω-μm^2 for years.

Table FEP11 Thermal, Thin Film, Doping Process Technology Requirements — Rc expressed here as $\Omega\cdot\mu m^2$
Year of Production: 2013 | 2014 | 2015 | 2016 | 2017
Contact maximum resistivity for multi-gate MPU/ASIC ($\Omega\cdot\mu m^2$): 1.5 | 1.3 | 1.0 | 0.9 | 0.8

See also, e.g., Agrawal et al., Fermi level depinning and contact resistivity reduction using a reduced titania interlayer in n-silicon metal-insulator-semiconductor ohmic contacts, abstract (Applied Physics</td></tr>
</table>

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	Letters 104, 112101 2014) ("Experimental evidence" showing "Ultra-low contact resistivity of 9.1 x 10^{-9} Ω-cm^2 [= 0.91 $\Omega\cdot\mu m^2$] was obtained using Ti/10 Å TiO_{2-x}/n+ Si, which is a dramatic 13X reduction").
19 The structure of claim 1, wherein the semiconductor region comprises silicon, the semiconductor oxide comprises an oxide of silicon, the metal oxide comprises an oxide of titanium, and the metal electrical contact comprises titanium.	Acorn incorporates by reference all exemplary evidence related to claim 1 above. As shown as described above with respect to claim limitation 1[a], the semiconductor region comprises silicon, the semiconductor oxide comprises silicon oxide, an oxide of silicon, the metal oxide comprises titanium silicon oxide, which comprises an oxide of titanium, and the metal electrical contact comprises tungsten and titanium nitride, and thus comprises titanium.
20 The structure of claim 1, wherein the dielectric tunnel barrier is configured to reduce a height of a Schottky barrier between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween.	Acorn incorporates by reference all exemplary evidence related to claim 1 above. The accused dielectric tunnel barrier, identified with respect to claim limitation 1[a] as the silicon oxide layer, is configured to reduce a height of a Schottky barrier between the metal electrical contact (including tungsten and titanium nitride) and the silicon-based semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the silicon oxide layer disposed therebetween. For example, the top image below shows an EDX oxygen elemental intensity map (oxygen indicated by green in top image below) showing a silicon oxide interface layer between the source/drain region of a FinFET transistor and a corresponding contact in an exemplary Samsung Accused Product. The next image below shows a TEM image and the corresponding EELS elemental intensity map of the same area showing a silicon oxide interface layer that appears to be approximately 2 nm thick.

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	Metal (tungsten) Silicon oxide Titanium silicon oxide Silicon (S/D) fin O 20 nm MAG: 1250kx HV: 200kV Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	 Samsung 14nm LPE - Exynos 7420 (Galaxy S6) As described in the Complaint and the '691 Patent, at a typical metal-semiconductor junction, there exists a Schottky barrier (the energy needed to move an electron between the metal Fermi level and the semiconductor conduction band) that, for a low work function metal, is higher than simple theoretical models based on the workfunction of the metal would predict. This heightened Schottky barrier is due to the Fermi level of the metal being "pinned" between the valence and conduction bands of the semiconductor. As described in the '691 Patent, an interface layer of the correct material(s) and of sufficient thickness can "depin" the Fermi level of the metal, so as to reduce the Schottky barrier. The thin silicon oxide interface layer depicted herein between the source/drain region of a FinFET transistor and its corresponding contact is configured to reduce a height of a Schottky barrier between the contact metals and the semiconductor from that which would exist at a contact junction between the contact

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	metals and the semiconductor without the interface layer disposed therebetween. *See, e.g.*, '691 Patent, 10:14-16 ("Often, the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm.") For example, the interface layer is sufficiently thick to terminate substantially all the silicon semiconductor surface dangling bonds. *See, e.g.*, '691 Patent, 15:50-56 ("The role played by interface layer 620 in tuning, adjusting, or controlling the height of the barrier between the conductor 630 and the semiconductor 610 may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds."). It is also sufficiently thick to reduce the formation of MIGS—metal induced gap states—in the semiconductor. *See id.* at 15:56-59 ("Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor."). The conductor electron wave function penetration distance is 1-3 nm, or less, and thus does not substantially penetrate the silicon semiconductor. *See, e.g.*, Kobayashi et al., *Fermi-Level Depinning in Metal/Ge Schottky Junction and Its Application to Metal Source/Drain Ge NMOSFET*, 2008 Symposium on VLSI Technology Digest of Technical Papers, IEEE, pp. 54-55; Connelly et al., *A New Route to Zero-Barrier Metal Source/Drain MOSFETs*, IEEE Transactions on Nanotechnology, Vol. 3, No. 1, March 2004, pp. 98-10; Hu et al., *Fermi Level Depinning For the Design of III-V FET Source/Drain Contacts*, 2009 Symposium on VLSI Technology, IEEE, pp. 123-124; Mönch, *On the alleviation of Fermi-level pinning by ultrathin insulator layers in Schottky contacts*, Journal of Applied Physics, Vol. 111, pp. 073706-1 – 073706-7 (2012).
22 The structure of claim 1, wherein the dielectric tunnel barrier layer is configured to reduce contact resistivity between the metal electrical contact and the semiconductor region from that which would exist at a contact	Acorn incorporates by reference all exemplary evidence related to claim 1 above. The accused dielectric tunnel barrier, identified with respect to claim limitation 1[a] as the silicon oxide layer, is configured to reduce contact resistivity between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact (including tungsten and titanium nitride) and the silicon-based semiconductor region without the silicon oxide layer disposed therebetween. As described in the Complaint and the '691 Patent, at a typical metal-semiconductor junction, there exists a Schottky barrier (the energy needed to move an electron between the metal Fermi level and the semiconductor conduction band) that, for a low work function metal, is higher than simple theoretical models based on the workfunction of the metal would predict. This heightened Schottky barrier is due to

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween.	the Fermi level of the metal being "pinned" between the valence and conduction bands of the semiconductor thereby inhibiting current flow thus increasing resistivity. As described in the '691 Patent, an interface layer of the correct material(s) and of sufficient thickness can "depin" the Fermi level of the metal, so as to reduce the Schottky barrier thus decreasing resistivity. The thin silicon oxide interface layer depicted herein between the source/drain region of a FinFET transistor and its corresponding contact is configured to reduce a height of a Schottky barrier between the contact metals and the semiconductor from that which would exist at a contact junction between the contact metals and the semiconductor without the interface layer disposed therebetween thereby reducing the contact resistivity. *See, e.g.*, '691 Patent, 10:14-16 ("Often, the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm."); *id.* at 14:34-45 ("At large thicknesses, the interface layer poses significant resistance to current. As thickness decreases, resistance falls due to increased tunneling current. However, there comes a point where even as the interface layer continues to get thinner, resistance increases. This is due to the effect of MIGS, which increasingly pull the Fermi level of the metal down towards mid-gap of the semiconductor, creating a Schottky barrier. The present inventors have discovered that this competition results in an optimum thickness, as shown in the illustration [Fig. 8] where the resistance is minimum.") For example, the interface layer is sufficiently thick to terminate substantially all the silicon semiconductor surface dangling bonds. *See, e.g.*, '691 Patent, 15:50-56 ("The role played by interface layer 620 in tuning, adjusting, or controlling the height of the barrier between the conductor 630 and the semiconductor 610 may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds."). It is also sufficiently thick to reduce the formation of MIGS—metal induced gap states—in the semiconductor. *See id.* at 15:56-59 ("Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor."). The conductor electron wave function penetration distance is 1-3 nm, or less, and thus does not substantially penetrate the silicon semiconductor. *See, e.g.*, Kobayashi et al., *Fermi-Level Depinning in Metal/Ge Schottky Junction and Its Application to Metal Source/Drain Ge NMOSFET*, 2008 Symposium on VLSI Technology Digest of Technical Papers, IEEE, pp. 54-55; Connelly et al., *A New Route to Zero-Barrier Metal Source/Drain MOSFETs*, IEEE Transactions on Nanotechnology, Vol. 3, No. 1, March 2004, pp. 98-10; Hu et al.,

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	Fermi Level Depinning For the Design of III-V FET Source/Drain Contacts, 2009 Symposium on VLSI Technology, IEEE, pp. 123-124.
25[a] An electrical junction	To the extent the preamble is limiting, the Samsung Accused Devices include electrical junctions. Broadly speaking, the Samsung Accused Devices are processors, such as the Exynos 7420, the Snapdragon 820, and the Apple A9, which are devices that use electrical energy to operate, and electronic devices incorporating those processors, such as the Galaxy S6, the LG G5, and the iPhone 6s. The below pictures depict, as an example, a teardown of a Galaxy S6 to reveal the Exynos 7420 processor therein, outlined in red.

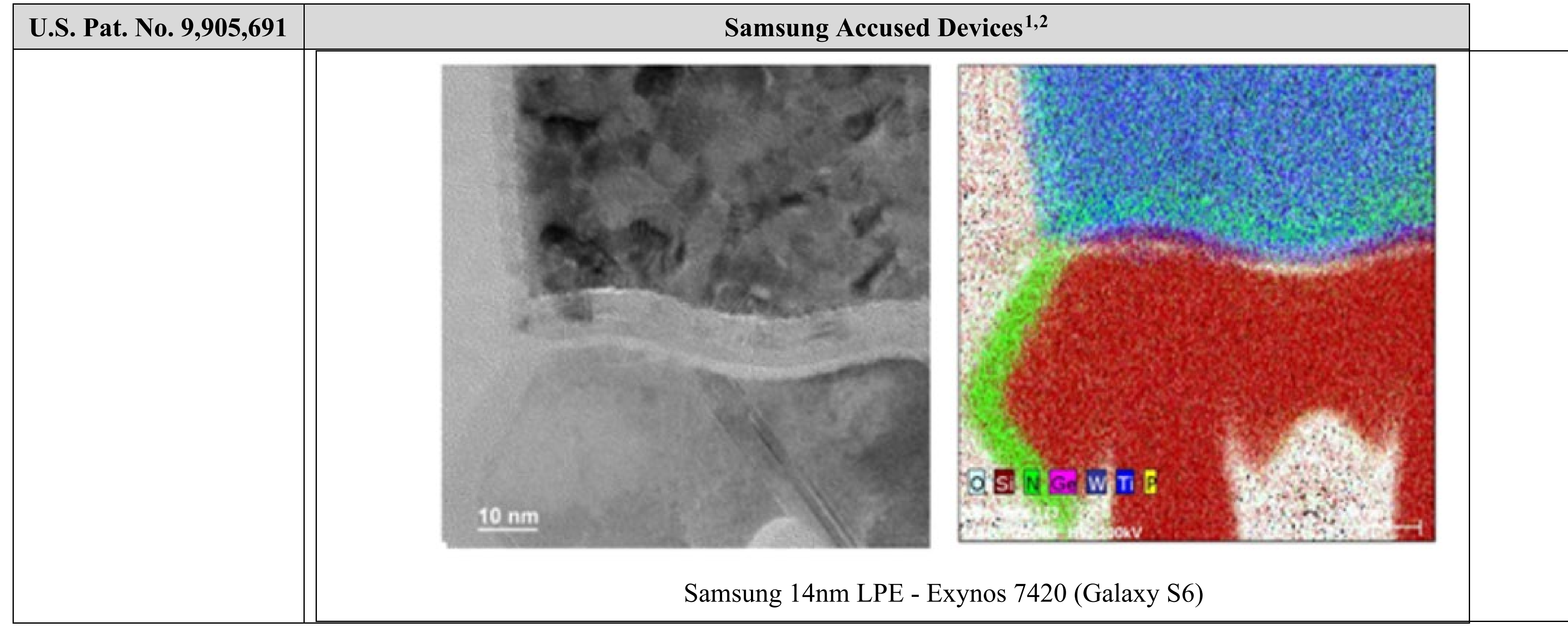
U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]

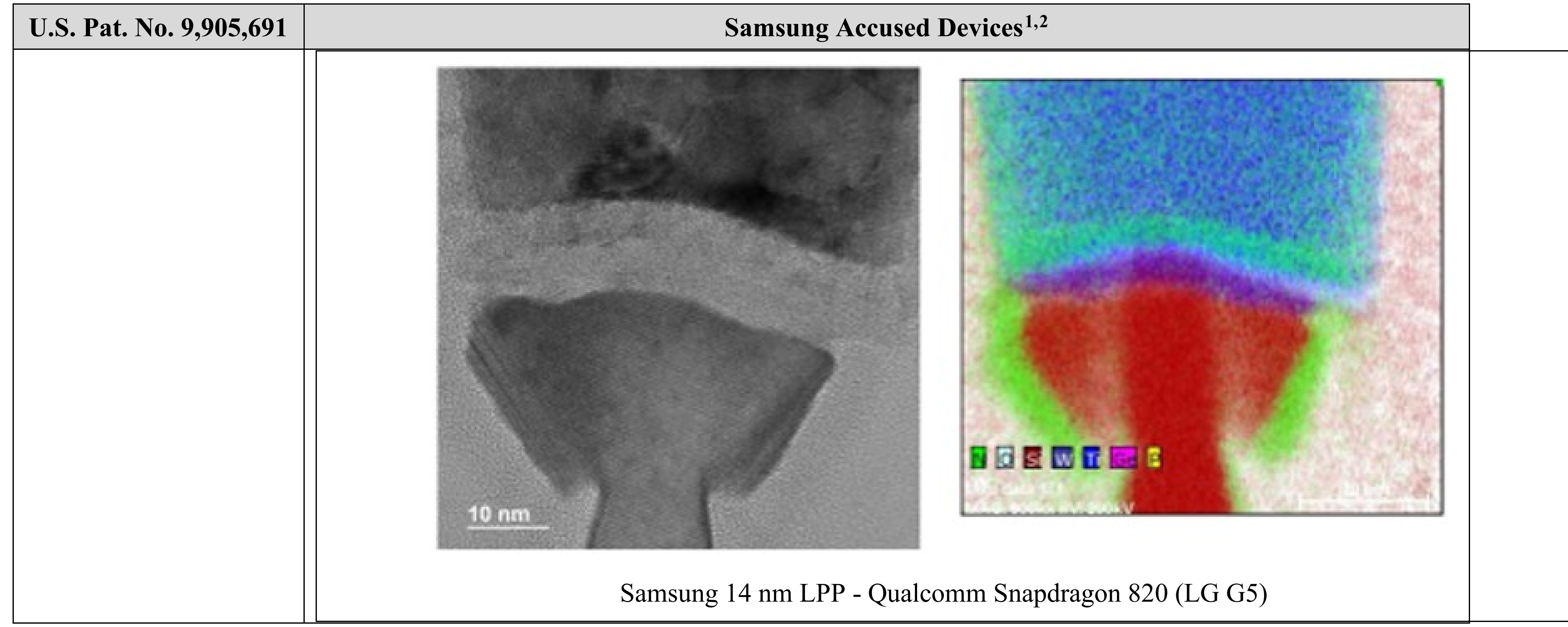
5364176

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	See https://www.ifixit.com/Teardown/Samsung+Galaxy+S6+Teardown/39174 (last visited February 28, 2020). The Samsung Accused Devices include billions of FinFET transistors packed closely together and corresponding contacts, with electrical junctions between the semiconductor of the transistors and the contacts. Taking a random cross section from one Samsung accused processor reveals the following transmission electron microscope (TEM) image, which depicts the source/drain semiconductor region of two FinFET transistors (each of the transistors having four fins), their corresponding metal electrical contacts, and the electrical junctions between them.

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	100 nm Samsung 14nm LPE - Exynos 7420 (Galaxy S6) The images below are similar TEM images, zoomed in more closely. The images on the left below are close-up TEM images of the junction between a FinFET source/drain region and the corresponding contact in various exemplary Samsung Accused Devices. The color images on the right are EDX elemental intensity maps showing that the source/drain is made of a silicon-based semiconductor and the contact area includes two conductors, tungsten (W) and titanium nitride (TiN).

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	 Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	 Samsung 14 nm LPP - Qualcomm Snapdragon 820 (LG G5)

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	10 nm N O Si Ge W Ti Samsung 14 nm LPE - Apple A9 (iPhone 6s)
25[b] comprising an interface layer disposed between a contact metal and a semiconductor,	The Samsung Accused Devices include FinFET transistors (with source/drain regions made up of a silicon-based semiconductor) and corresponding contacts (which include tungsten and titanium nitride), that are separated by an interface layer disposed between them. For example, the top image below shows an EDX oxygen elemental intensity map (oxygen indicated by green in top image below) showing an interface layer between the semiconductor source/drain region of a FinFET transistor and a corresponding contact metal (tungsten) in an exemplary Samsung Accused Product. That interface layer includes two oxide layers. The next image below shows a TEM image and the corresponding EELS elemental intensity map of the same area showing a silicon oxide passivation layer and a titanium silicon oxide separation layer located between contact metals of tungsten and titanium nitride and a silicon-based semiconductor.

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	Samsung 14nm LPE - Exynos 7420 (Galaxy S6)
25[c] the semiconductor comprising a source or drain of a transistor,	As described above with respect to claim limitations 25[a] and 25[b], the semiconductor of the accused electrical junctions comprises a source or drain of a transistor.
25[d] the interface layer comprising a metal oxide separation layer and a semiconductor oxide passivation layer	As described above with respect to claim limitation 25[b], the interface layer comprises a metal oxide separation layer of titanium silicon oxide and a semiconductor oxide passivation layer of silicon oxide.

<table>
<tr><th>U.S. Pat. No. 9,905,691</th><th>Samsung Accused Devices[1,2]</th></tr>
<tr><td>25[e] and configured to provide a specific contact resistivity between the contact metal and the semiconductor of less than 1 Ω·µm².</td><td>The interface layer of the accused electrical junctions is configured to provide a specific contact resistivity between the contact metal and the semiconductor of less than 1 Ω·µm². This is shown by the 2013 International Technology Roadmap for Semiconductors, which makes clear that doping process technology requirements for these devices have required specific contact resistances of less than 1 Ω-µm² for years.

<table>
<tr><td>Table FEP11 Thermal, Thin Film, Doping Process Technology Requirements</td><td></td><td></td><td colspan="3">Rc expressed here as Ω · µm²</td></tr>
<tr><td>Year of Production</td><td>2013</td><td>2014</td><td>2015</td><td>2016</td><td>2017</td></tr>
<tr><td>Contact maximum resistivity for multi-gate MPU/ASIC (Ω · µm²)</td><td>1.5</td><td>1.3</td><td>1.0</td><td>0.9</td><td>0.8</td></tr>
</table>

See also, e.g., Agrawal et al., Fermi level depinning and contact resistivity reduction using a reduced titania interlayer in n-silicon metal-insulator-semiconductor ohmic contacts, abstract (Applied Physics Letters 104, 112101 2014) ("Experimental evidence" showing "Ultra-low contact resistivity of 9.1 x 10^{-9} Ω-cm² [= 0.91 Ω·µm²] was obtained using Ti/10 Å TiO_{2-x}/n+ Si, which is a dramatic 13X reduction").</td></tr>
<tr><td>26 The electrical junction of claim 25, wherein the metal oxide separation layer comprises an oxide of titanium.</td><td>Acorn incorporates by reference all exemplary evidence related to claim 25 above.

As shown above with respect to claim limitation 25[b], the metal oxide separation layer comprises titanium silicon oxide, which comprises an oxide of titanium.</td></tr>
<tr><td>27 The electrical junction of claim 26, wherein the semiconductor oxide passivation layer comprises an oxide of the semiconductor.</td><td>Acorn incorporates by reference all exemplary evidence related to claim 26 above.

As shown above with respect to claim limitation 25[b], the semiconductor oxide passivation layer comprises an oxide of the semiconductor, silicon oxide.</td></tr>
<tr><td>28 The electrical junction of claim 27,</td><td>Acorn incorporates by reference all exemplary evidence related to claim 27 above.</td></tr>
</table>

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
wherein the semiconductor oxide passivation layer has a thickness of approximately 0.1 nm to 5 nm.	The TEM image and corresponding EELS elemental intensity map of the same area reproduced below show that the semiconductor oxide passivation layer (made of silicon oxide) has a thickness of approximately 2 nm, which is between 0.1 nm and 5 nm. Samsung 14nm LPE - Exynos 7420 (Galaxy S6)
29 The electrical junction of claim 27, wherein the semiconductor oxide passivation layer is	Acorn incorporates by reference all exemplary evidence related to claim 27 above. The semiconductor oxide passivation layer, the silicon oxide layer, is adjacent the silicon semiconductor region. The top image below shows an EDX oxygen elemental intensity map (oxygen indicated by green in top image below) showing the silicon oxide layer adjacent the silicon region.

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
adjacent the semiconductor.	The next image below shows a TEM image and the corresponding EELS elemental intensity map of the same area again showing the silicon oxide layer adjacent the silicon region. Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

U.S. Pat. No. 9,905,691	Samsung Accused Devices[1,2]
	Samsung 14nm LPE - Exynos 7420 (Galaxy S6)
30 The electrical junction of claim 25, wherein the contact metal is a metal or a stack of metals deposited on the interface layer.	Acorn incorporates by reference all exemplary evidence related to claim 25 above. As shown above with respect to claim limitation 25[d], the contact metal is a stack of metals, titanium nitride and tungsten, deposited on the interface layer.