conductor with a bandgap at least this large), or nearly 1.0 V using silicon. Such high barrier heights imply the ability to withstand high voltages before breakdown occurs. Thus, Schottky barriers having such high barrier heights may be particularly useful in high-voltage Schottky diodes.

Another advantage achieved through the use of the interface layer **620** is greater flexibility afforded in selecting a conductor **630**. Typically, metals chosen for application in classic Schottky diodes are those that can form a silicide with a silicon semiconductor. The formation of the silicide helps to reduce surface states (resulting, from dangling bonds), but not the effects of MIGS. Thus, the Fermi level at the semiconductor surface is still pinned. Using metals that form silicides upon contact with silicon may thus help to make the devices more reproducible in a manufacturing environment, but such devices still suffer from the drawback of having a barrier height that is fixed.

According to one embodiment of the present invention, however, one may select a conductor that is not able (or not readily able) to form a silicide with the semiconductor. The metal silicide is not needed because the interface layer provided in accordance with the present invention passivates the semiconductor surface and also reduces or eliminates the effect of MIGS. This may allow for selection of a metal that has properties such as a desirable work function or Fermi level energy, even though that metal may not form a metal silicide.

For example, to make large-barrier diodes, for an n-type doped silicon semiconductor, a metal may be selected that has a work function that is either substantially equal to the valence band energy of the semiconductor or that is within about 0.1 eV to about 0.3 eV of the valence band energy of the semiconductor. Similarly, for a p-type doped silicon semiconductor, a metal may be selected that has a work function substantially equal to the conduction band energy of the semiconductor. For Schottky diodes configured in accordance with the present invention, the Fermi level of the metal may lie anywhere in the bandgap of the semiconductor when an interface layer is disposed within the junction, resulting in diodes of various barrier heights. The Fermi level of the metal may also lie in the conduction or valence band of the semiconductor.

The use of interface layer **620** thus provides a way to tune, adjust, or control the height of the barrier between the conductor and the semiconductor. Without the interface layer **620**, the barrier height would be substantially un-tunable, un-adjustable, and fixed (as discussed above).

The role played by interface layer **620** in tuning, adjusting, or controlling the height of the barrier between the conductor **630** and the semiconductor **610** may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds. Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor. The electron wave function ray instead penetrate into the interface layer and form MIGS within the interface layer at an energy related to the states of the interface layer material. As desired, the density of the MIGS and the depth of MIGS penetration into the interface layer may be reduced by choosing an interface layer material or materials having a larger bandgap or higher effective mass than the semiconductor.

According to one embodiment of the present invention then, the interface layer **620** is incorporated into a device operable to pass current through the semiconductor surface and the interface layer during device operation. In such an embodiment, it may be desirable to use an interface layer having a thickness of a monolayer, or, for example between about 0.1 nm and about 0.3 nm, and also having a wide bandgap (as compared to that of the semiconductor) so that the interface layer both de-pins the Fermi level (so that the barrier height depends predominantly on bulk properties of the junction materials) and allows sufficient current transfer across it. Advantageously, such interface layers may be sufficiently thin to provide low impedance to current flow (due to the exponential dependence of direct tunneling on barrier thickness), which is desirable for many semiconductor devices, while also providing sufficient semiconductor surface passivation to allow an adjustable barrier height. That is, the interface layer may allow passivation of surface states and reduction (or elimination) of MIGS in the semiconductor to allow for an adjustable barrier height with a substantially thin layer that allows sufficient current to be transferred across the interface layer.

There are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning. In other words, some embodiments may allow for a sufficiently thin interface layer so that not all of the effects of MIGS in the Si are eliminated. Further, the pinning may be varied by combinations of thickness of the interface layer and the choice of interface material. The metal in contact with the interface layer may be pinned by MIGS at different levels in different materials. Conversely, or in addition, the passivation may be left incomplete to allow for an effective level of unpassivated states. Complete depinning of the Fermi level (that is removal of all surface states in Si including MIGS) is another option, in which case one could tune the barrier height simply by choosing a pure metal or an alloy that possesses the desired workfunction. In that case, the barrier height is determined by Equation (1), which until now has been an unrealizable idealization. Note that the type of tuning being discussed here is adjustment of the barrier height by altering the structure of the junction at the time of manufacture, not by varying an externally applied condition during junction operation.

FIGS. **7***a*–**7***d* show relationships between Fermi energy, conduction band energy, and valence band energy for various Schottky barriers containing a metal in contact with (or in close proximity to) a semiconductor, where the bandgap (E_g) of the semiconductor exists between the conduction band (E_e) and the valence band (E_v). In this example, the work function of the metal Φ_M is chosen to be approximately equal to the electron affinity X_S of the semiconductor. In FIG. **7***a*, an unpassivated Schottky barrier **700** is shown. In this example, the Fermi level (E_F) of the metal **730** is pinned in the bandgap of the semiconductor **710**. This results in a discontinuity in the vacuum level caused by a charged dipole at the interface.

In FIG. **7***b*, the interface layer **720***b* is thick enough to passivate dangling bonds at the surface of the semiconductor **710**, but not thick enough to eliminate or sufficiently reduce the effect of MIGS. As a result, the band structure is largely unaltered from that seen in the previous illustration. Similarly, in FIG. **7***c*, when the interface layer **720***c* is sufficiently thick to eliminate or reduce the effect of MIGS but not to passivate the semiconductor surface, little change in the energy band structure is observed. However, as shown in FIG. **7***d*, when the interface layer **720***d* is sufficient to both eliminate or reduce the effect of MIGS and to passivate the semiconductor surface, we see the Fermi level of the metal aligning with the conduction band of the semiconductor (i.e., the Fermi level of the semiconductor has been depinned and no longer lines up with the Fermi level of the metal). The vacuum level is now continuous as there is no charged dipole at the interface. Thus, the band structure of a device constructed in this fashion is a result of only bulk material properties, not properties of the surface. By way of example, the materials in such cases nay be Al and Si, with a work function for Al of approximately Φ_M=4.1 eV and the electron affinity for Si of approximately X_S=4.05 eV.

V. Transistors Containing Passivated Semiconductor Surfaces

The interface layers described herein may be used in connection with a semiconductor surface of a channel in a field effect transistor. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail in co-pending U.S. patent application No.: 10/342,576 entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed Jan. 14, 2003 by the present inventors, and assigned to the assignee of the present invention.

The source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention. In the past, such contacts generally comprised a silicide-n^+-Si junction, which formed a somewhat "leaky" Schottky diode, with a Fermi level of the semiconductor pinned at the midgap. In contrast, the present invention provides a contact wherein the Fermi level of the metal is aligned with the conduction band of the semiconductor (e.g., as shown in FIG. **7***d*). Note that in other cases, depending on the type of semiconductor material and conductors used, the Fermi level of the metal may align with the valence band of the semiconductor.

Although both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide—semiconductor junction a Schottky barrier is formed which is comprised of a depletion layer. The tunnel barrier presented by such a depletion layer may be an order of magnitude thicker than the dielectric tunnel barrier in the present invention. The thinner interface layers provided by the present invention permit higher current across the junction (i.e., lower junction specific contact resistance).

Two other properties of the dielectric deserve mention. First is the property of the height of the barrier compared to the semiconductor conduction band (for electrons). In making the barrier thinner than a silicide barrier, the tradeoff may be a higher tunnel barrier (e.g., 2 eV for nitride, compared with about half the gap of 0.6 eV for silicide). Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV). Nevertheless, even with the higher barrier to electrons, the present inventors have determined that the resistance can still be one hundred times lower than a contact to silicon with a silicide barrier.

The second property is the effective mass of electrons in the dielectric. Larger mass electrons will not penetrate as far (i.e., because of their shorter wavelength) from the metal into the semiconductor. The less the electrons penetrate into the dielectric, the less the effect of MIGS in the dielectric. Thus, MIGS in the dielectric are reduced with larger bandgap and larger effective mass.

In addition the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility). The high doping profiles were required in the past in order to keep the junction depletion layer relatively thin, so as to increase the tunneling current, thus reducing the junction resistance. However, it is becoming increasingly difficult to increase doping profiles in order to provide low resistance junctions. It may be possible to reach the same level of resistance with a lower doping concentration using the present invention. It may further be possible to achieve much lower resistance even with lower doping concentration. When the present invention is used with high doping levels, the resistance will be further reduced.

Thus, methods and applications for semiconductor-interface layer-metal junctions have been described. Although described with reference to specific embodiments it should be remembered that various modifications and changes may be made to the techniques described herein without departing from the broader spirit and scope of the invention. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense and the invention measured only in terms of the claims, which follow.

What is claimed is:

1. An electrical device, comprising:

a metal;

a silicon-based semiconductor; and

an interface layer of less than 1 nm thickness in a vicinity disposed between and in contact with both the metal and the semiconductor and configured to depin a Fermi level of the metal,

wherein the electrical device has a specific contact resistance of less than or equal to approximately 1000 Ω-μm^2.

2. The electrical device of claim **1** wherein the interface layer includes a passivating material.

3. The electrical device of claim **2** wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.

4. The electrical device of claim **3** wherein the interface layer consists essentially of a monolayer.

5. The electrical device of claim **2** wherein the interface layer further includes a separation layer.

6. The electrical device of claim **1** wherein the specific contact resistance is less than or equal to approximately 100 Ω-μm^2.

7. The electrical device of claim **1** wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

8. The electrical device of claim **1** wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

9. The electrical device of claim **1** wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

10. The electrical device of claim **1** wherein the interface layer comprises a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material.

11. The electrical device of claim **10** wherein the nitrogenous material comprises at least one of ammonia (NH_3), nitrogen (N_2) or unbound nitrogen (N).

12. An electrical device, comprising a metal—interface layer—Si-based semiconductor junction in which the interface layer is less than 1 nm thick in a vicinity of the junction and includes a passivating material and the electrical device has a specific contact resistance of less than approximately 1000 Ω-μm^2.

13. The electrical device of claim **12** wherein the specific contact resistance is less than or equal to approximately 100 Ω-μm^2.

14. The electrical device of claim **12** wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

15. The electrical device of claim **12** wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

16. The electrical device of claim **1** wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

17. The electrical device of claim **12**, wherein the passivating material comprises one or more of a nitride, an oxide, an oxynitride a hydride, a fluoride and/or an arsenide of silicon.

18. The electrical device of claim **17**, wherein the interface layer comprises a passivation layer and a separation layer.

19. A method, comprising depinning a Fermi level of a conductor in an electrical junction with a silicon-based semiconductor through the use of an interface layer disposed between a surface of the semiconductor and the conductor, wherein the interface layer (i) has a thickness of less than 1 nm in a vicinity of the junction yet sufficient to reduce effects of metal-induced gap states in the semiconductor while providing the junction with a specific contact resistance of less than approximately 1000 Ω-μm^2, and (ii) passivates the surface of the semiconductor.

20. The method of claim **19** wherein the specific contact resistance is less than or equal to approximately 100 Ω-μM^2.

21. The method of claim **19** wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

22. The method of claim **19** wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

23. The method of claim **19** wherein the specific contact resistance is less than or equal to approximately 1 Ω-μM^2.

24. The method of claim **19** wherein the interface layer has a thickness sufficient to provide a specific contact resistance of the electrical junction of less than or equal to approximately 1 Ω-μm^2.

25. The method of claim **19** wherein the interface layer includes a passivating material selected from the list comprising: an arsenide, a hydride, a fluoride, an oxide, an oxynitride and a nitride of silicon.

26. The method of claim **25** wherein the interface layer consists essentially of a monolayer.

27. The method of claim **19** wherein the interface layer is grown on the semiconductor surface at temperatures above approximately 300° C.

28. The method of claim **27** wherein the interface layer is grown in the presence of a nitrogenous material.

29. The method of claim **28** wherein the nitrogenous material comprises one of ammonia (NH_3), nitrogen (N_2), or unbound nitrogen (N).

30. The method of claim **19** wherein the interface layer includes a passivation layer grown by immersion of the semiconductor in a liquid containing hydrogen and fluorine ions.

31. An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness of less than 1 nm in a vicinity of the junction yet that allows a Fermi level of the conductor to align with a conduction band of the semiconductor, wherein the electrical device has a specific contact resistance less than approximately 1000 Ω-μm^2.

32. The electrical device of claim **31** wherein the specific contact resistance is less than or equal to approximately 100 Ω-μm^2.

33. The electrical device of claim **31** wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

34. The electrical device of claim **31** wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

35. The electrical device of claim **31** wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

36. An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness of less than 1 nm in a vicinity of the junction yet that allows a Fermi level of the conductor to align with a valence band of the semiconductor, wherein the electrical device has a specific contact resistance less than approximately 1000 Ω-μm^2.

37. The electrical device of claim **36** wherein the specific contact resistance is less than or equal to approximately 100 Ω-μm^2.

38. The electrical device of claim **36** wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

39. The electrical device of claim **36** wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

40. The electrical device of claim **36** wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

41. An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness of less than 1 nm in a vicinity of the junction yet that allows a Fermi level of the semiconductor to be independent of a Fermi level of the conductor, wherein the electrical device has a specific contact resistance less than approximately 1000 Ω-μm^2.

42. The electrical device of claim **41** wherein the specific contact resistance is less than or equal to approximately 100 Ω-μm^2.

43. The electrical device of claim **41** wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

44. The electrical device of claim **41** wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

45. The electrical device of claim **41** wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

46. An electrical device, comprising:

a silicon-based semiconductor of either n-type or p-type semiconductor material;

a metal having a workfunction approximately equal to a conduction band of the semiconductor if the semiconductor is of n-type semiconductor material or having a workfunction approximately equal to a valence band of the semiconductor if the semiconductor is of p-type semiconductor material; and an interface layer of less than 1 nm thickness in a vicinity disposed between and in contact with both the semiconductor and the metal, wherein the electrical device has a specific contact resistance of less than or approximately equal to 1000 Ω-μ^2.

47. The electrical device of claim **46** wherein the interface layer includes a passivating material.

48. The electrical device of claim **47** wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.

49. The electrical device of claim **48** wherein the interface layer consists essentially of a monolayer.

50. The electrical device of claim **47** wherein the interface layer further includes a separation layer.

51. The electrical device of claim **46** wherein the specific contact resistance is less than or equal to approximately 100 Ω-μm^2.

52. The electrical device of claim **46** wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

53. The electrical device of claim **46** wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

54. The electrical device of claim **46** wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

55. The electrical device of claim **46** wherein the interface layer comprises a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material.

56. The electrical device of claim **55** wherein the nitrogenous material comprises at least one of ammonia (NH_3), nitrogen (N_2) or unbound nitrogen (N).

57. An electrical device, comprising:

a silicon-based semiconductor of either n-type or p-type semiconductor material;

a metal having a workfunction near or substantially equal to a conduction band edge of the semiconductor if the semiconductor is of p-type semiconductor material, or having a workfunction near or substantially equal to a valence band edge of the semiconductor if the semiconductor is of n-type semiconductor material; and

an interface layer of less than 1 nm thickness in a vicinity disposed between and in contact with both the semiconductor and the metal and configured to depin a Fermi level of the metal.

58. The electrical device of claim **57** wherein the interface layer includes a passivating material.

59. The electrical device of claim **58** wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.

60. The electrical device of claim **57** wherein the interface layer consists essentially of a monolayer.

61. The electrical device of claim **57** wherein the interface layer further includes a separation layer.

62. An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness sufficient to depin a Fermi level of the conductor in a vicinity of the junction yet thin enough to provide the junction with a specific contact resistance that is generally dependent on the workfunction of the conductor.

63. The electrical device of claim **62** wherein the interface layer includes a passivating material.

64. The electrical device of claim **63** wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.

65. The electrical device of claim **63** wherein the interface layer consists essentially of a monolayer.

66. The electrical device of claim **63** wherein the interface layer further includes a separation layer.

67. The electrical device of claim **62** wherein the interface layer comprises a passivation the semiconductor in the presence of nitrogenous material.

68. The electrical device of claim **67** wherein the nitrogenous material comprises one of: ammonia (NH_3), nitrogen (N_2), or unbound nitrogen (N).

69. The electrical device of claim **62** wherein the interface layer includes a passivation layer grown by immersion of the semiconductor in a liquid containing hydrogen and fluorine ions.

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