UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner

v.

ACORN SEMI, LLC,
Patent Owner

Case IPR2020-_____

U.S. Patent No. 9,905,691
Title: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
Issue Date: February 27, 2018

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,905,691

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157 Cong. Rec. S5429 (daily ed. Sept. 8, 2011)..58

Joe Matal, *A Guide to the Legislative History of the America Invents Act: Part II of II*, 21 FED. CIR. B.J. 539 (2012) 58

All citations to 35 U.S.C. §§ 102 and 112 in this paper refer to the pre-AIA statute unless otherwise noted.

All emphases are added unless otherwise noted.

This paper includes color illustrations and should be viewed in color.

PETITIONER'S EXHIBIT LIST

Petitioner Exhibit No.	DESCRIPTION
1001	U.S. Patent No. 9,905,691.
1002	File History of U.S. Patent No. 7,084,423.
1003	U.S. Patent No. 7,084,423.
1004	File History of U.S. Patent No. 6,833,556.
1005	U.S. Patent No. 6,833,556.
1006	File History of U.S. Patent No. 7,462,860.
1007	U.S. Patent No. 7,462,860.
1008	File History of U.S. Patent No. 7,884,003.
1009	U.S. Patent No. 7,884,003.
1010	File History of U.S. Patent No. 8,431,469.
1011	U.S. Patent No. 8,431,469.
1012	File History of U.S. Patent No. 9,425,277.
1013	U.S. Patent No. 9,425,277.
1014	File History of U.S. Patent No. 9,905,691.
1015	U.S. Patent No. 7,176,483 (cited as "Grupp '483").
1016	Declaration of Dr. E. Fred Schubert (cited as "Schubert Decl.").
1017	E.H. Rhoderick, *Metal-semiconductor contacts*, 129 IEE REV. 1 (Feb. 1982) (cited as "Rhoderick").
1018	C.Y. Chang et al., *Specific contact resistance of metal-semiconductor barriers*, 15 SOLID STATE ELECS. 541 (1971) (cited as "Chang").
1019	S.M. Goodnick et al., *Effects of a thin SiO_2 layer on the formation of metal-silicon contacts*, 18 J. VAC. SCI. & TECH. 949 (Apr. 1981) (cited as "Goodnick").
1020	M.A. Sobolewski and C.R. Helms, *Studies of barrier height mechanisms in metal-silicon nitride-silicon Schottky barrier diodes*, J. VAC. SCI. & TECH. B 971 (Jul./Aug. 1989) (cited as "Sobolewski").
1021	U.S. Patent No. 4,110,488 (cited as "Risko").
1022	M.A. Taubenblatt et al., *Interface effects in titanium and hafnium Schottky barriers on silicon*, 44 APPLIED PHYS. LETTERS 895 (cited as "Taubenblatt 1984").
1023	U.S. Patent No. 3,983,264 (cited as "Schroen").
1024	U.S. Patent No. 4,845,050 (cited as "Kim").
1025	Japanese Laid-Open App. No. JPH11162874A (June 18, 1999).

Petitioner Exhibit No.	**DESCRIPTION**
1026	Certified Translation of Japanese Laid-Open App. No. JPH11162874A (June 18, 1999) (cited as "Iwaguro").
1027	Gary P. Carver et al., *Specific Contact Resistivity of Metal-Semiconductor Contacts—A New, Accurate Method Linked to Spreading Resistance*, 35 IEEE TRANS. ELECTRON DEVICES 489 (Apr. 1988) (cited as "Carver").
1028	Redline of Specification of U.S. Patent No. 7,176,483 Against Specification of U.S. Patent No. 7,084,423.
1029	N.D. Lang and W. Kohn, *Theory of Metal Surfaces: Work Function*, 3 PHYS. REV. B 1215 (1971) (cited as "Lang").
1030	W. Zheng et al., *Electronic Structure Differences in* ZrO_2 *vs.* HfO_2, 109 J. Phys. Chem. A 109 (2005) (cited as "Zheng").
1031	Complaint in *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, Case No. 2:19-cv-00347, ECF No. 1 (E.D. Tex. Oct. 23, 2019).
1032	Summons and Return of Service in *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-00347, ECF No. 8 (E.D. Tex. Oct. 29, 2019).
1033	Second Amended Docket Control Order, *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-00347, ECF No. 39 (E.D. Tex. Apr. 21, 2020).
1034	Cover Pleading to Acorn's Preliminary Infringement Contentions in *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-00347 (March 9, 2020).
1035	Exhibit E to Acorn's Preliminary Infringement Contentions in *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-00347 (March 9, 2020).

All citations to specific pages of exhibits follow the pagination added to those exhibits per 37 C.F.R. § 42.63(d)(2)(i).

I. Introduction

Petitioner Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review and cancellation of Claims 1-4, 6, 8, 10-13, 15-20, 22, and 25-30 ("the challenged claims") of U.S. Patent No. 9,905,691 ("the '691 Patent"), assigned to Acorn Semi, LLC ("Acorn"). The '691 Patent purports to claim a priority date of August 12, 2002 through a series of parent applications, the earliest of which issued as U.S. Patent No. 7,084,423. ('691 Patent at Cover, 1:8-21; Ex. 1003.)

The '691 Patent and the challenged claims generally relate to metal-semiconductor junctions with an interface layer between the metal and the semiconductor. ('691 Patent at 1:25-29.) The interface layer includes both a semiconductor oxide and a generic metal oxide. (*Id.* at Claims 1-4, 6, 8, 10-13, 15-20, 22, 25-30, Certificate of Correction.) But not all of the parent applications of the '691 Patent describe the genus of metal oxides. Indeed, the first time the patentee even arguably described a generic metal oxide for an interface layer was in the originally filed claims of parent application U.S. Patent App. No. 13/022,522—which was not filed until February 7, 2011. (Ex. 1010, at 48.) As a result, no challenged claim can possibly obtain a priority date earlier than February 7, 2011.

Claims 18 and 25-30 cannot even obtain that February 7, 2011 date: none of the '691 Patent's parent applications enables the full scope of their open-ended recitations of a specific contact resistivity "less than 1 Ω-μm^2." Specific contact resistivity is also called specific contact resistance. (Carver at 2.) Although the specification that the '691 Patent shares with its parent applications purports to describe achieving some "minimum specific contact resistance," that shared specification does not put a lower bound on that "minimum specific contact resistance." ('691 Patent at 4:8-22.) Nor does it describe how to achieve specific contact resistances (resistivities) down to and including approximately zero.

That, however, did not stop the patentee from attempting to tie up future efforts to reduce specific contact resistivity via open-ended claiming. Instead of claiming, for instance, an electrical junction with "a specific contact resistivity between approximately 1000 Ω-μm^2 and 1 Ω-μm^2," the inventors drafted unbounded claims whose specific contact resistivity is "less than 1 Ω-μm^2." With no lower bound to that specific contact resistivity limitation, no parent application can enable the ***full*** scope of any of Claims 18 and 25-30, including specific contact resistivities down to and including approximately zero. And Claim 30 has yet another deficiency: no parent application of the '691 Patent describes its recitation of "a stack of metals deposited on the interface layer." Thus, Claims 18 and 25-30 cannot obtain a filing date any earlier than that of the '691 Patent: February 19, 2016.

Under either the February 7, 2011 or the February 19, 2016 priority date, U.S. Patent No. 7,176,483 (Ex. 1015, "Grupp '483")—which issued in 2007 and which has the same ancestor as the '691 Patent—qualifies as prior art to the challenged claims. As shown herein and as further explained in the declaration of Dr. E. Fred Schubert, an expert in metal-semiconductor junctions with more than thirty years of experience (Schubert Decl. ¶¶ 8-21), Grupp '483 anticipates every challenged claim. Petitioner therefore respectfully requests that the Board institute *inter partes* review, hold the challenged claims unpatentable, and cancel the challenged claims.

II. Mandatory Notices

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner identifies itself; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC as real parties-in-interest.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

1. Judicial Matters

The following judicial matters may affect or be affected by this proceeding: *Acorn Semi, LLC v. Samsung Electronics Co. Ltd.*, Civil Action No. 2:19-cv-347 (E.D. Tex.) ("the Acorn Litigation"), in which Patent Owner Acorn Semi, LLC ("Acorn") filed a complaint alleging that Petitioner and its real parties-in-interest infringe the '691 Patent. (Ex. 1031 ¶¶ 98-107.) Acorn first served that complaint on October 24, 2019. (Ex. 1032.)

2. Administrative Matters

Public PAIR lists the following patents and applications that purport to claim the benefit of the priority of the filing date of the '691 Patent:

Patent or Application No.	Filing Date
U.S. Patent No. 9,812,542	August 30, 2016
U.S. Patent No. 10,388,748	October 9, 2018
U.S. Patent No. 10,090,395	January 23, 2018
U.S. Patent No. 10,186,592	May 16, 2018
U.S. Patent App. No. 16/506,022	July 9, 2019

Petitioner is concurrently filing one or more petitions for *inter partes* review against the following patents related to the '691 Patent: U.S. Patent No. 7,084,423; U.S. Patent No. 8,766,336; U.S. Patent No. 9,209,261; U.S. Patent No. 9,461,167; and U.S. Patent No. 10,090,395. Those proceedings may affect or be affected by this proceeding. Further, Acorn has asserted those five other patents against Petitioner and its real parties-in-interest in the Acorn Litigation. (Ex. 1031 ¶¶ 68-97, 108-117.)

C. Designation of Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

With this petition, Petitioner is filing a power of attorney appointing the practitioners associated with Customer Number 132,593. Petitioner designates the following lead and back-up counsel:

Lead Counsel	Back-up Counsel
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D. Service Information (37 C.F.R. § 42.8(b)(4))

Please direct all correspondence to lead and back-up counsel at the addresses listed above. Petitioner consents to electronic service at the following email addresses: jdesmarais@desmaraisllp.com; kkm-ptab@desmaraisllp.com; cmaier@desmaraisllp.com; and tkonstantakopoulos@desmaraisllp.com.

III. Fees

Petitioner is concurrently electronically submitting the required fees for this Petition. The Board is authorized to charge Desmarais LLP's deposit account, No. 50-6822, for any fee deficiency.

IV. Grounds for Standing

Petitioner certifies that the ’691 Patent is available for *inter partes* review. Petitioner further certifies that neither Petitioner nor any real party-in-interest or privy is estopped or barred from requesting *inter partes* review of the challenged claims on the grounds identified in this petition.

V. Identification of Challenge and Relief Requested

Petitioner requests *inter partes* review and cancellation of Claims 1-4, 6, 8, 10-13, 15-20, 22, 25-30 of the ’691 Patent.

A. Identification of Prior Art

1. Grupp ’483 (Ex. 1015)

As discussed in detail below in **Section IX**, no challenged claim is entitled to a priority date earlier than February 7, 2011, the filing date of U.S. Patent App. No. 13/022,522. U.S. Patent No. 7,176,483 to Grupp et al. (Ex. 1015, “Grupp ’483”), issued on February 13, 2007, qualifies as prior art to all challenged claims either at least pre-AIA 35 U.S.C. § 102(b).

Further, Claims 18 and 25-30 cannot even obtain that February 7, 2011 priority date; instead, their priority date can be no earlier than the filing date of the ’691 Patent on February 19, 2016. Grupp ’483 also qualifies as prior art to Claims 18 and 25-30 under AIA 35 U.S.C. § 102(a)(1).

B. Statutory Grounds of Unpatentability

Ground 1: Grupp '483 anticipates Claims 1-4, 6, 8, 10-13, 15-20, 22, 25-30 under at least pre-AIA 35 U.S.C. § 102(b). Because Claims 18 and 25-30 cannot obtain a priority date earlier than the February 19, 2016 filing date of the '691 Patent, Grupp '483 also anticipates Claims 18 and 25-30 under AIA 35 U.S.C. § 102(a)(1).

VI. Overview of the '691 Patent

A. Technical Background

Metal-semiconductor junctions are a basic electronic component. (Schubert Decl. ¶¶ 34-35; '691 Patent at 1:33-34.) Those junctions are generally characterized by a barrier to the movement of charge carriers at the interface between the metal and the semiconductor, called a Schottky barrier. (Rhoderick at 1; '691 Patent at 1:46-48; Schubert Decl. ¶ 36.) The barrier's width and its height each affect the junction's specific contact resistance. (Chang at 5-6; Schubert Decl. ¶¶ 37-43.)

The Schottky barrier height of a metal-semiconductor junction can become fixed at a particular height in a phenomenon known as Fermi-level pinning. ('691 Patent at 2:4-61, 5:24-27, 7:44-48; Schubert Decl. ¶¶ 44-48.) Electron states, including Bardeen states (such as dangling bonds at the semiconductor surface) and metal-induced gap states (energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal), can cause the Fermi level to become pinned between the semiconductor's conduction and valence bands, typically at or near the midgap. ('691 Patent at 2:35-3:3, 16:52-55; Schubert Decl. ¶¶ 48-49.) Fig. 7a shows a metal-semiconductor junction with a pinned Fermi level:

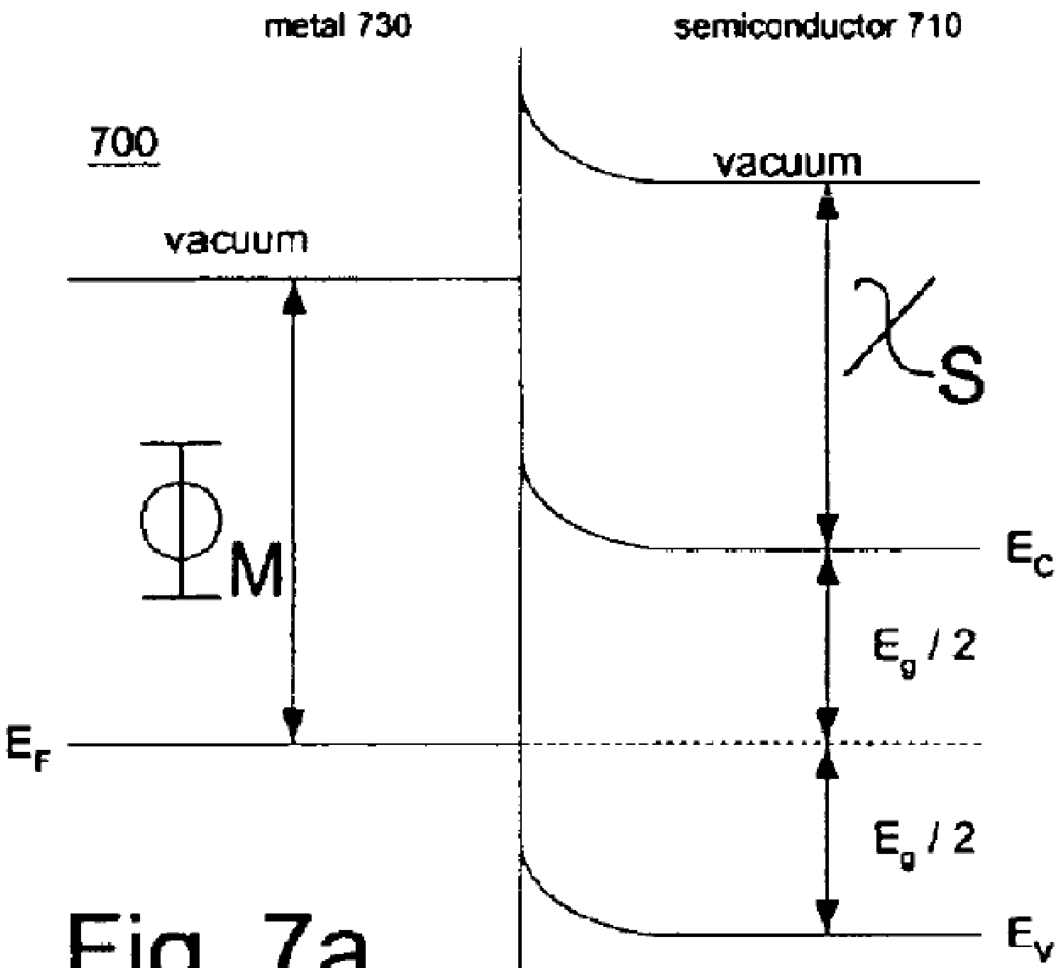


Fig. 7a

('167 Patent at Fig. 7a, 16:52-55.)

As Fig. 7a depicts, the pinned Fermi level E_F is not aligned with the conduction band edge E_C of the semiconductor at the interface. For an n-type semiconductor, the difference between the Fermi level E_F and the conduction band edge of the semiconductor E_C at the interface produces a barrier to the flow of electrons of height Φ_b, as shown in Fig. 4 of the '691 Patent:

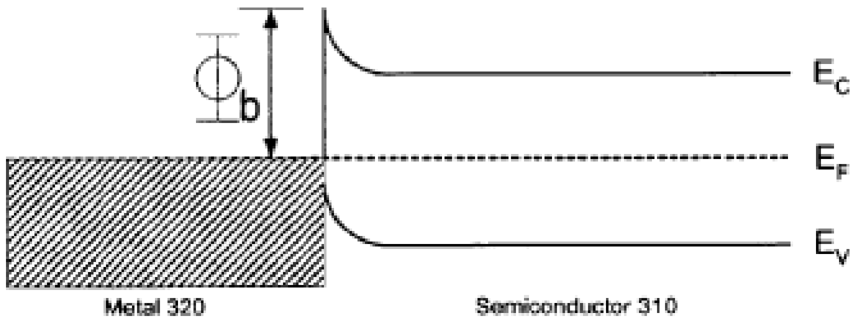


Fig. 4 (Prior Art)

('691 Patent at Fig. 4, 4:40-41, 7:24-48; Schubert Decl. ¶ 49.)

"The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics." ('691 Patent at 3:4-8.) According to the '691 Patent, depinning a Fermi level is one technique for accomplishing that. (*Id.* at 16:23-44, Schubert Decl. ¶ 50.) But even before the earliest alleged priority date of the '691 Patent, techniques for depinning a Fermi level and controlling barrier height were well-known, as were techniques for reducing specific contact resistance. (Schubert Decl. ¶¶ 51-53.)

Indeed, even before the earliest alleged priority date of the challenged claims in August 2002, the prior art was replete with examples of interface layers that depin a Fermi level by passivating the semiconductor surface (thereby satisfying dangling bonds and reducing Bardeen states) and reducing the effects of metal-induced gap states, including the examples described in the Goodnick, Rhoderick, and

Sobolewski references. (Schubert Decl. ¶¶ 52-55; Goodnick at 1; Rhoderick at 3, Sobolewski at 1.) It was similarly known that an interfacial oxide could reduce the barrier height of a metal-semiconductor junction. (Schubert Decl. ¶¶ 56-58; Risko at 1:43-50; Taubenblatt 1984 at 3.) Likewise, prior art spanning three decades taught that an interface layer could reduce the specific contact resistance of a metal-semiconductor junction: for example, the 1976 Schroen patent, the 1989 Kim patent, and the 1999 Iwaguro patent application publication. (Schubert Decl. ¶¶ 59-63; Schroen at Abstract; Kim at 4:63-5:1, 5:27-30; Iwaguro at [0005]-[0006], [0012]-[0014].)

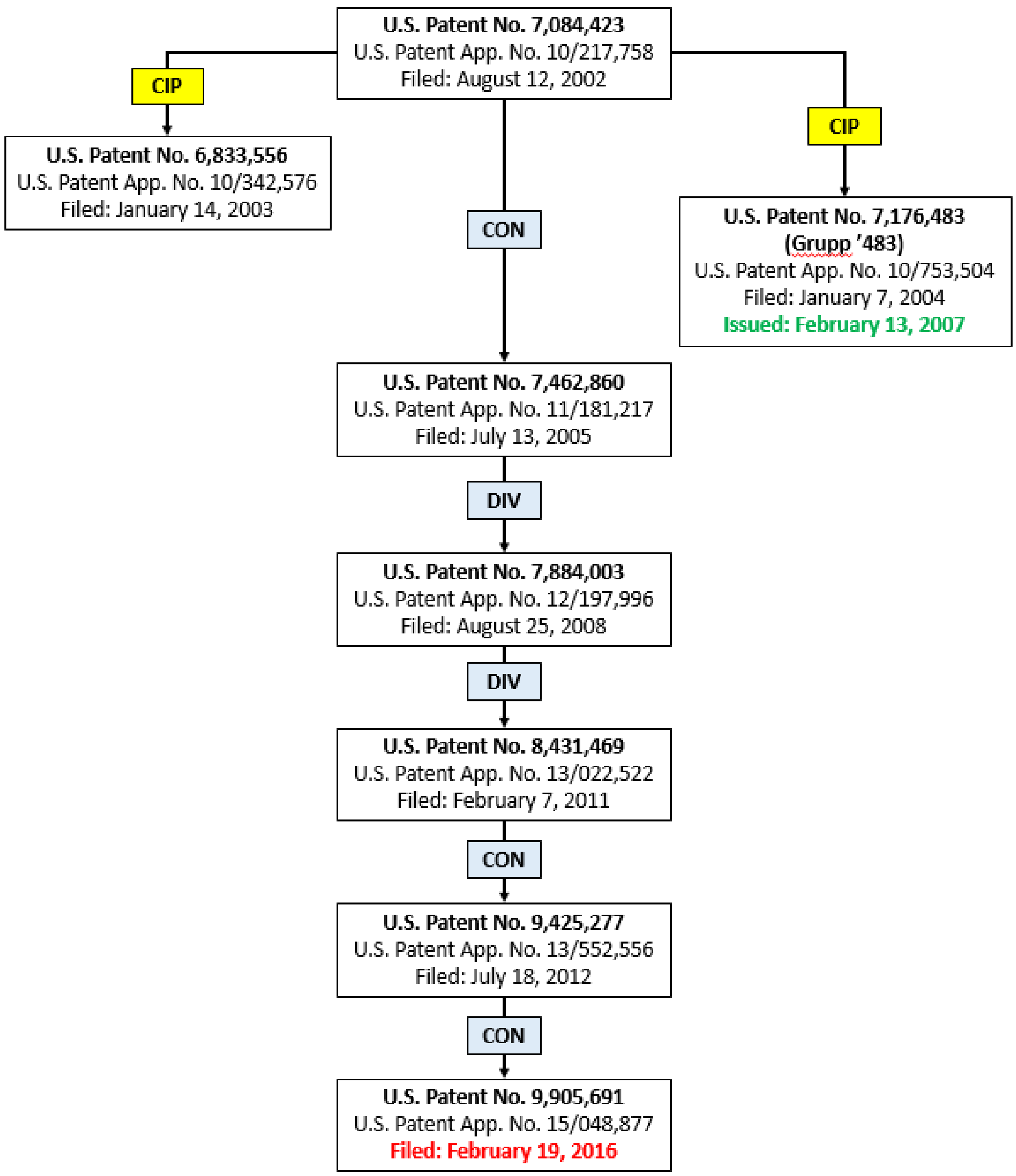
B. The Purported Invention of the ’691 Patent

The purported invention of the ’691 Patent, like the prior art, involves providing an interface layer between the metal and the semiconductor in a metal-semiconductor junction. (’691 Patent at 1:25-39.) Claim 25 illustrates that uninventive approach:

> An electrical junction comprising an interface layer disposed between a contact metal and a semiconductor, the semiconductor comprising a source or drain of a transistor, the interface layer comprising a metal oxide separation layer and a semiconductor oxide passivation layer and configured to provide a specific contact resistivity between the contact metal and the semiconductor of less than 1 Ω-μm^2.

C. Prosecution History

The '691 Patent began as U.S. Patent App. No. 15/048,877 ("the '877 Application"), filed on February 19, 2016. (Ex. 1014, at 9, 73.) The '691 Patent purports to claim a priority date of August 12, 2002 through a series of parent applications, as shown in the partial family tree below:



(Ex. 1005, at Cover; Ex. 1014, at 9; Grupp '483 at Cover, 1:8-19.)

Each challenged claim was among the originally filed claims of the ’877 Application. (Ex. 1014, at 61-64.) In June 2016, the Examiner signed the applicants’ information disclosure statements and allowed the originally filed claims on the first action. (*Id.* at 118-130, 142-152.) The Examiner’s stated reasons for allowance tracked the language of originally filed Claims 1 and 25. (*Id.* at 123-124.)

After that June 2016 notice of allowance, the applicants paid the issue fee, but the ’877 Application did not issue. (Ex. 1014, at 158.) But in February 2018, the Examiner entered a corrected notice of allowance with an Examiner’s amendment to Claims 1, 6, 15, and 19. (*Id.* at 163-168.) The ’877 Application then issued as the ’691 Patent. But, the Examiner’s amendment in the corrected notice of allowance did not make it into the issued claims. The patentee requested a certificate of correction to effect the Examiner’s amendment, and the Office granted that request. (*Id.* at 183-187, 191.) This petition addresses the claims as corrected.

Notably, the Examiner did not cite any prior art against any claim during the prosecution of the ’877 Application, nor did the Examiner expressly determine any of the claims’ priority dates.

VII. Level of Ordinary Skill in the Art

Any of the following combinations of education and experience would have qualified someone as an ordinarily skilled artisan in the field of the ’691 Patent:

- a Ph.D. in electrical engineering, physics, materials science, or chemical engineering, with two years of practical experience with semiconductor research and design;
- a Master's degree in electrical engineering, physics, materials science, or chemical engineering, with four years of practical experience with semiconductor research and design; or
- a Bachelor's degree in electrical engineering, physics, materials science, or chemical engineering, with six to eight years of practical experience with semiconductor research and design. (Schubert Decl. ¶¶ 70-71.)

Further, additional education could make up for less practical experience, and vice versa. (*Id.*) The same level of ordinary skill would have been applicable in August 2002, February 2011, or February 2016. (*Id.*)

VIII. Claim Construction

For petitions filed after November 13, 2018, the Board "constru[es] the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b); *see also Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). The Board need only construe claim terms to the extent necessary to resolve a controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Below, Petitioner construes the term "specific contact resistivity." As for all remaining claim terms, the challenged claims are unpatentable under those terms' ordinary and customary meanings, as explained in detail below. The Board need not expressly construe any other term at this stage.[1]

A. Claims 18 and 25-30: "specific contact resistivity"

The term "specific contact resistivity" appears in Claims 18 and 25-30. Ordinarily skilled artisans commonly (if not universally) used the terms "specific contact resistivity" and "specific contact resistance" interchangeably. (Carver at 2; *see also* Schubert Decl. ¶¶ 74-76.) The '691 Patent's use of "specific contact resistivity" in Claims 18 and 25-30 tracks that common interchangeable use: the specification of the '691 Patent never uses the phrase "specific contact resistivity," but it does discuss specific contact resistance as part of the invention. (*E.g.*, '691 Patent at 3:19-23, 3:36-39, 3:46-47, 4:14-22.) Thus, an ordinarily skilled artisan

[1] Petitioner reserves all rights to raise claim construction arguments and other arguments in the Acorn Litigation or other proceedings involving the '691 Patent. For example, Petitioner has not raised all of its challenges to the '691 Patent here, including invalidity under 35 U.S.C. § 112. Further, comparing the claims to the accused products in the Acorn Litigation may raise controversies that require claim construction in that litigation, but not here.

would have understood the term "specific contact resistivity" to refer to specific contact resistance in Claims 18 and 25-30. (Schubert Decl. ¶¶ 74-76.)

IX. The challenged claims are not entitled to any priority date before February 7, 2011.

The '691 Patent purports to claim priority to August 12, 2002, the filing date of the application that issued as U.S. Patent No. 7,084,423. ('691 Patent at Cover, 1:8-21; Ex. 1003, at Cover.) For the challenged claims to receive the benefit of the priority of that August 12, 2002 filing date, every application in the priority chain leading to the application that issued as the '691 Patent must support every limitation of the challenged claims under 35 U.S.C. § 112 ¶ 1. *In re NTP, Inc.*, 654 F.3d 1268, 1277 (Fed. Cir. 2011). Thus, every parent application of the '691 Patent must both describe and enable every limitation of every challenged claim. *Id.*; *Fiers v. Revel*, 984 F.2d 1164, 1169-70 (Fed. Cir. 1993).

But the challenged claims have at least three limitations that the parent applications fail to support: (1) a generic "metal oxide" for an interface layer as in every challenged claim; (2) "a stack of metals deposited on the interface layer" as in Claim 30; and (3) a specific contact resistivity of less than "1 Ω-μm^2" in Claims 18 and 25-30. Those unsupported limitations are discussed below with reference to the '395 Patent's disclosure, including incorporated-by-reference U.S. Patent No. 6,833,556. (Ex. 1005.) The parent applications' specifications and figures are substantively identical to the '691 Patent, including in their incorporation by reference of U.S. Patent No. 6,833,556. Thus, if a limitation lacks support in the ’395 Patent’s disclosure, it also lacks support in the parent applications’ disclosures, and vice versa. (Ex. 1002, at 5-52; Ex. 1003; Ex. 1006, at 3-42; Ex. 1007; Ex. 1008, at 8-49; Ex. 1009; Ex. 1010, at 14-51; Ex. 1011; Ex. 1012, at 6-46; Ex. 1013; Schubert Decl. ¶¶ 84-86, 102-104.)

The only differences among the parent applications and the ’691 Patent are their respective abstracts and claims. But, even those abstracts and claims cannot provide the challenged claims with any priority date earlier than February 7, 2011. In particular, the patentee did not even arguably disclose a generic “metal oxide” for an interface layer until February 7, 2011, in the originally filed claims of U.S. Patent App. No. 13/022,522. (Ex. 1010, at 48; Schubert Decl. ¶¶ 89-90.)

Thus, no challenged claim can possibly obtain a priority date earlier than February 7, 2011. *In re NTP*, 654 F.3d at 1276-77. Claims 18 and 25-30 fare even worse than that. No parent application describes Claim 30’s “stack of metals deposited on the interface layer; and no parent application enables the full scope of the limitation “a specific contact resistivity “less than 1 Ω-μm^2” as in Claims 18 and 25-30. That leaves Claims 18 and 25-30 with a priority date no earlier than February 19, 2016, the filing date of the ’691 Patent. But Grupp ’483, which issued in 2007, qualifies as prior art under 35 U.S.C. § 102(b) to every challenged in even the best-case scenario for those challenged claims, and it also qualifies as prior art under AIA 35 U.S.C. § 102(a)(1) to Claims 18 and 25-30.

A. The ’691 Patent’s parent applications do not describe every limitation of the challenged claims.

As discussed above, the challenged claims cannot obtain their alleged August 12, 2002 priority date unless all of the ’691 Patent’s parent applications describe all of their limitations. *In re NTP*, 654 F.3d at 1277. “[T]he test for sufficiency is whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). Thus, “[a] disclosure in a parent application that merely renders the later-claimed invention obvious is not sufficient to meet the written description requirement; the disclosure must describe the claimed invention with all its limitations.” *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1158 (Fed. Cir. 1998). Here, there are two limitations lacking written description support throughout the ’691 Patent’s parent applications: (1) a generic “metal oxide” for an interface layer as in every challenged claim; and (2) “a stack of metals deposited on the interface layer” as in Claim 30.

1. All Challenged Claims: No parent application before February 7, 2011 describes a generic "metal oxide" layer.

To support a claim to a genus, the specification must disclose "either a representative number of species falling within the scope of the genus or structural features common to the members of the genus so that one of skill in the art can 'visualize or recognize' the members of the genus." *Ariad*, 598 F.3d at 1350. Here, every challenged claim includes a generic "metal oxide" interface layer. The first time that the patentee even arguably disclosed a generic "metal oxide" interface layer is in the originally filed claims of U.S. Patent App. No. 13/022,522, filed on February 7, 2011. (Ex. 1010, at 48; Schubert Decl. ¶ 89.) The only possible example of a metal oxide interface layer described in any earlier parent application is a TiO_2 spacer layer: "[s]pacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV)." ('691 Patent at 14:45-52; Schubert Decl. ¶ 90.)

Although incorporated-by-reference U.S. Patent No. 6,833,556 describes a generic metal oxide and four example metal oxides, those metal oxides are only used to electrically isolate a transistor's gate from its channel "such that essentially no current flows between the gate 270 and the channel 220"—not as an interface layer through which current does flow, as is claimed. (Ex. 1005, at 7:60-8:22, *see also id.* at 13:44-14:20; '691 Patent at 14:45-52; Schubert Decl. ¶ 91.) Even if Acorn contends that those metal oxides could have been suitable for use as the claimed interface layers, U.S. Patent No. 6,833,556 does not describe using them for that purpose. (Schubert Decl. ¶¶ 92-93; Ex. 1005, at 7:60-8:22, 13:44-14:20.) And even if it would have been obvious to use them for that purpose, that still would not have satisfied the written description requirement. *Tronzo*, 156 F.3d at 1158.

Thus, the relevant question is whether the earlier parent applications' statement that "[s]pacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV)" provides written description of the entire genus of metal oxide interface layers. ('691 Patent at 14:45-52.) And the answer is no: some metal oxides present considerably higher barriers than the "barrier of less than 1 eV" ascribed to TiO_2. For example, hafnium oxide and zirconium oxide are metal oxides with barriers to aluminum of 2 eV and 2.43 eV, respectively—well above the "less than 1 eV" presented by TiO_2 as described in the '691 Patent's parent applications. ('691 Patent at 14:45-52; Lang at 4; Zheng at 1; Schubert Decl. ¶ 94.) Moreover, aluminum is identified as a low workfunction metal in the '691 Patent's parent applications. ('691 Patent at 13:58-63.) Hafnium oxide and zirconium oxide present even higher barriers to metals with high workfunctions. (*Id.* at 13:64-67; Schubert Decl. ¶ 95.)

That discrepancy shows that neither TiO_2 nor "lower barriers" represents the full genus of metal oxides. Those disclosures, whether taken alone or together, do not reflect the full variation across the genus of metal oxide interface layers, including the variation in barrier heights across the genus of metal oxide interface layers. Thus, no application prior to U.S. Patent App. No. 13/022,522 provides written description of a generic "metal oxide" interface layer.

Indeed, "[a] patentee will not be deemed to have invented species sufficient to constitute the genus by virtue of having disclosed a single species when, as is the case here, the evidence indicates ordinary artisans could not predict the operability in the invention of any species other than the one disclosed." *In re Curtis*, 354 F.3d 1347, 1358 (Fed. Cir. 2004). *In re Curtis* involved claims directed to PTFE dental floss reciting a genus of friction-enhancing coatings, but the specification only identified only one friction-enhancing coating: microcrystalline wax (MCW). *Id.* at 1349, 1358. Because neither the specification nor any other evidence conveyed that any other coating was suitable as a friction-enhancing coating for PTFE dental floss, the Federal Circuit held that the lone disclosed example could not support a claim to a genus of friction-enhancing coatings. *Id.* at 1358.

Like the lone example in *In re Curtis*, TiO_2 is the only metal oxide interface layer disclosed in the parent applications predating U.S. Patent App. No. 13/022,522. Finally, Acorn's own complaint alleges that the operability of the claimed interface layers was unpredictable; indeed, it alleges that using ***any*** interface layer was "counter-intuitive." (Ex. 1031 ¶¶ 6, 48; Schubert Decl. ¶ 96.) Thus, just as the lone example of MCW in *In re Curtis* could not support a claim to the genus of friction-enhancing coatings, the previous parent applications' lone example of TiO_2 as a spacer layer cannot support claims to a generic "interface layer comprising a metal oxide." Accordingly, no challenged claim can possibly obtain a priority date earlier than February 7, 2011, the filing date of U.S. Patent App. No. 13/022,522. (Schubert Decl. ¶ 97.)

2. Claim 30: No parent application describes "a stack of metals deposited on the interface layer."

Claim 30 fares even worse than its brethren: it cannot obtain a priority date before the '691 Patent's filing date because no parent application describes "a stack of metals deposited on the interface layer." Although the '691 Patent and its parent applications describe depositing a metal on an interface layer, and although they describe various examples of metals for depositing on the interface layer, none describes depositing a stack of metals on an interface layer. At most, they describe depositing a single body of metal or alloy on an interface layer. ('691 Patent at Fig. 6, Figs. 7a-7d, 11:15-19, 13:45-67; Schubert Decl. ¶ 99.) The same is true of the incorporated-by-reference disclosure of U.S. Patent No. 6,833,556. (Ex. 1005, at Figs. 1-3, Fig. 6B, 4:64-67, 7:8-12, 7:49-53, 8:67-9:6, 14:54-67; Schubert Decl. ¶¶ 99-100.)

B. Claims 18 and 25-30: No parent application enables the full scope of the "specific contact resistivity . . . less than 1 Ω-μm^2" limitations.

"The enablement requirement asks whether 'the specification teach[es] those in the art to make and use the invention without undue experimentation.'" *Enzo Life*

Scis., Inc. v. Roche Molecular Sys., Inc., 928 F.3d 1340, 1345 (Fed. Cir. 2019), *cert. denied*, 589 U.S. ___ (Mar. 30, 2020) (quoting *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988)). "This important doctrine prevents both inadequate disclosure of an invention and overbroad claiming that might otherwise attempt to cover more than was actually invented." *Magsil Corp. v. Hitachi Global Storage Techs., Inc.*, 687 F.3d 1377, 1380-81 (Fed. Cir. 2012). Thus, "the specification must teach those of skill in the art how to make and how to use the invention as broadly as it is claimed." *In re Goodman*, 11 F.3d 1046, 1050 (Fed. Cir. 1993).

The disclosure that the '691 Patent shares with its parent applications falls well short of that mark. Claims 18 and 25-30 recite or include "a specific contact resistivity . . . less than 1 Ω-μm^2." As written, that claim limitation has no lower bound on specific contact resistivity. The specification imposes no lower bound on specific contact resistivity, either, as it does not quantify or describe any lower bound for the "minimum specific contact resistance" that it purports to describe. ('961 Patent at Fig. 8, 4:9-22, 14:29-49.) Thus, the "less than 1 Ω-μm^2" part of that limitation encompasses specific contact resistivities down to and including approximately zero.

But specific contact resistances down to and including approximately zero cannot be achieved according to the teachings of the '691 Patent and its parent applications. Their shared disclosure purports to describe an interface layer that minimizes the total specific contact resistance (specific contact resistivity) of a metal-semiconductor junction, represented below by the "total current" curve that sums (1) resistance to tunneling current and (2) resistance to current by electron emission:

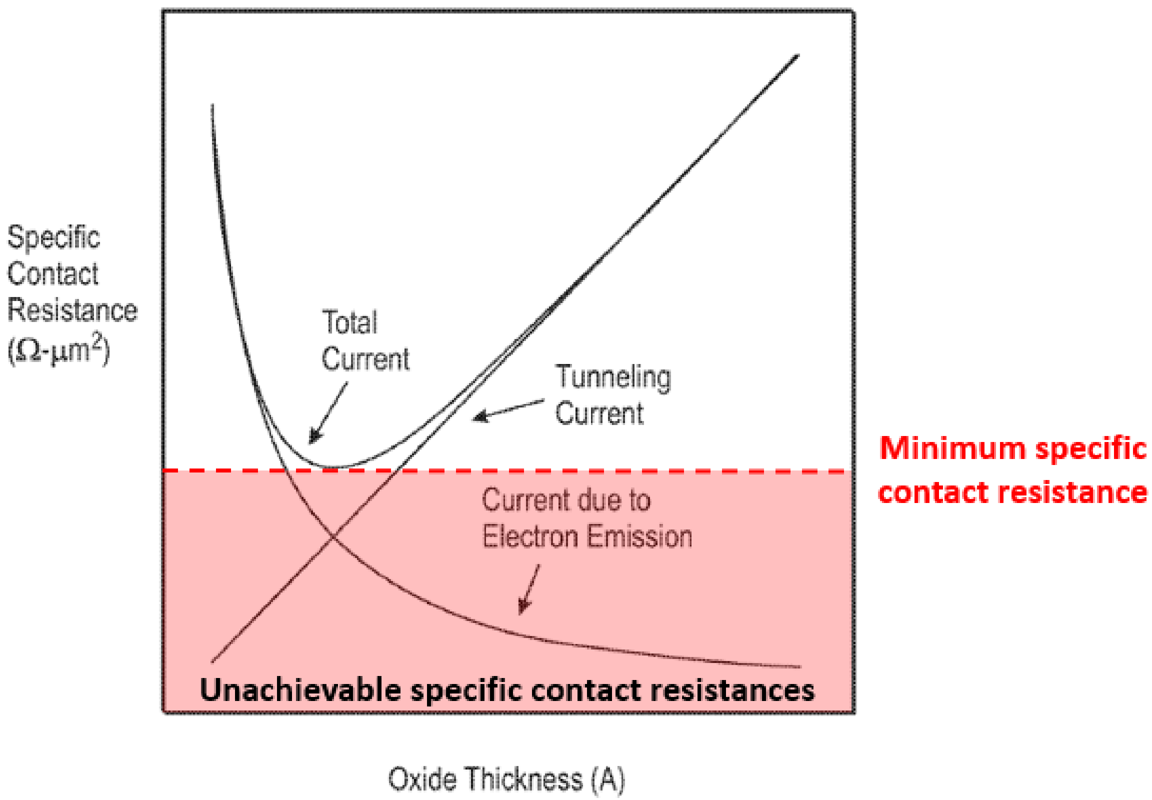


Fig. 8

('691 Patent at Fig. 8 (annotations added), 14:29-49; Schubert Decl. ¶¶ 105-107.)

As can be seen from the annotated figure above, the nadir of Fig. 8's "total current" curve indicates a range of specific contact resistivities down to and including approximately zero that an ordinarily skilled artisan could not have attained by following the teachings of the '691 Patent and its parent applications.

Thus, those parent applications fail to enable the ***full*** scope of the "specific contact resistivity . . . less than 1 Ω-μm^2" limitations in Claims 18 and 25-30.

Nor should the Board constrain "less than 1 Ω-μm^2" to some lower bound in order to enable Claims 18 and 25-30. That would be tantamount to redrafting those claims, and the Federal Circuit "repeatedly and consistently has recognized that courts may not redraft claims, whether to make them operable or to sustain their validity." *Chef America, Inc. v. Lamb-Weston, Inc.*, 358 F.3d 1371, 1374 (Fed. Cir. 2004). Rather, "a patentee chooses broad claim language at the peril of losing any claim that cannot be enabled across its full scope of coverage." *Magsil*, 687 at 1381.

Indeed, Claims 18 and 25-30 closely resemble the non-enabled claims in *Magsil*. *Magsil* involved claims to a tri-layer tunnel junction "wherein applying a small magnitude of electromagnetic energy to the junction reverses at least one of the magnetization directions and causes a change in the resistance by at least 10% at room temperature." 687 F.3d at 1379. While the patent at issue described certain resistance change values within that range—"as much as 11.8% change was seen"—the inventors did not attain even an 18% change until after the filing date. *Id.* at 1381-82. The district court nonetheless followed the plain language of the claims in construing them to cover from a 10% change to an infinite percentage change in resistance. *Id.* at 1382. It then granted the defendant summary judgment that the claims were not enabled. *Id.* at 1380.

The Federal Circuit affirmed both the district court's claim construction and its enablement decision. *Magsil*, 687 F.3d at 1382-85. Noting that the patentee chose to draft open-ended claims, it held the patentee to the consequences of that choice: "MagSil's difficulty in enabling the asserted claims is a problem of its own making." *Id.* at 1384. The Court emphasized the lack of working examples in the specification, and further noted that junctions with even a 100% to 120% change in resistance had not been developed until twelve years after the patent's filing date. *Id.* at 1381-82. That led the Federal Circuit to uphold the district court's summary judgment of non-enablement. *Id.* at 1382.

Claims 18 and 25-30 are no better off than the non-enabled claims in *Magsil*. The disclosure that the '691 Patent shares with its parent applications does not describe ***any*** working examples of an electrical junction with a specific contact resistivity under 1 Ω-μm^2, down to and including approximately zero—a range encompassed by each of Claims 18 and 25-30. Worse still, despite the '691 Patent and its parent applications expressly teaching that the disclosed techniques cannot reduce specific contact resistivity below some unspecified minimum, the patentee nonetheless drafted open-ended claims with no lower bound on specific contact resistivity. ('691 Patent at Fig. 8, 14:29-49; Schubert Decl. ¶¶ 105-108.)

Because Claims 18 and 25-30 encompass a range of specific contact resistivities down to and including approximately zero that cannot be achieved according to the '691 Patent's parent applications, those parent applications cannot enable the full scope of the challenged claims. *Magsil*, 687 F.3d at 1382. And when the breadth of a claim alone indicates that the claim is not enabled—as is the case here—that disposes of the enablement issue in its entirety, as it did in *Magsil*. *CommVault Sys., Inc. v. Realtime Data, LLC*, Case IPR2017-01710, Paper 11, at 20 (PTAB Jan. 18, 2018) (citing *Magsil*, 687 F.3d at 1382). Because no parent application enables the full scope of the challenged claims, their priority date is the filing date of the '691 Patent: February 19, 2016.

* * *

In sum, no challenged claim can obtain a priority date earlier than February 7, 2011, when the applicants first disclosed a generic "metal oxide" interface layer. Further, Claims 18 and 25-30 cannot obtain a priority date earlier than the '691 Patent's filing date of February 19, 2016, as no parent application supports those claims. Under either date, Grupp '483 qualifies as prior art, and it anticipates every challenged claim.

X. The challenged claims are unpatentable.

A. Ground 1: Grupp '483 anticipates Claims 1-4, 6, 8, 10-13, 15-20, 22, 25-30.

1. Overview of Grupp '483

Grupp '483 is a continuation-in-part of an August 2002 application that issued as U.S. Patent No. 7,084,423. (Grupp '483 at Cover, 1:8-19.) The '691 Patent purports to claim priority to that same August 2002 application through a chain of parent applications. ('691 Patent at Cover, 1:8-21.) Thus, Grupp '483 (on the one hand) and the '691 Patent and its parent applications (on the other hand) have significantly overlapping disclosures. But, Grupp '483 discloses at least one claim feature missing from the '691 Patent's parent applications: Claim 30's "stack of metals deposited on the interface layer." (Grupp '483 at 14:38-41, 14:50-53, Claim 10; Ex. 1028, at 25.) Thus, Grupp '483 teaches more of the claimed subject matter than even the '691 Patent's parent applications. And, Grupp '483 anticipates every challenged claim.

2. Claim 1

i. A structure, comprising

The preamble is not limiting. Nonetheless, Grupp '483 discloses a structure: an electrical junction. (Schubert Decl. ¶ 110.) For example, "[i]n one embodiment, the present invention provides an electrical junction that includes a semiconductor (e.g., C, Ge, or an Si-based semiconductor), a conductor, and an interface layer disposed therebetween." (Grupp '483 at 3:44-47; *see also id.* at 3:18-22, 5:49-58, 19:26-27.)

ii. a semiconductor region in a substrate,

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 111-112.) For example, "[t]he present inventors have determined that for thin interface layers disposed between a metal and a semiconductor (e.g., C, Ge, Si, SiC and SiGe), so as to form a metal—interface layer–semiconductor junction, there exist corresponding minimum specific contact resistances." (Grupp '483 at 3:18-22.) "In one embodiment, the present invention provides an electrical junction that includes a semiconductor (e.g., C, Ge, or an Si-based semiconductor), a conductor, and an interface layer disposed therebetween." (*Id.* at 3:44-47.)

One example of a semiconductor region in a substrate that Grupp '483 discloses is a source or drain of a transistor. (Schubert Decl. ¶ 112.) In a section on "Transistors Containing Passivated Semiconductor Surfaces," Grupp '483 discloses that "the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility)." (Grupp '483 at 18:19-20, 19:11-15.) As Dr. Schubert explains, "[g]enerally, in a transistor, a 'well' is a doped region of a semiconductor in which source and drain regions are formed by implanting dopants; the source and drain regions have a doping opposite that of the well." (Schubert Decl. ¶ 112.)

iii. a metal electrical contact to said semiconductor region, and

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 113.) For example, "[i]n further embodiments the present invention provides an electrical device in which an interface layer is disposed between and in ***contact with a metal*** and a semiconductor . . . ." (Grupp '483 at 4:21-23; *see also id*. at Fig. 7d, 3:18-22, 3:44-47, 5:49-58, 18:4-17 (describing an interface layer between silicon and aluminum).)

iv. a metal oxide layer, and

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 114-117.) As discussed above in **Section X.A.2.iii**, Grupp '483 discloses an interface layer "disposed between and in contact with a metal and a semiconductor . . . ." (Grupp '483 at 4:21-23.) Grupp '483 further discloses that the interface layer includes (1) a passivation layer, which can be a semiconductor oxide; and (2) a separation layer. (*Id.* ¶ 114.) "The interface layer includes a passivating material, for example, a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of the semiconductor, and in some cases may also include a ***separation layer***." (Grupp '483 at 3:53-56; *see also id.* at 4:28-31, 4:53-55, 8:64-9:10, 9:39-43, 10:34-44, 10:48-54, 10:60-63, 11:35-38, 13:41-46.)

Turning specifically to the separation layer, Grupp '483 further discloses that the separation layer can be an oxide. (Grupp '483 at 11:35-38.) More specifically, Grupp '483 discloses that the separation layer can be a "spacer layer" of TiO_2, which is titanium dioxide: "[s]pacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV)." (*Id.* at 18:65-67; *see also id.* at 18:45-65; Schubert Decl. ¶ 116.) Thus, Grupp '483 discloses an interface layer that includes a metal oxide layer: titanium dioxide. (Schubert Decl. ¶¶ 116-117.)

v. a passivating dielectric tunnel barrier layer between said semiconductor region and said metal electrical contact,

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 118-124.) As discussed above in **Section X.A.2.iv**, Grupp '483 discloses an interface layer "disposed between and in contact with a metal and a semiconductor . . . ." (Grupp '483 at 4:21-23.) Grupp '483 further discloses that the interface layer disposed between the metal (metal electrical contact) and the semiconductor (semiconductor region) includes (1) a passivation layer, which can be a semiconductor oxide; and (2) a separation layer. (*Id.* ¶ 118.) "The interface layer includes a passivating material, for example, a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of the semiconductor, and in some cases may also include a separation layer." (Grupp '483 at 3:53-56; *see also id.* at 4:28-31, 4:53-55, 8:64-9:10, 9:39-43, 10:34-44, 10:48-54, 10:60-63, 11:35-38, 13:41-46.)

Grupp '483 further discloses using an oxide of silicon as the material for that passivation layer. (Grupp '483 at 10:27-34, 10:48-54, 10:60-63.) Further, Grupp '483 discloses that "passivation layers made using N and/or ***O*** [oxygen] may not require distinct separation layers, as ***these elements may form a layer of a compound of Si*** [silicon] with a thickness that can be varied depending on processing." (*Id.* at 10:60-63.) Although that excerpt discusses examples that "may not require distinct separation layers," Grupp '483 expressly discloses using a separation layer when the passivating material is an oxide. (*Id.* at 11:35-38.) Grupp '483 also discloses silicon dioxide, another oxide of silicon, as a passivating material. (*Id.* at 8:64-9:10.)

Both silicon oxide and silicon dioxide are semiconductor oxides, and semiconductor oxides are examples of dielectric materials. (Schubert Decl. ¶¶ 119-122.) Indeed, U.S. Patent No. 6,833,556, which is incorporated by reference into both the '691 Patent and Grupp '483, identifies "an oxide of a semiconductor" as an example of a dielectric material. (Ex. 1005 at 7:60-61; *see also* '691 Patent at 1:8-21; Grupp '483 at 1:8-19.) Thus, the passivating layers of silicon oxide and silicon dioxide described in Grupp '483 are also dielectric layers.

Finally, Grupp '483 describes those passivating dielectric layers as tunnel barrier layers. "[B]oth types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents . . . The tunnel barrier presented by such a depletion layer may be an order of magnitude thicker than the ***dielectric tunnel barrier*** in the present invention." (*Id.* at 18:45-56; *see also* Schubert Decl. ¶ 123.) Accordingly, Grupp '483 discloses a passivating dielectric tunnel barrier layer between said semiconductor region and said metal electrical contact: a silicon oxide or a silicon dioxide layer.

vi. said semiconductor region being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer and said metal oxide layer,

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 125-126.) For example, "the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a semiconductor and is configured to depin the Fermi level of the semiconductor while still ***permitting current flow between the metal and the semiconductor*** when the electrical device is biased." (Grupp '483 at 4:21-26.) As discussed above in **Sections X.A.2.iv and X.A.2.v**, that interface layer that permits current to flow between the metal and the semiconductor includes the passivating dielectric tunnel barrier layer and the metal oxide layer.

vii. wherein said passivating dielectric tunnel barrier layer comprises a semiconductor oxide.

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 127.) "The interface layer includes a passivating material, for example, a nitride, a fluoride, ***an oxide***, an oxynitride, a hydride and/or an arsenide ***of the semiconductor***, and in some cases may also include a separation layer." (Grupp '483 at 3:53-56; *see also id.* at 4:28-31, 4:53-55, 8:64-9:10, 9:39-43, 10:34-44, 10:48-54, 10:60-63, 11:35-38, 13:41-46.) And, as discussed above in **Section X.A.2.v**, Grupp '483 discloses using that semiconductor oxide, which can be silicon oxide or silicon dioxide, as the passivating dielectric tunnel layer.

3. Claim 2

i. The structure of claim 1,

Grupp ’483 discloses the structure of Claim 1, as discussed above in **Section X.A.2.** (Schubert Decl. ¶ 129.)

ii. wherein the semiconductor oxide comprises an oxide of the semiconductor region.

Grupp ’483 discloses this limitation. (Schubert Decl. ¶¶ 130-132.) As discussed above in **Section X.A.2.v**, Grupp ’483 discloses a passivating dielectric tunnel barrier layer that comprises a semiconductor oxide.

Grupp ’483 further discloses using an oxide of a silicon semiconductor region as the semiconductor oxide in the passivating dielectric tunnel barrier layer. (Grupp ’483 at 10:27-34, 10:48-54, 10:60-63; Schubert Decl. ¶ 131.) Grupp ’483 discloses that “passivation layers made using N and/or ***O*** [oxygen] may not require distinct separation layers, as ***these elements may form a layer of a compound of Si*** [silicon] with a thickness that can be varied depending on processing.” (*Id.* at 10:60-63.) Although that excerpt discusses examples that “may not require distinct separation layers,” Grupp ’483 expressly discloses using a separation layer when the passivating material is an oxide. (*Id.* at 11:35-38.) Finally, Grupp ’483 also discloses silicon dioxide, another oxide of silicon, as a passivating dielectric tunnel barrier layer. (*Id.* at 8:64-9:10; Schubert Decl. ¶ 132.)

4. Claim 3

i. The structure of claim 1,

Grupp '483 discloses the structure of Claim 1, as discussed above in **Section X.A.2.** (Schubert Decl. ¶ 134.)

ii. wherein the semiconductor oxide of the dielectric tunnel barrier layer has a thickness of approximately 0.1 nm to 5 nm.

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 135-136.) "The interface layer includes a passivating material, for example, a nitride, a fluoride, an ***oxide***, an oxynitride, a hydride and/or an arsenide ***of the semiconductor***, and in some cases may also include a separation layer." (Grupp '483 at 3:53-56; *see also id.* at 4:28-31, 4:53-55, 8:64-9:10, 9:39-43, 10:34-38, 10:48-54, 10:60-63, 11:35-38, 13:41-46.) Grupp further discloses that the interface layer's passivating material—*i.e.*, the semiconductor oxide—can be 0.1 nm to 5 nm thick: "the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm." (Grupp '483 at 10:66-11:1; *see also id.* at 11:1-4.)

5. Claim 4

i. The structure of claim 3,

Grupp '483 discloses the structure of Claim 3, as discussed above in **Section X.A.4.** (Schubert Decl. ¶ 138.)

ii. wherein the semiconductor region comprises an n-type doped source or drain of a transistor.

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 139-145.) Grupp '483 discloses that the semiconductor can be an n-type doped semiconductor. (Grupp '483 at 6:5-9.) Further, Grupp '483's Fig. 7d depicts a junction between a metal and an n-type doped semiconductor with an interface layer in accordance with the invention. (Grupp '483 at Fig. 7d; *see also id.* at Fig. 4, Fig. 7a, 5:37-40, 18:4-10; Schubert Decl. ¶¶ 140-142.) As Dr. Schubert explains, Grupp '483's Fig. 7a depicts the same band bending as Grupp '483's Fig. 4, which is described as a junction between a metal and an n-type semiconductor:

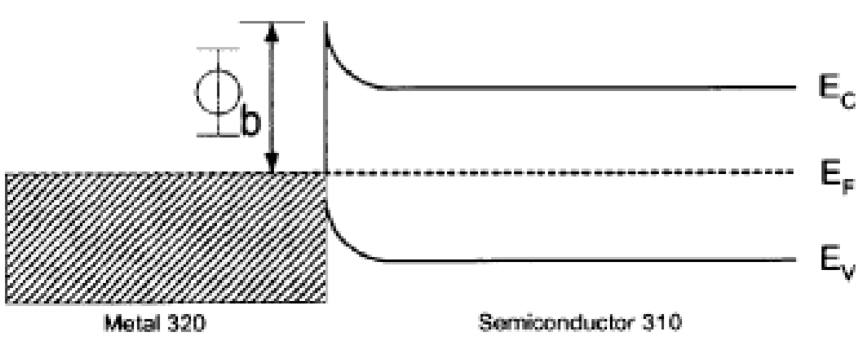


Fig. 4 (Prior Art)

(Grupp '483 at Fig. 4, 5:22-23, 8:10-15; Schubert Decl. ¶¶ 140-142.)

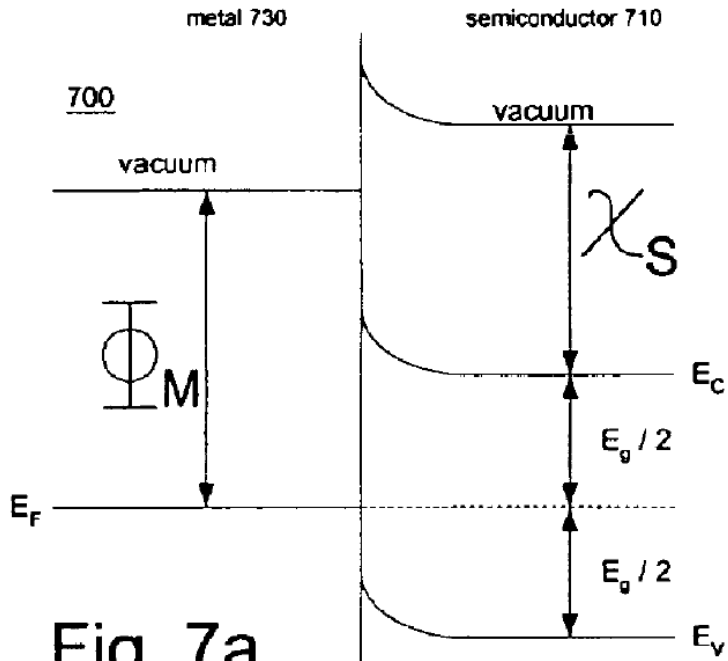


Fig. 7a

(Grupp '483 at Fig. 7a, 17:57-60; Schubert Decl. ¶¶ 140-142.)

Fig. 7d depicts that n-type semiconductor in a metal-semiconductor junction with an interface layer and a depinned Fermi level in accordance with the invention:

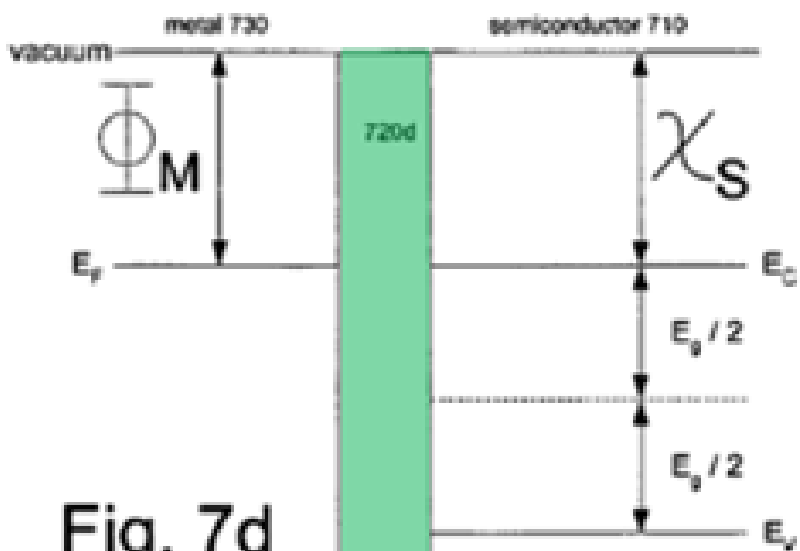


Fig. 7d

(Grupp '483 at Fig. 7d (annotation added), 18:4-17; Schubert Decl. ¶ 140.)

Grupp ’483 further states that its invention encompasses a broad category of metal-interface layer-semiconductor contacts. (Grupp ’483 at 18:32-35; Schubert Decl. ¶ 143.) And, in a section entitled “Transistors Containing Passivated Semiconductor Surfaces,” Grupp ’483 discloses that “the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility).” (Grupp ’483 at 18:19-20, 19:11-15.) As Dr. Schubert explains, “[i]n a transistor, a ‘well’ is a doped region of a semiconductor in which source and drain regions are formed by implanting dopants; the source and drain regions have a doping opposite that of the well.” (Schubert Decl. ¶ 144.)

In sum, Grupp ’483 discloses that the semiconductor region can be both (1) n-type doped and (2) the source or drain of a transistor. Accordingly, Grupp ’483 discloses the limitation “wherein the semiconductor comprises an n-type doped source or drain of a transistor.” (Schubert Decl. ¶ 145.)

6. Claim 6

i. The structure of claim 3,

Grupp ’483 discloses the structure of Claim 3, as discussed above in **Section X.A.4.** (Schubert Decl. ¶ 147.)

ii. wherein the metal oxide layer comprises an oxide of titanium.

Grupp ’483 discloses this limitation. (Schubert Decl. ¶ 148.) As discussed above in **Section X.A.2.iv**, Grupp ’483 discloses a titanium dioxide (TiO_2) spacer layer: “Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV).” (Grupp ’483 at 18:65-67.)

7. Claim 8

i. The structure of claim 6,

Grupp ’483 discloses the structure of Claim 6, as discussed above in **Section X.A.6.** (Schubert Decl. ¶ 150.)

ii. wherein the semiconductor region comprises an n-type doped source or drain of a transistor.

This limitation also appears in Claim 4. Grupp ’483 discloses this limitation, as discussed above in **Section X.A.5.ii**. (Schubert Decl. ¶ 151.)

8. Claim 10

i. The structure of claim 6,

Grupp ’483 discloses the structure of Claim 6, as discussed above in **Section X.A.6.** (Schubert Decl. ¶ 153.)

ii. wherein the semiconductor oxide comprises an oxide of silicon.

Grupp ’483 discloses this limitation. (Schubert Decl. ¶ 154.) As discussed above with respect to Claim 1 in **Section X.A.2.vii** and Claim 2 in **Section X.A.3.ii**, Grupp '483 discloses two semiconductor oxides as passivating dielectric tunnel barrier layers: silicon oxide and silicon dioxide. (Grupp '483 at 10:27-34, 10:48-54, 10:60-63 (silicon oxide); *id.* at 8:64-9:10 (silicon dioxide).) Both silicon oxide and silicon dioxide are oxides of silicon.

9. Claim 11

i. The structure of claim 6,

Grupp '483 discloses the structure of Claim 6, as discussed above in **Section X.A.6.** (Schubert Decl. ¶ 156.)

ii. wherein the semiconductor oxide of the dielectric tunnel barrier layer is adjacent the semiconductor region.

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 157-161.) As discussed above with respect to Claim 1 in **Section X.A.2.vii** and Claim 2 in **Section X.A.3.ii**, Grupp '483 discloses two semiconductor oxides as passivating dielectric tunnel barrier layers: silicon oxide and silicon dioxide. (Grupp '483 at 10:27-34, 10:48-54, 10:60-63 (silicon oxide); *id.* at 8:64-9:10 (silicon dioxide).) Turning to silicon oxide, Grupp '483 further discloses forming a passivation material such as silicon oxide on a silicon surface such that it is adjacent to the silicon and bonds to the silicon. (*Id.* at 10:27-34.) Turning to silicon dioxide, Grupp '483 discloses forming a silicon dioxide layer by exposing the silicon to oxygen so that the oxygen bonds to the silicon's surface, forming silicon dioxide adjacent to the silicon. (*Id.* at 8:64-9:10.)

10. Claim 12

i. The structure of claim 6,

Grupp '483 discloses the structure of Claim 6, as discussed above in **Section X.A.6.** (Schubert Decl. ¶ 163.)

ii. wherein the metal electric contact comprises titanium.

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 164.) As discussed above in **Section X.A.2.iii**, Grupp '483 discloses a metal electrical contact. Further, Grupp '483 discloses using titanium (Ti) as the metal electrical contact. (Grupp '483 at 4:13-20, 14:58-15:2, Claim 7.)

11. Claim 13

i. The structure of claim 3,

Grupp '483 discloses the structure of Claim 3, as discussed above in **Section X.A.4.** (Schubert Decl. ¶ 166.)

ii. wherein the semiconductor oxide comprises an oxide of silicon.

This limitation also appears in Claim 10. Grupp '483 discloses this limitation, as discussed above in **Section X.A.8.ii**. (Schubert Decl. ¶ 167.)

12. Claim 15

i. The structure of claim 13,

Grupp '483 discloses the structure of Claim 13, as discussed above in **Section X.A.11.** (Schubert Decl. ¶ 169.)

ii. wherein the metal oxide layer comprises an oxide of titanium.

This limitation also appears in Claim 6. Grupp '483 discloses this limitation, as discussed above in **Section X.A.6.ii**. (Schubert Decl. ¶ 170.)

13. Claim 16

i. The structure of claim 15,

Grupp '483 discloses the structure of Claim 15, as discussed above in **Section X.A.12.** (Schubert Decl. ¶ 172.)

ii. wherein the metal electrical contact comprises titanium.

This limitation is substantially identical to Claim 12's recitation of "wherein the metal electric contact comprises titanium." Grupp '483 discloses this limitation for the reasons discussed above in **Section X.A.10.ii**. (Schubert Decl. ¶ 173.)

14. Claim 17

i. The structure of claim 15,

Grupp '483 discloses the structure of Claim 15, as discussed above in **Section X.A.12.** (Schubert Decl. ¶ 175.)

ii. wherein the semiconductor comprises an n-type doped source or drain of a transistor.

The meaning of this limitation is unclear, as there is no antecedent basis for the term "the semiconductor" in either Claim 17 or the claims from which Claim 17 depends. But, Grupp '483 discloses a semiconductor that comprises an n-type doped source or drain of a transistor for the reasons discussed above in **Section X.A.5.ii**. (Schubert Decl. ¶ 176.)

15. Claim 18

i. The structure of claim 17,

Grupp '483 discloses the structure of Claim 17, as discussed above in **Section X.A.13.** (Schubert Decl. ¶ 178.)

ii. wherein a specific contact resistivity between the n-type doped source or drain and the metal electric contact is less than 1 Ω-µm^2.

Grupp '483 provides presumptively enabling disclosure of a specific contact resistivity within the specified range, thereby satisfying this limitation. (Schubert Decl. ¶¶ 179-183.) As discussed above in **Section VIII.A**, "specific contact resistivity" is interchangeable with "specific contact resistance," so the analysis for this limitation focuses on specific contact resistance.

Grupp '483 discloses that "the present inventors have determined that for thin interface layers disposed between a metal and a semiconductor, so as to form a metal-interface layer-semiconductor junction, there exist corresponding minimum specific contact resistances." (Grupp '483 at 5:64-6:1.) "Indeed, minimum specific contact resistances of . . . even less than or equal to approximately 1 Ω-μm^2 may be achieved for such junctions in accordance with the present invention." (Grupp '483 at 6:1-5; *see also id.* at 3:40-43, 5:64-6:1, 8:58-61, 10:44-47; 15:52-57.) Grupp '483 therefore discloses some non-zero specific contact resistivity of less than 1 Ω-μm^2, such as a specific contact resistivity just under 1 Ω-μm^2, between the n-type doped source or drain and the metal electric contact. (Schubert Decl. ¶¶ 179-182.)

Grupp '483's disclosure of a non-zero, but less than 1 Ω-μm^2 specific contact resistivity is presumed enabling. *Amgen, Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1355 (Fed. Cir. 2003) ("[W]e hold a presumption arises that both the claimed and unclaimed disclosures in a prior art patent are enabled."). Further, Grupp '483's presumptively enabled non-zero, but less than 1 Ω-μm^2 specific contact resistivity suffices to satisfy this limitation for anticipation: "[w]hen a patent claims a range, as in this case, that range is anticipated by a prior art reference if the reference discloses a point within the range." *Ineos USA LLC v. Berry Plastics Corp.*, 783 F.3d 865, 869 (Fed. Cir. 2015) (citing *Titanium Metals Corp. v. Banner*, 778 F.3d 775, 782 (Fed. Cir. 1985)). So, while Grupp '483 may not enable a specific contact resistivity all the way down to and including approximately zero, it does not need to. Its disclosure of a non-zero, but less than 1 Ω-μm^2 specific contact resistivity (such as a specific contact resistivity just under 1 Ω-μm^2) is presumed enabling, and that disclosure satisfies this limitation for anticipation. (Schubert Decl. ¶ 183.)

16. Claim 19

i. The structure of claim 1,

Grupp '483 discloses the structure of Claim 1, as discussed above in **Section X.A.2.** (Schubert Decl. ¶ 185.)

ii. wherein the semiconductor region comprises silicon,

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 186.) For example, Grupp '483 discloses that "[t]he present inventors have determined that for thin interface layers disposed between a metal and a semiconductor (e.g., C, Ge, Si, SiC and SiGe), so as to form a metal—interface layer—semiconductor junction, there exist corresponding minimum specific contact resistances." (Ex. 1015 [Grupp '483] at 3:18-22.) "Si" refers to silicon. (Schubert Decl. ¶ 186.)

iii. the semiconductor oxide comprises an oxide of silicon,

Grupp '483 discloses wherein the semiconductor oxide comprises an oxide of silicon, as discussed above for Claim 10 in **Section X.A.8.ii**. (Schubert Decl. ¶ 187.)

iv. the metal oxide layer comprises an oxide of titanium, and

Grupp '483 discloses wherein the semiconductor oxide comprises an oxide of titanium, as discussed above for Claim 6 in **Section X.A.6.ii.** (Schubert Decl. ¶ 188.)

v. the metal electrical contact comprises titanium.

This limitation is substantially identical to Claim 12's recitation of "wherein the metal electric contact comprises titanium." Grupp '483 discloses this limitation for the reasons discussed above in **Section X.A.10.ii**. (Schubert Decl. ¶ 189.)

17. Claim 20

i. The structure of claim 1,

Grupp '483 discloses the structure of Claim 1, as discussed above in **Section X.A.2.** (Schubert Decl. ¶ 191.)

ii. wherein the dielectric tunnel barrier layer is configured to reduce a height of a Schottky barrier between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween.

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 192-201.) In particular, Grupp '483 discloses reducing the height of the Schottky barrier by providing an interface layer of the appropriate thickness. (Grupp '483 at 15:34-57, 15:50-54; Schubert Decl. ¶ 192.)

Grupp '483 also discloses that its interface layer reduces the Schottky barrier height from that which would exist at a contact junction between the contact metal and the semiconductor without the interface layer disposed therebetween. (Schubert Decl. ¶¶ 193-200.) Grupp '483 discloses that feature by contrasting Fig. 7a, which depicts a metal-semiconductor junction with no interface layer and a barrier height Φ_b; and Fig. 7d, which depicts a metal (aluminum) to n-type semiconductor (silicon) junction with an interface layer—and a lower barrier height because the conduction band of the semiconductor E_C at the interface is aligned with the Fermi level E_F, reducing the barrier height. (Grupp '483 at Fig. 4, Fig. 7a, Fig. 7d, 5:22-23, 8:10-34, 18:4-17; Schubert Decl. ¶¶ 193-200.) The annotated figures below depict the interface layer reducing barrier height from Φ_b to zero:

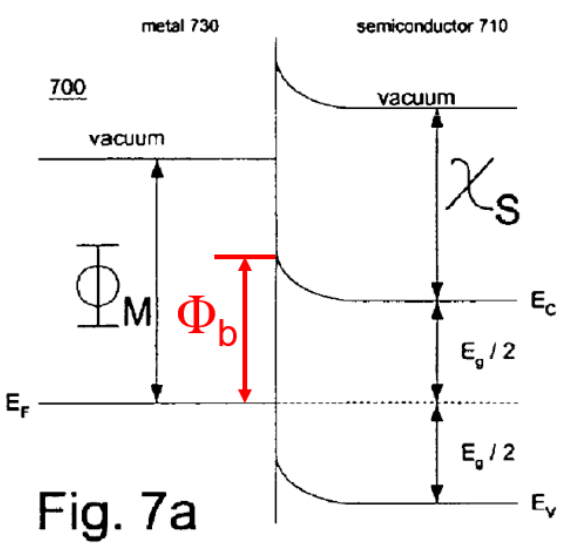
<table>
<tr><th>Fig. 7a: no interface layer; barrier height of Φ_b</th><th>Fig. 7d: interface layer present; zero barrier height</th></tr>
<tr><td>


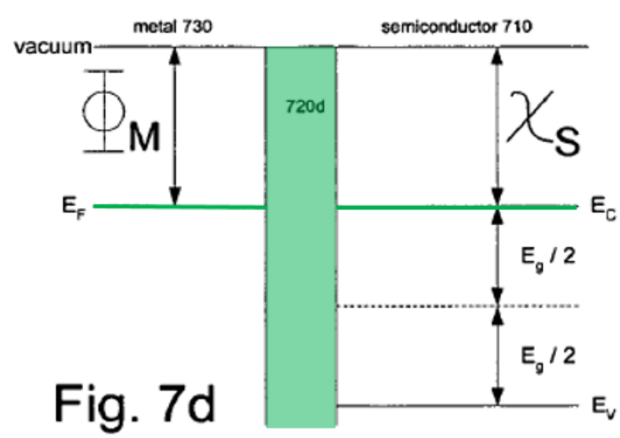
Fig. 7a
</td><td>


Fig. 7d
</td></tr>
<tr><td>(Grupp '483 at Fig. 7a (annotations added), 5:37-40; 8:10-34; Schubert Decl. ¶ 197.)</td><td>(Grupp '483 at Fig. 7d (annotations added), 18:4-17; Schubert Decl. ¶¶ 198-199.)</td></tr>
</table>

With continued reference to the reduction in barrier height depicted between Fig. 7a and Fig. 7d, Grupp '483 explains that "when the interface layer 720d is sufficient to both eliminate or reduce the effect of MIGS and ***to passivate the***

semiconductor surface, we see the Fermi level of the metal aligning with the conduction band of the semiconductor (i.e., the Fermi level of the semiconductor has been depinned and no longer lines up with the Fermi level of the metal)." As Dr. Schubert explains, "[t]he passivating dielectric tunnel barrier of the interface layer contributes to that reduction in barrier height by passivating the semiconductor surface." (Schubert Decl. ¶ 200.) And, Grupp '483 discloses a passivating dielectric tunnel barrier layer of silicon oxide or silicon dioxide for the reasons discussed above in **Section X.A.2.v.**

Grupp '483 therefore discloses a dielectric tunnel barrier layer configured to reduce a height of a Schottky barrier between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween. (Schubert Decl. ¶ 201.)

18. Claim 22

i. The structure of claim 1,

Grupp '483 discloses the structure of Claim 1, as discussed above in **Section X.A.2.** (Schubert Decl. ¶ 203.)

ii. wherein the dielectric tunnel barrier layer is configured to reduce contact resistivity between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween.

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 203.) As discussed above in **Section X.A.17.ii**, Grupp '483 discloses a dielectric tunnel barrier layer configured to reduce a height of a Schottky barrier between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween. (*Id.* ¶ 204.)

Specific contact resistivity depends on barrier height, so decreasing barrier height decreases specific contact resistivity. (Chang at 5-6; Schubert Decl. ¶ 204.) To the extent "contact resistivity" is construed to be interchangeable with "specific contact resistivity" (Carver at 2), decreasing specific contact resistivity decreases "contact resistivity." But if "contact resistivity" is construed to refer to specific contact resistivity divided by the area of the contact—another quantity to which the term "contact resistivity" refers—decreasing specific contact resistivity would also decrease "contact resistivity" under that construction. (Schubert Decl. ¶ 204.)

Grupp '483 further discloses that its invention includes a "passivated Schottky barrier junction" that reduces specific contact resistivity from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween:

> "Although both types of junctions (i.e., ***the new passivated Schottky barrier junction*** and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide-semiconductor junction a Schottky barrier is formed which is comprised of a depletion layer. The tunnel barrier presented by such a depletion layer may be an order of magnitude thicker than the dielectric tunnel barrier in the present invention. ***The thinner interface layers provided by the present invention permit higher current across the junction (i.e., lower junction specific contact resistance)***."
>
> (Grupp '483 at 18:44-59; *see also* Schubert Decl. ¶ 205.)

Grupp '483 therefore discloses a dielectric tunnel barrier layer configured to reduce contact resistivity between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween.

19. Claim 25

i. An electrical junction comprising

The preamble is not limiting. Nevertheless, Grupp '483 discloses it. (Schubert Decl. ¶ 207.) For example, "[i]n one embodiment, the present invention provides an electrical junction that includes a semiconductor (e.g., C, Ge, or an Si-based semiconductor), a conductor, and an interface layer disposed therebetween." (Grupp '483 at 3:44-47; *see also id.* at 3:18-22, 5:49-58, 19:26-27.)

ii. an interface layer disposed between a contact metal and a semiconductor,

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 208.) For example, "[i]n further embodiments the present invention provides an electrical device in which ***an interface layer is disposed between and in contact with a metal and a semiconductor*** . . . ." (Grupp '483 at 4:20-22; *see also id.* at Fig. 7d, 3:18-22, 3:44-47, 5:49-58, 18:4-17 (describing an interface layer between silicon and aluminum); Schubert Decl. ¶ 208.)

iii. the semiconductor comprising a source or drain of a transistor,

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 209.) As discussed above in **Section X.A.5.ii**, Grupp '483 discloses a semiconductor that comprises an n-type source or drain of a transistor, satisfying this limitation. (*Id.* ¶ 209.)

iv. the interface layer comprising a metal oxide separation layer and a semiconductor oxide passivation layer and

Grupp ’483 discloses this limitation. (Schubert Decl. ¶¶ 210-213.) Grupp ’483 discloses an interface layer that includes (1) a passivation layer, which can be a semiconductor oxide; and (2) a separation layer, which can be titanium dioxide, a metal oxide. (*Id.* ¶¶ 210-211.) “The interface layer includes a passivating material, for example, a nitride, a fluoride, an ***oxide***, an oxynitride, a hydride and/or an arsenide ***of the semiconductor***, and in some cases may also include ***a separation layer***.” (Grupp ’483 at 3:53-56; *see also id.* at 4:28-31, 4:53-55, 8:64-9:10, 9:39-43, 10:34-44, 10:48-54, 10:60-63, 11:35-38, 13:41-46.)

In turn, the separation layer can be an oxide. (Grupp ’483 at 11:35-38.) More specifically, the separation layer can be a “spacer layer” of TiO_2, which is titanium dioxide: “[s]pacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV).” (*Id.* at 18:65-67; *see also id.* at 18:45-65; Schubert Decl. ¶ 212.) Thus, Grupp ’483 discloses an interface layer comprising a metal oxide (titanium dioxide) and an oxide of the semiconductor. (Schubert Decl. ¶ 213.)

v. configured to provide a specific contact resistivity between the contact metal and the semiconductor of less than 1 Ω-μm^2.

As discussed above in **Section X.A.15.ii**, Grupp ’483 provides presumptively enabling disclosure of a specific contact resistivity within the claimed range between a metal electrical contact (contact metal) and semiconductor (source or drain of a transistor): namely, a specific contact resistivity just under 1 Ω-μm^2. (Grupp '483 at 5:64-6:5, 15:52-57; Schubert Decl. ¶ 214.) Grupp '483 attributes that specific contact resistivity to a sufficiently thin (*i.e.*, appropriately configured) interface layer: "the layer is still sufficiently thin to allow significant current flow across the interface layer. Contact resistances . . . even less than or equal to 1 Ω-μm^2 may be achieved." (Grupp '483 at 15:52-57; *see also id.* at 5:64-6:5, 8:58-61, 10:44-47.) Thus, Grupp '483 satisfies this limitation.

20. Claim 26

i. The electrical junction of claim 25,

Grupp '483 discloses the electrical junction of Claim 25, as discussed above in **Section X.A.20.** (Schubert Decl. ¶ 216.)

ii. wherein the metal oxide separation layer comprises an oxide of titanium.

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 217.) As discussed above in **Section X.A.19.iv**, Grupp '483 discloses an interface layer that includes a titanium dioxide spacer (separation) layer: "[s]pacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV)." (Grupp '483 at 18:65-67.) TiO_2 is titanium dioxide, an oxide of titanium. (Schubert Decl. ¶ 217.)

21. Claim 27

i. The electrical junction of claim 26,

Grupp '483 discloses the electrical junction of Claim 26, as discussed above in **Section X.A.20.** (Schubert Decl. ¶ 219.)

ii. wherein the semiconductor oxide passivation layer comprises an oxide of the semiconductor.

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 220.) "The interface layer includes a ***passivating material***, for example, a nitride, a fluoride, an ***oxide***, an oxynitride, a hydride and/or an arsenide ***of the semiconductor***, and in some cases may also include a separation layer." (Grupp '483 at 3:53-56; *see also id.* at 4:28-31, 4:53-55, 8:64-9:10, 9:39-43, 10:34-44, 10:48-54, 10:60-63, 11:35-38, 13:41-46.)

22. Claim 28

i. The electrical junction of claim 27,

Grupp '483 discloses the electrical junction of Claim 27, as discussed above in **Section X.A.21.** (Schubert Decl. ¶ 222.)

ii. wherein the semiconductor oxide passivation layer has a thickness of approximately 0.1 nm to 5 nm.

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 223-224.) "The interface layer includes a ***passivating material***, for example, a nitride, a fluoride, an ***oxide***, an oxynitride, a hydride and/or an arsenide ***of the semiconductor***, and in some cases may also include a separation layer." (Grupp '483 at 3:53-56; *see also id.* at 4:28-31, 4:53-55, 8:64-9:10, 9:39-43, 10:34-44, 10:48-54, 10:60-63, 11:35-38, 13:41-46.) Grupp '483 further discloses that the semiconductor oxide passivation layer can be 0.1 nm to 5 nm thick: "the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm." (Grupp '483 at 10:66-11:1; *see also id.* at 11:1-4.)

23. Claim 29

i. The electrical junction of claim 27,

Grupp '483 discloses the electrical junction of Claim 27, as discussed above in **Section X.A.21.** (Schubert Decl. ¶ 226.)

ii. wherein the semiconductor oxide passivation layer is adjacent the semiconductor.

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 227.) As discussed above in **Section X.A.9.ii**, Grupp '483 discloses using a layer of silicon oxide or silicon dioxide as a passivation layer, and both are oxides of the semiconductor silicon. (*Id.*) As also discussed above in **Section X.A.9.ii**, Grupp '483 further discloses that the silicon oxide layer or silicon dioxide layer is formed on the silicon surface and bonds to the silicon surface, indicating that those semiconductor oxide passivation layers are adjacent the silicon. (Grupp '483 at 8:64-9:10 (silicon dioxide passivation layer), 10:27-34 (silicon oxide passivation layer); Schubert Decl. ¶ 227.)

24. Claim 30

i. The electrical junction of claim 25,

Grupp ’483 discloses the electrical junction of Claim 25, as discussed above in **Section X.A.19.** (Schubert Decl. ¶ 229.)

ii. wherein the contact metal is a metal or a stack of metals deposited on the interface layer.

Grupp ’483 discloses this limitation. (Schubert Decl. ¶¶ 230-232.) Although Grupp ’483 need only disclose either (1) a metal deposited on the interface layer or (2) a stack of metals deposited on the interface layer to satisfy this limitation, Grupp ’483 teaches both alternatives.

First, Grupp ’483 discloses a contact metal that is a metal deposited on the interface layer. (Schubert Decl. ¶ 231.) “An interface layer formed in this fashion may be best suited for applications where a subsequent metal layer is deposited over the interface layer in a generally non-invasive fashion, for example using a thermally evaporated source.” (Grupp ’483 at 11:66-12:3.) “The use of non-invasively deposited metals may allow for forming the metal on a thin interface layer without disrupting the passivation properties of the layer.” (*Id.* at 14:32-34.)

Second, Grupp ’483 discloses a contact metal that is a stack of metals deposited on the interface layer. (Schubert Decl. ¶ 232.) As discussed previously, Grupp ’483 describes depositing metals on an interface layer. (Grupp ’483 at 11:66-12:3, 14:32-34.) Further, “[a] conductor may also consist of one conductor at the interface covered by a second conductor." (*Id.* at 14:50-51; *see also id.* at Claim 10.) For example, "[a] submonolayer metal covered by a different metal may result in a workfunction different than either individual metal." (*Id.* at 14:38-40.)

XI. The discretionary factors favor instituting trial.

A. 35 U.S.C. § 325(d)

The Board employs a two-part framework in assessing whether to institute trial in light of 35 U.S.C. § 325(d): (1) whether the Office has been presented with the same or substantially the same prior art or arguments; and (2) if so, whether the Office erred in a manner material to the patentability of the challenged claims. *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, Case IPR2019-01469, Paper 6, at 8 (PTAB Feb. 13, 2020) (designated precedential). That framework favors institution for every ground here.

To start, the record of the Office's previous consideration of Grupp '483 with respect to the '691 Patent consists of the Examiner signing off on it in an information disclosure statement. (Ex. 1014, at 144.) The record of the Office's consideration of Grupp '483 in the '691 Patent's parent applications is similarly limited: it consisted of (1) the Examiner of a parent application identifying Grupp '483 as a pertinent reference; and (2) the Examiners of other parent applications signing off on Grupp '483 in information disclosure statements. (Ex. 1008, at 127-133; Ex. 1010, at 133; Ex. 1012, at 106.)

Crucially, no Examiner cited either Grupp '483 against any claim of the '691 Patent or of any parent application. And merely signing an information disclosure statement or identifying a reference as pertinent does not warrant denying institution. *E.g.*, *Zip Top, LLC v. Stasher, Inc.*, Case IPR2018-01216, Paper 14, at 35-36 (PTAB Jan. 17, 2019); *Navistar, Inc. v. Fatigue Fracture Tech., LLC*, Case IPR2018-00853, Paper 13, at 16-17 (PTAB Sept. 12, 2018).

Finally, the Examiner did not expressly determine the priority date of any challenged claim during the prosecution of the '691 Patent, as discussed above in **Section VI.C**. Indeed, the Office does not ordinarily determine priority dates during prosecution. *In re NTP*, 654 F.3d at 1278 (citing *PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1305 (Fed. Cir. 2008)). And even if the Examiner did tacitly determine that the challenged claims are entitled to an August 12, 2002 priority date, the Examiner erred for the reasons discussed above in **Section IX**.

B. 35 U.S.C. § 314(a)

1. *General Plastic*

This is Petitioner's first petition against the '691 Patent. Further, this petition involves only one reference and one ground. The *General Plastic* factors therefore do not weigh against institution here. *General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, Case IPR2016-01357, Paper 19, at 9-10 (PTAB Sept. 6, 2017) (designated precedential).

2. *NHK Spring* / *Apple*

Despite concurrent litigation involving the '691 Patent, discretionary denial of institution under *NHK Spring Co., Ltd. v. Intri-Plex Techs., Inc.*, Case IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018) (designated precedential) is unwarranted. Denying institution based on the presence or stage of concurrent litigation thwarts Congress's deliberate decision to provide *inter partes* review petitioners with a full year to file a petition after service of an infringement complaint. 35 U.S.C. § 315(b). Indeed, Congress initially considered giving *inter partes* review petitioners only six months. Joe Matal, *A Guide to the Legislative History of the America Invents Act: Part II of II*, 21 FED. CIR. B.J. 539, 611-612 (2012). But Congress instead decided to grant *inter partes* review petitioners a full year, and with good reason: Congress recognized that petitioners deserved a "reasonable opportunity to identify and understand the patent claims that are relevant to the litigation" when a patent owner asserts "multiple patents with large numbers of vague claims." *Id.* (citing 157 Cong. Rec. S5429 (daily ed. Sept. 8, 2011) (statement of Sen. Kyl)).

Here, Acorn has asserted ***108 claims across six patents*** in the Acorn Litigation, including ***23 claims of the '691 Patent***—precisely the scenario that prompted Congress to give *inter partes* review petitioners a full year to file. (Ex. 1034, Ex. 1035.) Thus, denying institution because of concurrent litigation involving the '691 Patent would contradict Congress's intent in enacting the AIA.

In any event, the six factors in *Apple Inc. v. Fintiv, Inc.*, Case IPR2020-00019, Paper 11, at 6 (PTAB Mar. 20, 2020) (designated precedential) that guide the Board's discretion collectively favor instituting trial, as explained below.

i. *Apple* factor 1: whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted

This factor favors instituting trial. Petitioner will be promptly moving to stay the Acorn Litigation. Although the Court presiding over the Acorn Litigation infrequently grants pre-institution motions to stay, it nonetheless invites defendants to renew their motions to stay once the Board institutes trial. And it has granted those renewed motions to stay even when the stage of the case has significantly advanced in the interim—even after claim construction has occurred.

For example, in *Image Processing Techs. LLC v. Samsung Elecs. Co., Ltd.*, the Court denied Samsung's pre-institution motion to stay, but invited Samsung to renew its motion to stay if the Board instituted trial. Case No. 2:16-cv-505-JRG, 2017 WL 10185855, at *1 (E.D. Tex. Feb. 17, 2017). The litigation proceeded in the interim, and the Court construed the claims four months later. 2017 WL 2672616 (E.D. Tex. June 21, 2017). Four months after that claim construction order, the Court granted Samsung's renewed motion to stay after the Board instituted trial. 2017 WL 7051628, at *1 (E.D. Tex. Oct. 25, 2017). While the Court noted that decisions on motions to stay are by nature fact-dependent, it concluded that a stay was appropriate—despite the advanced stage of the case—because the Board instituted *inter partes* review on all but one asserted claim. *Id.*

Thus, even if the Acorn Litigation reaches an advanced stage by the time the Board decides whether to institute trial—indeed, even if claim construction has already taken place—the Acorn Litigation Court could still stay that litigation in view of a favorable institution decision. This factor therefore favors institution.

ii. *Apple* factor 2: proximity of the court's trial date to the Board's projected statutory deadline for a final written decision

Although the district court's trial date is currently ahead of the Board's projected statutory deadline for the final written decision, that trial date does not favor denying institution here. While the Acorn Litigation is scheduled for trial in April 2021 (Ex. 1033), jury trial dates—to say nothing of dates for post-trial briefing—are inherently subject to change. *Precision Planting, LLC v. Deere & Co.*, Case IPR2019-01044, Paper 17, at 15 (PTAB Dec. 2, 2019). The inherent uncertainty in any district court schedule weighs against denying institution. And it weighs especially heavily against denying institution here given the Acorn Litigation Court's willingness to stay advanced cases when the Board has instituted trial on the asserted claims. *Image Processing Techs.*, 2017 WL 7051628, at *1.

iii. *Apple* factor 3: investment in the parallel proceeding by the court and the parties

This factor largely overlaps with factor 2; for similar reasons, it does not favor denying institution. Whatever investment in the Acorn Litigation that the parties and Court might make between now and the Board's institution decision, the Acorn Litigation Court has shown a willingness to stay cases for instituted *inter partes* reviews—even four months after a claim construction order. *Image Processing Techs.*, 2017 WL 7051628, at *1.

Further, the Board has held "that it is often reasonable for a petitioner to wait to file its petition until it learns which claims are being asserted against it in the parallel proceeding." *Apple*, Case IPR2020-00019, Paper 11, at 11. Here, Acorn identified only one representative claim for each of six patents in its October 2019 complaint, including only one claim of the '691 Patent, Claim 25. (Ex. 1031 ¶¶ 63, 73, 83, 93, 103, 113.) Later, in March 2020, Acorn served its infringement contentions—which collectively span ***108 claims*** across those six patents, including ***22 previously unidentified claims*** of the '691 Patent. (Ex. 1034; Ex. 1035.) Petitioner promptly filed this petition (and will be promptly filing its petitions against the asserted claims in other patents) after receiving those infringement contentions.

iv. *Apple* factor 4: overlap between issues raised in the petition and in the parallel proceeding

Although Petitioner is also challenging the validity of Claims 1-6 and 8-16 in the Acorn Litigation, that does not favor denying institution here. Instituting trial would make it possible for the Acorn Litigation Court to stay the Acorn Litigation, preventing the overlap of issues between the petition and the Acorn Litigation.

Further, it is unlikely that the Acorn Litigation will resolve the validity of all 23 challenged claims of the '691 Patent. While Acorn may commit to bringing all 23 challenged claims to trial, the far more likely outcome is that some claims will drop out before trial, leaving the Board as the only tribunal to assess them. Finally, to reduce overlap, if the Board institutes trial here, Petitioner will promptly cease asserting Grupp '483 and its pre-grant publication as prior art references to the challenged claims in the Acorn Litigation. Thus, this factor favors institution.

v. *Apple* factor 5: whether the petitioner and the defendant in the parallel proceeding are the same party

Petitioner and its real parties-in-interest are the defendants in the Acorn Litigation. But, that does not automatically favor denying institution. Rather, the Board principally considers this factor to avoid duplicating another tribunal's work. *Apple*, Case IPR2020-00019, Paper 11, at 13-14. And, as discussed above for factors 1-4, there is minimal risk of that happening here given (1) the Acorn Litigation Court's willingness to grant stays where the Board has instituted trial on the asserted claims; and (2) Petitioner's willingness to cease asserting Grupp '483 and its pre-grant publication against the challenged claims in the Acorn Litigation if the Board institutes trial.

vi. *Apple* factor 6: other circumstances that impact the Board's exercise of discretion, including the merits

This factor favors institution: Petitioner has presented a compelling anticipation ground using Grupp '483. Further, *Apple* states that considerations similar to those under 35 U.S.C. § 325(d) are relevant. Case IPR2020-00019, Paper 11, at 16. As discussed above in **Section XI.A**, the prosecution history of the '691 Patent does not indicate that the Office has addressed the priority date issues herein or cited Grupp '483 against the claims. That favors instituting trial.

* * *

In conclusion, the district court's willingness to grant stays, Petitioner's diligence in preparing petitions against six patents spanning 108 asserted claims, the minimum likelihood of overlap, and Petitioner's strong merits case based on a previously unaddressed priority challenge collectively favor instituting trial. Moreover, the Acorn Litigation trial date is not set in stone, and even if it were, that trial date would only be "an additional factor" for the Board to consider. *NHK Spring*, Case IPR2018-00752, Paper 8, at 19-29. Indeed, "*NHK Spring* does not suggest, much less hold, that *inter partes* review should be denied under § 314(a) solely because a district court is scheduled to consider the same validity issues before the *inter partes* review would be complete." *Intuitive Surgical, Inc. v. Ethicon LLC*, Case IPR2018-01703, Paper 7, at 13 (PTAB Feb. 19, 2019). The Board should therefore institute trial.

XII. Conclusion

Petitioner respectfully requests that the Board institute *inter partes* review, hold the challenged claims unpatentable, and cancel the challenged claims.

Dated: June 29, 2020

Respectfully submitted,

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CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

I hereby certify that this paper, excluding the portions exempted under 37 C.F.R. § 42.24(a), has:

- 12,696 words as counted by Microsoft Word 2016, the word-processing system used to prepare this paper; and

- 265 words in the illustrations, counted manually.

This paper's total word count, excluding the portions exempted under 37 C.F.R. § 42.24(a), is **12,961** words.

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CERTIFICATE OF SERVICE

Under 37 C.F.R. § 42.6(e), the undersigned certifies that on June 29, 2020, a complete copy of the foregoing and all accompanying papers and exhibits were served via Federal Express Priority Overnight shipping, which is at least as fast and reliable as U.S. Priority Mail Express, on counsel of record for Acorn at the correspondence address indicated in PAIR:

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