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Interface effects in titanium and hafnium Schottky barriers on silicon

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The effect of Si surface contaminants present prior to metal deposition, and that of post-metallization anneals has been investigated for Ti and Hf Schottky barriers on Si. These diodes have been prepared in ultrahigh vacuum, characterized with Auger spectroscopy and measured *in situ* using internal photoemission, and *ex situ* using current-voltage measurements. Although barriers to p-type Si as high as 0.9 eV have been reported in the literature for these metals, barriers of 0.72 eV were the highest observed in this investigation, for surfaces contaminated with significant amounts of oxygen.

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Titanium and hafnium Schottky barriers are of interest in integrated circuit and photovoltaic technologies, and for theoretical study, due to their reported anomalously high (low) barriers to p-type (n-type) silicon.[1-5] Spectroscopic studies in this laboratory[6] and others[4,7-10] have shown that Ti and Hf do not form silicide until relatively high temperatures ($TiSi_2$ at 500 °C, and $HfSi_2$ at 550 °C and $HfSi_2$ at 750 °C) although interfacial intermixing and grain boundary diffusion (proposed) can occur at temperatures well below this.[10] They have relatively high heats of formation, and react with SiO_2 and carbon to form metal oxides and carbides.

Previous studies[1-5,9,11-13] have reported a range of values for barrier height for these metals and their silicides, for samples prepared using a variety of processing procedures. In those studies, the level and nature of contamination on the silicon surface prior to metal deposition and that accruing during metal deposition and post-metalization anneals were not well determined or controlled, making it difficult to ascertain the important factors contributing to the barrier height values obtained.

In this letter we report on a carefully controlled study of the effect of Si surface contaminants and anneals on the barrier heights for these column IV transition metals. In order to determine the effect of interface chemistry in a rigorous way, we have developed an UHV (ultrahigh vacuum) analysis system capable of *in situ* internal photoemission measurement of barrier height, in addition to surface analysis (Auger, photoemission spectroscopies, etc.) and sample preparation (annealing to 1000 °C, cooling to − 150 °C, sputtering, metals evaporation, and gas exposures). A novel scheme employing WSi_2 as a backside contact as well as a front side contact to the thin (≈ 100 Å) metal layer is used, to ensure stability after high-temperature anneals. This contact pad arrangement allows good Ohmic contact to the diode and is stable for anneals greater than 1000 °C. Preparation of the diodes in UHV is critical for the control and determination of contaminants. In addition, measurement of the barrier *in situ* is advantageous for a number of reasons. Post-deposition processing, such as annealing, which is critical for typical device fabrication, can be easily done on the same sample. No contamination can occur from gas exposure or diffusion, which is especially important during anneals. And finally, and most importantly, the surface and interface may be monitored with spectroscopic tools before and after metal deposition and anneals, at the same time that barrier measurements are made.

During a typical experiment the surface is prepared in the desired manner, characterized using surface spectroscopies, and approximately 100 Å of the metal is then deposited using e-beam evaporation. The barrier (Φ_b) is then determined by internal photoemission, using front side illumination, over a photon energy ($h\nu$) range of 0.6–1.0 eV. The yield (Y, electrons, collected per photon) can be described by $Y = C_1(h\nu - \Phi_b)^2 h\nu$.[14] This equation accounts for a proper normalization of absorbed photons not present in the more commonly used Fowler equation, $Y = C(h\nu - \Phi_b)^2$,[15] and gives an improved fit, especially for low barrier heights, and a slight increase in calculated barrier height (≈ 0.02 eV) in this energy range.

In the studies reported here we have investigated the Ti-Si system in detail for the following sample types. Starting material in all cases was Si (100) $10^{16}/cm^3$: (1) clean Si (100) prepared by sputtering and annealing (900 °C) versus post-metal annealing temperatue, p and n types; (2) Si (100) chemically prepared using the RCA clean[16] without the final HF dip, p and n types, versus post-metal annealing temperature, p type; (3) Si (100) chemically prepared using the RCA clean, versus post-metal annealing temperature, p type.

We have also studied Hf deposited on sample types (2) and (3) above, for low-temperature anneals, on p type using both internal photoemission and I-V (current-voltage) measurements.

In order to relate observed barrier heights to known integrated circuit chemical cleaning procedures the effect of surface preparation on surface contaminant levels was determined using Auger electron spectroscopy. Auger spectra from the Si surface are shown in Fig. 1, for two common procedures—the RCA clean with and without the final Hf dip. The RCA clean, after air exposure, leaves approximately one monolayer of carbon, and approximately one-half monolayer of oxygen. If the HF dip is omitted, a surface with a thin SiO_2 layer of two to three monolayers and less than 0.2 monolayers of carbon is produced. The presence of the thin oxide on the surface prepared by the RCA clean without the HF dip is also evidenced by the major change in the Si LVV line shape, consistent with 2-3 monolayers of SiO_2 on the surface. It is interesting to note that ellipsometer thickness

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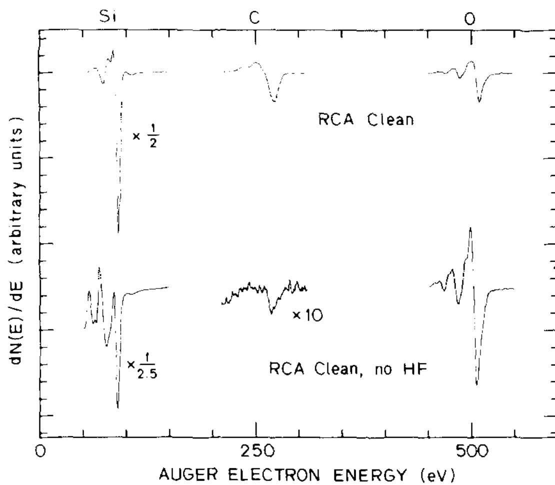

FIG. 1. Comparison of chemical cleaning procedures using Auger electron spectroscopy. The RCA clean leaves approximately one monolayer of carbon, and one-half monolayer of oxygen. Omitting the final HF dip from the procedure leaves two to three monolayers of SiO_2 and less than 0.2 monolayer of carbon.

measurements of these oxides give much larger values for the thickness, definitely inconsistent with the large substract component present in the LVV spectra.

The barrier height of Ti deposited on clean Si (100) *p* and *n* type prepared by *in situ* sputtering and annealing, and on samples prepared by the RCA clean without HF as a function of annealing temperature is shown in Fig. 2. These barrier heights were determined from internal photoemission to ± 0.01 eV and are uncorrected for image force or tunnel lowering. A typical internal photoemission spectrum is shown in the insert, where $(Yh\nu)^{1/2}$ vs $h\nu$ is plotted for a $TiSi_2$ barrier formed by annealing Ti deposited on clean Si (100) to 500 °C. We find for the Ti-Si system, the initial barrier to clean, *n*-type, sputter/annealed (900 °C) Si is 0.51 eV. This barrier varies only slightly for anneals below 500 °C, even though interfacial intermixing between Ti and Si occurs at 300 °C.[10] The barrier increases sharply to 0.58 eV for anneals above this temperature when $TiSi_2$ is formed (as verified by Rutherford backscattering). These results are similar to those obtained by Kato and Nakamura[9] for Ti films sputtered onto chemically cleaned Si. However, this behavior is markedly different than that of V[17] where it is found that the barrier stabilizes at the silicide value during the intermixing phase, which is at much lower temperatures (350 °C). On *p*-type Si the initial barrier is 0.60 eV, which varies only slightly for anneals up to 800 °C.

The RCA clean without HF dip, which has a thin interfacial oxide present, shows a high barrier to *p* type of 0.72 eV, and a correspondingly low barrier on *n* type of 0.3 eV. Annealing at 300 °C causes this high barrier on *p* type to decrease to 0.63 eV. It continues to decrease until silicide is formed, in agreement with silicide value for a clean starting surface. For samples prepared using the full RCA clean, where minimal oxygen was present, a barrier height similar to that on clean Si is obtained. This value of the barrier height is in agreement with that of Cowley[1] for a similar surface preparation, although measurements of the interface contamination levels were not made in that study. Our *I-V* measurements on Ti *p*-type diodes prepared in UHV and

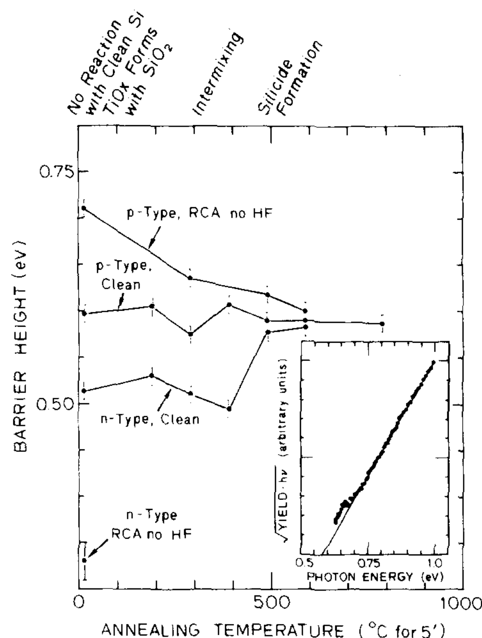

FIG. 2. Schottky barrier height on clean Si(100) prepared by sputtering and annealing (900 °C) and on Si with 2 or 3 monolayers of SiO_2, prepared using the RCA clean with no final HF dip, vs post-metallization annealing (5') temperature, for *p*- and *n*-type silicon. Various regions of interaction have been determined from spectroscopic studies as noted. Insert: internal photoemission data, $TiSi_2$ barrier formed by 500 °C anneal on clean *p*-type Si, $(Yh\nu)^{1/2}$ vs $h\nu$. *x* intercept gives Φ_b.

measured *ex situ* show a barrier of 0.72 eV with an ideality factor *n* of 1.1 to samples prepared with an RCA without the HF dip, and 0.56 ($n \approx 1.3$) for an RCA clean, in good agreement with the *in situ* internal photoemission measurements. The behavior of the barrier heights for the Ti-Si system can be understood in terms of the thermodynamics of the Ti-O-Si system.[6] For thin layers on the order of a monolayer concentration, the Ti will react with the oxide forming Ti oxides plus silicon and possibly Ti silicide. This allows reasonably intimate contact between the Ti and Si giving a value of barrier height similar to the clean surface values. For thicker oxides (still only 2–3 monolayers!) the Ti will still react with the surface, but apparently does not penetrate through the oxide, giving a barrier height no longer representative of the Ti-Si interface. Upon annealing the kinetics of the $TiSiO_2$ reaction is accelerated so that ultimately intimate contact between Ti or Ti silicide and Si is again achieved.

The results for Hf metal, on *p*-type Si, are similar to those found for Ti. These barriers were prepared in UHV and measured *ex situ* using both internal photoemission and *I-V*. Diodes prepared with several monolayers of SiO_2 show a barrier of 0.66 eV for both internal photoemission and *I-V*, with an ideality factor *n* less than 1.05, and excellent reproducibility. This barrier decreases to 0.56 eV when heated to 200 °C (in N_2). Diodes prepared with the RCA clean including the HF dip have a lower barrier of 0.54 eV from internal photoemission and 0.56 eV for *I-V* with an ideality factor of 1.06–1.12.

None of our sample preparations produced a barrier as high as the reported 0.9 eV on *p*-type silicon for Hf[2–4] or Ti.[5] In these previous studies the metal was either sputter deposited or evaporated in a relatively poor vacuum (10^{-6} Torr). A

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surface preparation similar to the RCA clean was used, with the exception of[5] where an RCA clean without an HF dip was used and a premetallization anneal of 520 °C was required to produce a high barrier. Lower barriers in the Hf-Si system were found in this work and by Beguwala[11] where the Hf was deposited by *e*-beam evaporation in a superior vacuum (10^{-8} Torr). In one case [12] a low barrier was found for sputter deposited Hf. However, in this study the Si surface was first sputter cleaned without annealing which we have found can significantly alter the barrier height, and the substrate reached a temperature of 200 °C during deposition, which we have found is high enough to cause significant changes in the barrier height due to metal reaction with the interfacial impurities. In those studies reporting high barrier heights, the diodes were prepared by methods with unknown levels of contaminants, and the presence of additional contaminants (such as hydrogen) may be responsible. Another explanation may be the presence of a thicker insulating layer consisting of SiO_2 and metal oxides, carbides or hydrides, which may be present on the Si surface initially or result from interfacial segregation of impurities in the metal film during annealing.

Nevertheless, interfacial SiO_2 does increase (decrease) the barrier of these metals *p*-type (*n*-type) silicon by more than 0.1 eV. The barrier height measurements are very sensitive to low barrier regions and we observe no additional tails for the yield plots on the high barrier samples indicating a nearly continuous layer is present. The effect of interfacial oxides on barrier height has been explained by Turner and Rhoderick[18] as being due to a reduction in Si interface states due to oxygen bonding to Si. This results in a reduction, in turn, of the pinning ability of the states, so that the barrier behaves more like an ideal Schottky barrier, with low work function metals having high (low) barriers to *p*-type (*n*-type) silicon. Card and Rhoderick[19] have analyzed the effect of an interfacial oxide layer theoretically, and using *I-V* and *C-V* (capacitance-voltage) measurements. A small increase in barrier height due to the tunneling barrier is expected for both *n*- and *p*-type silicon. A larger shift in barrier height predominated though, and was attributed to fixed oxide charge. Positive oxide charge (as is usually observed in metal-oxide-semiconductor devices) would account for an increase in the barrier to *p*-type. However, one would expect oxide charge of this nature to be relatively independent of the metal, whereas the barrier shifts seem to vary with metal work function as reported by Turner and Rhoderick.[18] An effective average work function due to microclusters of varying phase as proposed by Freeouf[20–22] may also explain the observed behavior. An increased barrier to *p*-type would require titanium oxide phases to have a work function less than that of titanium silicide phases. Experimental data,[23] however, indicate a relatively high work function for TiO_2 (5.7 eV) compared to that of Ti (4.33 eV),[24] Si[4.85 eV, cleaved (111)],[25] and the probable work functions of titanium silicides. In addition, low barrier regions representative of more intimate silicon-titanium junctions would also be expected. Since we observe no such low barrier regions, if they are present at all, their physical extent must be much less than the silicon Debye length (400 Å for $10^{16}/cm^3$ doping).

The increased (decreased) barrier to *p*-type (*n*-type) silicon occurs only if several monolayers of SiO_2 are present. In fact it is remarkable that only a few monolayers of SiO_2 are sufficient to produce the high *p*-type barriers observed. For contamination of order a monolayer, Ti reacts to form Ti-O complexes[6,10] which could remove the passivating effect of the Si-O bonding, or the fixed charge, resulting in a barrier similar to that on the clean surface. The nature of the Ti-Si bonding is also important, since the barrier to *n*-type Si varies little from the as-deposited value until silicide is formed even though interfacial intermixing of the Ti and Si is occurring.

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