

# Studies of barrier height mechanisms in metal-silicon nitride-silicon Schottky barrier diodes

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In this paper we present a complete experimental study and theoretical treatment of the barrier height of metal-silicon nitride-silicon Schottky barrier diodes. This study avoids the ambiguities of previous investigations of metal-insulator semiconductor Schottky barriers by use of a more complete and more exact model and a wider range of experimental conditions. The barrier height of these diodes was measured as a function of nitride thickness for a variety of contact metals. From this data the effects of interface traps, fixed charge defects and band lineups can be distinguished from each other and the role that each of these mechanisms plays in determining the barrier height can be ascertained. The barrier height vs metal and barrier height vs thickness data show no signs of the effects of interface traps. Instead, the differences in barrier height observed depend solely on the band lineup at the metal-nitride interface, and fixed charge defects.

## I. INTRODUCTION

A thin ( $< 30 \text{ \AA}$ ) insulating layer present at a metal-semiconductor interface results in a device that will still behave electrically as a Schottky barrier. However, the barrier height of such a metal-insulator semiconductor (MIS) Schottky barrier will in general differ from that obtained in the absence of the insulating layer. At present, despite years of study, the mechanisms that determine the Schottky barrier heights of both MIS Schottky barriers and intimate contact metal-semiconductor diodes are still not fully understood. It is well established that the first proposed model of barrier height, the Schottky model,<sup>1</sup> is typically not supported by experimental data. The barrier height of contacts to all semiconductors is *pinned* depending more weakly on metal than predicted by Schottky from differences in work function. This experimental fact can be explained by a variety of possible mechanisms. For example, pinning has been attributed to the presence of defect states,<sup>2-4</sup> using the model originally proposed by Bardeen.<sup>5</sup> Alternate explanations interpret pinning as an intrinsic property of the interface dipole that determines the lineup of the metal and semiconductor bands at the interface. For example, one theory states that pinning is due to dielectric screening of the interface dipole.<sup>6-9</sup> This screening may be related to the penetration of the tails of metal wave functions into the semiconductor.<sup>6,7</sup> Other models have attributed pinning to chemical effects such as a change in the "effective work function" of the metal near the interface<sup>10</sup> or the presence of interface dipoles that depend on the details of metal-semiconductor bonding.<sup>11</sup> Although they do not vary over as wide a range as predicted by Schottky,<sup>1</sup> the barrier heights of MIS diodes,<sup>2,13</sup> compared to the barrier heights of intimate contact diodes,<sup>14-16</sup> do show a greater dependence on metal. This can be attributed either to a passivation of semiconductor interface states by the insulating layer, to a reduction of the penetration of metal wave functions into the semiconductor, to the chemistry of the metal-insulator interface, or to some combination of these effects. Furthermore, the barrier

height of MIS diodes may be affected by fixed charge defects, which are commonly found at silicon-silicon dioxide interfaces.<sup>17</sup>

Even with these complications the study of MIS Schottky barriers does, however, have certain advantages. First, if an appropriate insulating layer of sufficient thickness is chosen, chemical interaction between metal and semiconductor can be eliminated. Also, the band lineups at the metal-insulator and semiconductor-insulator interfaces can be measured on thicker insulating layers, independent of measurements of MIS Schottky barrier height. Furthermore, for MIS Schottky barriers, the density of interface states can be measured from current-voltage ( $I-V$ )<sup>18-20</sup> and capacitance-voltage ( $C-V$ )<sup>21,22,23</sup> characteristics, whereas these techniques are not successful for intimate contacts. In order to determine the effects of interface states, the separation of these states from the metal must also be known. For MIS diodes, this separation length can be taken to be the insulating layer thickness, which is easily measured and can be varied experimentally. These experimental advantages allow tests of the various models of Schottky barrier height to be performed on MIS devices that are not possible for intimate contacts.

The test described here requires measurement of the barrier heights of a range of metals deposited on identical insulating layers, repeated over a range of insulating layer thicknesses. Although MIS Schottky barriers, especially metal-silicon dioxide-silicon diodes, have been widely studied, such a test has not been performed previously. Studies of barrier heights for a single metal on a range of insulating layers,<sup>24-27</sup> or of a range of metals on one insulating layer<sup>12</sup> have been performed but do not provide enough information to determine the origin of the barrier height of these devices.

For example, measurement of the sensitivity of barrier height to metal work function for a single insulating layer may result in ambiguous conclusions as pinning may be attributed either to interface state defects or purely to processes (such as dielectric screening or chemical effects) that affect the band lineups at the metal-insulator interface. An additional measurement of the barrier height as a function of

insulating layer thickness provides a means to detect fixed charge defects and to distinguish them from interface traps. Previous calculations of the change in barrier height with insulating layer thickness, however, have not been sufficiently general (only considering interface trap defects alone,<sup>27</sup> or fixed charge defects alone),<sup>28</sup> nor sufficiently precise (only considering first order terms) for this purpose. The more exact analysis presented here does provide a means to distinguish between the effects of interface trap states and fixed charge defects. By comparing these predictions with experimental data, the densities of each type of defect can be determined.

We have chosen films of thermally-grown silicon nitride, rather than silicon dioxide, to serve as insulating layers. Growth of the films by thermal nitridation is self-limiting at thicknesses in the desired thickness range depending on the growth temperature. The slow etch rate of silicon nitride in HF solutions allows the thickness of even these extremely thin films to be reliably reduced without disturbing the underlying silicon-silicon nitride interface. Nitrides are more effective diffusion barriers than oxides<sup>29,30</sup>; this may prevent the penetration of metal atoms towards the substrate which has been suggested to occur in oxides.<sup>20</sup> The greater conductance through nitrides (presumably resulting from lower tunnel barriers, due to its smaller band gap) and its higher dielectric constant, compared to silicon dioxide, allow the  $I$ - $V$  and  $C$ - $V$  characteristics of metal-silicon nitride-silicon Schottky barriers to remain nearly ideal out to greater thicknesses than oxides.

## II. EXPERIMENTAL DETAILS

Nitride layers were grown by rapid thermal nitridation of silicon in pure  $\text{NH}_3$  at temperatures ranging from 1000 °C to 1250 °C for times of 20 s. Nitridations were performed in an A. G. Associates Heat Pulse 2146<sup>TM</sup> rapid thermal annealing system heated by quartz lamps. Details of the sample processing and the materials properties of the nitride layers are described in detail elsewhere.<sup>31-33</sup> Diodes were formed on both  $n$ -type and  $p$ -type substrates, using a wide range of metals including Ni, Co, Mo, Cr, Ti, Au, Pd, and Pt. To produce a range of nitride thicknesses, films were grown at varying temperatures, and in addition selected samples were subsequently etched in 10:1 solutions of  $\text{NH}_4\text{F}:\text{HF}$ . Barrier heights were measured by the  $C$ - $V$  technique<sup>34,35</sup> and, on selected samples, by the activation energy method<sup>34,35</sup> as well. The ac characteristics of metal-silicon nitride-silicon diodes were measured at 10 kHz to 1 MHz with a HP4277A<sup>TM</sup> LCZ bridge at room temperature. The dc electrical characteristics were measured using a HP4140B<sup>TM</sup> picoammeter at room temperature and, for selected samples, at lower temperatures down to 100 °K and elevated temperatures up to 350 °K. Room-temperature measurements were performed in a shielded probe station. Low-temperature measurements were performed in a vacuum chamber to prevent condensation of water vapor.

In the next section a general model of MIS Schottky barrier height is derived and used to predict the dependence of barrier height on metal, on insulating layer thickness, and on

applied voltage. Following sections detail comparison of experimental results to these predictions.

## III. BARRIER HEIGHT MODEL

The simplest model of Schottky barrier height,<sup>1</sup> stated that the barrier height is determined only by the metal-semiconductor work function difference. Bardeen<sup>5</sup> proposed a model in which the barrier height depended on the work function difference, the surface state density at the semiconductor surface, and the separation between the metal and semiconductor surfaces. Cowley and Sze,<sup>36</sup> Crowell *et al.*,<sup>37</sup> and Rhoderick<sup>34</sup> developed Bardeen's model further, explicitly considering the presence of an interfacial insulating layer of greater than atomic dimensions, and replacing Bardeen's surface states by analogous interface trap defects. Pruniaux<sup>27</sup> used Crowell's model to calculate, to first order, the dependence of barrier height on the thickness of the insulating layer. Peckarer<sup>28</sup> considered the presence of fixed charge defects and calculated the dependence of barrier height on insulating layer thickness when fixed charge, but no interface trap states, were present.

The model that we present includes all of these factors: it is an extension of Bardeen's model to include fixed charge distributed arbitrarily through the insulating film. However some effects are not considered. For simplicity, the substrate is assumed to be uniformly doped, with only one species of dopant and no traps present. The substrate space charge layer is assumed to be in depletion, not accumulation or inversion. Voltage drops across the surface screening region of the metal<sup>34,38</sup> are ignored. Interface trap defects are assumed to be located exactly at the semiconductor-insulator interface. Image force effects<sup>34,35</sup> are not included: they are less important in MIS Schottky barriers than intimate contact Schottky barriers.<sup>39</sup> We also assume that the dipoles at the metal-insulator and semiconductor-insulator interfaces are independent of insulating layer thickness, and that insulating layer is sufficiently thick that these dipoles do not overlap.

Figure 1 shows band diagrams of both  $p$ -type and  $n$ -type MIS diodes, and defines several of the parameters used by the model. The metal work function  $\Phi_m$  and semiconductor electron affinity  $\chi_s$  are referenced to the conduction band of the insulating layer. They do not represent values measured on metal or silicon free surfaces. The MIS work function difference, referenced to the majority carrier band edge of the semiconductor, is given by:  $\Phi_{\text{mis}} = \Phi_m - \chi_s$  for  $n$  type, or  $\Phi_{\text{mis}} = -\Phi_m + \chi_s + E_g$  for  $p$  type. The potential drops across the substrate depletion region and the insulating layer are  $V_d$  and  $V_i$  respectively.  $V$  is the bias applied to the metal relative to the grounded substrate.  $V_d$  and  $V_i$  are defined as positive in the sense shown in the figure;  $V$  is defined positive for forward bias. The barrier height is defined as the separation between the metal quasi Fermi level and the majority carrier band edge at the silicon surface and is given by  $\phi_b = V_d + \xi + V$ , where  $\xi$  is the separation between the Fermi level and the majority carrier band deep in the bulk of the semiconductor:  $\xi = (kT/q)\ln(N_b/N)$ , where  $N_b$  is the effective density of states<sup>35</sup> in the majority carrier band,  $N$  the concentration of dopant atoms,  $T$  the absolute tempera-

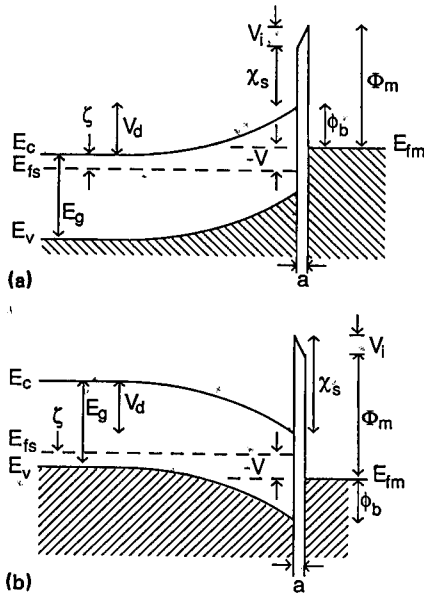


FIG. 1. Band diagrams for (a) *n* type and (b) *p* type MIS Schottky barriers in reverse bias. The figure is not drawn to scale: the bandbending in the substrate occurs over hundreds of angstroms, while the insulating layer thickness *a* is < 30 Å. All parameters are defined as positive for the sense shown, except the applied voltage *V*.

ture, *q* the electronic charge and *k* Boltzmann's constant. The equilibrium condition is  $\Phi_{\text{mis}} - V_i - V_d - \zeta = 0$ . When voltage is applied, the Fermi levels of the substrate and the metal are split, and

$$\Phi_{\text{mis}} - V_i - V_d - \zeta - V = \Phi_{\text{mis}} - V_i - \phi_b = 0. \quad (1)$$

Applying Gauss's law yields  $\epsilon_i E_i = Q_{\text{sc}} + Q_{\text{it}}$ .  $Q_{\text{sc}}$  is the area density of charge in the semiconductor depletion region and  $Q_{\text{it}}$  is the area density of charge present in interface states, here assumed to be located exactly at the semiconductor-insulator interface.  $\epsilon_s$  is the semiconductor dielectric constant. Fixed charge defects, however, are considered throughout the insulating layer, with an arbitrary profile of volume concentration  $\rho(y)$ , where *y* is measured from the semiconductor-insulator interface. The solution to Poisson's equation within the insulating layer is thus

$$\pm C_i V_i = \epsilon_i E_i + \frac{1}{a} \int_0^a dz \int_0^z \rho(y) dy, \quad (2)$$

where  $C_i$  is the capacitance per unit area of the insulating layer  $C_i \equiv \epsilon_i/a$ . The positive sign is for *n*-type, negative for *p*-type (this convention is followed below). The final term is the total amount of charge in the film  $Q_f$  weighted by  $\bar{x}$ , its mean distance from the metal:

$$\frac{1}{a} \int_0^a dz \int_0^z \rho(y) dy = \frac{Q_f \bar{x}}{a}, \quad (3)$$

$$Q_f \equiv \int_0^a \rho(y) dy, \quad \bar{x} \equiv \frac{1}{Q_f} \int_0^a (a-y)\rho(y) dy \quad (4)$$

Eliminating  $V_i$  and  $E_i$  from Eq. (2) results in:

$$\pm C_i (\Phi_{\text{mis}} - \phi_b) = Q_{\text{sc}} + Q_{\text{it}} + \frac{1}{a} \int_0^a dz \int_0^z \rho(y) dy. \quad (5)$$

$Q_{\text{sc}}$  obtained from the solution of Poisson's equation for a nondegenerate semiconductor with dopant atom concentration *N* and no traps present in the substrate is<sup>34,35</sup>:

$$Q_{\text{sc}} = \pm \sqrt{2q\epsilon_s N \left( V_d - \frac{kT}{q} \right)} \quad (6)$$

Differentiation of this equation with respect to  $\phi_b$  at zero bias yields the capacitance of the depletion region/unit area:

$$\left( \frac{\partial Q_{\text{sc}}}{\partial \phi_b} \right)_{V=0} = \pm \sqrt{\frac{q\epsilon_s N}{2(V_d - kT/q)}} \equiv \pm C_d \quad (7)$$

Finally, the interface state charge  $Q_{\text{it}}$  is given<sup>17</sup> by:

$$Q_{\text{it}} = -q \int_{E_v}^{E_c} D_{\text{it}}^a(E) f_{\text{it}}(E, V) dE + q \int_{E_v}^{E_c} D_{\text{it}}^d(E) dE \quad (8)$$

where  $D_{\text{it}}^a(E)$  and  $D_{\text{it}}^d(E)$  are the densities (per area per unit energy) of acceptor and donor interface states and  $D_{\text{it}}(E) = D_{\text{it}}^a(E) + D_{\text{it}}^d(E)$ . The occupation function of the interface states  $f_{\text{it}}(E, V)$  is assumed to be equal for both donor and acceptor states. At zero applied bias the occupation function  $f_{\text{it}}(E, 0)$  is just the Fermi-Dirac distribution function. Substitution of the zero-temperature approximation to the Fermi-Dirac distribution yields:

$$\left( \frac{\partial Q_{\text{it}}}{\partial \phi_b} \right)_{V=0} = \pm q D_{\text{it}}(E_f - E_v) \equiv \pm C_{\text{ss}} \quad (9)$$

where  $E_f$  is the position of the Fermi level at the interface at zero bias:  $E_f - E_v = \phi_b$  for *p* type,  $E_f - E_v = E_g - \phi_b$  for *n* type.

If the defect densities  $D_{\text{it}}(E)$  and  $\rho(y)$  are specified then Eqs. (5), (6), and (8) can be solved for  $\phi_b$ . Three simple cases shown in Fig. 2 illustrate the effects of  $D_{\text{it}}(E)$  and  $\rho(y)$  on the barrier height. For *p*-type diodes,  $\phi_b$  is plotted as a function of nitride thickness for a range of values of  $\Phi_m - \chi_s$ . Figure 2(a) shows  $\phi_b$  calculated for the case of no fixed charge density and a constant density of donor interface traps  $D_{\text{it}}^d(E) = 3 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ . As the thickness of the nitride layer increases the traps become more effective at pinning the barrier height. Here, pinning is used in a relative sense to describe the reduction in the differences in barrier height between metals, the reduction in the rate of change of barrier height with thickness, and the motion of the barrier height towards the neutral level of the interface traps. In the limit of a very thick insulating layer the barrier height becomes absolutely pinned—fixed at the neutral level of the traps, independent of metal and of thickness. On the other hand, in the limit of zero insulator thickness, the model predicts that the barrier height does not depend on the density of traps at all, it is given solely by the band lineup:  $\phi_b = \Phi_{\text{mis}} = E_g - \Phi_m + \chi_s$  (for *p* type). We do not, however, expect the model presented here to yield valid predictions for insulating layers less than a monolayer thick, nor for intimate contacts due to chemical reactions between metal and semiconductor, defects particular to metal-semiconductor interfaces, and significant penetration into the semiconductor of the tails of extended states in the metal. Nevertheless, despite the breakdown of the model at monolayer thicknesses, extrapolation to zero thickness from experimental measurements made over the thickness range for

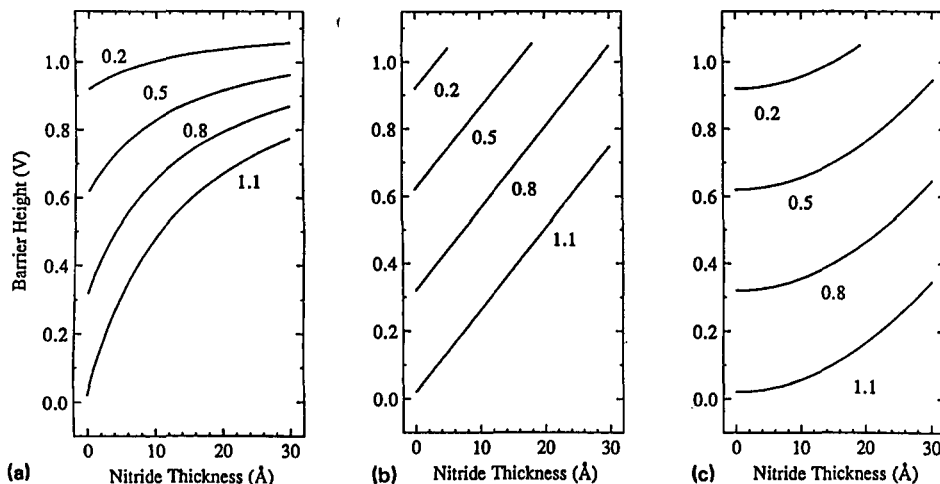


FIG. 2. The effect of interface traps and fixed charge on the barrier height of metal-silicon nitride-silicon Schottky barriers as a function of nitride thickness. Calculations for  $p$  type diodes are shown. The curves were calculated for six different values of  $\Phi_m - \chi_s$ , as indicated, to illustrate the behavior of the barrier height for different contact metals. In (a)  $D_{it}^d(E) = 3 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ , and fixed charge is neglected. In (b) interface traps are neglected, but a quantity of positive fixed charge ( $1.6 \mu\text{C cm}^{-2}$ ) is located at the semiconductor-insulator interface. In (c) fixed charge is distributed through the nitride with density  $4.8 \text{ C cm}^{-3}$ . Interface states can be distinguished from fixed charge effects from the sign of the curvature of the plots and the reduction in the sensitivity of the barrier height to  $\Phi_m - \chi_s$ , for greater thicknesses apparent in (a).

which the model is valid can yield accurate values of  $\Phi_{\text{mis}}$ .

Figure 2(b) also illustrates the effects of fixed charge on the barrier height for  $D_{it}(E) = 0$  and  $Q_f = 1.6 \mu\text{C cm}^{-2}$  (placed at the exact semiconductor-insulator interface). In the limit of zero thickness, fixed charge has no effect and the model predicts  $\phi_b = \Phi_{\text{mis}}$ , exactly as in Fig. 2(a). With increasing insulator thickness  $\phi_b$  shifts linearly away from  $\Phi_{\text{mis}}$ . The direction of this shift is determined by the sign of the fixed charge and the magnitude of its slope  $\partial\phi_b/\partial a$  is determined by the fixed charge density. This slope is the same for all the metals. In Fig. 2(c), fixed charge has been distributed through the insulator with constant volume density  $\rho(y) = 4.8 \text{ C cm}^{-3}$ . The slope  $\partial\phi_b/\partial a$  increases with insulator thickness, but  $\partial\phi_b/\partial\Phi_m$  is still independent of insulator thickness. Thus, experimental measurement of  $\partial\phi_b/\partial a$  and  $\partial\phi_b/\partial\Phi_m$  as a function of insulating layer thickness can be used to distinguish between the effects of interface traps and fixed charge, and to determine the location of the fixed charge. These derivatives are calculated explicitly in the following sections.

Differentiating Eq. (5) at  $V = 0$  and substitution of Eqs. (7) and (9) yield the dependence of the barrier height (at zero bias) on  $\Phi_m$ , the band lineup at the metal-nitride interface:

$$\frac{\partial\phi_b}{\partial\Phi_m} = \pm \frac{C_i}{C_i + C_d + C_{ss}} \quad (10)$$

It is seen that  $\partial\phi_b/\partial\Phi_m$  is independent of fixed charge density but is explicitly dependent on insulator thickness (through  $C_i$ ). For nonzero insulator thickness  $|\partial\phi_b/\partial\Phi_m| < 1$ , even in the absence of defects. Even without interface states, not all of the work function difference will be dropped across the depletion region; rather, a fraction will be dropped across the insulating layer, and thus will not contribute to the barrier height. However, for lightly doped substrates, with thin insulators (i.e., for  $C_i \ll C_d$ , the voltage drop across the insulating layer will be small. For the nitrides used in this study, we estimated  $C_i = 1$  to  $3 \mu\text{F cm}^{-2}$ ,

given  $a = 15$  to  $30 \text{ \AA}$ , and the silicon nitride static dielectric constant  $\epsilon_i = 7.5 \epsilon_0$ .<sup>35</sup> Given diodes that are neither accumulated nor inverted, and given substrate dopant densities of  $N = 2 \times 10^{15} \text{ cm}^{-3}$  for  $p$  type or  $N = 5 \times 10^{14} \text{ cm}^{-3}$  for  $n$  type,  $C_d = 10$ – $30 \text{ nF cm}^{-2}$  (at zero bias) and  $C_d/C_i < 0.01$ . Thus the effect of terms in Eq. (10) of order  $C_d/C_i$  is too small to be detected. Neglecting these terms:

$$\frac{\partial\phi_b}{\partial\Phi_m} = \pm \frac{C_i}{C_i + C_{ss}} \quad (11)$$

Note this equation is exact if the density of interface states  $D_{it}(E)$  is uniform through the part of the bandgap, where the barrier heights of the relevant metals lie.

From Eq. (11) it is seen that if  $\Delta\phi_b$  is measured for two different insulating layer thicknesses,  $C_i/C_{ss}$  can be determined independently of any knowledge of or assumption about the  $\Phi_m$  values of the chosen metals. Equations equivalent to Eq. (11) have previously been used to estimate the density of interface states in both MIS diodes and intimate contact Schottky barriers.<sup>1,12,13,34,40</sup> However, previous investigators have used  $\Delta\phi_b$  values measured for only one insulating layer thickness (or, in the intimate contact case, for one assumed value of  $C_i$ ), together with values of  $\Phi_m$  estimated from vacuum work functions, from electronegativities, or from calculated internal potentials. But these methods of estimating  $\Phi_m$  are not sufficiently accurate and are not consistent. For MIS devices,  $\Phi_m$  can be measured directly in devices with thicker insulating layers by internal photoemission<sup>17,41</sup> and  $C$ - $V$  techniques.<sup>17,41,42</sup>

The rate of change of barrier height with nitride thickness  $\Delta\phi_b/\partial a$  can also be calculated from Eq. (5). In calculating this derivative, it is assumed that the density of interface states  $D_{it}(E)$  does not depend explicitly on nitride thickness. It is also assumed that the fixed charge density in the nitride depends only on  $y$ , the distance from the silicon-silicon nitride interface, not on total insulator thickness or on distance from the metal-semiconductor interface. Under these assumptions, the solution for  $\partial\phi_b/\partial a$  is

$$\frac{\partial\phi_b}{\partial a} = \pm \frac{-Q_{sc} - Q_{it} - Q_f}{a(C_i + C_d + C_{ss})} \quad (12)$$

In the absence of fixed charge, this reduces to

$$\frac{\partial\phi_b}{\partial a} = \frac{C_i(\phi_b - \Phi_{mis})}{a(C_i + C_d + C_{ss})} \quad (13)$$

Here it is seen explicitly that, as the thickness of the insulating layer increases, interface states shift the barrier height away from the value  $\phi_b = \Phi_{mis}$  predicted purely by band lineups. In previous studies,<sup>24-27</sup> this result has been used extensively to explain experimental data. However, these arguments depend on the values assumed for  $\Phi_{mis}$ , which may not be reliable, and do not allow discrimination between fixed charge effects and interface state effects. Nevertheless,  $Q_{it}$  can be distinguished from  $Q_f$  through the curvature of the plot of barrier height vs thickness as seen in Fig. 2.

Measurement of the change in barrier height with applied bias can be used to determine the capacitance of the insulating layer and density of interface states directly. The dependence of the barrier height on bias is determined by differentiating Eq. (5):

$$(C_i + C_d) \frac{\partial\phi_b}{\partial V} - C_d \pm \frac{\partial Q_{it}}{\partial V} = 0. \quad (14)$$

Solving for  $\partial\phi_b/\partial V$  requires that the change in interface state charge  $\partial Q_{it}/\partial V$  be determined. But at arbitrary applied voltage the occupancy of the interface states  $f_{it}(E, V)$  is no longer given by an equilibrium distribution, and the solution for  $\partial Q_{it}/\partial V$  may be quite complicated. The general, nonequilibrium solution for  $f_{it}(E, V)$  was calculated by Tseng and Wu,<sup>43</sup> using Shockley-Read-Hall statistics.<sup>44</sup> This treatment results in quite simple behavior in certain ranges of bias. In strong reverse bias (starting at 0 to 0.5 V reverse bias, depending on the capture cross sections and zero-bias barrier heights),  $f_{it}(E, V)$  becomes fixed. In this bias range both  $f_{it}(E, V)$  and  $Q_{it}$  no longer change with bias.

In strong forward bias (0.4 to 0.5 V) the occupation function of the interface states becomes completely controlled by majority carriers, bringing the states into quasi equilibrium with the substrate quasi Fermi level  $E_{fs}$ , where  $E_{fs} - E_v = \phi_b - V$  for  $p$  type, and  $E_{fs} - E_v = E_g - \phi_b + V$  for  $n$  type. So,

$$\frac{\partial Q_{it}}{\partial V} = \frac{\partial Q_{it}}{\partial E_{fs}} \frac{\partial E_{fs}}{\partial V} = \pm qD_{it}(E_{fs}) \left( \frac{\partial\phi_b}{\partial V} - 1 \right) \quad (15)$$

in forward bias.

Substituting these forms into Eq. (14) yields:

$$\frac{\partial\phi_b}{\partial V} = \frac{C_d}{C_i + C_d} \quad (16)$$

in strong reverse bias,

$$\frac{\partial\phi_b}{\partial V} = \frac{C_d + qD_{it}(E_{fs})}{C_i + C_d + qD_{it}(E_{fs})} \quad (17)$$

in strong forward bias.

#### IV. EXPERIMENTAL RESULTS

In Fig. 3, barrier height data is plotted vs nitride thickness, varied by changing the nitride growth temperature over the

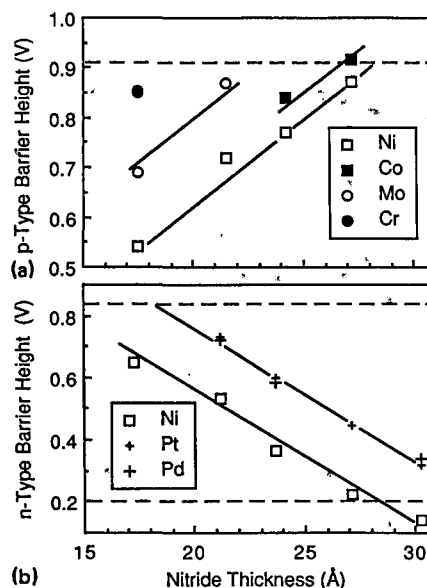


FIG. 3.  $C$ - $V$  Barrier heights of metal-silicon nitride-silicon Schottky barriers vs nitride thickness for a variety of metals for (a)  $p$  type and (b)  $n$  type diodes. Five wafers were nitridized at 1000, 1100, 1150, 1200, and 1250 °C to produce the range of nitride thicknesses shown. Thickness was measured by ellipsometry. For each thickness, metals were deposited on identical nitride samples, split from the same wafer. Accurate measurement of the barrier height by the  $C$ - $V$  method is not possible for values above strong inversion, i.e., at  $\phi_b = 0.90$  V for  $p$  type ( $N = 1.5 \times 10^{15} \text{ cm}^{-3}$ ) and at  $\phi_b = 0.84$  V for  $n$  type ( $N = 5 \times 10^{14} \text{ cm}^{-3}$ ), indicated by the dotted lines. The lines were drawn by assuming identical slopes then performing a least-squares fit to determine the offsets.

range 1000–1250 °C, while fixing the nitridation time at 20 s. These barrier heights were determined by the  $C$ - $V$  technique.<sup>34,35</sup> In addition, barrier heights of selected diodes were also measured by the activation energy method.<sup>34,35</sup> Results from the two techniques agreed within 0.04 V. The  $C$ - $V$  barrier height values represent averages of at least three diodes from each sample. The variation of barrier height values across each sample was  $\pm 0.02$  V.  $C$ - $V$  measurement of  $p$  type barrier heights  $> 0.91$  V (and  $n$  type  $> 0.84$  V) are affected by an artifact brought on by strong inversion of the silicon surface<sup>34,45,46</sup> and are not shown.

The barrier height increases with increasing nitride thickness for  $p$ -type and it decreases for  $n$ -type. The change in barrier height is roughly linear, suggesting the presence of fixed charge [compare to Fig. 2(b)]. The value of  $\partial\phi_b/\partial a$  obtained from the data is 34 mV/Å for  $p$ -type substrates (44 mV/Å for  $n$  type). Therefore, according to Eq. (13), the total charge  $Q_{sc} + Q_{it} + Q_f$  must be positive and  $> aC_i\partial\phi_b/\partial a$  ( $2.3 \mu\text{C cm}^{-2}$  for  $p$ -type and  $2.9 \mu\text{C cm}^{-2}$  for  $n$  type). The depletion region charge ( $Q_{sc} < 30 \text{ nC cm}^{-2}$ ) is too small to account for  $\partial\phi_b/\partial a$ , and is the wrong sign for  $p$  type: depletion charge along should lead to a reduction in barrier height with thickness for both  $n$  and  $p$  type.  $Q_{it}$  will only have the proper sign (positive) if the neutral level of the interface traps is close to the conduction band. However, if  $Q_{it}$  were large, we would expect curvature in the barrier height vs thickness plot, which is not observed.

A linear change in barrier height with nitride thickness could be produced by interface states only in special cases, when the expected curvature is fortuitously cancelled by a variation in  $D_{it}(E)$  through the bandgap or between samples, or by curvature of the opposite sign introduced by the simultaneous presence of fixed charge within the nitride. However, barrier height vs metal results, discussed in the next section, rule out this possibility, as not all of the metals would be equally affected by such a decline in  $D_{it}(E)$ . Furthermore,  $C-V$  measurements on thicker ( $> 60 \text{ \AA}$ ) thermal nitride films show the opposite behavior:  $D_{it}(E)$  increases from midgap towards either band edge.<sup>29,30</sup> Similarly, positive fixed charge spread through the nitride layer could cancel the effects of interface traps, but only for a single metal—other metals would show curvature and the difference in barrier height between metals would still decline with nitride thickness, which is not observed.

Admittedly, the nitride samples of Fig. 3, grown at different temperatures, may differ not only in thickness but in defect density as well; and interpretation of the data using Eqs. (12)–(14) may not be valid. Nevertheless, barrier height measurements of etched nitrides shown in Fig. 4 do not support this objection. In this figure the dependence of nickel–silicon nitride–silicon barrier height on nitride thickness is shown for five  $p$ -type wafers nitridized at different temperatures and subsequently etched in 10:1  $\text{NH}_4\text{F}:\text{HF}$ , each for a range of etch times. Unetched, as-grown data from these wafers is also shown, indicated by the open circles. The barrier heights for nitrides grown at different temperatures but etched back to similar thicknesses are in agreement. This indicates that the defect density in the nitrides is not strongly dependent on nitridation temperature and furthermore that the measured change in barrier height with nitride thickness is an explicit thickness effect, for both as-grown and etched nitrides, consistent with the presence of fixed charge. For several samples, the data is strictly linear with etch time,

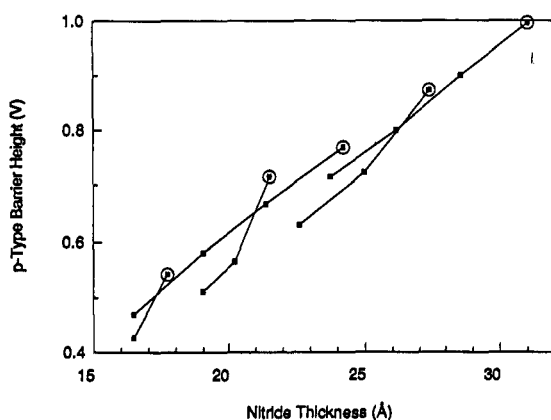


FIG. 4.  $C-V$  barrier heights of nickel contacts to  $p$  Si for as-grown and etched nitrides. Five  $p$  type wafers were nitridized at different temperatures (1000, 1100, 1150, 1200, and 1250 °C) to produce a range of initial nitride thicknesses. Prior to metal deposition, each wafer was quartered. One quarter from each wafer remained unetched, it is shown as the circled point; the other quarters underwent timed etches in 10:1  $\text{NH}_4\text{F}:\text{HF}$  for a range of times. Thicknesses were measured from etch times, assuming a uniform etch rate of 1.2  $\text{\AA}/\text{min}$ , calibrated by ellipsometry.

indicating that all of the fixed charge defects are closer to the interface than the region sampled—none are removed by the etch. Other samples show positive second derivatives, indicating the presence of fixed charge in the portion of the nitride removed by the etch.

Thus barrier height vs thickness data indicates that interface states do not play a significant role in controlling the barrier height. Nevertheless, the results of calculations indicate that interface state densities  $< 3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$  would not introduce measurable amounts of curvature, so the presence of interface states at densities below that level can not be ruled out. Furthermore the conclusion that interface states are negligible is restricted to the range of the band gap over which barrier heights could be measured.

The linearity of barrier height vs thickness data in Figs. 3 and 4 is strong evidence that interface traps are not present in significant quantities. Additional evidence is provided by the observation that  $\Delta\phi_b$ , the difference in barrier height between metals, does not measurably vary with nitride thickness. This is seen in Fig. 3 and also more clearly in Fig. 5, where experimental values of  $\Delta\phi_b$  are shown. Barrier height values of Cr, Mo, and Co on  $p$ -type and Au, Pd, and Pt on  $n$ -type were referenced to the values for Ni, as measured on identical nitrides, split from the same wafer (in order to minimize the effects of any wafer-to-wafer variations). The data shown were measured on the as-grown nitride samples shown in Fig. 3 as well as the etched samples of Fig. 4.

The  $\Delta\phi_b$  values shown are constant, except for small random errors. There is no systematic trend with nitride thickness, even over a range of a factor of two in thickness. This strongly suggests that if interface states are present, they are present only in small quantities (such that  $C_{ss} \ll C_i$ ) and, therefore, do not affect the barrier height. As interface state effects are negligible, Eq. (11) simply reduces to  $\Delta\phi_b = \Delta\Phi_m$ . Thus relative values of  $\Phi_m$  can be obtained from the  $\Delta\phi_b$  data and are shown (relative to the value of

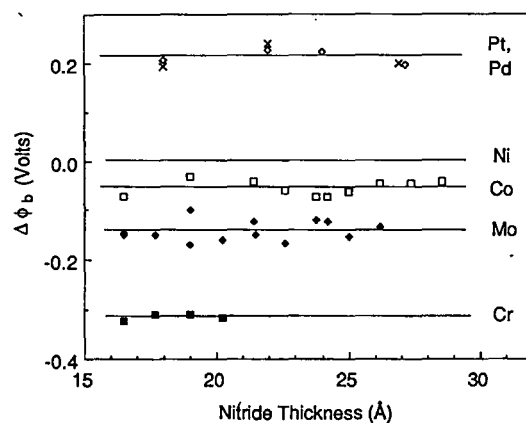


FIG. 5. Differences in  $C-V$  barrier height between the indicated metals and nickel are plotted vs nitride thickness. The nickel values themselves are given in Fig. 3 and 4. Both as-grown nitrides and nitrides etched in 10:1  $\text{NH}_4\text{F}:\text{HF}$  are shown. Within experimental error the barrier height differences  $\Delta\phi_b$  are independent of nitride thickness.  $\square$  Ni-Co ( $p$ ),  $\blacklozenge$  Ni-Mo ( $p$ ),  $\blacksquare$  Ni-Cr ( $p$ ),  $\times$  Pd-Ni ( $n$ ) and  $\diamond$  Pt-Ni ( $n$ ).

TABLE I. Barrier height differences  $\Delta\phi_b$  of metal-silicon nitride-silicon Schottky barriers vs other metallic properties. The listed values for each metal were obtained by referencing the barrier heights for that metal to those of nickel, measured on identical nitrides (positive values indicate  $n$  type barrier heights higher than nickel or  $p$  type barrier heights lower than nickel). The values are averages of data measured on many samples of varying nitride thickness.

Metal	Cr	Mo	Co	Ni	Au	Pd	Pt
$\Delta\phi_b$ , for nitrides	-0.31	-0.14	-0.05	0	0.16	0.21	0.21
Work function <sup>a</sup>	4.5	4.6	5.0	5.15	5.1	5.1	5.65
Internal potential <sup>b</sup>	-0.84	-0.45		-2.04	-2.25	-2.75	-1.81
Electronegativity <sup>c</sup>	1.6	1.8	1.8	1.8	2.4	2.2	2.2
$\Phi_m$ (SiO <sub>2</sub> ) <sup>d</sup> , from:					2.4	2.2	2.2
internal							
photoemission				3.7 <sup>e</sup>	4.1 <sup>e</sup>	4.2 <sup>f,g</sup>	4.5 <sup>g,h</sup>
C-V vs metal <sup>i</sup>				3.65 <sup>e</sup>	4.1 <sup>e</sup>		
C-V vs thickness	3.28 <sup>j</sup>	3.9 <sup>k</sup>			4.16 <sup>j</sup>		

<sup>a</sup>Michaelson (Ref. 49).

<sup>b</sup>Internal potentials, relative to the metal Fermi level, Varena (Ref. 47).

<sup>c</sup>Pauling (Ref. 48) metal-oxide-semiconductor.

<sup>d</sup> $\Phi_m$  was obtained from MOS work functions by subtracting the electron affinity of SiO<sub>2</sub> (0.9 eV) (Ref. 50) and from MOS work function differences using the lineup of the conduction bands of Si and SiO<sub>2</sub> (3.23 eV).

<sup>e</sup>Deal, Snow, and Mead (Ref. 41).

<sup>f</sup>Lundstrom and Distefano (Ref. 51).

<sup>g</sup>In the absence of H<sub>2</sub>.

<sup>h</sup>Lundstrom, Distefano (Ref. 52).

<sup>i</sup>This technique only obtains differences in  $\Phi_m$  between metals. Absolute  $\Phi_m$  were obtained by setting Al to the value measured by internal photoemission.

<sup>j</sup>Kar (Ref. 53).

<sup>k</sup>Shah (Ref. 54).

$\Phi_m$  for nickel) in Table I, along with the internal potentials<sup>47</sup> (calculated by LMTO methods), electronegativities,<sup>48</sup> and vacuum work functions<sup>49</sup> of the metals. Also shown are values of  $\Phi_m$  (SiO<sub>2</sub>), the band lineup at a metal-silicon dioxide interface, measured on thermal oxide films hundreds of angstroms thick.

None of the metallic properties in Table I correlates perfectly with the  $\Delta\phi_b$  values. In particular,  $\Delta\phi_b$  is plotted against internal potentials in Fig. 6(a), and against  $\Phi_m$  (SiO<sub>2</sub>) in Fig. 6(b) as a test of a model<sup>6-9</sup> proposed for intimate contacts that attributes pinning of barrier heights to dielectric screening of band lineups at interfaces. In this model the magnitude of the potential step at the interface will be reduced by a factor  $1/\epsilon$  by screening—just as any potential step in a dielectric or metallic medium is screened—thus reducing the dependence of barrier height on metal. The effective dielectric constant  $\epsilon$  is taken as an average of the values on either side of the interface. Tersoff estimates  $\epsilon$  as twice the optical dielectric constant  $\epsilon_{hf}$  of the material of lower dielectric constant.<sup>6,7</sup> The prediction of the dielectric screening model is therefore:  $d\Phi_m/d\Phi_i = 1/2\epsilon_{hf} = 0.12$ , where  $\epsilon_{hf} = 4.2$  for silicon nitride.<sup>35</sup> The prediction in the absence of dielectric screening is:  $d\Phi_m/d\Phi_i = 1$ . A least-squares fit of the data in Fig. 6(a) has a slope of  $0.2 \pm 0.1$ . Thus the experimental data is in better agreement with the prediction that includes dielectric screening, but the deviations from this prediction are large. Indeed, internal potentials show a worse correlation to  $\Delta\phi_b$  than electronegativities or even vacuum work functions show.

In Fig. 6(b), the mean values of  $\Delta\phi_b$  have been plotted against  $\Phi_m$  (SiO<sub>2</sub>). According to dielectric screening models, the band lineup  $\Phi_m$  (SiO<sub>2</sub>) should be less than the difference in internal potentials by a factor of  $\epsilon_{hf}$  (SiO<sub>2</sub>) = 2.13.<sup>35</sup> So this model predicts a slope of  $d\Phi_m$  (Si<sub>3</sub>N<sub>4</sub>)/ $d\Phi_m$  (SiO<sub>2</sub>)

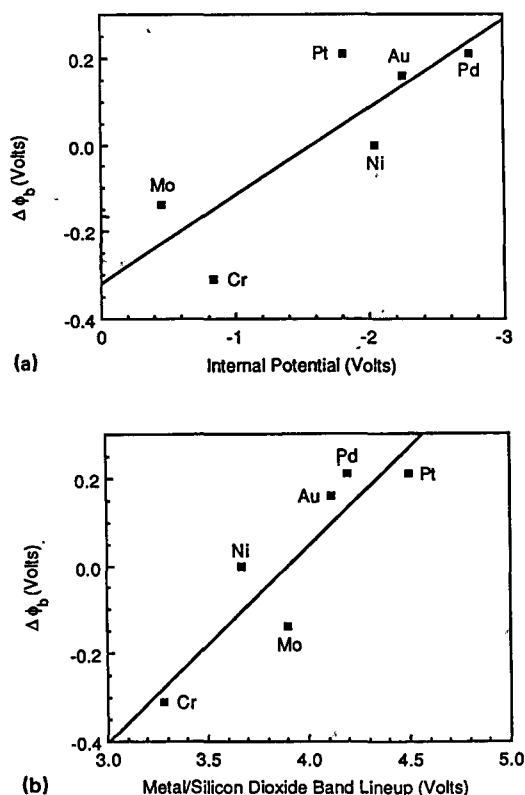


FIG. 6. Experimental tests of dielectric screening models. Barrier height differences  $\Delta\phi_b$  obtained experimentally are plotted (a) against  $\Phi_i$  the calculated internal potentials of the metals and (b) against  $\Phi_m$  (SiO<sub>2</sub>), the lineup of the metal Fermi level with the SiO<sub>2</sub> conduction band as measured on thick-insulator metal-oxide-semiconductor (MOS) devices. As interface trap defects are shown to be insignificant in determining the  $\Delta\phi_b$  values, these values are directly related to differences in  $\Phi_m$  (the magnitude of the band lineup at metal-silicon nitride interfaces). Linear least-squares fits of the data are shown. The slope of these fits is used as an experimental test of the predictions of dielectric screening models.

$= \epsilon_{\text{hf}}(\text{SiO}_2)/\epsilon_{\text{hf}}(\text{Si}_3\text{N}_4) = 0.51$ . The linear least-squares fit shown in the figure has a slope of  $0.44 \pm 0.15$ . Again, the predictions of dielectric screening models are in general agreement with the data, but there are exceptions, for instance the molybdenum data.

The correlation of measured barrier heights of intimate contact Schottky barriers to internal potentials is also poor,<sup>40</sup> and defect states have often been offered as one explanation. Here, interface trap defects have been shown to have a negligible effect on the barrier height, and still no agreement with internal potentials is obtained. The deviations seen in Fig. 6 must be attributed not to defects but to other chemical or physical properties of the interface relevant to the determination of the band lineups. It appears that the chemical environment and electronic structure of the interface must be examined in detail to determine these other relevant mechanisms.

We will now discuss the determination of  $C_i$  and  $D_{\text{it}}$  from  $I$ - $V$  measurements. They are detected through their effect on the dependence of the barrier height on applied bias  $\partial\phi_b(V)/\partial V$  which can be related to the ideality factor  $n$  and the reverse bias slope  $m$  [where  $n \equiv (q/kT) (d \ln(|I|)/d|V|)^{-1}$  in forward bias, and  $m \equiv (kT/q) (d \ln(|I|)/d|V|)$  in reverse bias]. Differentiation of the diode equation<sup>39</sup>:

$$I = AA^{**}T^2 \exp\left(-\frac{q\phi_b(V)}{kT}\right) \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad (20)$$

yields  $n = [1 - \partial\phi_b(V)/\partial V]^{-1}$  and  $m = \partial\phi_b(V)/\partial V$ . Then Eq. (16) can be used to determine  $C_i$  from  $m$  and Eq. (17) can be used to determine  $D_{\text{it}}(E_{\text{R}})$  from  $n$ . Values of  $C_i$  obtained in this manner were  $1$ - $3 \mu\text{F cm}^{-2}$ , in agreement with values of  $C_i = \epsilon_i/a$  estimated from ellipsometric thickness measurements and dielectric constants measured on thick silicon nitride films  $\epsilon_i = 7.5\epsilon_0$ .<sup>35</sup>

Ideality factors  $n$  range from 1.03 to 1.10 and calculated values of  $D_{\text{it}}$  from  $6 \times 10^{11}$  to  $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ . These  $D_{\text{it}}$  values are two orders of magnitude higher than that observed at the interfaces of thicker thermal nitride films that had been annealed after metal deposition,<sup>29,30</sup> but are low compared to the density of states required to pin the barrier height. These results do not contradict the  $\phi_b$  vs metal or  $\phi_b$  vs nitride thickness results, as densities below  $3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$  are too low to have a measurable effect on that data.

## V. CONCLUSIONS

In conclusion, the data presented here, together with the model derived indicate that interface trap defects do not play a measurable role in the determination of the barrier height of metal-silicon nitride-silicon Schottky barriers. Previous suggestions<sup>20,27</sup> that interface states are responsible for the change in barrier height with insulating layer thickness and are responsible for the relatively small dependence on metal are not supported. Measurement of the barrier height as a function of applied bias does indicate that interface trap defects are present in these devices at densities of  $6 \times 10^{11}$  to  $1.1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ , but these densities are too small to affect the barrier height (at zero bias) in any measurable

way. The complicated dependence on nitride thickness that is predicted if large densities of interface states are present is also not observed. Instead, the barrier height vs thickness data can be explained simply by a quantity of fixed charge in the nitrides of  $2$ - $3 \mu\text{C cm}^{-2}$  and relatively independent of the range of processing conditions described here. The differences between barrier heights of different metals vary less than would be expected from estimates of work function difference, but this was found not to be a result of pinning by interface trap states, as these differences were independent of nitride thickness. Instead, the relatively small dependence on metal is unrelated to defects, and appears to rely on an intrinsic property of the metal-nitride interface: the band lineup  $\Phi_m$ . The fact that  $\Phi_m$  varies less from metal to metal than work functions measured on metal surfaces can be partly explained by dielectric screening models. However, the experimental data does not correlate perfectly with the predictions of these models.

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