

# APPENDIX E

—  
**US 7,359,437**

# US 7,359,437



(12) **United States Patent**  
**Hwang et al.**  
 (10) **Patent No.:** US 7,359,437 B2  
 (45) **Date of Patent:** Apr. 15, 2008

- Title: Encoding method and system for reducing inter-symbol interference effects in transmission over a serial link

(54) **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

(75) Inventors: **Seung Ho Hwang**, Palo Alto, CA (US); **Paul Jano Banks**, Cupertino, CA (US); **Daniel Wolf**, San Carlos, CA (US); **Eric Lee**, San Jose, CA (US); **BaegIn Sung**, Sunnyvale, CA (US); **Albert M. Sealise**, San Jose, CA (US)

(73) Assignee: **Silicon Image, Inc.**, Sunnyvale, CA (US)

(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1333 days.

(21) Appl. No.: **10/036,234**

(22) Filed: **Dec. 24, 2001**

(65) **Prior Publication Data**  
 US 2003/0048851 A1 Mar. 13, 2003

**Related U.S. Application Data**

(63) Continuation-in-part of application No. 09/954,663, filed on Sep. 12, 2001.

(51) **Int. Cl.**  
**H04B 1/66** (2006.01)

(52) **U.S. CL.** ..... 375/240; 375/240.01; 375/240.23; 375/246; 375/254; 375/296; 348/423.1; 348/470

(58) **Field of Classification Search** ..... 375/219, 375/220, 240, 240.01, 240.23, 244, 246, 375/253, 254, 260, 285, 295, 296, 346, 348; 348/388, 398.1, 423.1, 470, 476, 477, 487  
 See application file for complete search history.

(56) **References Cited**

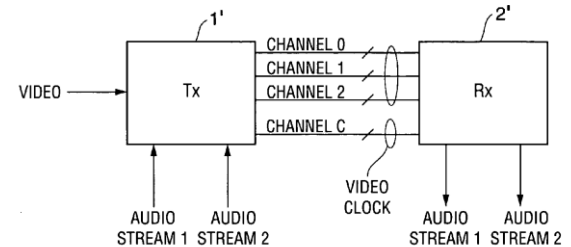
**U.S. PATENT DOCUMENTS**  
 5,150,211 A 9/1992 Charbonnel et al. .... 358/143  
 (Continued)

**FOREIGN PATENT DOCUMENTS**  
 WO WO 00/16525 3/2000

**OTHER PUBLICATIONS**  
 Goldie, John, "LVDS based FPD-Link spans industries with Gigabits @ milliwatts"; National Semiconductor Corporation, Online!, May 1, 2001, pp. 1 to 6, from http://www.national.com/nationaledge/may01/lvds.html.  
 (Continued)  
 Primary Examiner—Dac V. Ha  
 (74) Attorney, Agent, or Firm—Girard & Equitz LLP

(57) **ABSTRACT**  
 A communication system including a transmitter, a receiver, and a serial link, in which encoded data (e.g., encoded video data and encoded auxiliary data) are transmitted from the transmitter to the receiver. The serial link can but need not be a TMDS or TMDS-like link. In typical embodiments, alternating bursts of encoded video data and encoded auxiliary data are transmitted over each of one or more channels of the link. Other aspects of the invention are transmitters for use in encoding data for transmission over a serial link, and methods for sending encoded data over a serial link. In accordance with the invention, the data to be transmitted are encoded using a subset (sometimes referred to as a selected set of code words) of a full set of code words. The selected set of code words is selected such that each stream of encoded data (comprising only such code words) transmitted over a serial link has a bit pattern that is less susceptible to inter-symbol interference ("ISI") during transmission than is the bit pattern determined by a conventionally encoded version of the same data (comprising not only the selected set of code words but also other members of the full set). In general, the best choice for the selected set of code words selected from a full set of binary code words depends on the particular coding implemented by the full set. Typically, the selected set of code words includes words whose serial patterns (during transmission) have fewer contiguous zeros and ones (and thus are less susceptible to ISI during transmission) than do those code words in the full set that are not selected. In preferred embodiments in which the bits of the selected set of code words are transmitted over a serial link as sequences of rising and falling voltage transitions, the bit pattern of each transmitted stream of the selected set of code words implements DC balancing to limit the voltage drift over time.

53 Claims, 5 Drawing Sheets



Claim 41	VESA DisplayPort Standard v1.2				
<p>41. A method for encoding data for transmission over a serial link, said method including the steps of:</p>	<p><b>1.4 Glossary</b></p> <p style="text-align: center;"><b>Table 1-2: Glossary of Terms</b></p> <table border="1" data-bbox="519 372 1789 609"> <thead> <tr> <th data-bbox="523 375 852 434">Terminology</th> <th data-bbox="855 375 1785 434">Definition</th> </tr> </thead> <tbody> <tr> <td data-bbox="523 436 852 606">Symbol</td> <td data-bbox="855 436 1785 606"> <p>There are data symbols and control symbols.</p> <p>Data symbols contain 8 bits of data and are encoded into 10-bit data characters via channel coding as specified in ANSI X3.230-1994, clause 11 (abbreviated as “ANSI 8B/10B” in this document) before being transmitted over a link.</p> <p>DisplayPort also defines nine control symbols used to frame data symbols. Control symbols are encoded into nine of the twelve 10-bit special characters of ANSI 8B/10B (called K-codes).</p> </td> </tr> </tbody> </table> <p><b>1.7.1 Make-up of the Main Link</b></p> <p>The Main Link consists of one, two or four AC-coupled, doubly terminated differential pairs (called lanes). AC-coupling facilitates the silicon process migration since the DisplayPort transmitter and receiver may have different common mode voltages.</p> <p>All lanes carry data. There is no dedicated clock channel. The clock is extracted from the <u>data stream itself that is encoded</u> with ANSI 8B/10B coding rule (channel coding specified in ANSI X3.230-1994, clause 11).</p>	Terminology	Definition	Symbol	<p>There are data symbols and control symbols.</p> <p>Data symbols contain 8 bits of data and are encoded into 10-bit data characters via channel coding as specified in ANSI X3.230-1994, clause 11 (abbreviated as “ANSI 8B/10B” in this document) before being transmitted over a link.</p> <p>DisplayPort also defines nine control symbols used to frame data symbols. Control symbols are encoded into nine of the twelve 10-bit special characters of ANSI 8B/10B (called K-codes).</p>
Terminology	Definition				
Symbol	<p>There are data symbols and control symbols.</p> <p>Data symbols contain 8 bits of data and are encoded into 10-bit data characters via channel coding as specified in ANSI X3.230-1994, clause 11 (abbreviated as “ANSI 8B/10B” in this document) before being transmitted over a link.</p> <p>DisplayPort also defines nine control symbols used to frame data symbols. Control symbols are encoded into nine of the twelve 10-bit special characters of ANSI 8B/10B (called K-codes).</p>				

### Claim 41

providing words of input data capable of being encoded as a conventional sequence of code words of a full code word set;

### VESA DisplayPort Standard v1.2

Comment: A full code word set comprise  $2^{10} = 1024$  codewords of 10 bits. A conventional sequence of code words are elements of the full code word set but not included in the robust subset.

#### 2.2.1 Main Stream to Main Link Lane Mapping in the Source Device

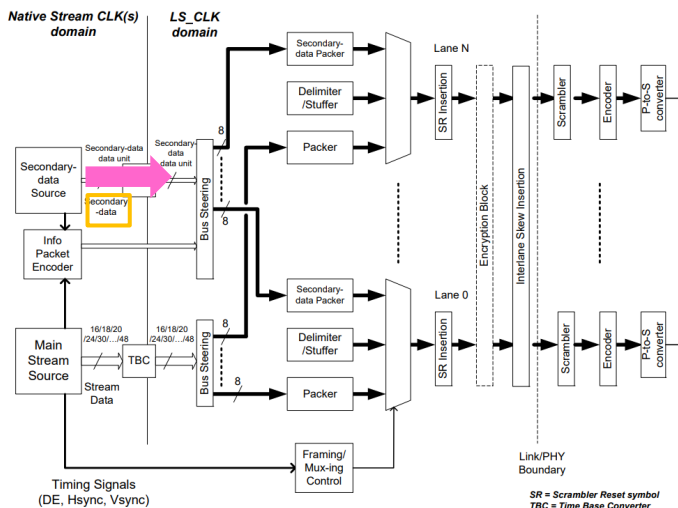


Figure 2-8: High Level Block Diagram of DP uPacket TX Main Link Data Path

### 1.4 Glossary

Table 1-2: Glossary of Terms

Terminology	Definition
Symbol	<p>There are data symbols and control symbols.</p> <p><u>Data symbols contain 8 bits of data and are encoded into 10-bit data characters</u> via channel coding as specified in ANSI X3.230-1994, clause 11 (abbreviated as “ANSI 8B/10B” in this document) before being transmitted over a link.</p> <p>DisplayPort also defines nine control symbols used to frame data symbols. Control symbols are encoded into nine of the twelve 10-bit special characters of ANSI 8B/10B (called K-codes).</p>

Claim 41	VESA DisplayPort Standard v1.2
<p>generating a sequence of selected code words by encoding the input data, wherein each of the selected code words is a member of a robust subset of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words;</p>	<p>Comments: DC balancing can reduce ISI.</p> <p><b>1.7.1 Make-up of the Main Link</b></p> <p>The Main Link consists of one, two or four AC-coupled, doubly terminated differential pairs (called lanes). AC-coupling facilitates the silicon process migration since the DisplayPort transmitter and receiver may have different common mode voltages.</p> <p>All lanes carry data. There is no dedicated clock channel. The clock is extracted from <u>the data stream</u> itself that is <u>encoded</u> with <u>ANSI 8B/10B coding rule</u> (channel coding specified in ANSI X3.230-1994, clause 11).</p> <p><b>3.1.7 Symbol Coding and Serialization/De-serialization</b></p> <p>The DisplayPort interface uses the <u>ANSI standard 8B/10B<sup>5</sup></u> as its channel coding scheme to <u>provide symbol-level DC balancing</u>. It also provides <u>high transition density</u> for link clock phase tracking at the receiver. Using this scheme, 8-bit data characters are treated as three bits and five bits mapped onto a 4-bit code group and a 6-bit code group, respectively.</p> <p>The control bit in conjunction with the data character is used to identify when to encode one of the Special Symbols included in the <u>8B/10B transmission code</u>.</p> <p><u>These code groups are concatenated to form a 10-bit symbol.</u></p> <p>As shown in Figure 3-21, ABCDE maps to abcdei and FGH maps to fghj.</p> <p><u>After coding, the ANSI 8B/10B symbols</u> are serialized so that the least significant bit (lsb) is transported first, and the most significant bit (msb) last.</p>

*Table 4-2. Valid Data Code-Groups (Part 1 of 9)*

Code-Group Name	Octet Value	Octet Bits	Current RD-	Current RD+
		HGF EDCBA	abcdei fghj	
D0.0	00	000 00000	100111 0100	011000 1011
D1.0	01	000 00001	011101 0100	100010 1011
D2.0	02	000 00010	101101 0100	010010 1011
D3.0	03	000 00011	110001 1011	110001 0100
D4.0	04	000 00100	110101 0100	001010 1011
D5.0	05	000 00101	101001 1011	101001 0100
D6.0	06	000 00110	011001 1011	011001 0100
D7.0	07	000 00111	111000 1011	000111 0100

*Table 4-2. Valid Data Code-Groups (Part 2 of 9)*

Code-Group Name	Octet Value	Octet Bits	Current RD-	Current RD+
		HGF EDCBA	abcdei fghj	
D8.0	08	000 01000	111001 0100	000110 1011
D9.0	09	000 01001	100101 1011	100101 0100
D10.0	0A	000 01010	010101 1011	010101 0100
D11.0	0B	000 01011	110100 1011	110100 0100
D12.0	0C	000 01100	001101 1011	001101 0100
D13.0	0D	000 01101	101100 1011	101100 0100
D14.0	0E	000 01110	011100 1011	011100 0100
D15.0	0F	000 01111	010111 0100	101000 1011
D16.0	10	000 10000	011011 0100	100100 1011
D17.0	11	000 10001	100011 1011	100011 0100
D18.0	12	000 10010	010011 1011	010011 0100
D19.0	13	000 10011	110010 1011	110010 0100
D20.0	14	000 10100	001011 1011	001011 0100
D21.0	15	000 10101	101010 1011	101010 0100
D22.0	16	000 10110	011010 1011	011010 0100
D23.0	17	000 10111	111010 0100	000101 1011
D24.0	18	000 11000	110011 0100	001100 1011
D25.0	19	000 11001	100110 1011	100110 0100
D26.0	1A	000 11010	010110 1011	010110 0100
D27.0	1B	000 11011	110110 0100	001001 1011
D28.0	1C	000 11100	001110 1011	001110 0100
D29.0	1D	000 11101	101110 0100	010001 1011
D30.0	1E	000 11110	011110 0100	100001 1011
D31.0	1F	000 11111	101011 0100	010100 1011
D0.1	20	001 00000	100111 1001	011000 1001
D1.1	21	001 00001	011101 1001	100010 1001
D2.1	22	001 00010	101101 1001	010010 1001
D3.1	23	001 00011	110001 1001	110001 1001
D4.1	24	001 00100	110101 1001	001010 1001
D5.1	25	001 00101	101001 1001	101001 1001
D6.1	26	001 00110	011001 1001	011001 1001
D7.1	27	001 00111	111000 1001	000111 1001
D8.1	28	001 01000	111001 1001	000110 1001

*Table 4-2. Valid Data Code-Groups (Part 3 of 9)*

Code-Group Name	Octet Value	Octet Bits	Current RD-	Current RD+
		HGF EDCBA	abcdei fghj	
D9.1	29	001 01001	100101 1001	100101 1001
D10.1	2A	001 01010	010101 1001	010101 1001
D11.1	2B	001 01011	110100 1001	110100 1001
D12.1	2C	001 01100	001101 1001	001101 1001
D13.1	2D	001 01101	101100 1001	101100 1001
D14.1	2E	001 01110	011100 1001	011100 1001
D15.1	2F	001 01111	010111 1001	101000 1001
D16.1	30	001 10000	011011 1001	100100 1001
D17.1	31	001 10001	100011 1001	100011 1001
D18.1	32	001 10010	010011 1001	010011 1001
D19.1	33	001 10011	110010 1001	110010 1001
D20.1	34	001 10100	001011 1001	001011 1001
D21.1	35	001 10101	101010 1001	101010 1001
D22.1	36	001 10110	011010 1001	011010 1001
D23.1	37	001 10111	111010 1001	000101 1001
D24.1	38	001 11000	110011 1001	001100 1001
D25.1	39	001 11001	100110 1001	100110 1001
D26.1	3A	001 11010	010110 1001	010110 1001
D27.1	3B	001 11011	110110 1001	001001 1001
D28.1	3C	001 11100	001110 1001	001110 1001
D29.1	3D	001 11101	101110 1001	010001 1001
D30.1	3E	001 11110	011110 1001	100001 1001
D31.1	3F	001 11111	101011 1001	010100 1001
D0.2	40	010 00000	100111 0101	011000 0101
D1.2	41	010 00001	011101 0101	100010 0101
D2.2	42	010 00010	101101 0101	010010 0101
D3.2	43	010 00011	110001 0101	110001 0101
D4.2	44	010 00100	110101 0101	001010 0101
D5.2	45	010 00101	101001 0101	101001 0101
D6.2	46	010 00110	011001 0101	011001 0101
D7.2	47	010 00111	111000 0101	000111 0101
D8.2	48	010 01000	111001 0101	000110 0101
D9.2	49	010 01001	100101 0101	100101 0101

Claim 41	VESA DisplayPort Standard v1.2				
<p>generating bursts of encoded control words by encoding control bits; and</p>	<p><b>1.4 Glossary</b></p> <p style="text-align: center;"><b>Table 1-2: Glossary of Terms</b></p> <table border="1" data-bbox="519 372 1789 609"> <thead> <tr> <th data-bbox="523 375 852 434">Terminology</th> <th data-bbox="855 375 1785 434">Definition</th> </tr> </thead> <tbody> <tr> <td data-bbox="523 436 852 606">Symbol</td> <td data-bbox="855 436 1785 606"> <p>There are data symbols and control symbols.</p> <p>Data symbols contain 8 bits of data and are encoded into 10-bit data characters via channel coding as specified in ANSI X3.230-1994, clause 11 (abbreviated as “ANSI 8B/10B” in this document) before being transmitted over a link.</p> <p>DisplayPort also defines nine control symbols used to frame data symbols. <u>Control symbols are encoded into nine of the twelve 10-bit special characters of ANSI 8B/10B (called K-codes).</u></p> </td> </tr> </tbody> </table> <p><b>3.1.7 Symbol Coding and Serialization/De-serialization</b></p> <p>The DisplayPort interface uses the ANSI standard 8B/10B<sup>5</sup> as its channel coding scheme to provide symbol-level DC balancing. It also provides high transition density for link clock phase tracking at the receiver. Using this scheme, 8-bit data characters are treated as three bits and five bits mapped onto a 4-bit code group and a 6-bit code group, respectively.</p> <p><u>The control bit</u> in conjunction with the data character is used to identify when to <u>encode one of the Special Symbols</u> included in the 8B/10B transmission code.</p> <p>These code groups are concatenated to form a 10-bit symbol.</p> <p>As shown in Figure 3-21, ABCDE maps to abcdei and FGH maps to fghj.</p> <p>After coding, the ANSI 8B/10B symbols are serialized so that the least significant bit (lsb) is transported first, and the most significant bit (msb) last.</p>	Terminology	Definition	Symbol	<p>There are data symbols and control symbols.</p> <p>Data symbols contain 8 bits of data and are encoded into 10-bit data characters via channel coding as specified in ANSI X3.230-1994, clause 11 (abbreviated as “ANSI 8B/10B” in this document) before being transmitted over a link.</p> <p>DisplayPort also defines nine control symbols used to frame data symbols. <u>Control symbols are encoded into nine of the twelve 10-bit special characters of ANSI 8B/10B (called K-codes).</u></p>
Terminology	Definition				
Symbol	<p>There are data symbols and control symbols.</p> <p>Data symbols contain 8 bits of data and are encoded into 10-bit data characters via channel coding as specified in ANSI X3.230-1994, clause 11 (abbreviated as “ANSI 8B/10B” in this document) before being transmitted over a link.</p> <p>DisplayPort also defines nine control symbols used to frame data symbols. <u>Control symbols are encoded into nine of the twelve 10-bit special characters of ANSI 8B/10B (called K-codes).</u></p>				

Claim 41

transmitting over the link a first burst of the encoded control words between a first burst of the video code words and the burst of the selected code words, and a second burst of the encoded control words between the burst of the selected code words and a second burst of the video code words.

VESA DisplayPort Standard v1.2

2.2.1 Main Stream to Main Link Lane Mapping in the Source Device

The Main Link must have one, two, or four lanes, with each lane capable of transporting eight bits of data per link symbol clock (LS\_Clk). Main stream data (the uncompressed video stream) must be packed, stuffed, framed and, optionally, multiplexed with secondary-data and inter-lane skewed before it is handed over to the PHY layer after the Link Layer data mapping for transport over the main link. The stream data must enter the link layer at the original stream clock (Strm\_Clk) rate and must be delivered to the PHY layer at the LS\_Clk rate after this mapping.

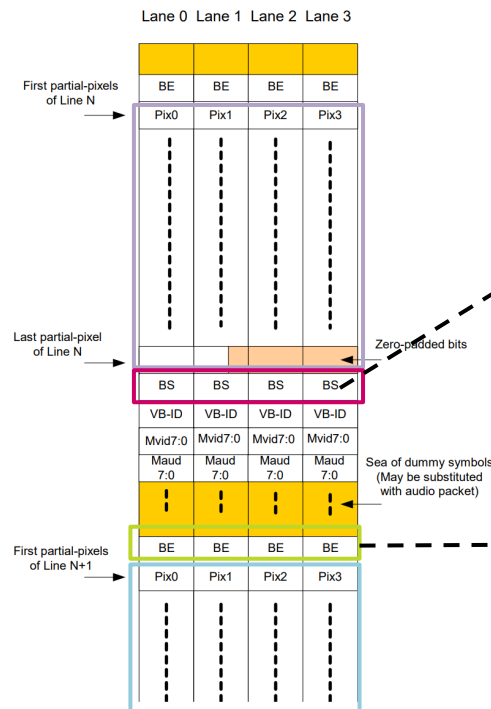


Figure 2-10: Main Video Stream Data Packing Example for a Four Lane Main Link

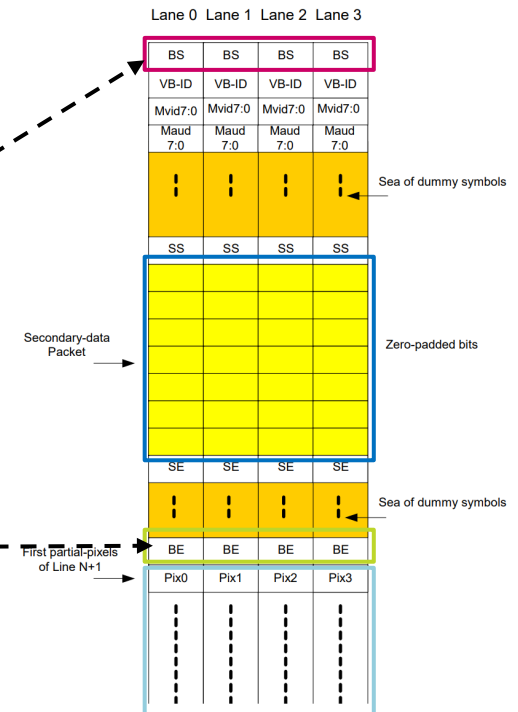


Figure 2-14: Secondary-Data Insertion