

Andrew Wolfe Ph.D.

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Education:

Ph.D. in Electrical and Computer Engineering, Carnegie Mellon University, 1992
Visiting Graduate Student, Center for Reliable Computing, Stanford University, 1988-1989
M.S. in Electrical and Computer Engineering, Carnegie Mellon University, 1987
B.S.E.E. in Electrical Engineering and Computer Science, The Johns Hopkins University, 1985

Academic Employment:

Adjunct Lecturer, [September 2013-present]
Santa Clara University

Teaching graduate and undergraduate courses on embedded computing, mechatronics, real-time systems, computer architecture, logic design, and community service.

Consulting Professor, [1999-2002]
Stanford University, Stanford, CA

Teaching computer architecture and microprocessor design.

Assistant Professor [1991 - 1997]
Princeton University, Princeton, NJ

Teaching and research in the Electrical and Computer Engineering department. Research in embedded computing systems, multimedia, video signal processors, compiler optimization, and high performance computer architecture. Principal investigator or project manager for ~\$6M in funded research.

Visiting Assistant Professor, [1992]
Carnegie Mellon University, Pittsburgh, PA

Research and preparation of teaching materials on advanced microprocessor designs including new superscalar and superpipelined processor architectures.

Industry Employment and Consulting:

Director, [2012-present]
Turtle Beach Inc., (NASDAQ: HEAR)

Corporate Governance. Served on Audit Committee. Chaired Nominating and Governance Committee.

Consultant, [October 2002-present]
Wolfe Consulting

Consultant on processor technology, computer systems, consumer electronics, software, design tools, and intellectual property issues. Testifying and consulting expert for IP and other technology-related litigation matters.

Sample clients include:

AMD	Nvidia	Samsung
IBM	Motorola/Lenovo	HTC
AT&T	Verizon Mobile	Huawei
Apple	T-Mobile	Western Digital
Nintendo	Google	Sonos
Sony	Netflix	Roku
Tivo	LG	TCL

Chief Technical Officer, [1999-2002]; Sr. VP of Business Development, [2001-2002]; VP, Systems Integration, S3 Fellow, [1998 – 1999]; Director of Technology, S3 Fellow, [1997 - 1998]
SONIC|blue, Inc., Santa Clara, CA (formerly S3 Inc.)

Developed and implemented strategy to reposition S3 from PC graphics into the leading networked consumer electronics company. Created and launched more than 30 new products.

Founder and Vice President and Consultant, [1989 - 1995]
The Graphics Technology Company, Inc., Austin, TX

Founded company to develop touch-sensitive components and systems for the first generation of PDA devices and interactive public systems. Obtained financing from Gunze Corp., Osaka, Japan. Company is now part of 3M.

Senior Electrical Engineer, [1989]
ESL - TRW, Advanced Technology Division, Sunnyvale, CA

Designed the architecture for an Intel i860-based multiple-processor digital signal processing system for advanced military applications. Designed several FPGA interface chips for VME-bus systems.

Design Consultant, [1986 -1987]
Carroll Touch Division, AMP Inc., Round Rock, TX

Developed several new technologies for touch-screen systems. Designed the first ASIC produced for AMP, a mixed-signal interface chip for controlling touch-screen sensors. Developed the system electronics, system firmware, and customer utility software for numerous products including those based on the new ASIC.

Senior Design Engineer, [1983 -1985]
Touch Technology Inc., Annapolis, MD

Awards:

IEEE Fellow - for contributions in hardware code compression of embedded software, power consumption analysis, and optimization, 2022
IEEE Computer Society Distinguished Contributor - 2021
Micro Test-of-Time Award (in recognition of one of the ten most influential papers of the first 25 years of the symposium), 2014
Business 2.0 “20 Young Executives You Need to Know”, 2002
Walter C. Johnson Prize for Teaching Excellence, 1997.
Princeton University Engineering Council Excellence in Teaching Award, Spring 1996
AT&T/Lucent Foundation Research Award, 1996.
Walter C. Johnson Prize for Teaching Excellence, 1995
IEEE Certificate of Appreciation, 1995, 2001.
AT&T Foundation Research Award, 1993.
Semiconductor Research Corporation Fellow, 1986 - 1991.
Burroughs Corporation Fellowship in Engineering, 1985 - 1986.

Professional Activities:

Program Chair: Micro-24, 1991, Hot Chips 13, 2001.
General Chair: Micro-26, 1993, Micro-33, 2000.
Associate Editor: IEEE Computer Architecture Letters; ACM Transactions in Embedded Computing Systems
Speaker at CES, WinHec, Comdex, Intel Dev. Forum, Digital Media Summit, Microprocessor Forum, etc.
Keynote speaker at Micro-34, ICME 2002
IEEE B. Ramakrishna Rau Award committee – 2012-2016
IEEE Computer Society Awards Committee – 2015
CES Awards Judge – 2016
Entrepreneurship Mentor – Draper University

Advisory Boards:

Director, Turtle Beach Corporation (NASDAQ:HEAR) (formerly Parametric Sound Corporation), KBGear Interactive, Inc., Comsilica, Inc., Rioport.com, various S3 subsidiaries.

Technical Advisory Boards, Ageia, Inc., Intellon, Inc., Comsilica, Inc., Entridia, Inc., Siroyan, Ltd., BOPS, Inc, Quester Venture Funds

Carnegie Mellon University Silicon Valley Advisory Board; Johns Hopkins University Tech Transfer Advisory Board

Publications

Book Chapters:

Tiwari, V., Malik, S., Wolfe, A., and Lee, M. T-C., “Instruction Level Power Analysis and Optimization of Software,” in *Technologies for Wireless Computing*, Kluwer Academic Publishers, 1996, Anantha P. Chandrakasan and Robert W. Brodersen, Editors.

Wolf, W., Liu, B., Wolfe, A., Yeung, M., Yeo, B., and Markham, D., “Video as Scholarly Material in the Digital Library,” Chapter 1 in *Advances in Digital Libraries '95*, Springer-Verlag, 1995.

Malik, S., Wolf, W., Wolfe, A., Li, Y-T. S. , and Yen, T., “Performance Analysis of Embedded Systems”, in *Hardware-Software Codesign*, Kluwer Academic publishers, NATO-ASI Series, G. DeMichelli and M. Sami ed., 1995.

Refereed Journal Papers:

Wolfe, A., and Noonburg, D., “A Superscalar 3D Graphics Engine”, *The Journal of Instruction Level Parallelism*, vol 2, May 2000, (<http://www.jilp.org/vol1>).

Kozuch, M., Wolf, W., and Wolfe, A., “An Experimental Analysis of Digital Video Library Servers. Multimedia Systems 8(2): 135-145, ACM/Springer, 2000.

Li, Y-T. S. , Malik, S., and Wolfe, A., “Performance Estimation of Embedded Software with Instruction Cache Modeling”, *ACM Transactions on Design Automation for Embedded Systems*, v. 4 n. 3, July 1999.

Dutta, S. , O’Connor, K., Wolf, W., and Wolfe, A., “A Design Study of a 0.25 μ m Video Signal Processor,” *IEEE Trans. on Circuits & Systems for Video Signal Processing*, Vol. 8, No. 4, pp. 501-519, Aug. 1998.

Dutta, S. , Wolf, W., and Wolfe, A., “A Methodology for Memory System Design for Programmable Video Processors,” *IEEE Trans. on Circuits & Systems for Video Signal Processing*, v. 8, n. 1 , pp. 36 –53, Feb. 1998.

Conte, T., Dubey, P., Jennings, M., Lee, R., Peleg, A., Rathnam, S., Schlansker, M., Song, P., and Wolfe, A., “Challenges to Combining General-Purpose and Multimedia Processors”, *IEEE Computer*, Vol. 30, No. 12, pp. 33-37, Dec. 1997.

de Souza, A. F., Fernandes, E. S. T., and Wolfe, A., “On the Balance of VLIW Architectures”, in *Journal of Systems Architectures*, Vol. 43, No. 1—5, March 1997, pp. 15—22.

Tiwari, V., Malik, S., Wolfe, A., Lee, T., “Instruction Level Power Analysis and Optimization of Software” (extended version), in *Journal of VLSI Signal Processing*, Nov. 1996.

Wolfe, A., “Issues for Low-Power CAD Tools: A System-Level Study”, *Design Automation for Embedded Systems*, v. 1, n. 4, pp. 315–332, Kluwer, Oct. 1996.

Wolf, W., Wolfe, A., Chinatti, S., Koshy, R., Slater, G., and Sun, S., "Lessons from the Design of a PC-Based Private Branch Exchange", *Design Automation for Embedded Systems*, v. 1, n. 4, pp. 297–314, Kluwer, Oct. 1996.

Wolfe, A., "Software-Based Cache Partitioning for Real-time Applications", *The Journal of Computer and Software Engineering*, v. 2, no. 3, pp. 315-327, 1994.

Tiwari, V., Malik, S., and Wolfe, A., "Power Analysis of Embedded Software: A First Step Towards Software Power Minimization", *IEEE Transactions on VLSI Systems*, v. 2, no. 4, pp. 437-445, Dec. 1994.

Refereed Conference Papers:

Wolfe, A., and Noonburg, D., "A Superscalar 3D Graphics Engine", *Micro 32, the 32nd International Symposium On Microarchitecture*, Haifa, Israel, Nov. 1999.

Benes, M., Nowick, S., and Wolfe, A., "A Fast Asynchronous Huffman Decoder for Compressed-Code Embedded Processors", *4th IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems (Async-98)*, San Diego, CA, March 1998.

Liao, H. and Wolfe, A., "Available Parallelism in Video Applications", in *Micro 30, the 30th International Symposium On Microarchitecture*, pp. 321-329, Raleigh, NC, Dec. 1997.

Kozuch, M., Wolf, W., and Wolfe, A., "An Approach to Network Caching for Multimedia Objects," in *ICCD '97*, IEEE Computer Society Press, Oct. 1997.

Li, Y-T. S. , Malik, S., and Wolfe, A., "Cinderella: A Retargetable Environment for Performance Analysis of Real-Time Software", *Euro-Par 1997*.

Benes, M., Wolfe, A., and Nowick, S., "A High-Speed Asynchronous Decompression Circuit for Embedded Processors", in *Advanced Research on VLSI*, Sep. 1997.

Santos, A., Wolfe, A., and Fernandes, E. S. T., "Functional Units Utilization in a Multiple-Instruction Issue Architecture," *Proceedings of the 23rd Euromicro Conference, Euromicro*, Peter Milligan and Patrick Corr (Editors), IEEE Computer Society, September 1997, pp. 228--233.

Kozuch, M., Wolf, W., Wolfe, A., and McKay, D., "Branch Libraries for Multimedia Repositories," in *ACM Digital Libraries '97*, ACM Press, pp. 261-262, 1997.

Wolfe, A., Wolf, W., Dutta, S., and Fritts, J., "A Design Methodology for Programmable Video Signal Processors", in *SPIE symposium on Electronic Imaging: Multimedia Hardware Architectures*, Feb. 1997.

Wolfe, A., Fritts, J., Dutta, S., and Fernandes, E. S. T., "Datapath Design for a VLIW Video Signal Processor", in *HPCA-3*, San Antonio, TX, Feb. 1997.

Li, Y-T. S. , Malik, S., and Wolfe, A., "Cache Modeling for Real-Time Software: Beyond Direct Mapped Instruction Caches", in *RTSS '96*, Washington, DC, Dec. 1996.

Dutta, S., Wolfe, A., Wolf, W., and O'Connor, K., "Design Issues for a Very-Long-Instruction-Word VLSI Video Signal Processor," in *VLSI Signal Processing IX*, pp. 95-104, San Francisco, CA , Oct. 1996.

Kozuch, M., Wolf, W., and Wolfe, A., "New Challenges for Video Servers: Performance of Non-Linear Applications Under User Choice", *ICCD '96*, pp. 145–146, Austin, TX, Oct., 1996.

Filho, E. M. C., Wolfe, A. and Fernandes, E. S. T., "Load Balancing on a Superscalar Architecture", *The 22nd Symposium on Microprocessing and Microprogramming, Euromicro '96*, pp. 651-658, IEEE, Prague, Czech Rep., Sept. 1996.

Dutta, S., O'Connor, K., and Wolfe, A., "High Performance Crossbar Interconnect for a VLIW Video Signal Processor", *1996 Ninth Annual IEEE International ASIC Conference*, pp. 45-49, Rochester, NY, Sept., 1996.

Filho, E. M. C., Fernandes, E. S. T., and Wolfe, A., "Functionality Distribution on a Superscalar Architecture" *Europar '96, Lecture Notes in Computer Science*, No. 1124, pp. 773-778, Springer-Verlag, Aug. 1996.

Wolfe, A., "Opportunities and Obstacles in Low-Power System-Level CAD", *33rd DAC*, Las Vegas, NV, June 1996.

Wolfe, A. and Lyon, S., "Learning at 40 feet/s: A System-Level Design Lab", *1996 ASEE Annual Conference*, Washington DC, June, 1996.

Sturm, J. and Wolfe, A., "Breadth and Unity: A Revised Electrical Engineering Curriculum at Princeton University", *1996 ASEE Annual Conference*, Washington DC, June, 1996.

Tiwari, V., Malik, S., Wolfe, A., Lee, T., "Instruction Level Power Analysis and Optimization of Software", *9th International Conf. on VLSI Design*, pp. 326-328, Bangalore, India, Jan. 1996.

Li, Y-T. S., Malik, S., and Wolfe, A., "Efficient Microarchitecture Modeling and Path Analysis for Real-Time Software", *RTSS '95*, Pisa, Italy, Dec. 1995.

Li, Y-T. S., Malik, S., and Wolfe, A., "Performance Estimation of Embedded Software with Instruction Cache Modeling", *ICCAD '95*, San Jose, CA., Nov. 1995.

Dutta, S., Wolf, W., and Wolfe, A., "VLSI Issues in Memory-System Design for Video Signal Processors," *ICCD '95*, pp. 498-503, IEEE Computer Society Press, Oct. 1995.

Wolfe, A. "A Case Study in Low-Power System-Level Design", *ICCD '95*, pp. 332-338, Oct. 1995.

Kozuch, M., Wolf, W., and Wolfe, A., "Client-server Architectures for Nonlinear Video Services", SPIE Conference on Integration Issues in Large Commercial Storage Systems, SPIE, Philadelphia, PA, Oct., 1995.

Filho, E. M. C., Wolfe, A., and Fernandes, E. S. T., "The Effect of Branch Units on the Performance of Superscalar Architectures", *The 21st Symposium on Microprocessing and Microprogramming, Euromicro '95*, pp. 277-284, IEEE, Como, Italy, Sep. 1995.

Wolf, W., Liu, B., Wolfe, A., Martonosi, M., and Liang, Y., "A Digital Video Library for Classroom Use", *International Symposium on Digital Libraries*, Tsukuba Science City, Japan, August, 1995.

Kozuch, M. and Wolfe, A., "Compression of Embedded System Programs", *ICCD '94*, pp. 270-277, Oct. 1994.

Tiwari, V., Malik, S., and Wolfe, A., "Power Analysis of Embedded Software: A First Step Towards Software Power Minimization", *International Conference on Computer Aided Design*, Nov. 1994.

Tiwari, V., Malik, S., and Wolfe, A., "Compilation Techniques for Low Energy: An Overview", *IEEE Solid-State Circuits Council 1994 Symposium on Low-Power Electronics*, 1994.

Wolf, W., Wolfe, A., Chinatti, S., Koshy, R., Slater, G., and Sun, S., "TigerSwitch: A Case Study in Embedded Computing System Design", *International Workshop on Hardware-Software Codesign*, IEEE, 1994.

Liu, B., Wolf, W., Kulkarni, S., Wolfe, A., *et. al.*, "The Princeton Video Library of Politics", *Digital Libraries '94 – The First Annual Conference on the Theory and Practice of Digital Libraries*, pp. 215-216, June 1994.

Malik, S. and Wolfe, A., "Harnessing the Performance of Microprocessors for Real-Time Applications," *ISCA '94 Workshop on Architectures for Real-Time Applications*, April, 1994.

Boleyn, R.. and Wolfe, A., "Two-Ported Cache Alternatives for Superscalar Processors", *Micro 26, the 26th International Symposium On Microarchitecture*, Dec. 1993.

Boleyn, R., Debardeleben, J., Tiwari, V., and Wolfe, A., "A Split Data Cache for Superscalar Processors", *ICCD '93*, Oct. 1993.

Wolfe, A., "Software-Based Cache Partitioning for Real-time Applications", *Third International Workshop on Responsive Computer Systems*, Sept. 1993.

Wolfe, A., and Chanin, A., "Executing Compressed Programs on an Embedded RISC Architecture", *Micro-25, the 25th Annual International Symposium on Microarchitecture*, pp. 81-91, Dec. 1992.

Maly, W., Patyra, M., Primatec, A., Raghavan, V., Storey, T., and Wolfe, A., "Memory Chip for 24-port Global Register File", *IEEE Custom Integrated Circuit Conference*, May 1991.

Wolfe, A., and Shen, J. P., "A Variable Instruction Stream Extension to the VLIW Architecture", *Fourth International Conf. on Architectural Support for Programming Languages and Operating Systems*, ACM, April 1991.

Wolfe, A., and Shen, J. P., "Flexible Processors: A Promising application-specific processor design approach", *Micro-21, the 21st Annual Workshop on Microprogramming and Microarchitecture*, IEEE, Dec. 1988, pp. 30-39.

Wolfe, A., Breternitz Jr., M., Stephens, C., Ting, A. L., Kirk, D. B., Bianchini Jr., R. P., Shen, J. P., "The White Dwarf: A High-Performance Application-Specific Processor", *15th Annual Symposium on Computer Architecture*, IEEE, June 1988, pp. 212-222.

Other Publications

Chan, Y, Sudarsanam, A, and Wolfe, A., "The Effect of Compiler-Flag Tuning on SPEC Benchmark Performance", *Computer Architecture News*, v. 22, no. 4, pp. 60-70, Sept. 1994.

Wolfe, A., "Retrospective on Code Compression and a Fresh Approach to Embedded Systems", *IEEE MICRO*, July/Aug. 2016, Invited paper.

Patents:

- U.S. Pat. 5,041,701 – *Edge Linearization Device for a Contact Input System*, Aug. 20, 1991.
- U.S. Pat. 5,438,168 – *Touch Panel*, Aug. 1, 1995.
- U.S. Pat. 5,736,688 – *Curvilinear Linearization Device for Touch Systems*, Apr. 7, 1998.
- U.S. Pat. 6,037,930 – *Multimodal touch sensitive peripheral device*, March 14, 2000.
- U.S. Pat. 6,408,421 – *High-speed asynchronous decoder circuit for variable-length coded data*, June 18, 2002.
- U.S. Pat. 6,865,668 – *Variable-length, high-speed, asynchronous decoder circuit*, March 8, 2005
- U.S. Pat. 7,079,133 – *Superscalar 3D Graphics Engine*, July 18, 2006
- EP 1 661 131 B1 – *PORTABLE ENTERTAINMENT APPARATUS*, Jan. 21, 2009
- U.S. Pat. 7,555,006 – *Method and system for adaptive transcoding and transrating in a video network*, June 30, 2009
- U.S. Pat. 7,996,595 – *Interrupt Arbitration for Multiprocessors*, Aug. 9, 2011
- EP 2 241 979 B1 – *Interrupt Arbitration for Multiprocessors*, Oct. 10, 2011
- U.S. Pat. 8,131,970 – *Compiler Based Cache Allocation*, March 6, 2012
- U.S. Pat. 8,180,963 – *Hierarchical read-combining local memories*, May 15, 2012
- U.S. Pat. 8,193,941 – *Snoring Treatment*, June 5, 2012
- U.S. Pat. 8,203,541 – *OLED display and sensor*, June 19, 2012
- U.S. Pat. 8,243,045 – *Touch-sensitive display device and method*, August 14, 2012
- U.S. Pat. 8,244,982 – *Allocating processor cores with cache memory associativity*, August 14, 2012
- U.S. Pat. 8,260,996 – *Interrupt Optimization for Multiprocessors*, Sept. 4, 2012
- 101185761 (KR) – *Noise Cancellation for Phone Conversation*, Sept. 19, 2012
- 101200740 (KR) – *OLED display and sensor*, November 7, 2012
- 101200741 (KR) – *Touch-sensitive display device and method*, November 7, 2012
- U.S. Pat. 8,321,614 – *Dynamic scheduling interrupt controller for multiprocessors*, Nov. 27, 2012
- U.S. Pat. 8,352,679 – *Selectively securing data and/or erasing secure data caches responsive to security compromising conditions*, Jan. 8, 2013
- U.S. Pat. 8,355,541 – *Texture Sensing*, Jan. 15, 2013
- U.S. Pat. 8,370,307 – *Cloud Data Backup Storage Manager*, Feb. 5, 2013
- U.S. Pat. 8,398,451 – *Tactile Input Interaction*, March. 19, 2013
- JP 5241032 B2 – *Routing Across Multicore Network Using Real World or Modeled Data*, April 13, 2013
- ZL201010124820.3 – *Interrupt Optimization for Multiprocessors*, April 17, 2013
- U.S. Pat. 8,428,438 – *Apparatus for Viewing Television with Pause Capability*, April 23, 2013
- JP 5266197 B2 – *Data Centers Task Mapping*, May 10, 2013
- U.S. Pat. 8,508,498 – *Direction and Force Sensing Input Device*, August 13, 2013
- U.S. Pat. 8,547,457 – *Camera Flash Mitigation*, October 1, 2013
- U.S. Pat. 8,549,339 – *Processor core communication in multi-core processor*, October 1, 2013
- 101319048 (KR) – *Camera Flash Mitigation*, October 10, 2013
- U.S. Pat. 8,628,478 – *Microphone for remote health sensing*, January 14, 2014
- 101362017 (KR) – *Thread Shift: Allocating Threads to Cores*, Feb. 5, 2014
- 101361928 (KR) – *Cache Prefill on Thread Migration*, Feb. 5, 2014
- 101361945 (KR) – *Mapping Of Computer Threads onto Heterogeneous Resources*, Feb. 5, 2014
- JP 5487307 B2 – *Mapping Of Computer Threads onto Heterogeneous Resources*, Feb. 28, 2014
- JP 5484580 B2 – *Task Scheduling Based on Financial Impact*, Feb. 28, 2014
- JP 5487306 B2 – *Cache Prefill on Thread Migration*, Feb. 28, 2014
- 101372623 (KR) – *Power Management for Processor*, March. 4, 2014
- 101373925 (KR) – *Allocating Processor Cores with Cache Memory Associativity*, March 6, 2014
- U.S. Pat. 8,676,668 – *Method for the determination of a time, location, and quantity of goods to be made available based on mapped population activity*, March 18, 2014
- U.S. Pat. 8,687,533 – *Energy Reservation in Power Limited Networks*, April 1, 2014
- 101388735 (KR) – *Routing Across Multicore Networks Using Real World or Modeled Data*, April 17, 2014
- U.S. Pat. 8,725,697 – *Cloud Data Backup Storage*, May 13, 2014
- U.S. Pat. 8,726,043 – *Securing Backing Storage Data Passed Through a Network*, May 13, 2014
- ZL201010124826.0 – *Dynamic scheduling interrupt controller for multiprocessors*, May 14, 2014
- JP 5547820 B2 – *Processor core communication in multi-core processor*, May 23, 2014
- U.S. Pat. 8,738,949 – *Power Management for Processor*, May 27, 2014

U.S. Pat. 8,751,854 – *Processor Core Clock Rate Selection*, June 10, 2014
 JP 5559891 B2 – *Thermal Management in Multi-Core Processor*, June 13, 2014
 101414033 (KR) – *Dynamic Computation Allocation*, June 25, 2014
 JP 5571184 B2 – *Dynamic Computation Allocation*, July 4, 2014
 101426341 (KR) – *Processor core communication in multi-core processor*, May 23, 2014
 U.S. Pat. 8,799,671 – *Techniques for Detecting Encrypted Data*, Aug 5, 2014
 101433485 (KR) – *Task Scheduling Based on Financial Impact*, Aug. 18, 2014
 U.S. Pat. 8,824,666 – *Noise Cancellation for Phone Conversation*, Sept. 2, 2014
 U.S. Pat. 8,836,516 – *Snoring Treatment*, Sept. 16, 2014
 U.S. Pat. 8,838,370 – *Traffic flow model to provide traffic flow information*, Sept. 16, 2014
 U.S. Pat. 8,838,797 – *Dynamic Computation Allocation*, Sept. 16, 2014
 U.S. Pat. 8,854,379 – *Routing Across Multicore Networks Using Real World or Modeled Data*, Oct. 7, 2014
 JP 5615361 B2 – *Thread Shift: Allocating Threads to Cores*, Oct. 15, 2014
 U.S. Pat. 8,866,621 – *Sudden infant death prevention clothing*, Oct. 21, 2014
 U.S. Pat. 8,881,157 – *Allocating threads to cores based on threads falling behind threads*, Nov. 4, 2014
 ZL201080024755.5 – *Camera Flash Mitigation*, Nov 5, 2014
 U.S. Pat. 8,882,677 – *Microphone for remote health sensing*, Nov. 11, 2014
 U.S. Pat. 8,924,743 – *Securing Data Cache through Encryption*, December 30, 2014
 U.S. Pat. 8,994,857 – *Camera Flash Mitigation*, March 31, 2015
 JP 5699140 B2 – *Camera Flash Mitigation*, April 8, 2015
 ZL201080035189.8 – *Thread Shift: Allocating Threads to Cores*, June 10, 2015
 ZL201180005030.6 – *Processor core communication in multi-core processor*, June 10, 2015
 U.S. Pat. 9,143,814 – *Method and system for adaptive transcoding and transrating in a video network*, Sept 22, 2015
 ZL201080035177.5 – *Mapping Of Computer Threads onto Heterogeneous Resources*, Oct. 14, 2015
 U.S. Pat. 9,178,694 – *Securing Backing Storage Data Passed Through a Network*, November 3, 2015
 U.S. Pat. 9,189,282 – *Thread-to-core mapping based on thread deadline, thread demand, and hardware characteristics data collected by a performance counter*, November 17, 2015
 U.S. Pat. 9,189,448 – *Routing image data across on-chip networks*, November 17, 2015
 U.S. Pat. 9,208,093 – *Allocation of memory space to individual processor cores*, December 8, 2015
 U.S. Pat. 9,239,994 – *Data Centers Task Mapping*, January 19, 2016
 ZL201080036611.1 – *Allocating Processor Cores with Cache Memory Associativity*, January 20, 2016
 EP2228779 B1 – *Traffic flow model to provide traffic flow information*, Jan. 27, 2016
 U.S. Pat. 9,262,628 – *Operating System Sandbox*, February 16, 2016
 GB2485682 – *Mapping Of Computer Threads onto Heterogeneous Resources*, Sept. 28, 2016
 U.S. Pat. 9,330,137 – *Cloud Data Backup Storage Manager*, May. 3, 2016
 ZL201080035185.X – *Cache Prefill on Thread Migration*, Aug. 24, 2016
 U.S. Pat. 9,519,305 – *Processor Core Clock Rate Selection*, December 13, 2016
 U.S. Pat. 9,569,270 – *Mapping thread phases onto heterogeneous cores based on execution characteristics and cache line eviction count*, February 14, 2017
 GB2485683 – *Thread Shift: Allocating Threads to Cores*, Oct. 18, 2017
 U.S. Pat. 9,852,435 – *Telemetry based location and tracking*, December 26, 2017.
 U.S. Pat. 9,915,994 – *Power management for processor*, March 13, 2018
 U.S. Pat. 9,927,254 – *Traffic flow model to provide traffic flow information*, March 27, 2018
 EP2254048 B1 – *Thread Mapping in Multi-Core Processors*, August 29, 2018
 U.S. Pat. 10,860,432 – *Cloud Data Backup Storage Manager*, December 8, 2020