UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS, LLC,
Petitioner

v.

PALISADE TECHNOLOGIES, LLP,
Patent Owner.

Case No. IPR2025-01008
U.S. Patent No. 8,327,051

DECLARATION OF DR. R. JACOB BAKER IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,327,051

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I, R. Jacob Baker, declare as follows:

I. INTRODUCTION

1. My name is R. Jacob Baker Ph.D., P.E., and I am a professor emeritus of electrical and computer engineering. I have prepared this declaration as an expert witness on behalf of Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC ("Petitioner"). In this declaration, I will give my opinion as to whether Claims 1-2, 4-8, 16-17, 20-21, and 23-27 of U.S. Patent No. 8,327,051 ("the '051 patent") (Ex. 1001) are valid. I also provide herein the technical bases for these opinions, as appropriate.

2. This declaration contains statements of my opinions formed to date, and the bases and rationale for these opinions. I may offer additional opinions based on further review of materials in this case, including opinions and/or testimony of other expert witnesses.

3. For my efforts in connection with the preparation of this declaration, I have been compensated at my usual and customary rate for this type of consulting activity. My compensation is in no way contingent on the results of these or any other proceedings related to the '051 patent.

4. I have no financial interest in Petitioner or any of its subsidiaries. I do not have any financial interest in the '051 Patent and have not had any contact with the named inventor of the '051 Patent.

5. Additional details about my employment history, fields of expertise, awards, publications, and other activities are further included in my curriculum vitae, attached as Ex-1003.

II. BACKGROUND AND QUALIFICATIONS

6. My qualifications generally are set forth in my Curriculum Vitae, which is attached as **Ex-1003**. Ex-1003 also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

7. I started working as an Engineer in 1985 and I started teaching Electrical and Computer Engineering courses in 1991. I am currently a professor emeritus of electrical and computer engineering at the University of Nevada, Las Vegas ("UNLV").

8. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

9. My doctoral research, culminating in the award of a Ph.D., investigated the use of power MOSFETs in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch higher voltages, that is, greater than 1,000 V and 100 Amps of current with nanosecond switching times. This work was reported in the paper

entitled “Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices,” published in the IEEE Transactions on Power Electronics. The paper received the Best Paper Award in 2000.

III. INDUSTRY EXPERIENCE

10. I have done technical and expert witness consulting for over 200 companies and their subsidiaries since I started working as an engineer in 1985. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada test site. During this time I designed, and oversaw the fabrication of, over 30 electronic and electro-optic instruments, including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel’s cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

11. My work during this time, as one example, had a direct impact on my doctoral research work using power MOSFETs, subsequent publishing efforts, and industry designs. In addition to the 2000 Best Paper Award from the IEEE Power Electronics Society, I published several other papers in related areas while working in industry. I hold a patent, Patent No. 5,874,830, in the area of power supply design, titled, “Adaptively biased voltage regulator and operating method,” which

was issued on February 23, 1999. I have designed dozens of linear and switching power supplies for commercial products and scientific instrumentation.

12. I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. ("MTI") in Boise, Idaho. I spent considerable time working on the development of flash memory chips while at MTI. My efforts resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that can improve a computing system's performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late

1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via interprocess communications (IPC) with the memory controller (MC). I provided technical assistance with MTI's acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology. Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and 2010. This work entailed the design of low-power, high-speed, and wide interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

13. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB, firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable energy, and power electronics. For example, a part of my research at Boise State,

for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias (TWVs), for high-density 3D packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle. As another example, I designed circuitry for use in implementing Universal Serial Bus (USB) interface circuits while I did consulting at Tower Semiconductor. I designed PCI communication circuits for IPC between a Graphics Processor Unit (GPU) and memory while consulting for Rendition, Inc. From 1994 to 1996, I worked on the design of displays at Micron Display and Micron Technology, Inc. ("Micron") in Boise, Idaho. This work was at a time when cathode ray tubes (CRTs) were still the dominant type of display. Flat panel displays were being developed with the hope of replacing CRTs in the consumer market. I worked on flat panel displays which resulted in 5 patents: 5,598,156, 5,638,085, 5,818,365, 5,894,293, and 5,909,201. I worked on the design of the pixels, both active and passive, as well as the supporting electronics for processing video signals. I was involved with the evaluation of display technologies including liquid crystal displays (LCDs), light-emitting diodes, plasma displays, and organic light emitting diode (OLED) displays; the display technologies that were looking to displace CRTs in the consumer market. I was also involved with the packaging of the displays including the vacuum sealing and deposition of the phosphors for light wavelength conversion. I also taught display design as a topic in my courses and did display design consulting again in industry for Cirque in 2013.

14. My current research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (Light Detection And Ranging). I have worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics, and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory. Further, part of my research for several years focused on the digitization of IQ channels using delta-sigma modulation. The knowledge and experience gained from this effort are reflected in my textbook CMOS Mixed-Signal Circuit Design and a presentation, which I have presented at several universities and companies, http://cmosedu.com/jbaker/papers/talks/BP_DSM_talk.pdf.

IV. ACADEMIC EXPERIENCE

15. I was an adjunct faculty member in the Electrical Engineering departments of UNLV and UNR from 1991-1993. From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University ("BSU"), where I served as department chair from 2004 to 2007. At BSU, I helped establish

graduate programs in Electrical and Computer Engineering including, in 2006, the university's second Ph.D. degree. In 2012, I re-joined the faculty at UNLV. Over the course of my career as a professor, I have advised more than 100 masters and doctoral students.

16. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the "Father of Silicon Valley"). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award every year it was awarded while I have been back at UNLV.

17. I have authored several books and papers in the electrical and computer engineering area. My published books include CMOS Circuit Design, Layout, and Simulation (Baker, R.J., Wiley-IEEE, ISBN: 9781119481515 (4th ed., 2019)) and CMOS Mixed-Signal Circuit Design (Baker, R.J., Wiley-IEEE, ISBN: 9780470290262 (2nd ed., 2009) and ISBN: 9780471227540 (1st ed., 2002)). I co-

authored DRAM Circuit Design: Fundamental and High-Speed Topics (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 9780470184752 (2008)), DRAM Circuit Design: A Tutorial (Keeth, B. and Baker, R.J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and CMOS Circuit Design, Layout and Simulation (Baker, R.J., Li, H.W., and Boyce, D.E., Wiley - IEEE, ISBN: 9780780334168 (1998)). I contributed as an editor and co-author on several other electrical and computer engineering books.

V. OTHER RELEVANT EXPERIENCE

18. I have performed technical and expert witness consulting for more than 200 companies and their subsidiaries and given more than 50 invited talks at conferences, companies, and universities. Further, I am the author or co-author of more than 100 papers and presentations in the areas of electrical and computer engineering design, fabrication, and packaging.

19. I currently serve, or have served, as a volunteer on the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-

State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-present). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing.

20. In addition to the above, I am an IEEE Fellow for contributions to semiconductor memory design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

VI. UNDERSTANDING OF THE LAW

21. I have applied the following legal principles provided to me by counsel in arriving at the opinions set forth in this declaration.

A. Legal Standard for Prior Art

22. I understand that a patent or other publication must first qualify as prior art before it can be used to invalidate a patent claim.

23. I understand that a U.S. or foreign patent qualifies as prior art to an asserted patent if the date of issuance of the patent is prior to the invention of the asserted patent. I further understand that a printed publication, such as a book or an article published in a magazine or trade publication, qualifies as prior art to an asserted patent if the date of publication is prior to the invention of the asserted patent. A paper or presentation may also qualify as prior art if presented at a

publicly available seminar, conference, or trade show prior to the invention in the asserted patent.

24. I understand that a U.S. or foreign patent qualifies as prior art to an asserted patent if the date of issuance of the patent is more than one year before the filing date of the asserted patent. I further understand that a printed publication, such as a book or an article published in a magazine or trade publication, constitutes prior art to an asserted patent if the publication occurs more than one year before the filing date of the asserted patent.

25. I understand that a U.S. patent qualifies as prior art to the asserted patent if the application for that patent was filed in the United States before the invention of the asserted patent.

26. I understand that to qualify as prior art, a reference must contain an enabling disclosure that allows one of ordinary skill to practice the claims without undue experimentation.

27. I understand that documents and materials that qualify as prior art can be used to invalidate a patent claim as anticipated or as obvious.

B. Legal Standard for Anticipation

28. I understand that once the claims of a patent have been properly construed, the second step in determining anticipation of a patent claim requires a

comparison of the properly construed claim language to the prior art on a limitation-by-limitation basis.

29. I understand that a prior art reference "anticipates" an asserted claim, and thus renders the claim invalid, if all elements of the claim are disclosed in that prior art reference, either explicitly or inherently (i.e., necessarily present or implied).

30. I understand that a patent is anticipated if before such person's invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it.

31. I have written this declaration with the understanding that in an inter partes review anticipation must be shown by a preponderance of the evidence.

C. Legal Standard for Obviousness

32. I have been instructed by counsel on the law regarding obviousness, and understand that even if a patent is not anticipated, it is still invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person of ordinary skill in the pertinent art.

33. I understand that a person of ordinary skill in the art provides a reference point from which the prior art and claimed invention should be viewed.

This reference point prevents a person of ordinary skill from using one's insight or hindsight in deciding whether a claim is obvious.

34. I also understand that an obviousness determination includes the consideration of various factors such as (1) the scope and content of the prior art, (2) the differences between the prior art and the challenged claims, (3) the level of ordinary skill in the pertinent art, and (4) the existence of secondary considerations such as commercial success, long-felt but unresolved needs, failure of others, etc.

35. I am informed that secondary considerations of non-obviousness may include (1) a long felt but unmet need in the prior art that was satisfied by the invention of the patent; (2) commercial success or lack of commercial success of processes covered by the patent; (3) unexpected results achieved by the invention; (4) praise of the invention by others skilled in the art; (5) taking of licenses under the patent by others; and (6) deliberate copying of the invention. I also understand that there must be a relationship between any such secondary indicia and the invention. I further understand that contemporaneous and independent invention by others is a secondary consideration supporting an obviousness determination.

36. I understand that an obviousness evaluation can be based on a combination of multiple prior art references. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the link between two or more prior art references is simple

common sense. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may be supplied by the direction of the marketplace.

37. I understand that if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

38. I also understand that practical and common-sense considerations should guide a proper obviousness analysis, because familiar items may have obvious uses beyond their primary purposes. I further understand that a person of ordinary skill in the art looking to overcome a problem will often be able to fit the teachings of multiple publications together like pieces of a puzzle, although the prior art need not be like two puzzle pieces that must fit perfectly together. I understand that obviousness analysis therefore considers the inferences and creative steps that a person of ordinary skill in the art would employ under the circumstances.

39. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. For example, when there is a design need or market pressure to solve a problem and there are a finite number of

identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

40. I understand that the combination of familiar elements according to known methods may be proven obvious when it does no more than yield predictable results. When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, obviousness likely bars its patentability.

41. It is further my understanding that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

42. I understand that a claim can be obvious in light of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in the reference can be supplied by the common sense of one of skill in the art.

43. I understand that a person of ordinary skill could have combined two pieces of prior art or substituted one prior art element for another if the substitution

can be made with predictable results, even if the swapped-in element is different from the swapped-out element. In other words, the prior art need not be like two puzzle pieces that must fit together perfectly. The relevant question is whether prior art techniques are interoperable with respect to one another, such that that a person of skill would view them as a design choice, or whether a person of skill could apply prior art techniques into a new combined system.

44. In sum, my understanding is that prior art teachings are properly combined where a person of ordinary skill in the art having the understanding and knowledge reflected in the prior art and motivated by the general problem facing the inventor, would have been led to make the combination of elements recited in the claims. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of multiple prior art references in the claimed manner.

45. I have been informed and understand that the obviousness analysis requires a comparison of the properly construed claim language to the prior art on a limitation-by-limitation basis.

46. I have written this declaration with the understanding that in an inter partes review obviousness must be shown by a preponderance of the evidence.

D. Legal Standard for Claim Construction

47. I have been instructed by counsel on the law regarding claim construction and patent claims and understand that a patent may include two types of claims, independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim or another dependent claim. I understand that a dependent claim includes all the limitations that it recites in addition to all of the limitations recited in the claim from which it depends.

48. It is my understanding that in proceedings before the USPTO, claims are construed similarly as in district court litigation, and that this standard is sometimes referred to as the *Phillips* standard. Under this standard, it is my understanding that claim terms are given the meaning the term would have to a person of ordinary skill in the art at the time of the invention, in view of the specification and file history.

49. In comparing the claims of the '051 patent to the prior art, I have carefully considered the '051 patent and its file history in light of the understanding of a person of skill at the time of the alleged invention.

50. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood disputed claim language to

mean. Such sources include the words of the claims themselves, the remainder of the patent's specification, the prosecution history of the patent (all considered "intrinsic" evidence), and "extrinsic" evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.

51. I understand that, in construing a claim term, one looks primarily to the intrinsic patent evidence, including the words of the claims themselves, the remainder of the patent specification, and the prosecution history.

52. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

53. I understand that words or terms should be given their ordinary and accepted meaning unless it appears that the inventors were using them to mean something else. In making this determination, the claims, the patent specification, and the prosecution history are of paramount importance. Additionally, the specification and prosecution history must be consulted to confirm whether the patentee has acted as its own lexicographer (*i.e.*, provided its own special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope.

54. I understand that the claims of a patent define the scope of the rights conferred by the patent. The claims particularly point out and distinctly claim the

subject matter which the patentee regards as his invention. Because the patentee is required to define precisely what he claims his invention to be, it is improper to construe claims in a manner different from the plain import of the terms used consistent with the specification. Accordingly, a claim construction analysis must begin and remain centered on the claim language itself. Additionally, the context in which a term is used in the asserted claim can be highly instructive. Likewise, other claims of the patent in question, both asserted and unasserted, can inform the meaning of a claim term. For example, because claim terms are normally used consistently throughout the patent, the usage of a term in one claim can often illuminate the meaning of the same term in other claims. Differences among claims can also be a useful guide in understanding the meaning of particular claim terms.

55. I understand that the claims of a patent define the purported invention. I understand that the purpose of claim construction is to understand how one skilled in the art would have understood the claim terms at the time of the purported invention.

56. I understand that a person of ordinary skill in the art is deemed to read a claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification. For this reason, the words of the claim must be interpreted in view of the

specification. The specification is the primary basis for construing the claims and provides a safeguard such that correct interpretations closely align with the specification. Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim as set forth in the patent itself.

57. I understand that it is improper to place too much emphasis on the ordinary meaning of the claim term without adequate grounding of that term within the context of the specification of the asserted patent. Hence, claim terms should not be broadly construed to encompass subject matter that, although technically within the broadest reading of the term, is not supported when the claims are read in light of the invention described in the specification. Put another way, claim terms are given a meaning that is consistent with the specification and the prosecution history. Art incorporated by reference or otherwise cited during the prosecution history is also highly relevant in ascertaining the breadth of claim terms.

58. I understand that the role of the specification is to describe and enable the invention. In turn, the claims cannot be of broader scope than the invention that is set forth in the specification.

59. I understand that claim terms must be construed in a manner consistent with the context of the intrinsic record. In addition to consulting the

specification, one should also consider the patent's prosecution file history, if available. The file history provides evidence of how both the Patent Office and the inventors understood the terms of the patent, particularly in light of what was known in the prior art. Further, where the specification describes a claim term broadly, arguments and amendments made during prosecution may require a narrower interpretation.

60. I understand that while intrinsic evidence is of primary importance, extrinsic evidence, *e.g.*, all evidence external to the patent and prosecution history, can also be considered, including expert and inventor testimony, dictionaries, and learned treatises. For example, technical dictionaries may help one better understand the underlying technology and the way in which one of skill in the art might use the claim terms. Extrinsic evidence should not be considered, however, unhinged from the context of the intrinsic evidence. Evidence beyond the patent specification, prosecution history, and other claims in the patent should not be relied upon unless the claim language is ambiguous in light of these intrinsic sources. Furthermore, while extrinsic evidence can shed useful light on the relevant art, it is less significant than the intrinsic record in determining the legally operative meaning of claim language.

61. I understand that in general, a term or phrase found in the introductory words of the claim, the preamble of the claim, should be construed as a limitation

if it recites essential structure or steps, or is necessary to give life, meaning, and vitality to the claim. Conversely, a preamble term or phrase is not limiting where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention. In making this distinction, one should review the entire patent to gain an understanding of what the inventors claim they actually invented and intended to encompass by the claims.

62. I understand that language in the preamble limits claim scope (i) if dependence on a preamble phrase for antecedent basis indicates a reliance on both the preamble and claim body to define the claimed invention; (ii) if reference to the preamble is necessary to understand limitations or terms in the claim body; or (iii) if the preamble recites additional structure or steps that the specification identifies as important.

E. Legal Standard for Priority Date

63. I further understand that the "critical date" for a patent is one year prior to its filing date. It is my understanding that the critical date is significant because patents, systems, or documents that are public prior to the critical date will invalidate a patent regardless of whether the inventors invented the claim if they disclose each and every limitation of the claims.

64. I further understand that the "priority date" of a patent is the date on which it is filed, or the date on which an earlier-filed patent application is filed if the patentee claims the benefit of priority to that earlier-filed patent application. I further understand that the priority date is significant because patents, systems, or documents that are public less than one year prior to the priority date may invalidate the claims. My understanding is that, for such prior art references, a patentee may attempt to show that the claimed invention was conceived prior to the publication date of the prior art reference.

65. I understand that a patent may be valid over prior art that was published or was publicly available before the priority date but after the critical date. To do so, it is my understanding that patentee must prove with corroborating evidence that the named inventors conceived of the claimed invention before the prior art and were diligent in reducing the claimed inventions to practice.

VII. RELIEF REQUESTED

66. It is my opinion that Claims 1-2, 4-8, 16-17, 20-21, and 23-27 of the '051 Patent would have been obvious under 35 U.S.C. § 103 on the following grounds:

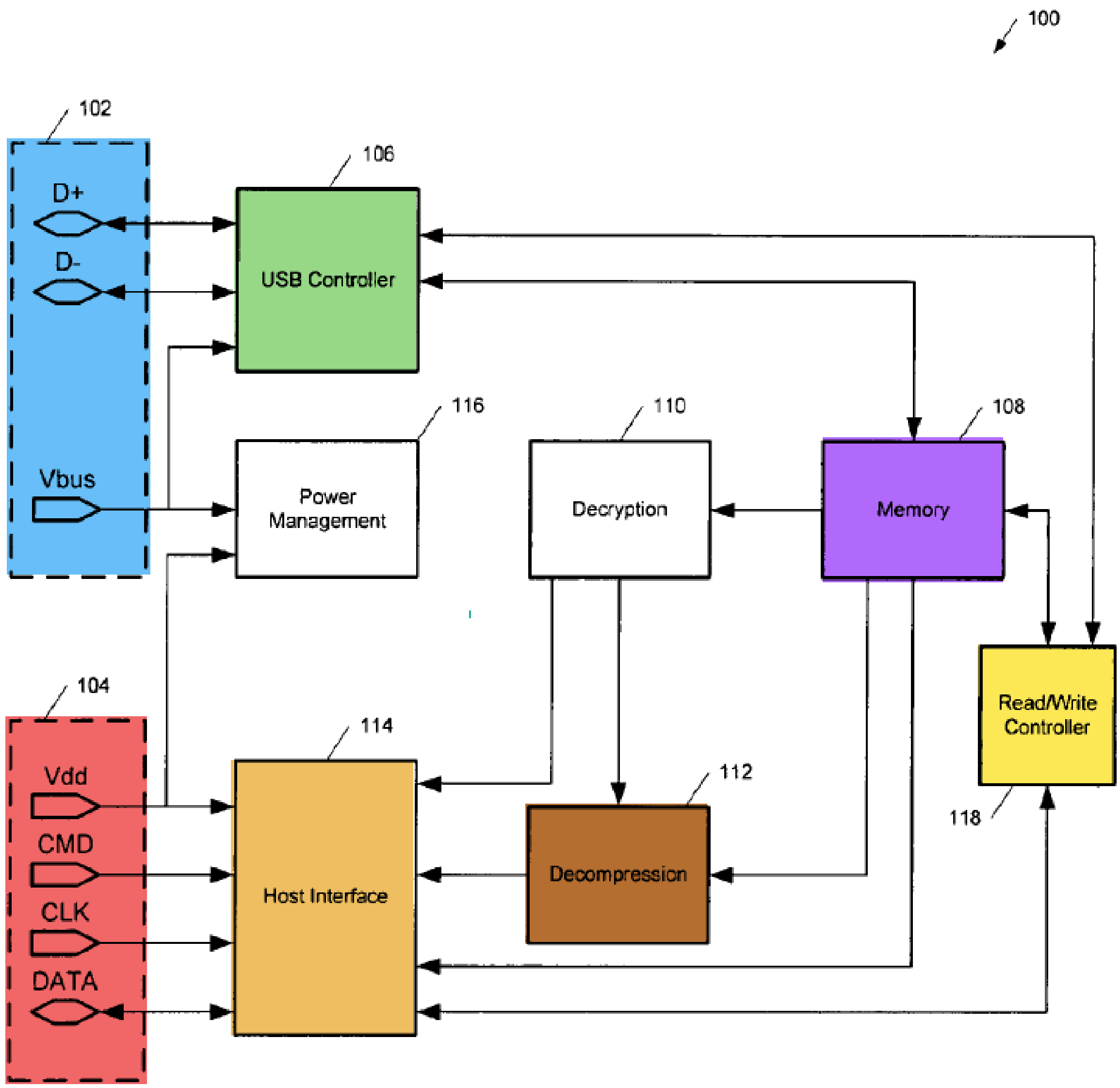
Ground	Summary
1	Claims 1, 4-8, 16, 20-21, and 23-27 are obvious over Diggs (Ex-1005).
2	Claims 2 and 17 are obvious over Diggs in view of Thorsten (Ex-1008).
3	Claims 1, 4-8, 16, 20-21, and 23-27 are obvious over Lin (Ex-1007).
4	Claims 2 and 17 are obvious over Lin in view of Thorsten.

VIII. THE CHALLENGED PATENT

A. The ’051 Patent

67. The’051 Patent “relates to memory devices, and particularly, to portable handheld memory cards configured to transfer data over various interfaces” to a host electronic device. Ex-1001 (’051 Patent), 1:6-16. The disclosed memory cards feature “a Universal Serial Bus (USB) port, USB controller circuitry, an input/output (I/O) port, a memory,” and “a housing storing the memory and exposing the USB port and the I/O port,” where “[t]he USB port and I/O port [are] positioned to allow a same-card insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port.” ’051 Patent, 1:61-2:4; *see also id.*, code (57).

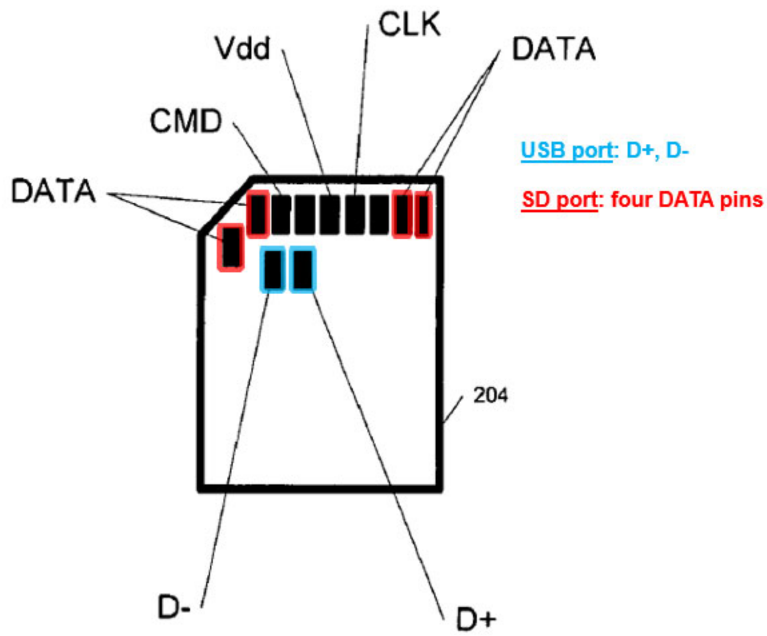
68. Figure 1, which I have annotated below, illustrates “an embodiment of a memory card 100.” ’051 Patent, 2:57-62. In operation, data is “transferred between the memory 108” (purple) “and an external device directly via the USB port 102” (blue). ’051 Patent, 3:32-35. The USB port includes “serial data lines D+ and D- and a bus voltage Vbus,” where the D+ and D- lines are “in communication with the USB controller 106” (green). ’051 Patent, 3:33-35, 45-48. As I have further shown, “[t]he memory card 100 may also communicate with external devices using an input/out (I/O) port, such as the SD port 104” (red). ’051 Patent, 3:64-66. The SD port “include[s] a voltage Vdd, a command line CMD, a clock line CLK, and a data bus DATA, all of which [are] in communication with the host interface circuit 114” (orange). ’051 Patent, 4:1-4. “The memory card 100 may also decompress compressed data” stored in memory 108 “with the decompression circuit 112” (brown) "so that a connected device does not need to include potentially costly and complex decompression circuitry.” ’051 Patent, 3:12-16. “Data flow to and from the memory 108 may be a managed by the read/write controller 118” (yellow), which “may be in communication with USB controller 106 and host interface 114 to control and coordinate read and write operations between” the memory and either of the two ports. ’051 Patent, 3:23-29.



’051 Patent, Fig. 1 (annotated).

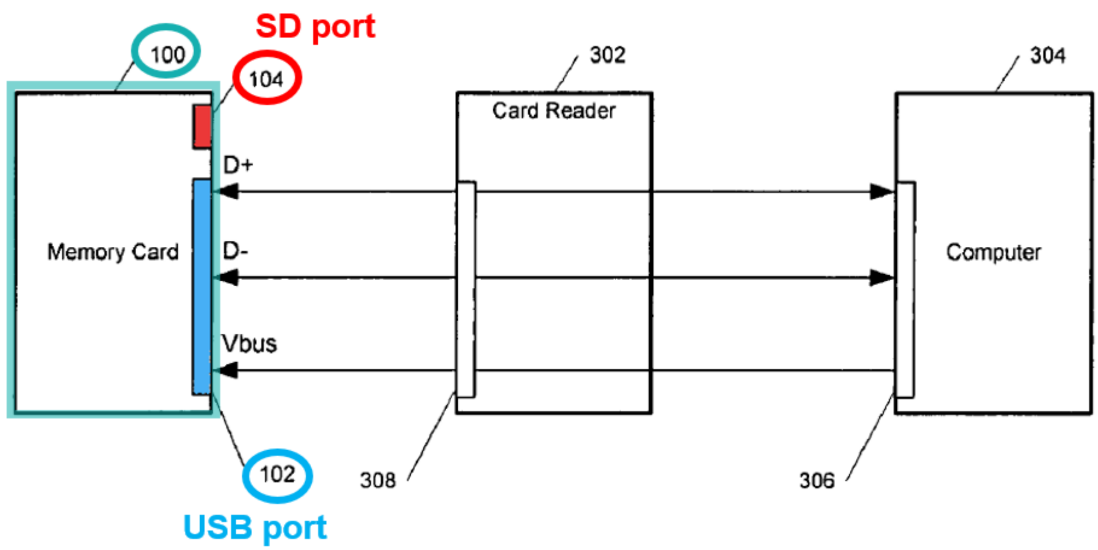
69. Figure 2 (annotated) shows “a schematic of an exemplary pinout of an embodiment of a memory card 200 … that complies with the Secure Digital standard,” where “the SD port shown in Fig. 2 … includ[es] pins for the voltage Vdd, the command line CMD, the clock link CLK, and the data bus DATA,”

whereas "the USB port shown in Fig. 2 includes serial data pins D+ and D-." '051 Patent, 4:38-61, Fig. 2.



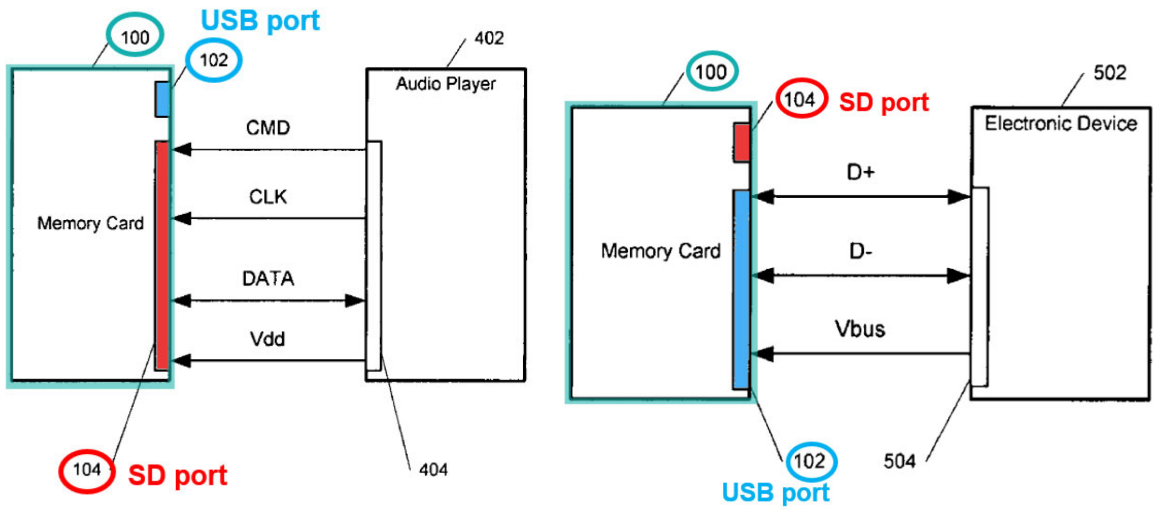
'051 Patent, Fig. 2 (annotated).

70. Figures 3-5 each show a memory card interfaced with a card reader and/or electronic device, to transfer data between the memory and the device. *See* '051 Patent, 5:10-12, 43-45, 6:3-5. In Figure 3, which I have annotated below, data is transferred between memory card 100 and a computer 304 using the USB protocol, such that "there may be no electrical connection to the SD port of the memory card 100 and only an electrical connection to the USB port 102 of the memory card 100 via the mating USB port 308 of the card reader 302." '051 Patent, 5:12-35.



’051 Patent, Fig. 3 (annotated).

71. Likewise, in Figure 5, which I have annotated below, data is “transferred between electronic device 502 and the memory card 100 using the USB protocol” via USB port 102, since “the electronic device 502” does not include a mating SD port.” ’051 Patent, 6:3-23. Conversely, in Figure 4, which I have annotated below, the memory card 100’s “SD port 104 interfaces with”—and is “electrically connected to”—“a mating SD port 404 of [an] audio player 402,” whereas “the USB port 102 of the memory card 100 is not electrically connected.” ’051 Patent, 5:43-53.



’051 Patent, Figs. 4-5 (annotated).

B. Prosecution History of the ’051 Patent

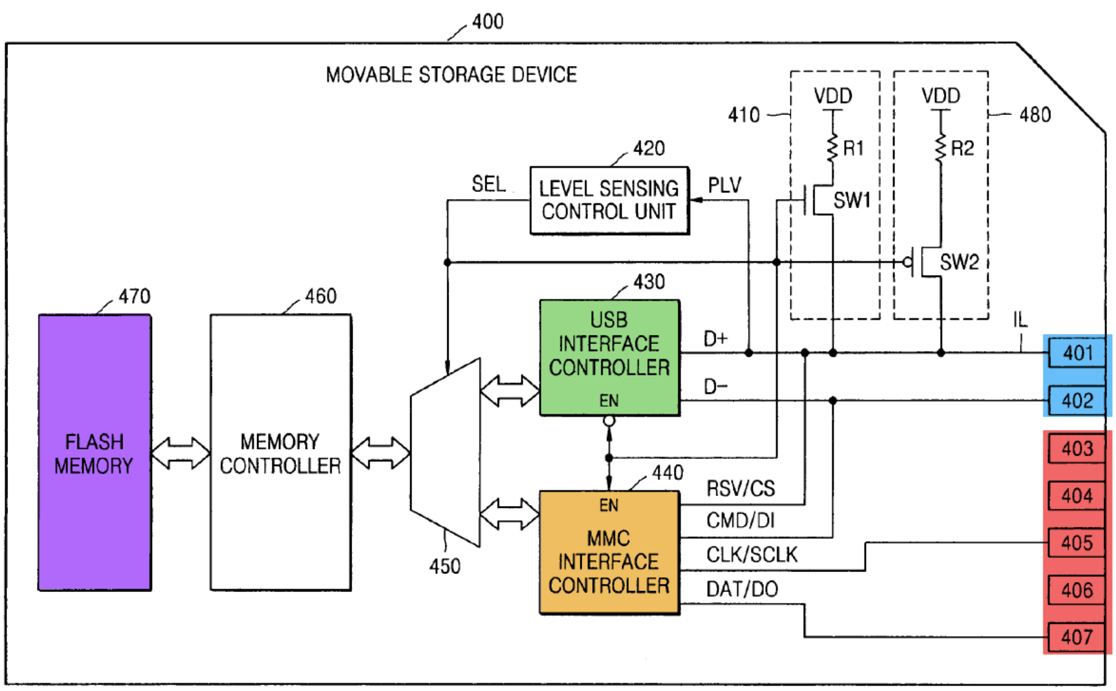
72. The ’051 file history is submitted as Ex-1004. Over the course of prosecution, the Examiner issued five rejections, prompting the Applicant to make aa series of amendments to the pending claims in order to eventually obtain issuance. Notably, the Examiner relied on the prior art Kim reference (Ex-1022), arguing that Kim’s Figure 8 (which I have reproduced below) discloses the majority of the ’051 Patent’s claim elements. Specifically the Examiner asserted that Kim discloses:

- a USB port comprising a first set of pins, and associated “USB controller circuitry” (Kim’s pins 401 and 402, and USB interface controller)
- an I/O port comprising a second set of pins, and associated “I/O controller circuitry” (Kim’s pins 402, 405, 407, and MMC interface controller)
- a memory in communication with both ports (Kim’s flash memory 470)

- a housing storing the memory and exposing both ports (Kim's movable storage device 400); and
- the ports being "positioned on a same end . . . to allow a same-card insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port"

See Ex-1004 ('051 File History) at 70-75 (February 14, 2012 Office Action at 2-7).

FIG. 8



Ex-1022 (Kim), Fig. 8 (annotated); Ex-1004 ('051 File History) at 70-75.

73. The Applicant did not dispute Examiner's identification of the above-listed features in Kim. Instead, the Applicant distinguished Kim—and thereby obtained allowance of the '051 Patent—by amending the claims to further specify that "the USB port and the I/O port are positioned such that when the I/O port is

electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device." Ex-1004 at 46-53 (July 16, 2012 Amendment and Response at 2-9). Applicant emphasized that this feature is consistent with Figure 1 of the '051 Patent, and is beneficial in that it "allow[s] the pin layout for the USB port to be different from the pin playout for the SD port"—i.e., the USB port's pinout "does not need to be forced into a particular layout (which may not be compatible with USB standards) in order to conform with the pinout of the second port." *Id.* at 52-53.

C. Level of Ordinary Skill in the Art

74. A person of ordinary skill in the art at the relevant time ("POSITA") would have had a bachelor's degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory systems with additional education substituting for experience and vice versa. I possessed and exceeded such experience and knowledge before and at the priority date.

IX. CLAIM CONSTRUCTION

75. I do not believe that any term requires explicit construction to resolve the issues presented in this Petition. I ascribe the plain meaning to each claim term, as that plain meaning would have been understood by a POSITA.

76. I reserve the right to offer opinions on any claim constructions proposed in this proceeding or to offer opinions on additional constructions in the district court.

X. TECHNOLOGICAL BACKGROUND

A. External memory cards having multiple ports were well known.

77. At the time of alleged invention of the ’051 Patent (November 2007), external memory cards having multiple ports were well-known.

78. For context, a “port” may refer to the physical interface between a device and a circuit, or it may also refer to the logical interface between two systems. Ex-1026 (Newton’s Telcom Dictionary 23rd ed (2007)) (“port”).

79. Multi-port memory cards were compatible with host devices that use various industry-standard protocols. These include: Universal Serial Bus (“USB”); MultiMediaCard (“MMC”); Secure Digital (“SD”), which is a successor to MMC; IEEE-1394, also known as “FireWire” for Apple products; Parallel ATA (PATA), originally AT Attachment, also known as Integrated Drive Electronics (IDE), for IBM products; and others.

80. The USB industry standard was introduced in 1996 and developed by the USB Implementers Forum (USB-IF) for digital data transmission and power delivery between various types of electronic devices. The USB 2.0 Specification, released in April 2000 (Ex-1033), introduced a number of modifications (called "engineering change notifications" (or ECNs)), including the Mini-A and Mini-B connector, and Micro-USB cables and connectors. The 2003 "On-The-Go" Supplement to the USC 2.0 Specification (Ex-1025) defines cables for compliance with "USB Mini-A and Mini-B. *See* Ex-1025 at 9-10.

81. The MMC standard, introduced in 1997, is based on a low-pin-count serial interface using a single memory stack substrate. The SD standard format was introduced in 1999 by the SD Association, as a successor to MMC. SD cards have been widely adopted in a variety of portable consumer electronics, including digital cameras, video game consoles, and mobile phones. A 2007 version of the SD Specification (SD Specifications Part E1 SDIO Simplified Specification Version 2.00) (Ex-1028, "Secure Digital Specification"), provides basic details regarding the SD standard, including pin assignments. *See* Ex-1028 at 3 ("Signal pins").

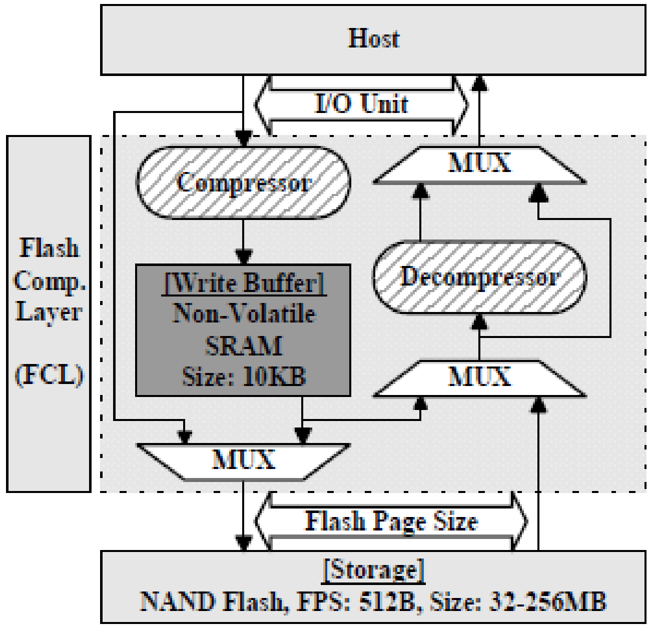
82. IEEE-1394, also known as "FireWire", is a serial bus interface standard for high-speed communications that was developed by Apple in the late 1980s and early 1990s. A 2000 Amendment to the IEEE-1394 Standard (IEEE

Standard for a High Performance Serial Bus—Amendment 1) (Ex-1029, "IEEE-1394 Specification") provides details regarding the four-pin version IEEE-1394 / FireWire connector socket. *See* Ex-1029 at 25-29.

B. Using compression techniques in conjunction with memory cards was well-known.

83. A POSITA would have known that using compression techniques in conjunction with memory cards was well-known and provided multiple benefits.

84. For example, Yim et al., *A Flash Compression Layer for SmartMedia Card Systems* (Feb. 2004) (Ex-1023, "Yim"), published in the IEEE Transactions on Consumer Electronics, recognized the increasing popularity of flash memory-based memory cards for mobile consumer electronics. Yim notes that "[s]ince flash memory is an order of magnitude more expensive than magnetic disks, ***data compression can be effectively used*** in managing flash memory based storage systems." Yim at 2. Yim discloses a "SmartMedia" memory card having a "compressor" and a "decompressor," as shown in Figure 5 below.



Ex-1023 (Yim), Fig. 5

85. As another example, U.S. Patent Application Pub. No. 2004/0250010 to Chen (Ex-1006, "Chen"), which published in December 2004, discloses "a storage device that utilizes compression technology to compress the data to be stored [in order] to boost data storage capacity." Ex-1006 (Chen), ¶¶1, 22. To do so, Chen's storage device includes "a data compression module 104" and "a data decompression module 105". Chen, ¶24. Chen teaches that its design achieves beneficial results, including boosting the "logical data storage capacity of the solid state storage medium ... without altering the physical storage capacity," along with improved access speed of the storage device." Chen, ¶32.

C. Using encryption techniques in conjunction with memory cards was well-known.

86. A POSITA would have known that using encryption techniques in conjunction with memory cards was well-known and provided multiple benefits. This is reflected, for example, in the Third Edition (2003) of the SMART CARD HANDBOOK textbook (Ex-1032). *See* Ex-1032 at 7-8, 19, 177-202.

87. As another example, Published German Patent Application No. DE 10220629A1 to Thorsten (certified translation, Ex-1009 ("Thorsten")) which published in November, 2003, discloses "data carrier"—e.g., memory card—"comprising a non-volatile memory, a data interface via which data can be written to and read from the non-volatile memory, and an interface module which is connected between the data interface and the memory and by way of which the data can be encrypted and/or decrypted." Thorsten, ¶1. As shown in Figure 1, "the interface module comprises a logic component that is responsible for the encryption and/or decryption process." Thorsten, ¶8. Thorsten teaches that its encryption and decryption technique protects sensitive data being stored into the memory, while remaining compatible with different host applications. Thorsten, ¶¶2, 4.

D. Using power management circuitry in conjunction with memory cards was well-known.

88. A POSITA would have known that incorporating power management circuitry in memory cards was well-known.

89. For example, U.S. Patent No. 7,082,483 to Poo (Ex-1030, "Poo") shows and describes, in Figure 1, a "power supply circuit 150" that "serves as a power source for various components of portable memory device 100," which includes a "USB controller 130." Ex-1030 (Poo) at 3:40-46, Fig. 1.

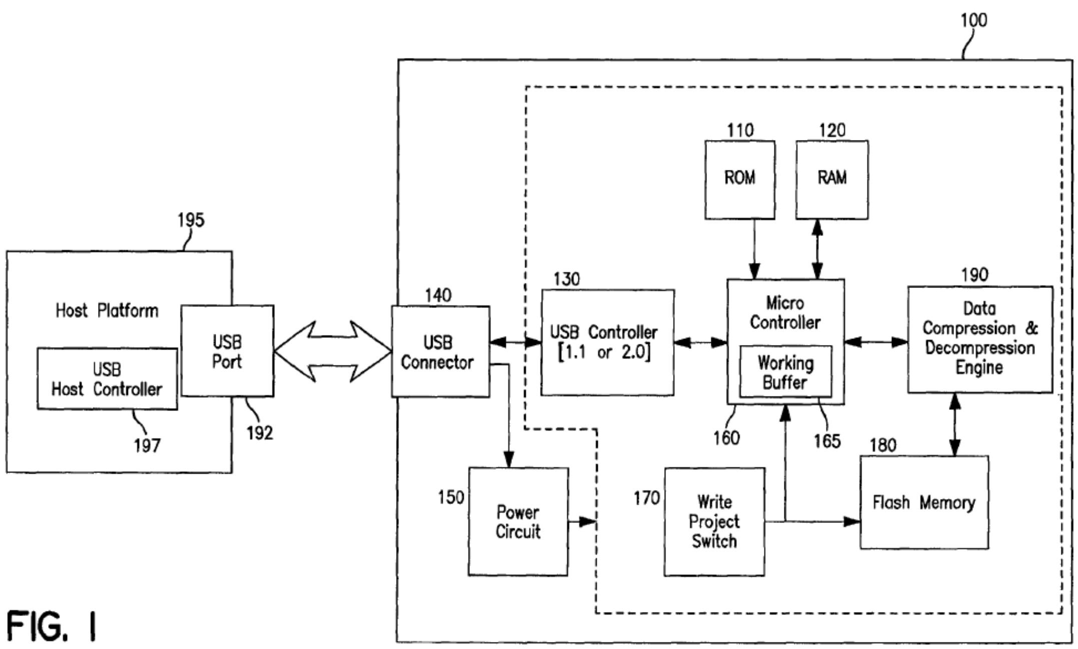


FIG. 1

Ex-1030 (Poo), Fig. 1.

90. As another example, published U.S. Patent Application No. 2005/0102471 to Tsai et al. (Ex-1031, "Tsai") similarly shows and describes, in Figure 3, an integrated portable storage apparatus that includes a "voltage adapter

134 [that] is provided to adapt the voltage and to supply a stable power source to the USB interface 131."

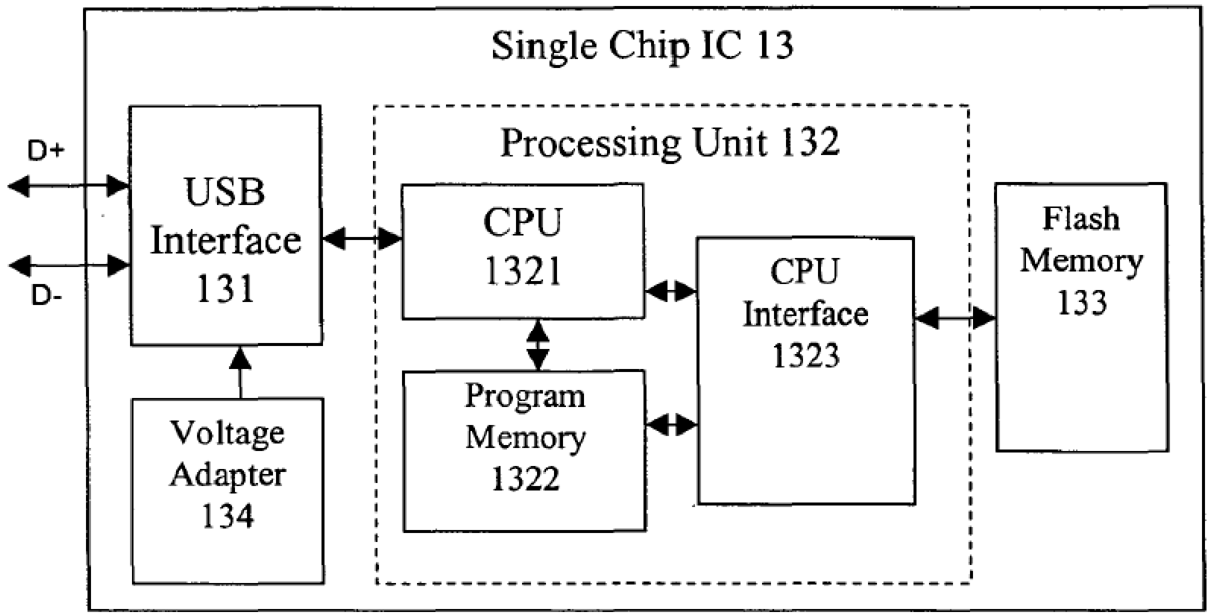


Figure 3

Ex-1031 (Tsai) at ¶25, Fig. 3.

XI. BRIEF DESCRIPTION OF THE APPLIED PRIOR ART REFERENCES

A. Diggs (Ex-1005)

91. Diggs (U.S. Patent Application Pub. No. US2009/0031073) was filed July 26, 2007, and published January 29, 2009. Diggs qualifies as prior art at least under pre-AIA §102(e).

92. Diggs discloses "[a] solid-state storage subsystem, such as a non-volatile memory card or drive, [that] includes multiple interfaces"—*i.e.*, "multiple

physical connectors and bus structures for different signal interfaces"—"and a memory area [for] storing information." Diggs, code (57), ¶10. Diggs's storage subsystem may be "simultaneously connected across multiple host systems, using ... a priority management scheme for handling multiple data access commands." Diggs, ¶12; *see also id.*, 9. Figure 2 shows multiple host systems (210, 211, and 212), each "utiliz[ing] a different signal interface to communicate with storage subsystem 100"—including a "USB interface 220" and "an IEEE-1394 interface 221." Diggs, ¶¶39, 26, Fig. 2. "Each recording system"—*i.e.*, host—"may be connected to the storage subsystem with a corresponding physical connector 223, 234, and 235 and over a bus structure 236, 237, and 238." Diggs, ¶40. In Figure 2, "audio recording system 210 is connected to USB controller 230 [while] video recording system 211 is connected to IEEE-1394 controller 231 ... Accordingly, physical connector 233 may be a USB mini-A connector [while] physical connector 234 may be a four-pin Firewire connector," and "[b]us structures 236 [and] 237 ... correspond to USB [and] IEEE-1394 bus structures ... respectively." Diggs, ¶ 40.

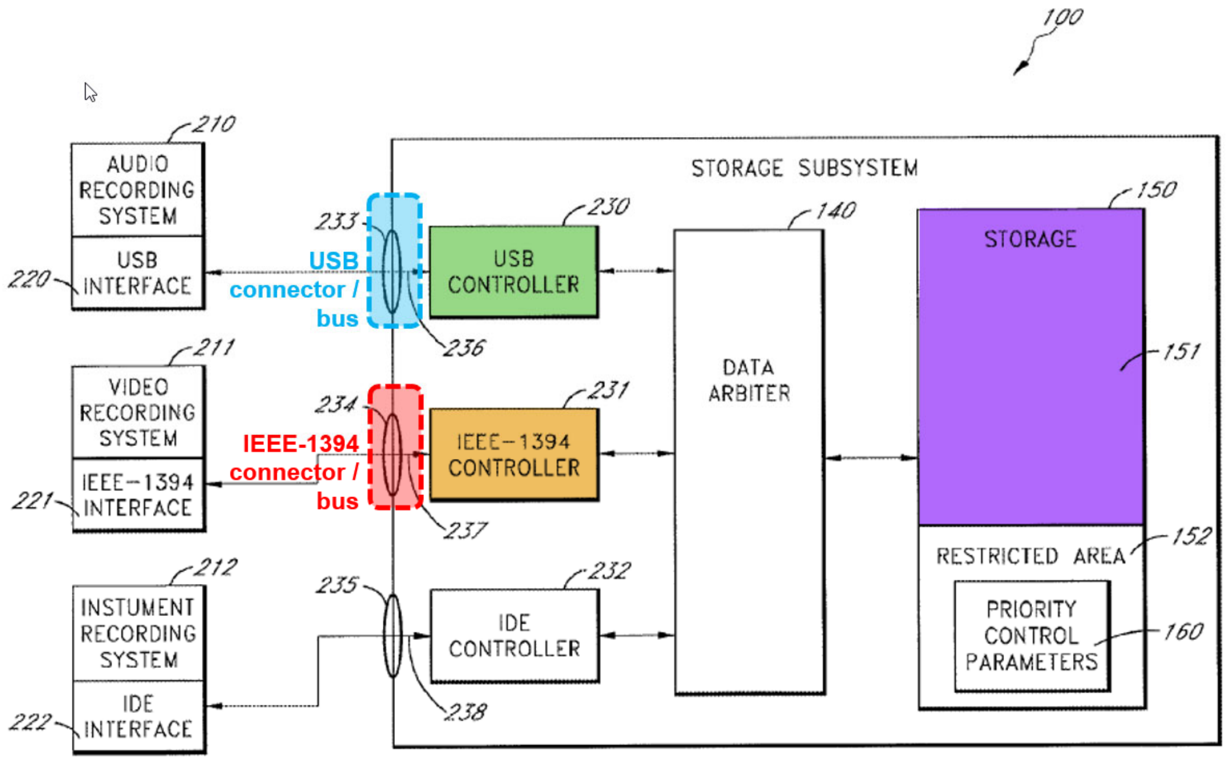


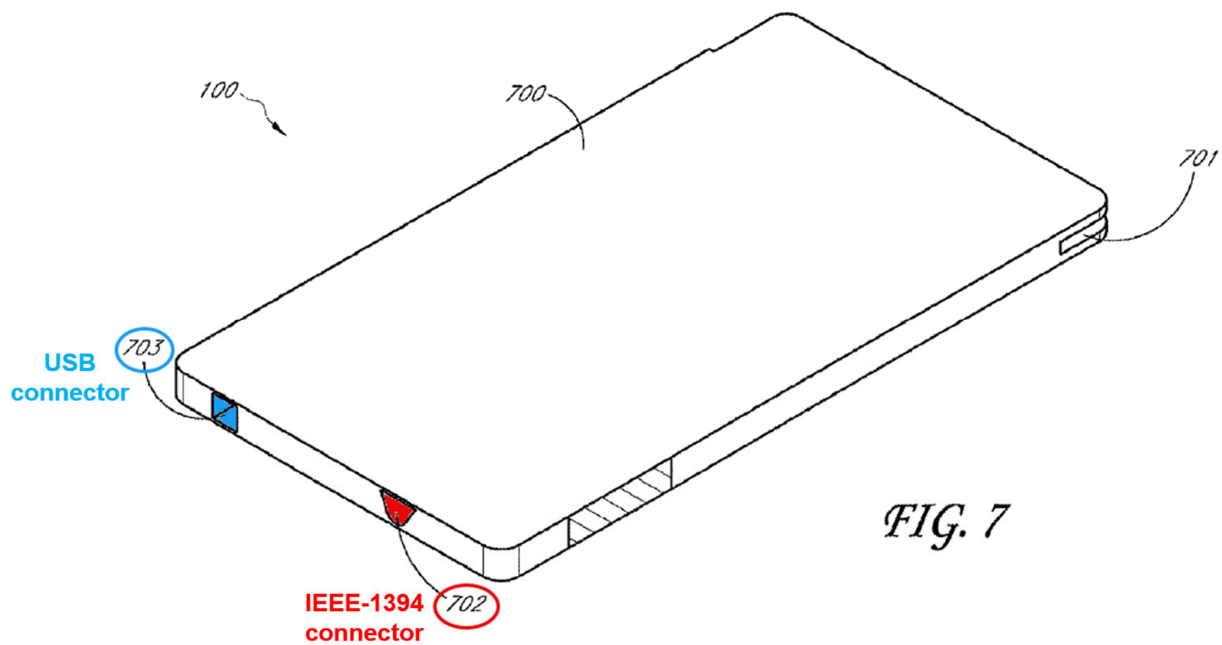
FIG. 2

Diggs, Fig. 2 (annotated).

93. "The storage subsystem further comprises a storage 150," which includes a "user data memory area 151 that is generally accessible by the operating systems of [the] host systems." Diggs, ¶¶ 30, 38. "Data arbiter 140 is responsible for prioritizing read/write commands received simultaneously from [the] multiple controllers," and does so based on "priority control parameters 160" that are stored in "a restricted memory area 152 of the storage 150." Diggs, ¶¶32-34.

94. The storage subsystem 100 of Figure 2 may have the "PC Card form factor" shown in Figure 7 (below). Diggs, ¶55. The subsystem includes "three

[separate] physical connectors 701, 702, and 703. . . Physical connector 702 comprises a USB mini-A connector and is connected to a USB con[troller] over a USB bus structure. Physical connector 7[0]3 comprises an IEEE-1394 four-pin connector, and is connected to an IEEE-1394 controller using IEEE-1394 bus structure." Diggs, ¶55.[1]



Diggs, Fig. 7 (annotated).

B. Thorsten (Ex-1009)

95. German Patent Application Publication No. DE 10220629A1 to Thorsten (Ex-1008) (certified translation, Ex-1009 ("Thorsten")) was filed on

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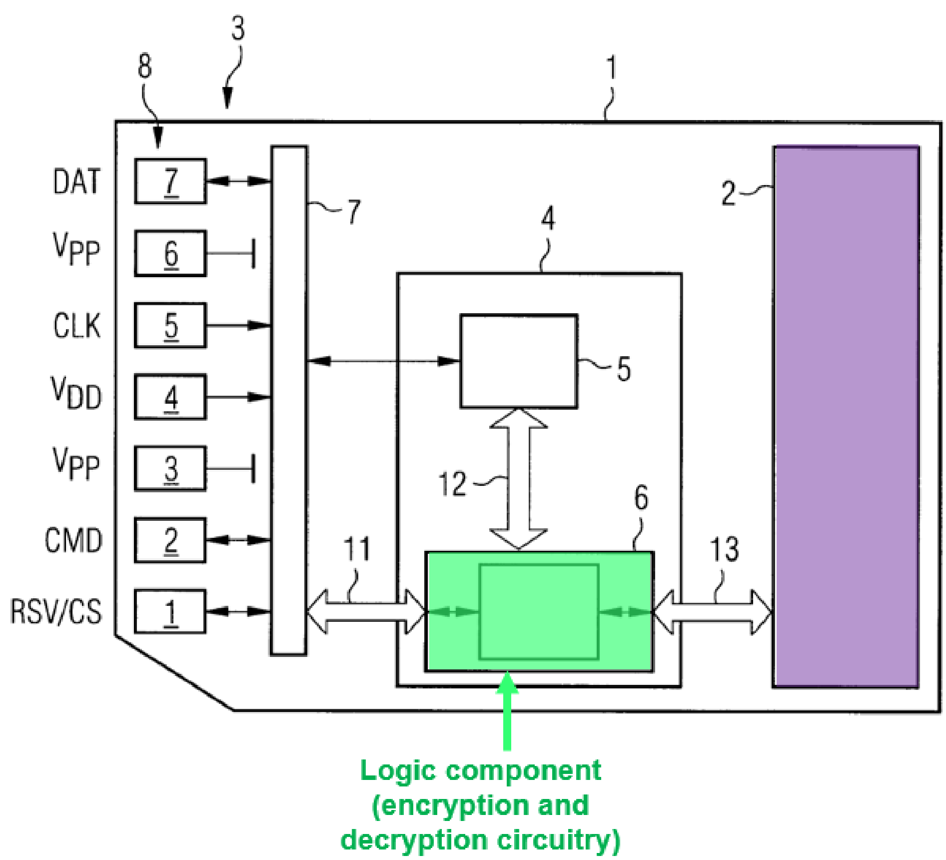
[1] Paragraph 55 of Diggs appears to include two typos: "793" should instead read "703," and "USB connector" should instead read "USB controller."

August 5, 2002, and was published on November 27, 2003. Thorsten qualifies as prior art under at least pre-AIA §102(b).

96. Thorsten discloses a "data carrier"—e.g., memory card— "comprising a non-volatile memory, a data interface via which data can be written to and read from the non-volatile memory, and an interface module which is connected between the data interface and the memory and by way of which the data can be encrypted and/or decrypted." Thorsten, ¶1. As shown in annotated Figure 1 below, "the interface module comprises a logic component" (light green) "that is responsible for the encryption and/or decryption process." Thorsten, ¶8.



Thorsten, Fig. 1 (annotated).

97. Specifically, "[d]ata to be transmitted from the data interface 3 to the memory 2 is encrypted in the logic component 6. When reading data from the memory card, data is transmitted from the memory 2 to the data interface 3, with decryption being performed by the logic component 6." Thorsten, ¶15. Thorsten explains that the logic component may be provided "by means of a function-programmable logic circuit." Thorsten, ¶10. Figure 1 shows that "the data path for encryption and decryption runs exclusively via the logic component 6, but not via the controller 5," Thorsten, ¶15, but Thorsten also states that "[i]n an advantageous implementation, the logic component 6 is designed as an additional module of a chip card controller 5. This enables a compact and cost-effective implementation." Thorsten, ¶17.

98. Thorsten acknowledges that "[i]f the data is sensitive, the data is usually stored in encrypted form," Thorsten, ¶2, but also teaches that "it is advantageous if the card itself"—rather than the host device—"handles the encryption and decryption, since in this case it is not necessary to know in advance which applications the memory card is to work with, and it is not necessary to ensure that these applications have the appropriate algorithms." Thorsten, ¶4.

C. Lin (Ex-1007)

99. Lin (U.S. Patent Application Pub. No. US 2006/0053241) was filed on July 27, 2005, and was published on March 9, 2006. Lin qualifies as prior art under at least pre-AIA §102(b).

100. Lin discloses "a removable memory card standard and method thereof." Lin, ¶2. Lin's memory card—referred to as "electronic device 30"—"is able to support modes of operations compatible with" different standard applications. Lin, ¶29. As illustrated in Fig. 1A, "electronic device 30 includes an interface (IF) mode detector 32" that "detects a mode of operation to distinguish among an MMC [(multi-media card)] mode, a USB mode, or a Mu mode when electronic device 30 is inserted into a host 40." Lin, ¶31. Device 30 also features an MMC "device controller 34, a wrapper 35, a universal serial bus (USB) physical layer (PHY) circuit 36, [and] a USB device controller 37." Lin, ¶31. Finally, the device includes an "[a]pplication module 38 [that] functions to serve as a memory storage or an input/output interface, depending on the operation mode detected." Lin, ¶31.

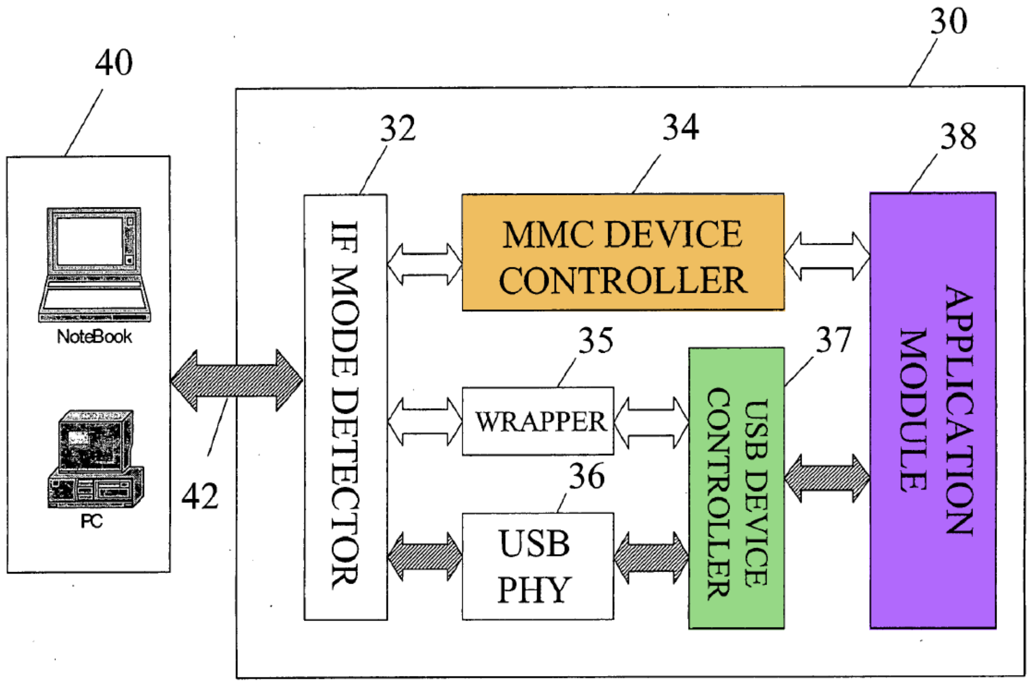


FIG. 1A

Lin, Fig. 1A (annotated).

101. "Fig. 4A is a proposed pin assignment chart" for Lin's electronic device. Lin, ¶38. For example, "[t]he fourteenth and fifteenth pins for the USB mode, *i.e.*, D+ and D-, are a pair of data signals, which may be used to determine whether the USB mode is selected." Lin, ¶38. The Fig. 4A assignment chart also features "MMC 4.0 [and] MMC SPI (serial-peripheral interface) applications," as well as "Mu-interface applications." Lin, ¶¶29, 38.

I/O Port

USB Port

Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3	VSS1	VSS1	VSS1	VSS1
4	VDD	VDD	VDD	VDD
5	CLK	SCLK		CLK
6	VSS2	VSS2	VSS1	VSS2
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

second set of pins

first set of pins

FIG. 4A

Lin, Fig. 4A (annotated).

102. Lin's electronic device, as further depicted in the Fig. 5, features "a notch 102 on the upper left-hand corner to prevent incorrect insertion of electronic device 100," and "a plurality of interweaving contact pads labeled 1 to 20, which correspond to the pins illustrated in Fig. 4A." Lin, ¶¶106-107.

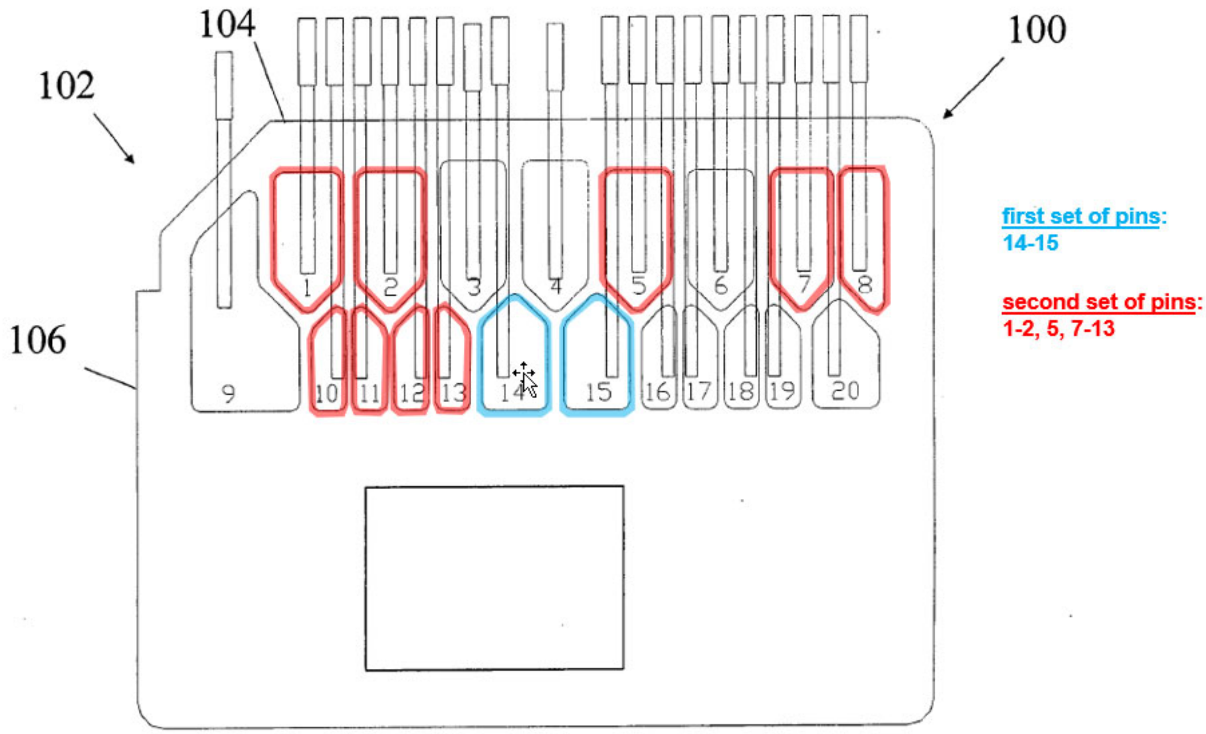


FIG. 5

Lin, Fig. 5 (annotated).

XII. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS

103. The ’051 Patent contains 27 claims. This Petition challenges independent Claims 1, 9, and 16 (directed to “a portable handheld memory card” or method of using the same), as well as dependent Claims 2, 4-8, 17, 20-21, and 23-27. In my opinion, the subject matter of the challenged claims is disclosed by the prior art as shown below.

A. Ground 1: Claims 1, 4-8, 16, 20-21, and 23-27 Are Obvious Over Diggs

104. As shown below, in my opinion, the subject matter of Claims 1, 4-8, 16, 20-21, and 23-27 are taught by Diggs alone.

1. Claim 1

a. Element 1[preamble]: A portable handheld memory card comprising:

105. In my opinion, if the preamble of Claim 1 is limiting, Diggs discloses it. Diggs discloses a "a solid state storage subsystem, such as a ***memory card***" (below, teal). *See, e.g.*, Diggs, code (57); *see also id.*, ¶60; Figs. 2, 7 ("storage subsystem 100").

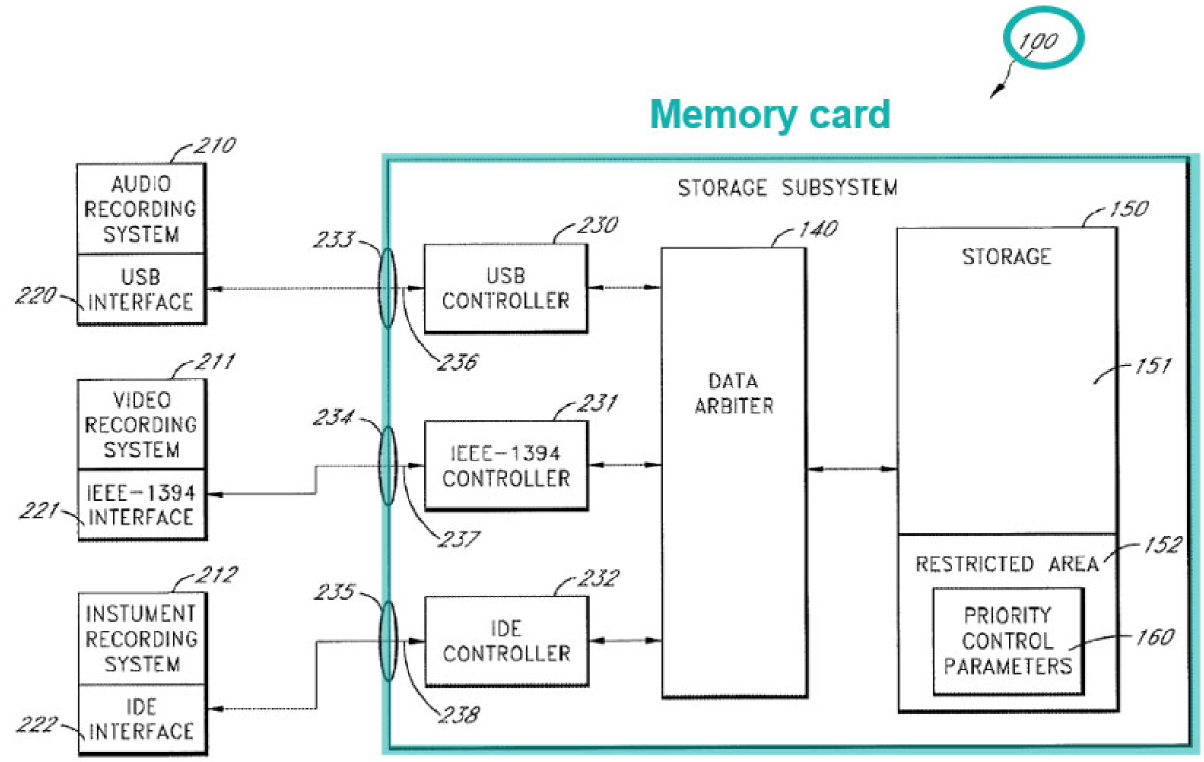


FIG. 2

Diggs, Fig. 2 (annotated).

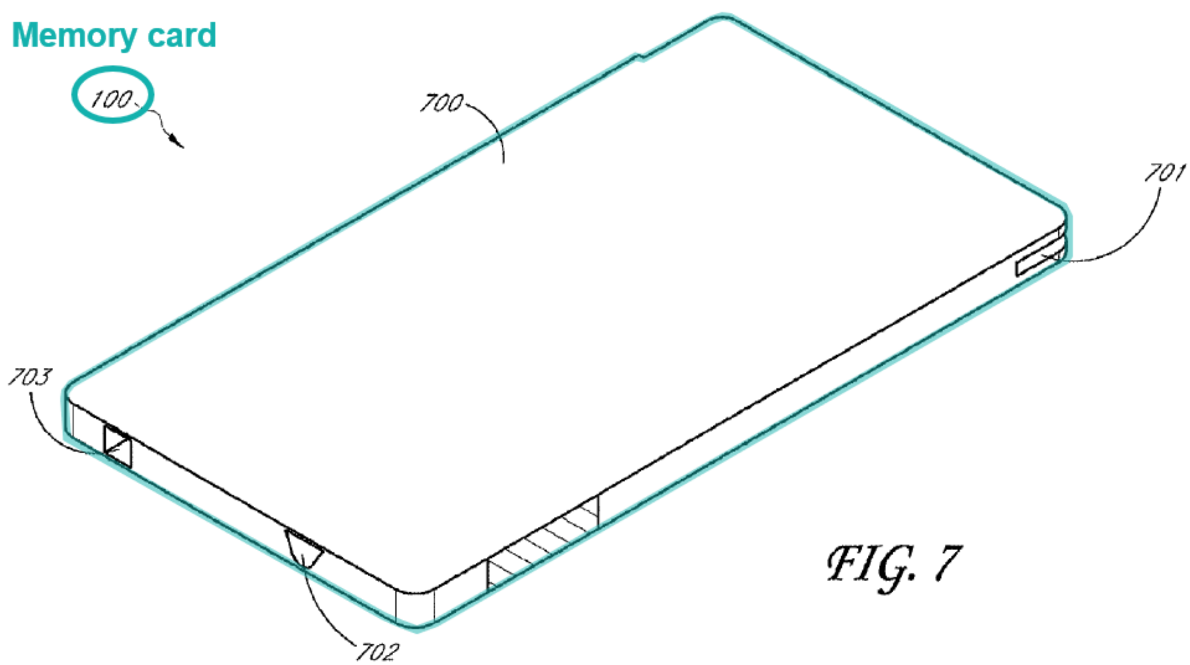


FIG. 7

Diggs, Fig. 7 (annotated).

106. Diggs further characterizes "[s]torage subsystem 100" as a "***portable*** memory device having a card type form factor," Diggs, ¶49, and explains that it is "a ***detachable*** device" that may be "***inserted*** into a PC Card slot on a host system," Diggs, ¶¶10, 55. A POSITA would have understood that a user that "inserts" or "detaches" the card does so with his hands, such that the memory card is "handheld" while the user is holding it before or after such actions. Furthermore, as I explain for Element 1[f] below, Diggs' memory card further includes a housing 700, which a POSITA would have recognized as protecting internal components from dust, moisture, or impact, thereby further confirming the "handheld" nature of the memory card.

b. Element 1[a]: a Universal Serial Bus (USB) port comprising a first set of pins;

107. In my opinion, Diggs discloses Element 1[a]. Diggs's solid-state storage subsystem "includes multiple physical connectors and bus structures for different interfaces." Diggs, ¶10. In Figure 2, an external host "audio recording system 210 is connected to USB controller 230… Accordingly, **physical connector 233** may be a USB mini-A connector" and **"[b]us structure[] 236"** corresponds to a USB bus structure. Diggs, ¶40. The USB mini-A connector 233, alone or in combination with the USB bus structure 236, collectively form a "**Universal Serial Bus (USB) port**," as I have annotated in Figure 2 below (blue).

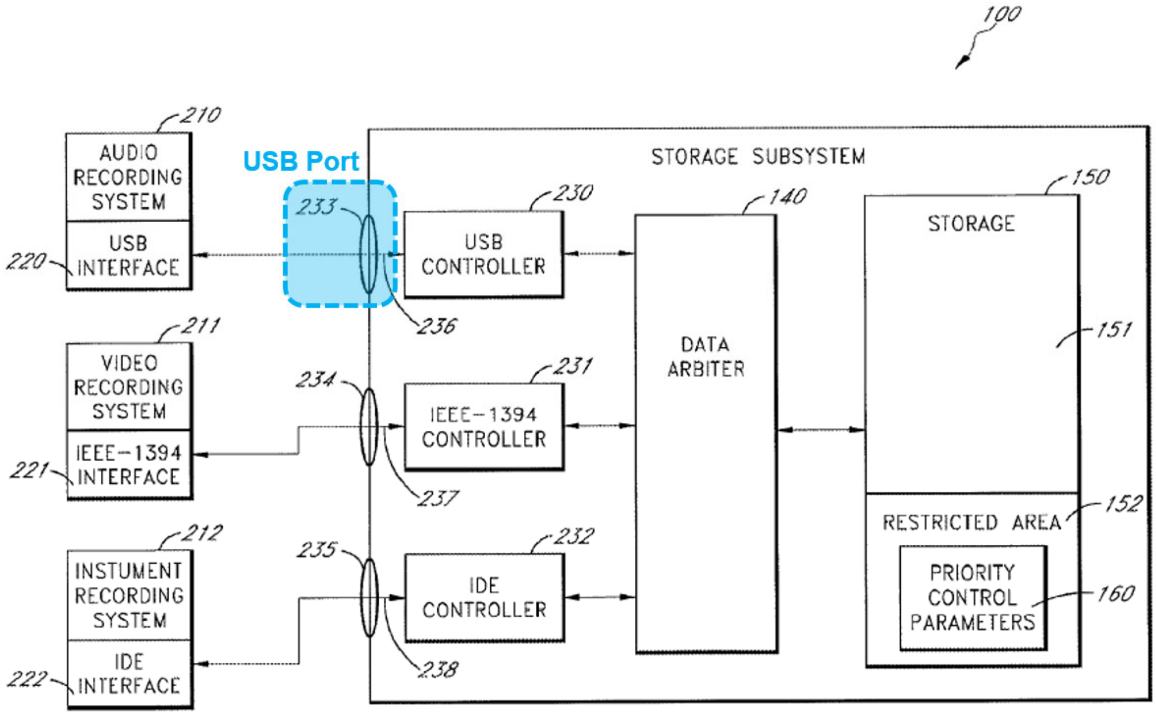
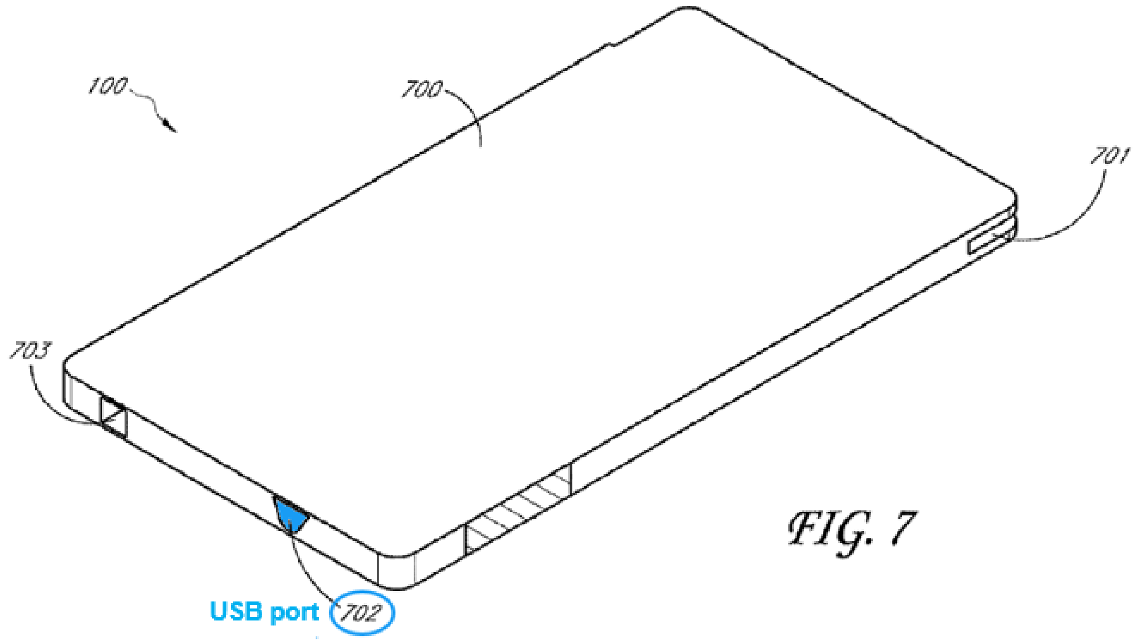


FIG. 2

Diggs, Fig. 2 (annotated).

108. Diggs's Figure 7 also shows the USB port (blue). Diggs explains that "[p]hysical connector 702 comprises a USB mini-A connector and is connected to a USB con[troller] over a USB bus structure."



Diggs, Fig. 7 (annotated).

109. Further, while Diggs does not explicitly identify the electrical pins associated with its physical connectors (*i.e.*, ports), it was well-understood to POSITAs that the USB mini-A standard is implemented with a set of five pins as detailed in the June, 2003 "On-The-Go" Supplement to the USB 2.0 Specification (Ex-1025, "USB mini-A Specification"),[2] where the following "Pin Assignment" table shows "[t]he usage and wiring assignments of the five pins in the Mini-A plug." Ex-1025 at 10.

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[2] Retrieved from https://web.archive.org/web/20060114004406/http://www.usb.org/developers/onthego/OTG1_0a%28PDFs%29.zip (captured on Jan 14, 2006) on March 24, 2025.

Table 4-2. Mini-A Plug Pin Assignments

Contact Number	Signal Name	Typical Wiring Assignment
1	VBUS	Red
2	D-	White
3	D+	Green
4	ID	< 10 Ω to GND
5	GND	Black
Shell	Shield	Drain Wire

Ex-1025 at 10.

110. As reflected above, the USB mini-A includes data pins D- and D+ for pins 2 and 3, respectively. Ex-1025 at 10. Thus, Diggs's USB port comprises a corresponding "first set of pins" (for example, data pins 2 and 3).[3]

c. Element 1[b]: USB controller circuitry electrically connected with the first set of pins of the USB port; and

111. In my opinion, Diggs discloses Element 1[b]. As discussed for Element 1[a], Diggs's memory card includes a "USB controller 230," as shown in Figure 2 below (green). Diggs, ¶40, Fig. 2.

---

[3] The three remaining power pins—*i.e.*, pin 1 (connected to VBUS) and pins 4 and 5 (connected to GND)—are not required to satisfy the claim's recitation of a "first set of pins," but they are each additional pins that comprise a "set of pins" under the applicable USB specifications.

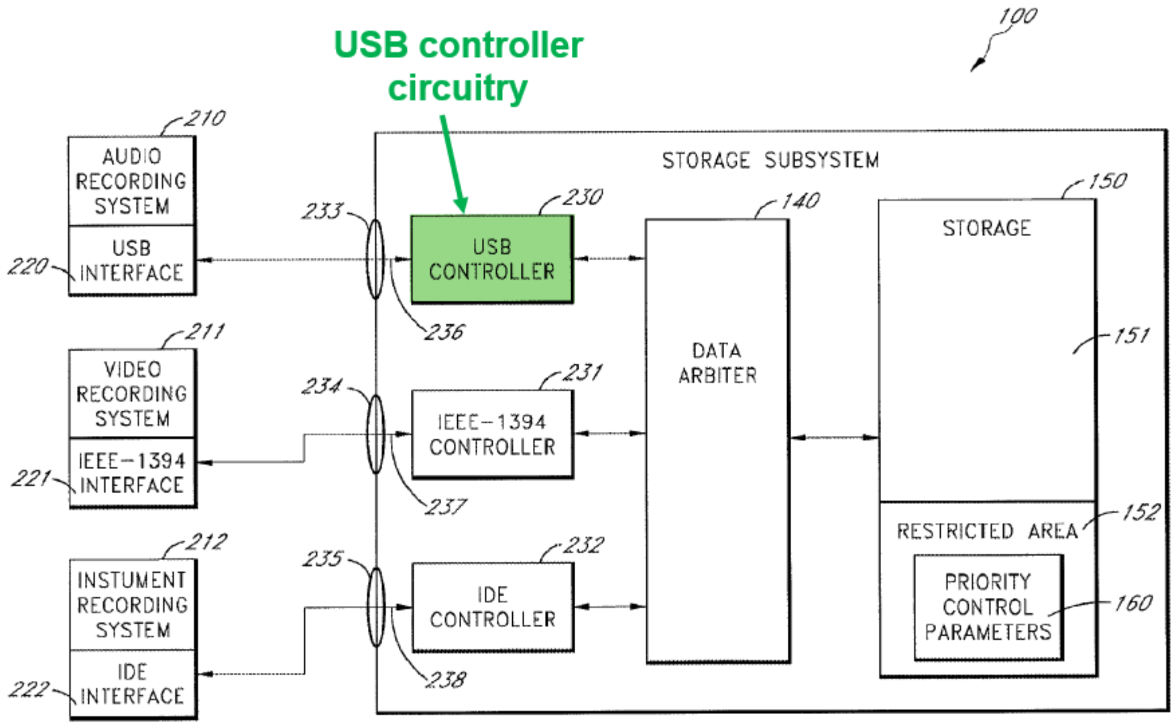


FIG. 2

Diggs, Fig. 2 (annotated).

112. Diggs explains that USB controller 230 "may receive storage access commands from a host system and translate these signals to access storage 150." Diggs, ¶40; *see also id.*, ¶29. In Figure 2, the host "audio recording system 210 is ***connected to*** USB controller 230," in order to facilitate these commands, which are received over the USB mini-A connector 233. Diggs, ¶40. Accordingly, the USB controller 230 circuitry is "electrically connected with the first set of pins of the USB port."

d. Element 1[c]: an input/output (I/O) port comprising a second set of pins; and

113. In my opinion, Diggs discloses Element 1[c]. In addition to its USB physical connector and corresponding USB bus structure, Diggs's storage subsystem includes **"physical connector 234** [that] may be a four-pin Firewire connector," **and corresponding bus structure 237** which is "IEEE-1394" compliant. Diggs, ¶40; *see also id.*, ¶4 (explaining that "the IEEE-1394 signal interface is commonly used for video applications because of the high data rates involved"). The physical connector 234, alone or in combination with the IEEE-1394 bus structure 237, collectively form **"an input/output (I/O) port**," as I have annotated in Figure 2 below (red).

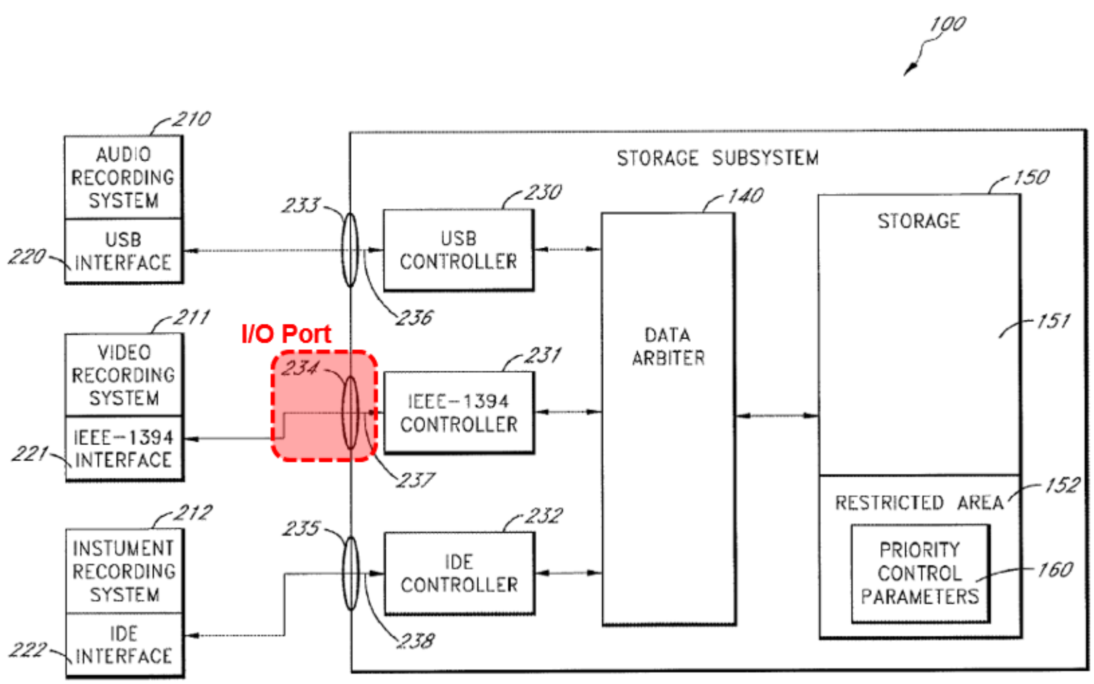
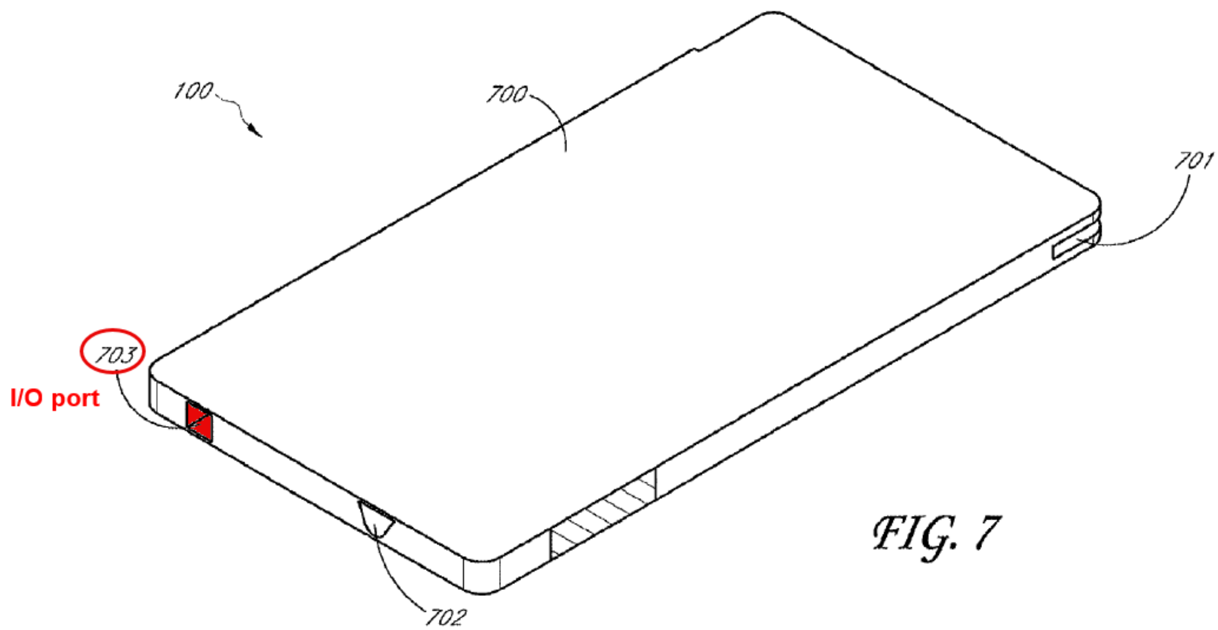


FIG. 2

Diggs, Fig. 2 (annotated).

114. Diggs's Figure 7 also shows the I/O port (red). Diggs explains that "[p]hysical connector 7[0]3 comprises an IEEE-1394 four-pin connector, and is connected to an IEEE-1394 controller using [an] IEEE-1394 bus structure." Diggs, ¶55.



Diggs, Fig. 7 (annotated).

115. The ***four pins*** associated with Diggs's IEEE-1394 physical connector 233 constitute the claimed "second set of pins" of the I/O port.[4] Diggs, ¶¶40, 55. Further, a POSITA would have understood that Diggs's second set of pins would

[4] It was well-understood by POSITAs that the "four-pin Firewire connector" associated with the IEEE-1394 carries only data, not power. Ex-1029 (IEEE-1394 four-pin Specification) at 27.

have the signal assignment shown in the following table, from the March 30, 2000 IEEE-1394 four-pin Specification (Ex-1029).

Table 4-11A — Connector socket signal assignment

Contact number	Signal name	Comment
1	TPB*	Strobe on receive, data on transmit (differential pair)
2	TPB	
3	TPA*	Data on receive, strobe on transmit (differential pair)
4	TPA	
Shell	VG	Necessary for ground reference

Ex-1029 at 35.

e. Element 1[d]: I/O controller circuitry electrically connected with the second set of pins of the I/O port;

116. In my opinion, Diggs discloses Element 1[d]. As discussed for Element 1[a], Diggs's memory card includes an "IEEE-1394 controller 231," as I have shown in Figure 2 below (orange). Diggs, ¶40, Fig. 2.

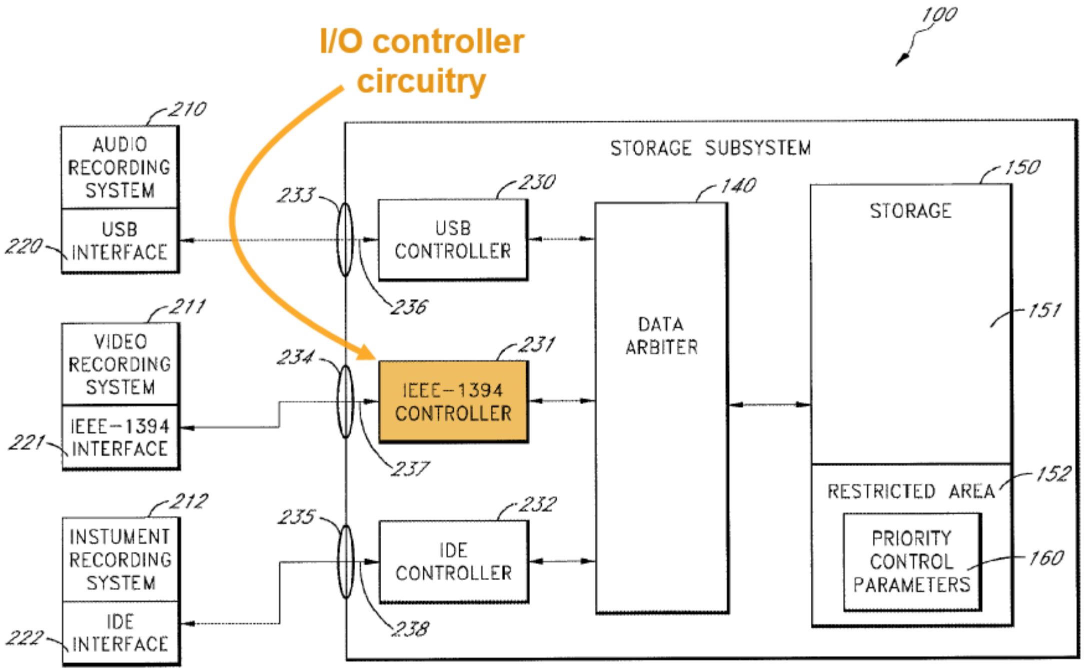


FIG. 2

Diggs, Fig. 2 (annotated).

117. As with USB controller 230, the IEEE-1394 controller 231 "may receive storage access commands from a host system and translate these signals to access storage 150." Diggs, ¶40; *see also id.*, ¶29. In Figure 2, the host "video recording system 211 is ***connected to*** IEEE-1394 controller 231," in order to facilitate these commands, which are received over the IEEE-1394 four-pin Firewire connector 234. Diggs, ¶40. Accordingly, the IEEE-1394 controller 231 circuitry is "electrically connected with the second set of pins of the I/O port."

f. Element 1[e]: a memory in communication with the USB port and the I/O port; and

118. In my opinion, Diggs discloses Element 1[e]. Diggs discloses that "[t]he storage subsystem 100 comprises a storage 150" that in turn "may comprise a plurality of solid-state storage devices." Diggs, ¶30. Storage 150 is separated into "a restricted memory area 152 [that] stores priority control parameters 160" and a "user data memory area 151 that is generally accessible by the operating systems of [the] host systems." Diggs, ¶¶34, 38; *see also id.*, ¶26 ("The host systems ... execute driver programs ... that provide functionality for communicating with the subsystem 100."). Further, the storage subsystem of Figure 2 is "simultaneously connected across multiple host systems"—*i.e.*, "audio recording system 210" and "video recording system 211—via the "USB port" and "I/O port" identified for Elements 1[a] and 1[c] above. Thus, Diggs's storage 150—or, specifically, the user data memory area 151—is "a memory in communication with the USB port and I/O port."

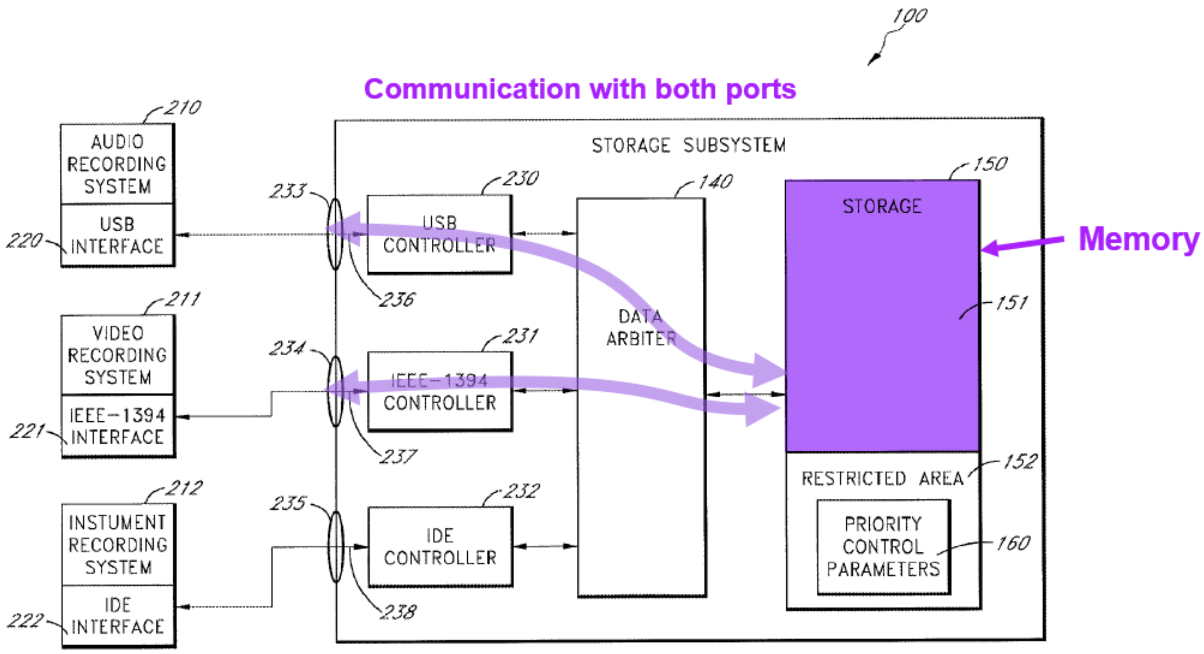
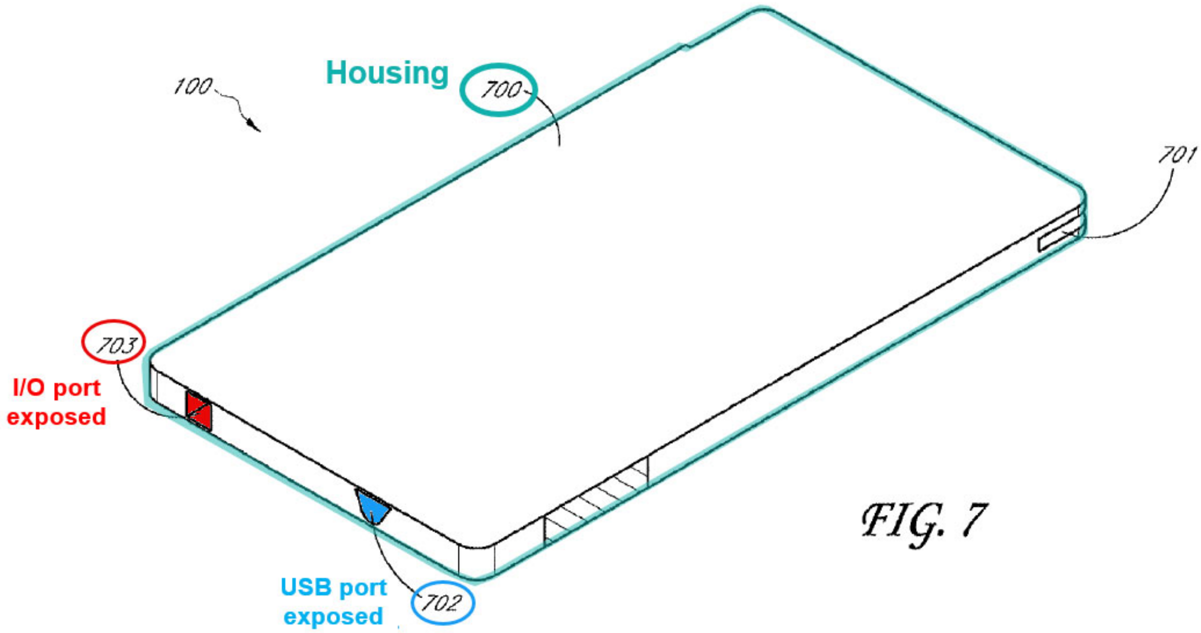


FIG. 2

Diggs, Fig. 2 (annotated).

g. Element 1[f]: a housing storing the memory and exposing the USB port and the I/O port;

119. In my opinion, Diggs discloses Element 1[f]. In Figure 7, for example, "[s]torage subsystem 100 is shown with a PC Card ***housing*** 700," which would house the storage 150. Diggs, ¶55, cl. 1.



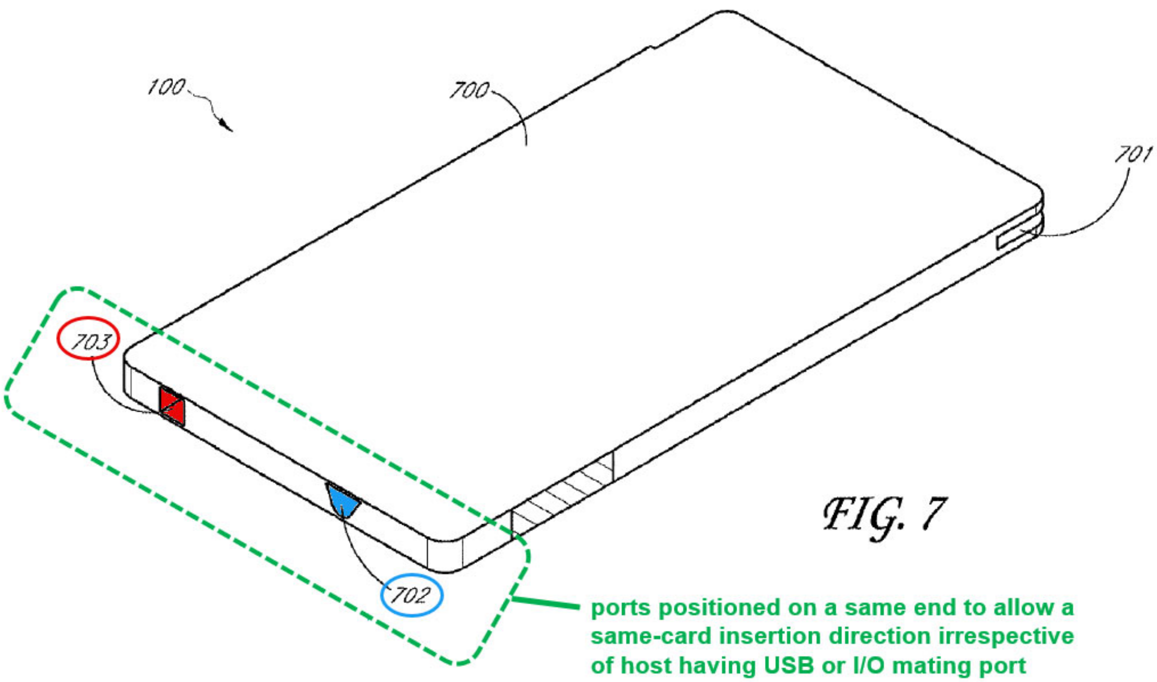
Diggs, Fig. 7 (annotated).

120. Figure 7 features a "[p]hysical connector 702" (*i.e.*, "a USB mini-A connector") and a "[p]hysical connector 7[0]3" (*i.e.*, "an IEEE-1394 four-pin connector"). Diggs, ¶55. As shown in Figure 7, "[p]hysical connector 702 and 703 are further ***accessible to be connected*** to USB and IEEE-1394 cable connections from additional host systems"—in other words, those USB and I/O ports are ***exposed*** by the housing 700.

h. Element 1[g]: wherein the USB port and the I/O port are positioned on a same end to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port; and

121. In my opinion, Diggs discloses Element 1[g]. In Diggs's memory card (*i.e.*, storage subsystem 100), the USB port and I/O port (702 and 703,

respectively) are positioned on the "same end"—specifically, the near, left end of the card in the perspective view of Figure 7. Diggs, ¶55, Fig. 7.



Diggs, Fig. 7 (annotated).

122. Further, this positioning "allow[s] a same-card insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port," because, as Diggs explains, the "[p]hysical connector[s] 702 and 703 are [] accessible to be connected" in that direction—*i.e.*, the near, left end-direction of the card—"to USB and IEEE-1394 cable connections from additional host systems." Diggs, ¶55.

i. Element 1[h]: wherein the USB port and the I/O port are positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and

123. In my opinion, Diggs discloses Element 1[h]. As shown and described for Figures 2 and 7, Diggs's USB port 702 and I/O port 703 are separate "physical connector" receptables. Diggs, Figs. 2, 7, ¶¶40, 55. Accordingly, their corresponding "first" and "second" sets of pins (identified for Elements 1[a] and 1[c] above, respectively) are likewise physically separate. Thus the positioning of these ports are such that "when the I/O port is electrically connected with the host device"—for example, with the video recording system 211, using an IEEE-1394 cable connection (Diggs, ¶¶39, 55)—"at least one of the first set of pins of the USB port is *not electrically connected* to the host device" because, in that circumstance, none of the USB mini-A pins (*see* Element 1[a], *supra*) are electrically connected with that IEEE-1394-compatible video recording system 211. Indeed, since the "host device" to which the I/O port is connected (video recording system 211) only has an IEEE-1394 interface, and no USB interface, it is not designed to connect to the USB port. *See* Diggs, ¶39 ("Each [host] system may utilize a **different** signal interface to communicate with storage subsystem 100.").

j. Element 1[i]: when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device.

124. In my opinion, Diggs discloses Element 1[i]. As discussed for Element 1[h] above, Diggs's USB port 702 and I/O port 703 are separate "physical connector" receptables. Diggs, Figs. 2, 7, ¶¶40, 55. Accordingly, their corresponding "first" and "second" sets of pins (identified for Elements 1[a] and 1[c] above, respectively) are likewise physically separate. Thus the positioning of these ports are such that "when the USB port is electrically connected with the host device"—for example, with the audio recording system 210, using a USB cable connection (Diggs, ¶¶39, 55)—"at least one of the second set of pins of the I/O port is *not electrically connected* to the host device" because, in that circumstance, none of the four IEEE-1394 Firewire connector pins (*see supra* Element 1[c]) are electrically connected with that USB-compatible audio recording system 210. Indeed, since the "host device" to which the USB port is connected (audio recording system 211) only has a USB interface, and no IEEE-1394 interface, it is not designed to connect to the I/O port. *See* Diggs, ¶39 ("Each [host] system may utilize a **different** signal interface to communicate with storage subsystem 100.").

2. Claim 4: The portable handheld memory card of claim 1 further comprising: a power management unit in communication with the USB controller circuitry.

125. In my opinion, Diggs teaches the further requirement of "a power management unit in communication with the USB controller circuitry." For example, Diggs acknowledges "power consumption" as a design constraint for solid-state storage subsystems generally. Diggs, ¶4. Further, Diggs discloses that in its subsystem, "[e]ach controller ... may be configured to write data to, and read data from, the storage 150 in response to memory/storage access commands from hosts," which entails "translat[ing] control, address, and data signals into storage access commands to storage 150. Controllers ... may also access and transmit data from storage 150 to host systems." Diggs, ¶29. Based on these teachings, a POSITA would have understood that Diggs's controllers—including USB controller 230—are in communication with power management circuitry, to facilitate such capabilities. Further, the USB mini-A Specification (Ex-1025) confirms that Diggs's USB mini-A port (*i.e.*, physical connector 230 (Fig. 2) or 702 (Fig. 7)) includes a "VBUS" pin that is connected to power management circuitry on the memory card, as required for USB mini-A compliance. Specifically, a POSITA would have understood that power management circuitry would have been connected to the USB controller circuitry of Diggs' card, in order

to facilitate required changes in voltage on the "VBUS" pin to communicate with the host device. *See* Ex-1025, 41-44 ("A-device electrical requirements").

126. Moreover, as I have shown in the below modification of Diggs's Figure 2, a POSITA would have been motivated to implement, in Diggs's memory card, a power management unit in communication with each of the controllers (including USB controller 230) to ensure that, when Diggs's device is connected to respective host devices like those shown in Figure 2, its power source voltage requirements are adjusted to comply with each of the applicable standards to ensure that the standard's requirements are met. As shown below, a POSITA would have recognized that it would have been sufficient to implement a single power management circuit that connects to each of the 3 controllers, which is an efficient design that minimizes redundant circuitry.

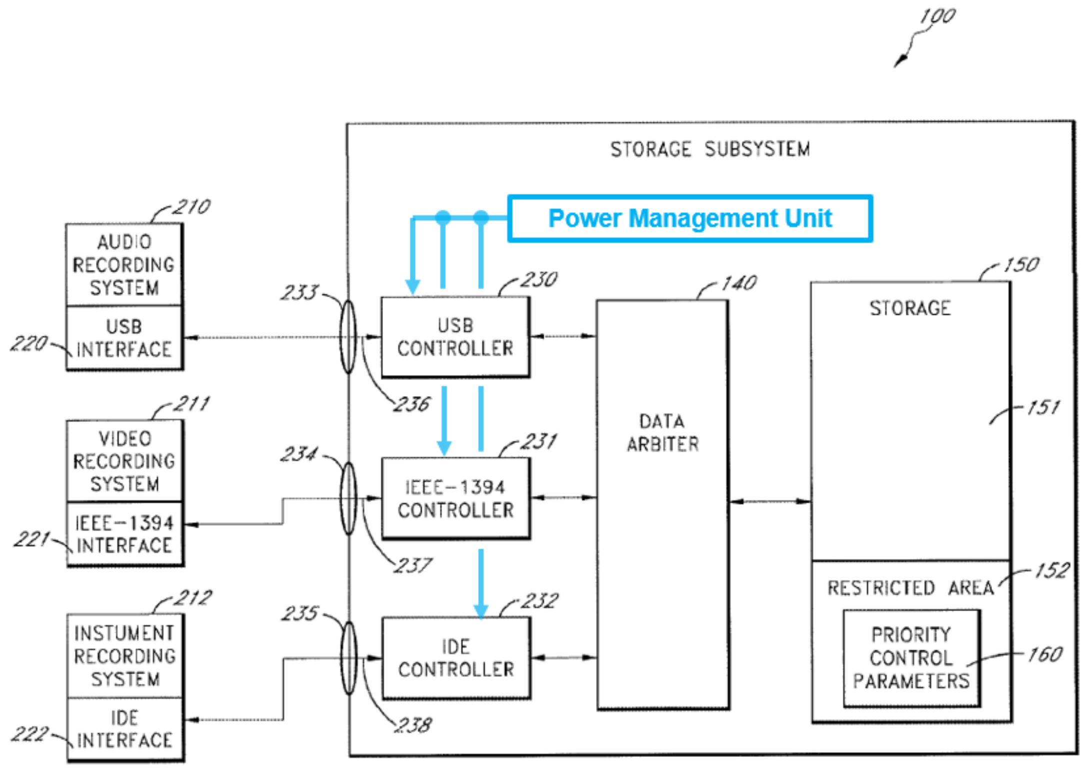


FIG. 2

Modification of Diggs Fig. 2 (showing power management unit).

3. Claim 5: The portable handheld memory card of claim 1 further comprising: a host interface module in communication with the I/O port.

127. In my opinion, Diggs discloses the added requirement of "a host interface module in communication with the I/O port." The '051 Patent specification discloses a "host interface circuit 114" that "may translate data" in order to be transferred via a given port. '051 Patent, 4:4-7.

128. As I have indicated in orange in Figure 2 below, Diggs's "IEEE-1394 controller 231" corresponds to the "host interface module" as understood from the intrinsic record.[5]

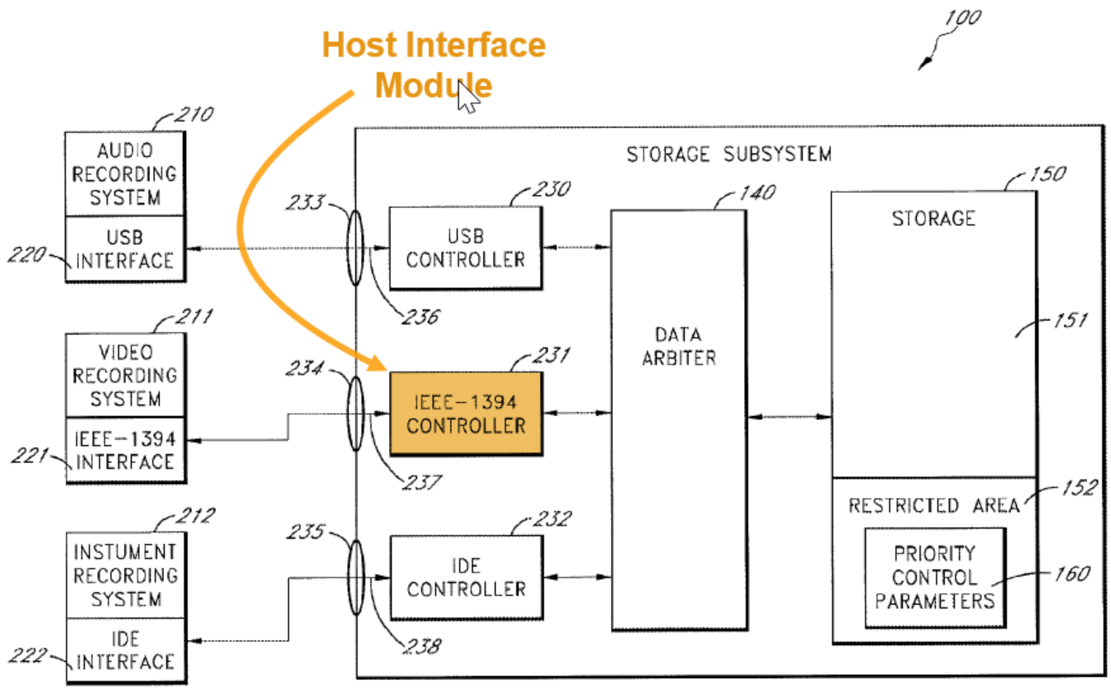


FIG. 2

Diggs, Fig. 2 (annotated).

129. Diggs discloses that "[e]ach controller may receive storage access commands from a host system and ***translate these*** signals to access storage 150," Diggs, ¶40, and further discloses that the host "video recording system 211 is

[5] I note that, during prosecution, the Applicant did not dispute Examiner's mapping of the "MMC interface controller" of the prior art Kim reference to the claimed "host interface module," despite also mapping that feature to the "I/O controller circuitry." *See* Ex-1004 at 72 (February 14, 2012 Office Action at 4).

connected to"—*i.e.*, ***interfaces*** with—"IEEE-1394 controller 231." *Id*. Accordingly, IEEE-1394 controller 231 is a host interface module.

130. Diggs further teaches that IEEE-1394 controller 231 communicates with the "I/O port"—*i.e.*, "physical connector 234 [that] may be a four-pin Firewire connector." Diggs, ¶40.

4. Claim 6: The portable handheld memory card of claim 1 further comprising: circuitry configured to control read and write operations to the memory.

131. In my opinion, Diggs discloses Claim 6. For example, Diggs states that in its subsystem, "[e]ach controller ... may be configured to write data to, and read data from, the storage 150 in response to memory/storage access commands from hosts," which entails "translat[ing] control, address, and data signals into storage access commands to storage 150. Controllers ... may also access and transmit data from storage 150 to host systems." Diggs, ¶29. Diggs further teaches that its "[d]ata arbiter 140 is responsible for prioritizing read/write commands received simultaneously from multiple controllers," and may do so "according to a priority ranking." Diggs, ¶33; *see also id.*, ¶40. Thus, as I have indicated in yellow in Figure 2 below, any or all of Diggs's controllers 230, 231, and 222, and "data arbiter 140," qualify as "circuitry configured to control read and write operations to the memory."

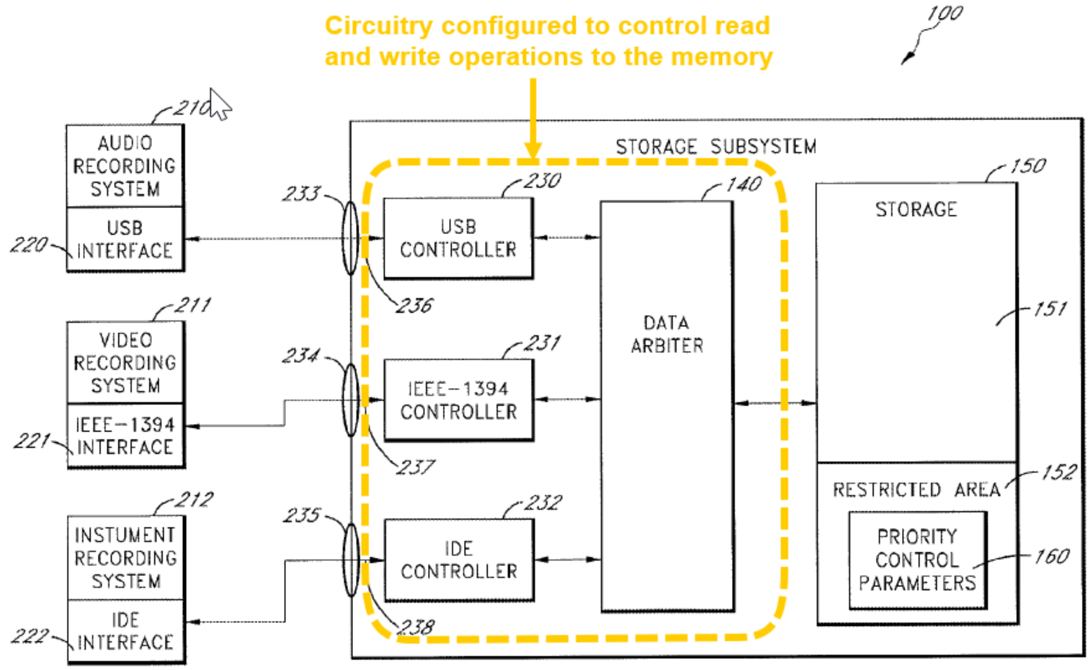


FIG. 2

Diggs, Fig. 2 (annotated).

5. Claim 7: The portable handheld memory card of claim 1, wherein the I/O port comprises a Secure Digital port.

132. In my opinion, Diggs teaches Claim 7. As discussed for Element 1[c] above, Diggs's Figure 2 memory card ("storage subsystem 100") includes an "input/output (I/O) port" in the form of a "physical connector 234 [that] may be a four-pin Firewire connector" and corresponding bus structure 237 which is "IEEE-1394" compliant. Diggs, ¶¶40, 4; *see also* Element 1[c], *supra*. Diggs further discloses that alternatively, "the storage subsystem 100 may, for example, be a solid-state memory card that connects to" a host according to the "SecureDigital" specification. Diggs, ¶60. Pursuant to this teaching, a POSITA would have

understood that an alternative embodiment would have been the below modification of Diggs's Figure 2, which shows an "SD Device Controller" in place of IEEE-1394 controller 231.

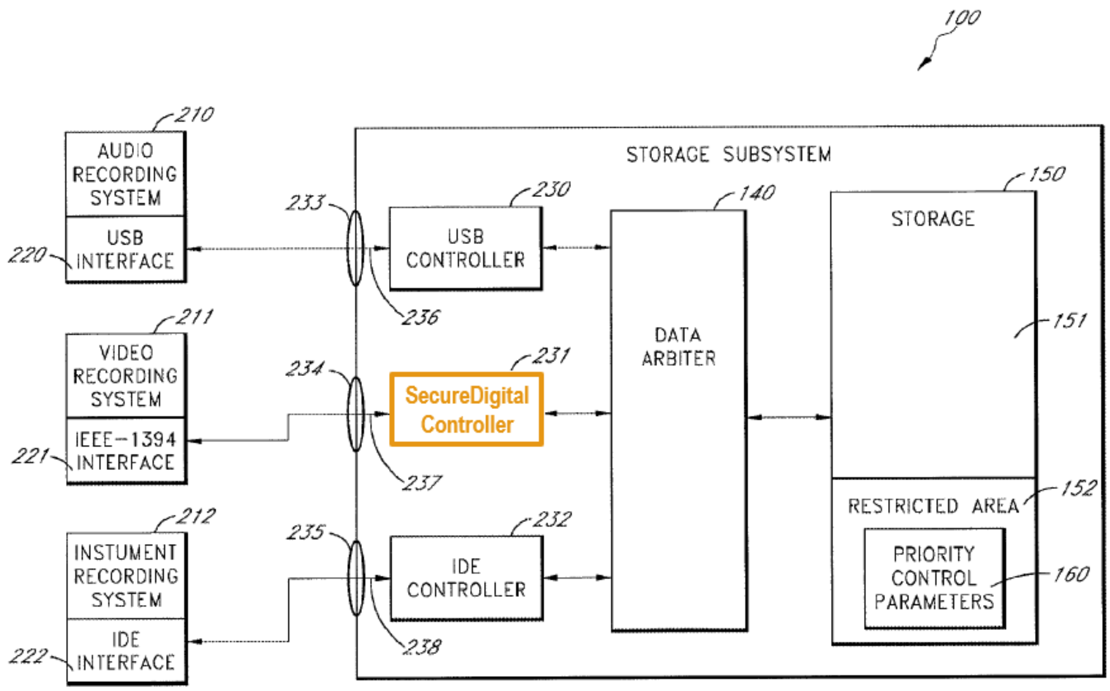


FIG. 2

Modification of Diggs Fig. 2 (including a "SecureDigital Controller" instead of an IEEE-1394 controller).

133. A POSITA would have understood that, in the above implementation of Diggs's memory card, physical connector 234 and corresponding bus structure 237 would be Secure-Digital compliant, and would therefore collectively form an "SD port." Further, as shown in Figure 7, the separate "[p]hysical connector[s] 702 and 703" would now correspond to an USB port and SD port, respectively, and the

positioning of these ports is such that, when the "set of pins" for one port is electrically connected to a host device, the other "set of pins" for the other port is not electrically connected to that host device.

6. Claim 8: The portable handheld memory card of claim 1, wherein the memory comprises Flash memory.

134. In my opinion, Diggs teaches the added requirement of Claim 8. Diggs discloses that "[s]torage 150 may comprise a plurality of solid-state storage devices," and that such "device[s] may comprise, for example, flash integrated circuits." Diggs, ¶30.

7. Claim 16:

a. Element 16[Preamble]: A method comprising:

b. Element 16[a]: with a portable handheld card comprising a Universal Serial Bus (USB) port comprising a first set of pins; USB controller circuitry electrically connected with the first set of pins of the USB port; an input/output (I/O) port comprising a second set of pins; I/O controller circuitry electrically connected with the second set of pins of the I/O port; a memory in communication with the USB port and the I/O port; and a housing storing the memory and exposing the USB port and the I/O port, wherein the USB port and the I/O port are positioned to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port and wherein the USB port and the I/O port are positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and when the USB port is electrically connected to the host device,

at least one of the second set of pins of the I/O port is not electrically connected to the host device:

135. In my opinion, Diggs teaches Elements 16[Preamble]-[a] for the reasons it teaches Claim 1. *See supra* Section XII.A.1 (Claim 1); Ex-1020 (Claim Mapping Table).

c. Element 16[b]: reading data from the memory;

136. In my opinion, Diggs teaches Element 16[b]. As discussed for Claim 6 above, Diggs discloses "circuitry configured to control read and write operations to the memory," which entails "reading data from the memory." *See* Claim 6, *supra*.

d. Element 16[c]: determining whether the data is to be transmitted via the USB port or I/O port; and

137. In my opinion, Diggs discloses Element 16[c]. Specifically, Diggs explains that "[e]ach controller ... may be configured to write data to, and read data from, the storage 150 in response to memory/storage access commands from hosts," which entails "translat[ing] control, address, and data signals into storage access commands to storage 150. Controllers ... may also access and transmit data from storage 150 to host systems." Diggs, ¶29. Diggs further teaches that "[d]ata arbiter 140 is responsible for prioritizing read/write commands received simultaneously from multiple controllers," and may do so "according to a priority ranking." Diggs, ¶33; *see also id.*, 40. "For instance, the data arbiter 140 may

determine that the priority control parameters 160 designate that commands received from the first host system []are of highest priority, and are therefore processed before commands received from the second host system." Diggs, ¶34. Based on these descriptions, and as reflected in Figure 2, a POSITA would have understood that during a "read" operation, the data arbiter 140 would determine whether the data accessed from the memory 150 "is to be transmitted via the USB port" (*i.e.*, through USB controller 230 and bus structure 236) "or I/O port" (*i.e.*, through IEEE-1394 controller 231 and bus structure 237).

e. Element 16[d]: transmitting the data to the host device via the determined port.

138. In my opinion, Diggs teaches Element 16[d]. *See* Claim 6 and Element 16[c], *supra*. During a read operation, Diggs's memory card "transmit[s] the data to the host device via the determined port."

8. Claim 20: The method of claim 16, wherein the I/O port comprises a Secure Digital port.

139. In my opinion, Diggs teaches Claim 20. *See* Claim 7, *supra*.

9. Claim 21: The method of claim 16, wherein the memory comprises Flash memory.

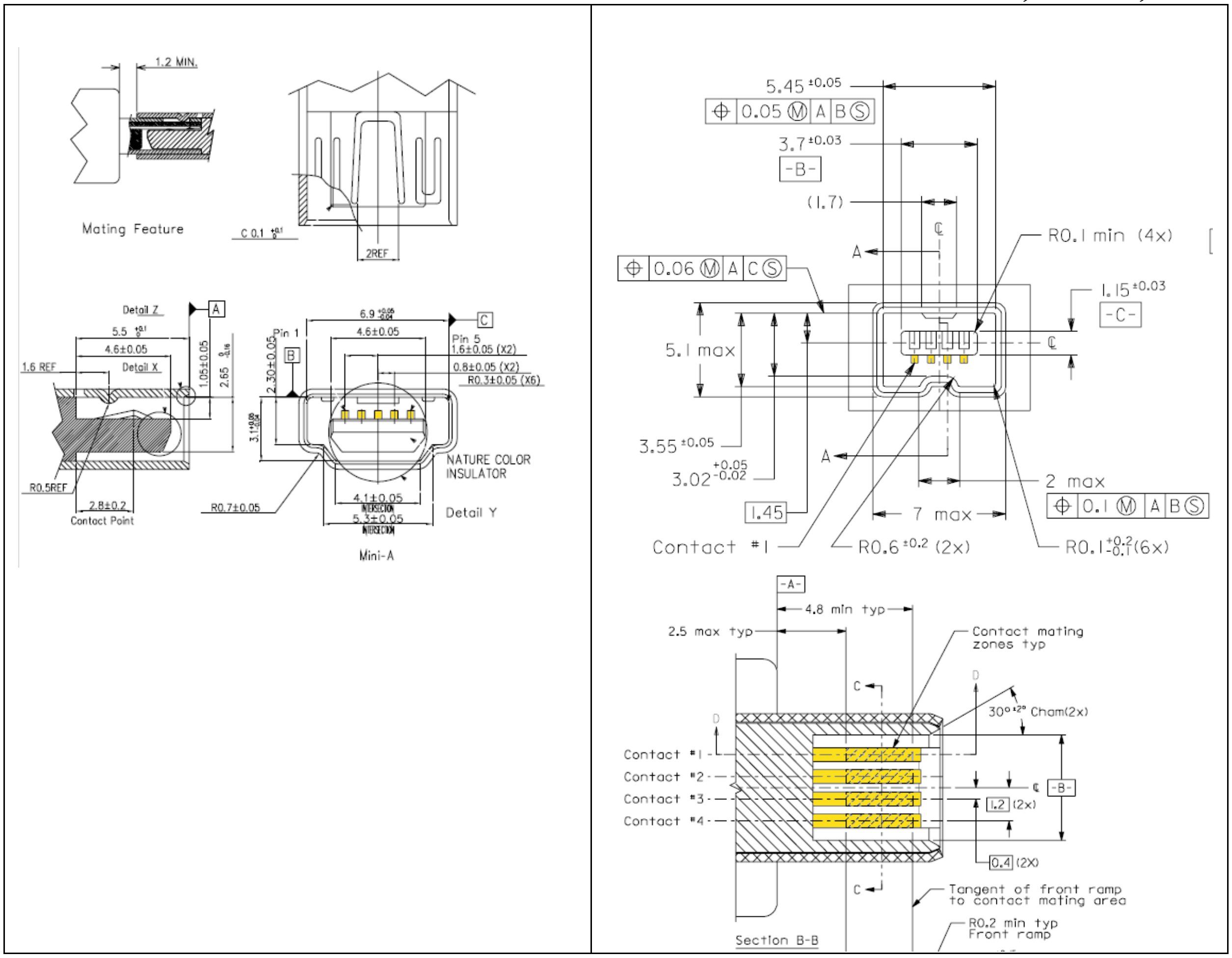
140. In my opinion, Diggs teaches Claim 21. *See* Claim 8, *supra*.

10. Claim 23: The portable handheld memory card of claim 1, wherein at least two pins of the USB port are parallel to at least two pins of the I/O port.

141. In my opinion, Diggs teaches Claim 23. As discussed for Element 1[g] above, Diggs discloses a USB port and I/O port—a USB mini-A port and IEEE-1394, respectively—which are positioned and oriented on the same end of the memory card as shown in Figure 7 (*i.e.*, as separate physical connectors 702 and 703, respectively, which are both located the near, left end). *See* Element 1[g], *supra*; Diggs, ¶55, Fig. 7.

142. While not explicitly shown in Figure 7, a POSITA would have understood that the respective sets of pins associated with the USB port and I/O port—*i.e.*, the five USB mini-A pins, and the four IEEE-1394 Firewire pins—would have been implemented such that they are parallel to one another. This is supported, for example, by the respective specifications for USB mini-A and the four-pin IEEE-1394 applications, which include the receptacle interface drawings shown below. *See* Ex-1025 at 21 (USB mini-A receptacle interface drawing); Ex-1029 at 35 (IEEE-1394 four-pin connector socket interface annotated drawings).

USB mini-A	**IEEE-1394**



143. These drawings, when considered against the positioning and orientation of the physical connector receptacle ports 702 and 703 in Figure 7 below, confirm that at least two of the pins of the USB port are in parallel to at least two of the pins of the I/O port, as required.

11. Claim 24: The portable handheld memory card of claim 1, wherein layout for the USB port is different from layout of the I/O port.

144. In my opinion, Diggs discloses Claim 24. As Diggs explains, and as shown in Figure 7, the USB port and I/O port are *separate physical connectors*:

one having five pins, compliant with the USB mini-A specification; the other having four pins, compliant with the IEEE-1394 specification. Diggs, ¶¶40, 55, Fig. 7. Accordingly, the respective layouts for these two ports are different from one another.

12. Claim 25: The portable handheld memory card of claim 1, wherein the I/O port is configured for mating with an external port.

145. In my opinion, Diggs discloses Claim 25. Diggs's "I/O port" (specifically, the IEEE-1394 "four-pin Firewire" physical connector 234) is configured for mating with an external port—for example, with the corresponding IEEE-1394-compliant port located at the "IEEE-1394 interface 221" of the "video recorder system 211" as shown in Figure 2. Diggs, ¶¶27, 39-40, Fig. 2; *see also id.*, ¶55 (stating that physical connector 703—*i.e.*, the I/O port of Figure 7—is "further accessible to be connected to [an] IEEE-1394 cable connection[] from [an] additional host system[].").

13. Claim 26: The portable handheld memory card of claim 1, wherein all of the first set of pins electrically connected with the USB controller circuitry is not electrically connected to the I/O controller circuitry.

146. In my opinion, Diggs discloses Claim 26. In Diggs's memory card, all of the "first set of pins" (*i.e.*, both of the data pins D+ and D- of the USB mini-A physical connector 233, as explained for Element 1[a] above) are electrically connected with the USB controller 230. Further, both pins are "not electrically

connected to the I/O controller circuitry" (*i.e.*, IEEE-1394 controller 231); Diggs discloses that instead, the IEEE-1394 controller is connected to an entirely separate physical connector—the "four-pin Firewire connector" 234, which is compliant with the IEEE-1394 standard instead of USB mini-A. Diggs, ¶¶40, 55, Figs. 2, 7.

14. Claim 27:

a. Element 27[preamble]: The portable handheld memory card of claim 1,

b. Element 27[a]: wherein the USB port comprises multiple data lines,

147. In my opinion, Diggs discloses Elements 27[preamble]-27[a]. The below pin assignment table in the USB mini-A specification shows two data pins: D- and D+ for pins 2 and 3, respectively.

Table 4-2. Mini-A Plug Pin Assignments

Contact Number	Signal Name	Typical Wiring Assignment
1	VBUS	Red
2	D-	White
3	D+	Green
4	ID	< 10 Ω to GND
5	GND	Black
Shell	Shield	Drain Wire

Ex-1025 at 10.

148. Accordingly, in Diggs's memory card, the "USB mini-A" physical connector 233 and corresponding bus structure 236 (*i.e.*, "USB port") includes multiple data pins and corresponding data lines. Diggs, ¶40, Fig. 2.

c. Element 27[b]: wherein the first set of pins comprise multiple data pins connected to the multiple data lines; and

149. In my opinion, Diggs teaches Element 27[b]. *See* Element 27[a], above.

a. Element 27[c]: wherein all of the multiple data pins are not electrically connected to the I/O controller circuitry.

150. In my opinion, Diggs teaches Element 27[c]. *See* Claim 26 above, explaining that, in Diggs's memory card, none of the "first set of pins" of the USB port—including the "multiple data pins"—are connected to the IEEE-1394 controller 231.

B. Ground 2: Claims 2 and 17 Are Obvious Over Diggs in View of Thorsten

151. As shown below, in my opinion, the subject matter of Claims 2 and 17 are disclosed by Diggs in view of Thorsten.

1. A POSITA would have been motivated to combine Diggs with Thorsten with a reasonable expectation of success.

152. In my opinion, a POSITA would have been motivated to combine Diggs with Thorsten and would have a reasonable expectation of success in doing so, because they are both from the same field and relate to the same well-known

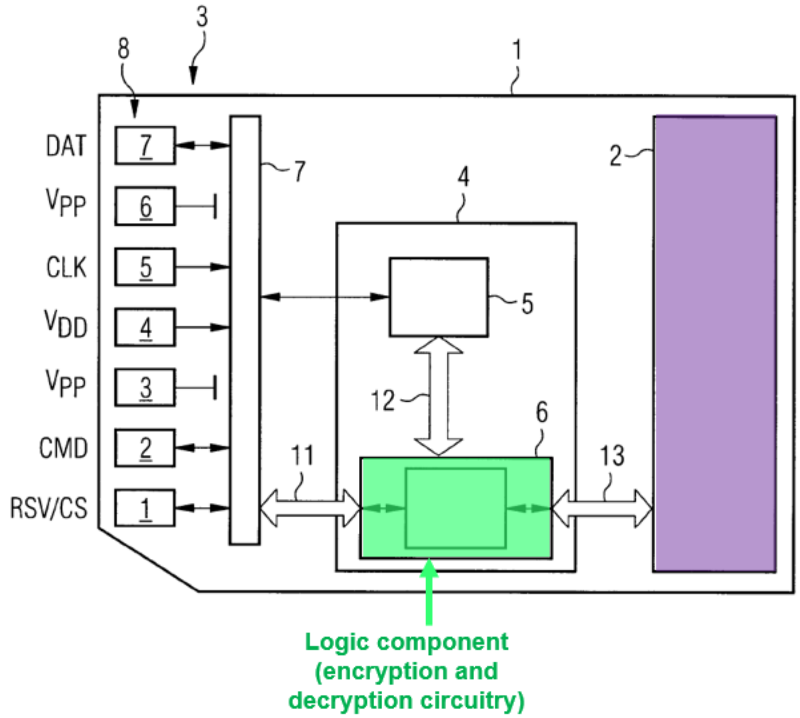
issues. Both references disclose memory cards, and external host devices that read data from, and write to, the memory. *Compare* Diggs, ¶¶29, 33 *with* Thorsten, ¶3. Like Diggs, Thorsten discloses a "memory card comprising a non-volatile memory 2," "a data interface 3 for connecting to a host," and "a controller 5." *E.g.*, Diggs, ¶¶29-30 Fig. 2; Thorsten, ¶13, Fig. 1. A POSITA seeking to store sensitive data in encrypted form, in a manner compatible with different host applications, would have looked to each of these references for teachings of how to reliably store sensitive data.

153. Diggs's memory card is capable of receiving read and write commands simultaneously from multiple connected external host devices compliant with different standards, including USB and IEEE-1394, and it includes separate corresponding physical connectors, bus structures, and controller circuits and corresponding to those multiple standards. *See* Diggs, ¶¶ 39, 40, Figs. 2, 7. Diggs is silent on the sensitivity of data to be stored in its memory card, or whether its memory card utilizes encryption or decryption. However, at the time of the '051 Patent, encryption and decryption techniques were a common feature of solid-state memory cards. *See* Section X.C above.

154. Thorsten, for example, acknowledges that sensitive data is usually stored in encrypted form, but recognizes that conventional "memory cards are designed in such a way that almost all hosts, which may belong to different

applications, … [s]o if a first application stores a data record that it has previously encrypted using a specific algorithm, the host of a second application … again must also have this algorithm, otherwise the data cannot be decrypted again." Thorsten, ¶3. To resolve this, Thorsten proposes a configuration in which "the card itself handles the encryption and decryption, [so that] it is not necessary to know in advance which applications the memory card is to work with, and it is not necessary to ensure that these applications have the appropriate algorithms." Thorsten, ¶4.

155. Thorsten's "data carrier 1" ("memory card") incorporates a "logic component 6" (light green) "that is responsible for the encryption and/or decryption process," Thorsten, ¶8, and which may be "a function-programmable logic circuit." Thorsten, ¶10.



Thorsten, Fig. 1 (annotated).

156. "Data to be transmitted from the data interface 3 to the memory 2 is encrypted in the logic component 6. When reading data from the memory card, data is transmitted from the memory 2 to the data interface 3, with decryption being performed by the logic component 6." Thorsten, ¶15. Figure 1 shows that "the data path for encryption and decryption runs exclusively via the logic component 6, but not via the controller 5" (Thorsten, ¶15), but "[i]n an advantageous implementation, the logic component 6 is designed as an additional module of a chip card controller 5. This enables a compact and cost-effective implementation." Thorsten, ¶17.

157. Accordingly, in my opinion, a POSITA would have understood and been motivated to incorporate, in Diggs' memory card, data encryption and decryption functionality that is compatible with various host applications, by implementing Thorsten's logic component (which is encryption and decryption circuitry), in order to reap Thorsten's disclosed benefits—namely, storing sensitive data while remaining compatible with various host applications. *See* Thorsten, ¶¶2-4. I understand that a motivation to combine exists when the "improvement" results in a product or process that is stronger, cheaper, faster, or more efficient.

158. Additionally, in my opinion, a POSITA would have had a reasonable expectation of success in achieving the collective objectives of Diggs and Thorsten—namely, obtaining a multiple standard-compliant memory card that can store sensitive data while remaining compatible with various host applications—by combining their teachings with no change in their respective functions, since Diggs and Thorsten disclose similar devices, and because Thorsten's encryption and decryption circuitry can be readily incorporated in to Diggs' device to achieve predictable results. As discussed in Ground 1 above, Diggs discloses a memory card featuring ***multiple controllers***, where "[e]ach controller . . . may be configured to write data to, and read data from, the storage 150 in response to memory/storage access commands from hosts," which entails "translat[ing] control, address, and data signals into storage access commands to storage 150."

Diggs, ¶29. Diggs further teaches that its "[d]ata arbiter 140 is responsible for prioritizing read/write commands received simultaneously from multiple controllers," and may do so "according to a priority ranking." Diggs, ¶¶ 33, 40; Fig 2. Thorsten's memory card likewise features a "controller 5" that keys instructions to the logic component. Thorsten, ¶16. According to Thorsten, controller 5 either "connects [to] the logic component" via "third interface 13" (Thorsten, ¶14, Fig. 1), or else "the logic component is designed as an additional module of [the] controller 5" (Thorsten, ¶17). Given that Thorsten teaches flexibility in implementation, a POSITA would have observed that the logic component could be readily implemented in Diggs's memory card consistent with Thorsten's teachings, as I have illustrated by the below modification of Diggs' Figure 2.[6]

[6] I note that the Diggs-Thorsten Modification could be implemented slightly differently than how I have shown here—for example, where the logic component is situated between the controllers and the data arbiter, which would still be consistent with the collective teachings of the references.

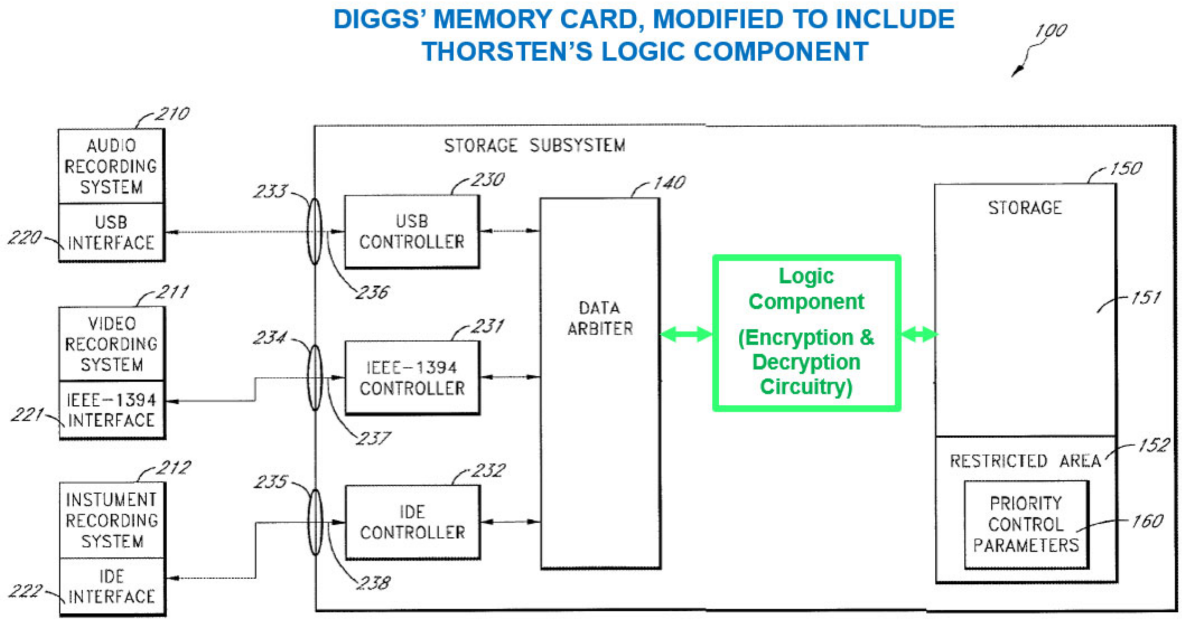


FIG. 2

Modification of Diggs, Fig. 2 (**"Diggs-Thorsten Modification"**).

159. In such an implementation, encryption and decryption instructions are keyed into the logic component (*i.e.*, programmable circuitry) by one of Diggs's controllers 230, 231, or 232, along with the data arbiter 140 (based on a priority ranking for simultaneously-received commands); depending on priority, "data to be transmitted … to [Diggs's] memory … is encrypted in the logic component 6. [Subsequently,] [w]hen reading data from the memory card, data is transmitted from the memory … with decryption being performed by the logic component 6." *See* Thorsten, ¶15. Thus, improving Diggs by implementing Thorsten's teachings would have constituted nothing more than the application of a known technique (*e.g.*, encryption and decryption circuity) to a known device (*e.g.*, Diggs' memory

card) to obtain predictable results (*e.g.*, storing and retrieving sensitive data in a manner compliant with various host applications).

2. Dependent Claim 2: The portable handheld memory card of claim 1 further comprising: decryption circuitry in communication with the memory and configured to decrypt encrypted data stored in the memory.

160. In my opinion, Diggs in view of Thorsten teaches Claim 2. As discussed in Ground 1, *supra*, Diggs teaches the portable handheld memory card of Claim 1. *See* Section XII.A.1, *supra*.

161. For the reasons discussed in Section XII.B.1, *supra*, Diggs-Thorsten teaches "decryption circuitry"—specifically, Thorsten's logic component (which I have annotated light green)—that is "in communication with the memory and configured to decrypt encrypted data stored in the memory."

3. Dependent Claim 17: The method of claim 16, wherein the data is encrypted data, and wherein the method further comprises: decrypting the encrypted data to decrypted data.

162. In my opinion, Diggs in view of Thorsten teaches Claim 17. As discussed in Ground 1, *supra*, Diggs teaches the method of Claim 16. *See* Section XII.A.7, *supra*.

163. For the reasons discussed in Section XII.B.1, *supra*, Diggs-Thorsten teaches the additional requirement that "the data [to be read from the memory] is

encrypted data, and wherein the method further comprises decrypting the encrypted data to decrypted data."

C. Ground 3: Claims 1, 4-8, 16, 20-21, and 23-27 Are Obvious Over Lin

164. As shown below, in my opinion, the subject matter of Claims 1, 4-8, 16, 20-21, and 23-27 are taught by Lin alone.

1. Claim 1

a. Element 1[preamble]: A portable handheld memory card comprising:

165. In my opinion, if the preamble of Claim 1 is limiting, Lin discloses it. Lin discloses "a removable memory card" (below, teal), also shown and described as a "removable electronic device." *See, e.g.*, Lin, ¶¶2, 21, 29, Fig 1A, 6A. ("removable electronic device 30"), Fig. 6A ("removable electronic device 120").

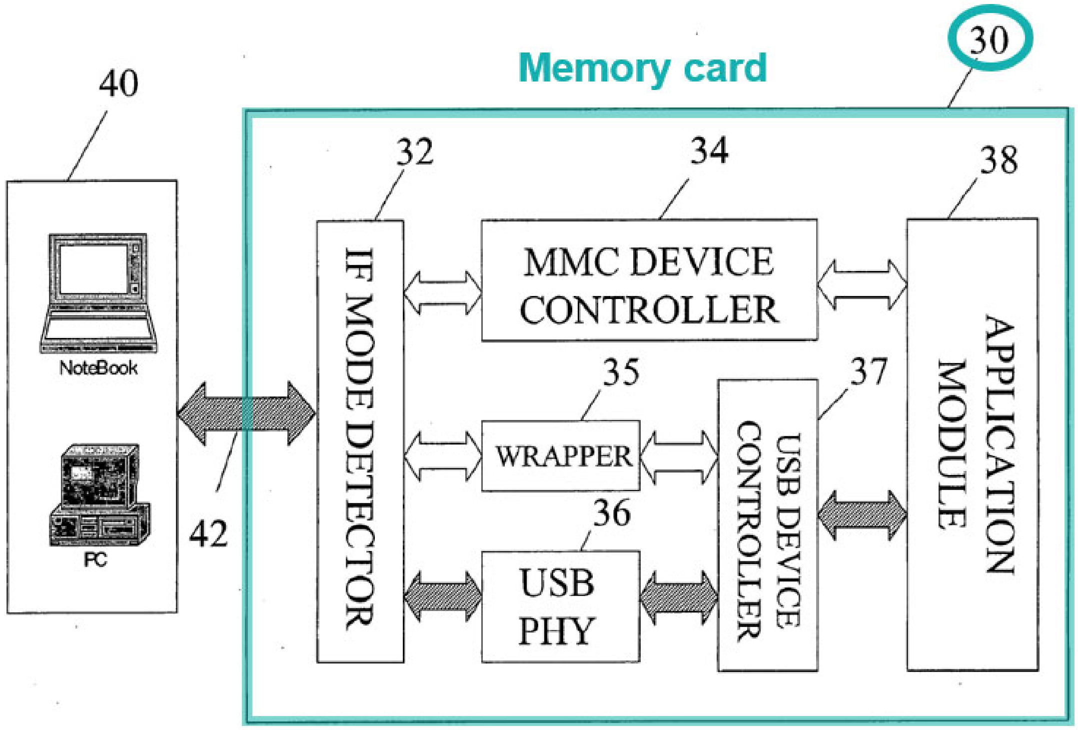


FIG. 1A

Lin, Fig. 1A (annotated).

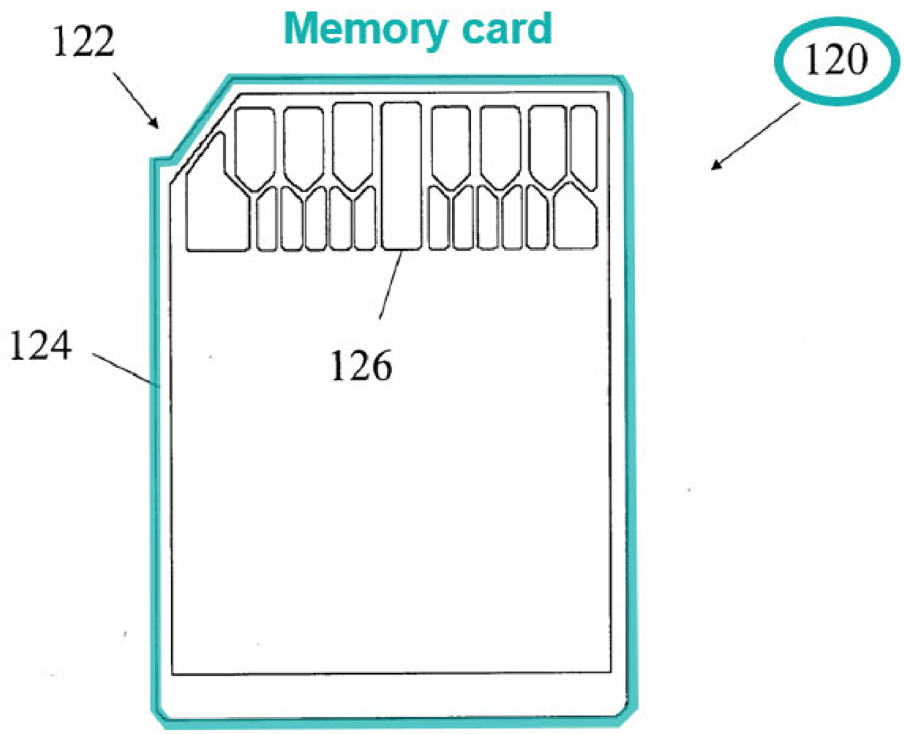


FIG. 6A

Lin, Fig. 6A (annotated).

166. Lin states that "[a] memory card is commonly known as a small ***portable*** package containing a digital memory," and is used to store data from various host "electronic devices that support removable data storage." Lin, ¶¶3-4. Lin also explains that its memory card is "*inserted* into a host ... for example, a notebook, a personal computer (PC), a cell phone, a tablet PC," Lin, ¶¶31, 106, and is "removable," *id.*, ¶¶2, 29. A POSITA would have understood that a user that "inserts" or "removes" the card does so with his hands, such that the memory card is "handheld" while the user is holding it before or after such actions. Lin's

memory card also includes a housing (*see* Element 1[f], *infra*), which a POSITA would have recognized as protecting internal components from dust, moisture, or impact, thus further confirming the "handheld" nature of the memory card.

b. Element 1[a]: a Universal Serial Bus (USB) port comprising a first set of pins;

167. In my opinion, Lin discloses Element 1[a]. Lin's removable electronic device is compatible with different modes of operation, including "a universal serial bus (USB) compatible mode." Lin, ¶8; *see also id.*, ¶5 (describing the USB standard). Fig. 1A, which I have annotated below, shows "electronic device 30 operating in a USB mode," as indicated by the blue bi-directional arrows. Lin, ¶31.

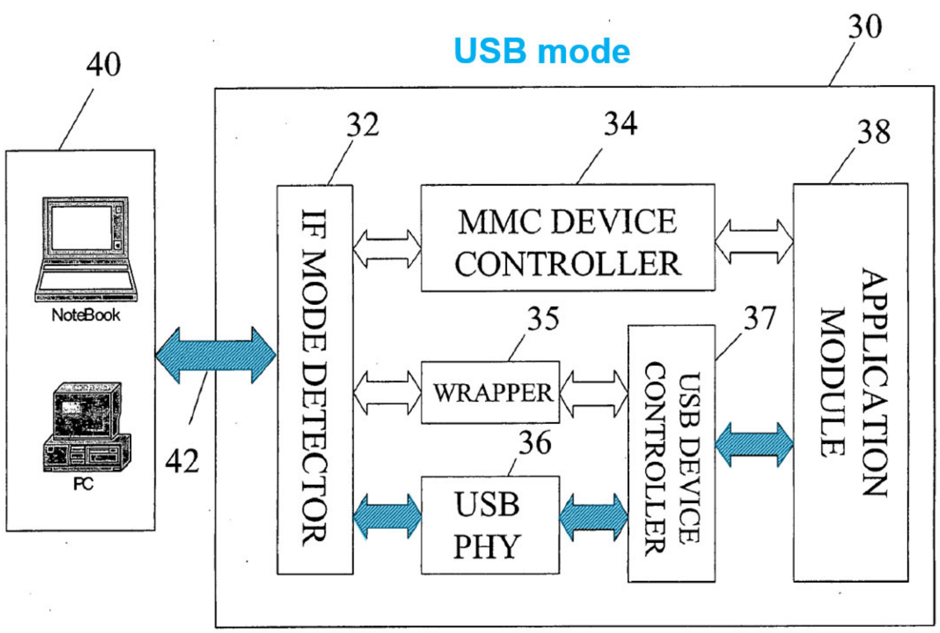


FIG. 1A

Lin, Fig. 1A (annotated).

168. Figure 4A shows "a proposed pin assignment chart" of an electronic device with USB compatibility. "The fourteenth and fifteenth pins for the USB mode, *i.e.*, D+ and D-, are a pair of data signals, which may be used to determine whether the USB mode is selected." Lin, ¶38. Specifically, D+ and D- are "a complementary pair in which one is at a high level when the other is at a low level." *Id.*

USB Port

Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3	VSS1	VSS1	VSS1	VSS1
4	VDD	VDD	VDD	VDD
5	CLK	SCLK		CLK
6	VSS2	VSS2	VSS1	VSS2
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

first set of pins

FIG. 4A

Lin, Fig. 4A (annotated).

169. Further, Figure 5, which I have also annotated below, shows "a diagram of a removable electronic device 100" that "includes a plurality of

interweaving contact pads labeled 1 to 20, which correspond to the pins illustrated in Fig. 4A." Lin, ¶¶106-107.

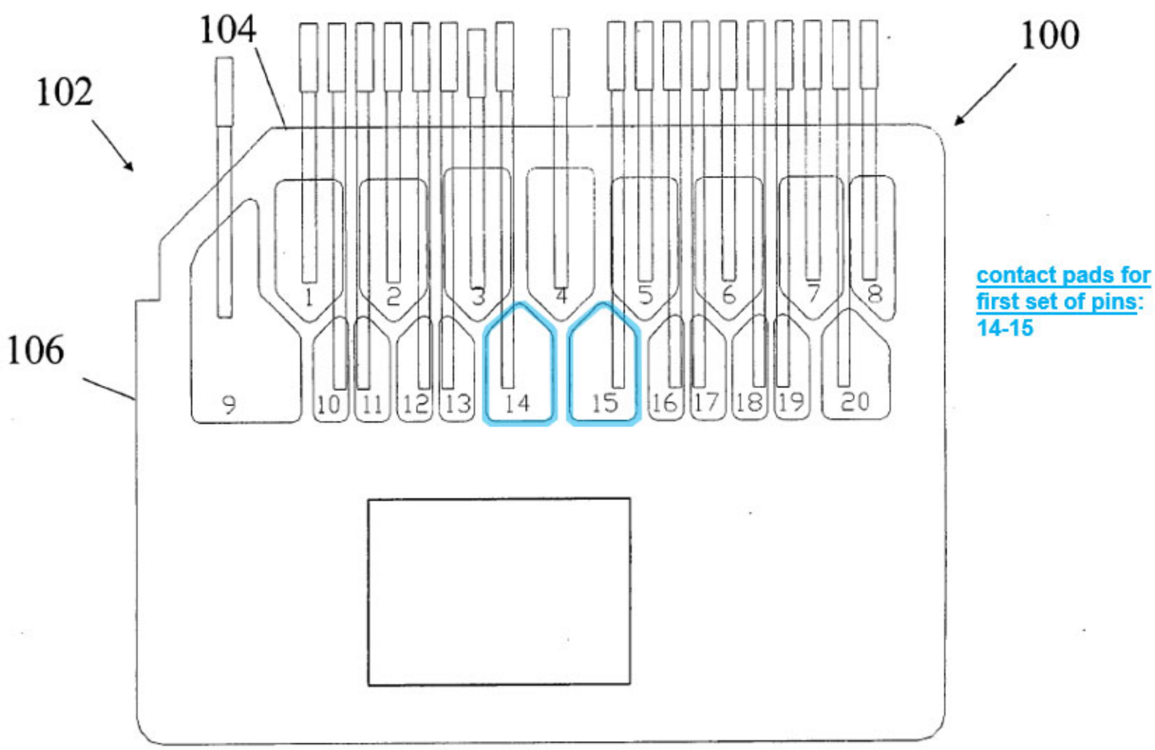


FIG. 5

Lin, Fig. 5 (annotated).

170. The claimed "USB port" is met by the set of pins, or else the corresponding set of contact pads, that are assigned to the USB mode according to Lin's Figure 4A. As shown in my Figure 4A and Figure 5 annotations above, the

corresponding "first set of pins" includes pins 14-15 associated with the USB mode of the device.[7]

c. Element 1[b]: USB controller circuitry electrically connected with the first set of pins of the USB port; and

171. In my opinion, Lin discloses Element 1[b]. Lin's memory card includes "a USB compatible device controller for controlling data transfer in the USB compatible mode." Lin, ¶8. Specifically, Fig. 1A, which I have annotated below, shows a "USB device controller 37" (green).

[7] Pins 3, 4, and 6, which provide power levels VSS1, VDD, and VSS2, respectively, while not required for my mapping to the claimed "first set of pins," could optionally be included.

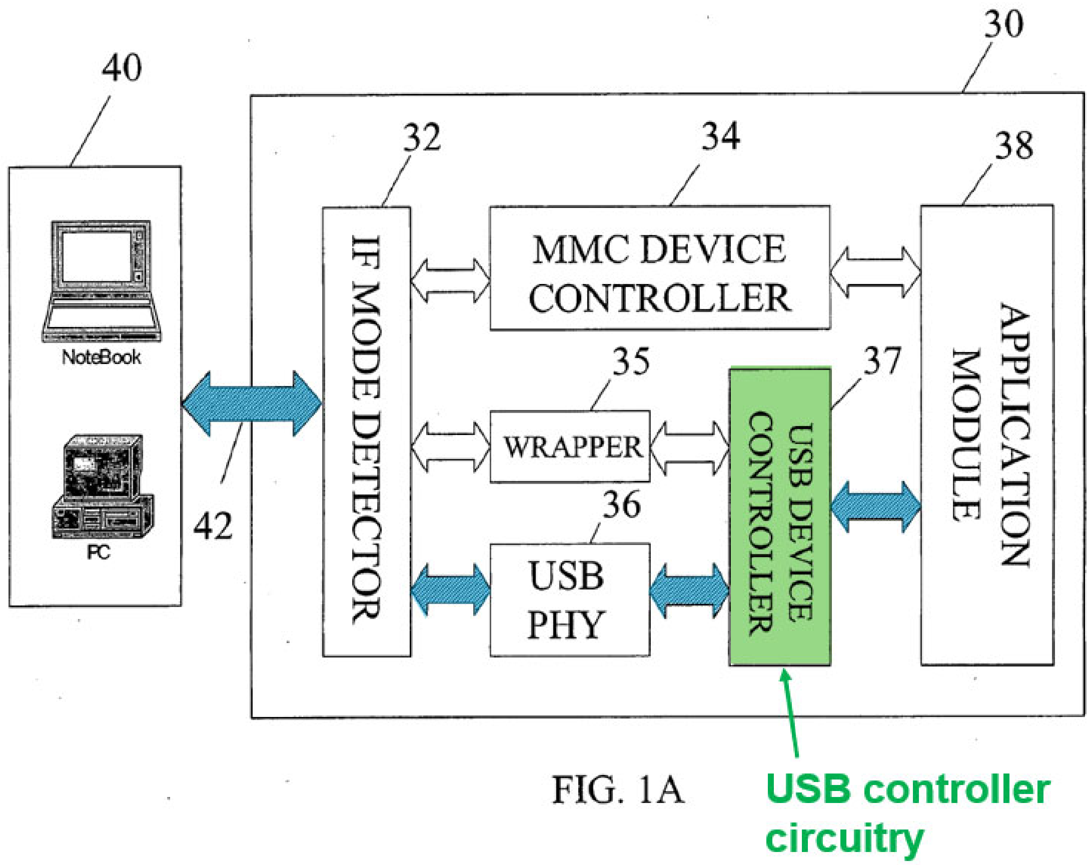


FIG. 1A

Lin, Fig. 1A (annotated).

172. The USB device controller is "electrically connected with the first set of pins of the USB port," for example, by way of the USB PHY circuit 36 and the IF mode detector 32 as reflected by the bi-directional arrows (which I have annotated in blue) in Fig. 1A.

d. Element 1[c]: an input/output (I/O) port comprising a second set of pins; and

173. In my opinion, Lin discloses Element 1[c]. Lin's removable electronic device features an "MMC compatible mode" that includes the "MMC 4.0 or MMC SPI (serial peripheral interface) applications." Lin, ¶¶ 7-8, 29; *see also id.*, ¶4

(describing "the MultiMedia Card ('MMC')" standard). Fig. 1C, which I have annotated below, shows "electronic device 30 operating in a MMC mode," as indicated by the red bi-directional arrows. Lin, ¶31.

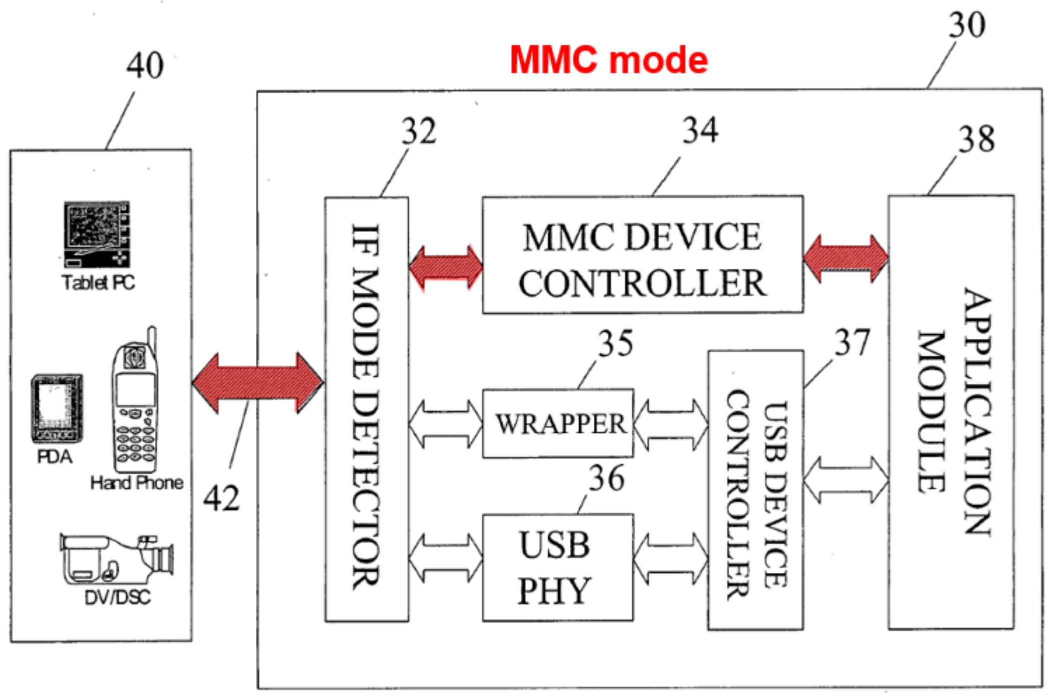


FIG. 1C

Lin, Fig. 1C (annotated).

174. The "pin assignment chart" of Fig. 4A shows how the electronic device features MMC compatibility. As I have shown in the below annotation of Figure 4A, the "MMC 4.0" standard uses pins 1-13 and 18-20. *See* Lin, Fig. 4A, ¶¶36, 38.

I/O Port

second set of pins

Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3	VSS1	VSS1	VSS1	VSS1
4	VDD	VDD	VDD	VDD
5	CLK	SCLK		CLK
6	VSS2	VSS2	VSS2	VSS2
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

FIG. 4A

Lin, Fig. 4A (annotated).

175. Further, Figure 5, also annotated below, shows "a diagram of a removable electronic device 100" that "includes a plurality of interweaving contact pads labeled 1 to 20, which correspond to the pins illustrated in Fig. 4a." Lin, ¶¶106-107.

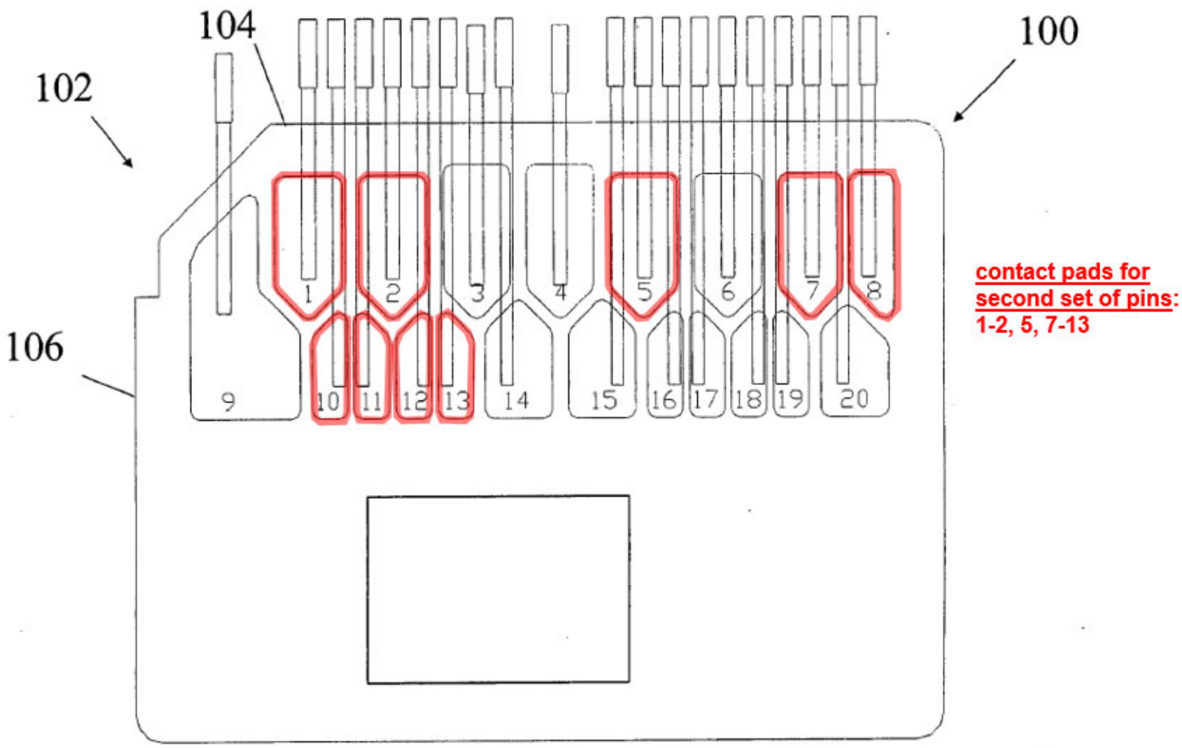


FIG. 5

Lin, Fig. 5 (annotated).

176. The claimed "I/O port" is met by the set of pins, or else the corresponding set of contact pads, that are assigned to the MMC 4.0 mode according to Lin's Figure 4A. As shown in my Figures 4A and 5 annotations above, the corresponding "second set of pins" includes pins 1-2, 5, and 7-13 associated with the MMC 4.0 mode of the device.[8]

[8] Pins 3, 4, and 6, which provide power levels VSS1, VDD, and VSS2, respectively, while not required for my mapping to the claimed "second set of pins," could optionally be included.

e. Element 1[d]: I/O controller circuitry electrically connected with the second set of pins of the I/O port;

177. In my opinion, Lin discloses Element 1[d]. Specifically, Lin's memory card includes "a multi-media card (MMC) device controller 34" (orange) that "controls data transfer between host 40 and application module 38" when "electronic device 30 is operating in an MMC mode." Lin, ¶¶31, 33.

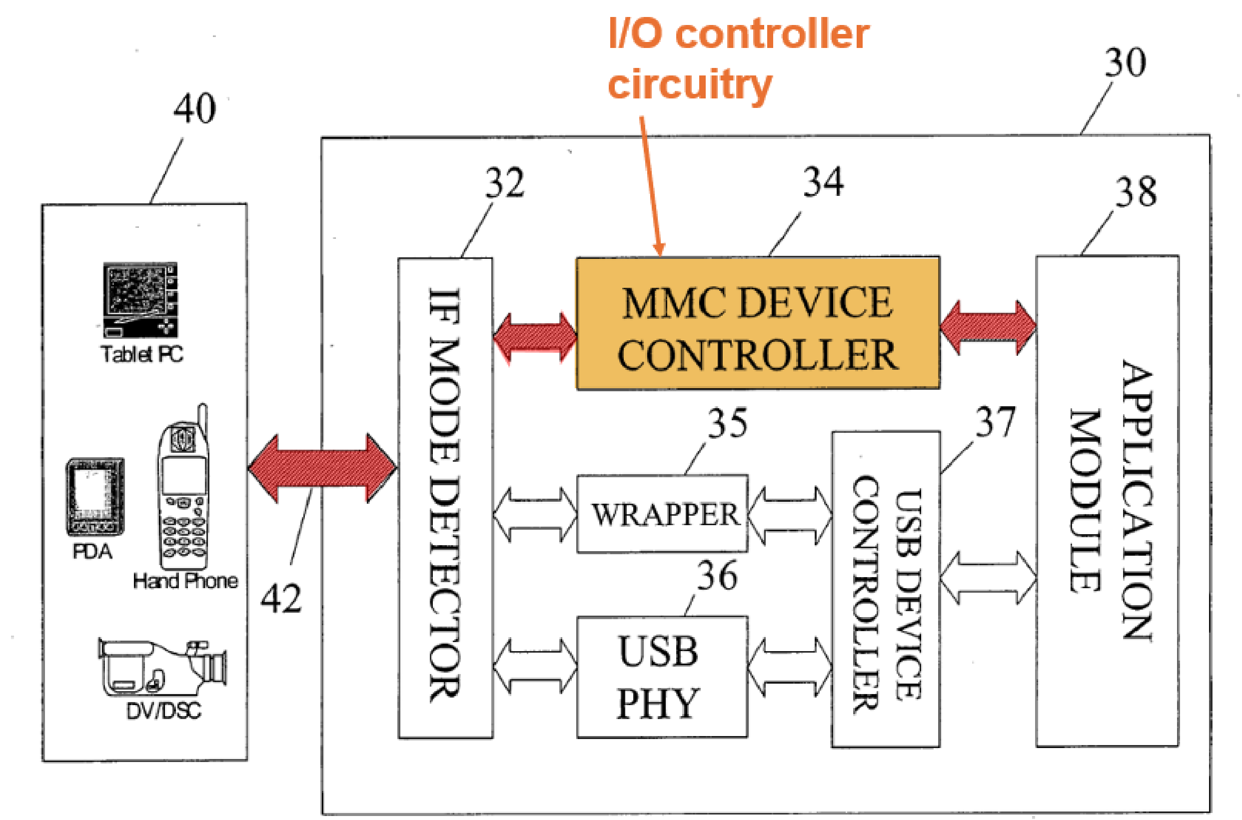


FIG. 1C

Lin, Fig. 1C (annotated).

178. A POSITA would have understood Lin's "MMC device controller 34" is "I/O controller circuitry" because a controller operates through circuitry.[9]

179. The MMC device controller is "electrically connected with the second set of pins of the I/O port," for example, by way of the IF mode detector 32 as reflected by the bi-directional arrows (annotated in red) in Figure 1C.

f. Element 1[e]: a memory in communication with the USB port and the I/O port; and

180. Lin discloses Element 1[e]. Lin discloses an "[a]pplication module 38," shown for example in Fig. 1C below (purple), that "functions to serve as a memory storage or an input/output (I/O) interface, depending on the operation mode detected." Lin, ¶31.

[9] As discussed in Section VIII.B, I note that during prosecution, the Applicant did not dispute the Examiner's mapping of the claimed "I/O controller circuity" to the "MMC interface controller" disclosed in the prior art Kim reference. *See* Ex-1004 at 73 (February 14, 2012 Office Action at 3).

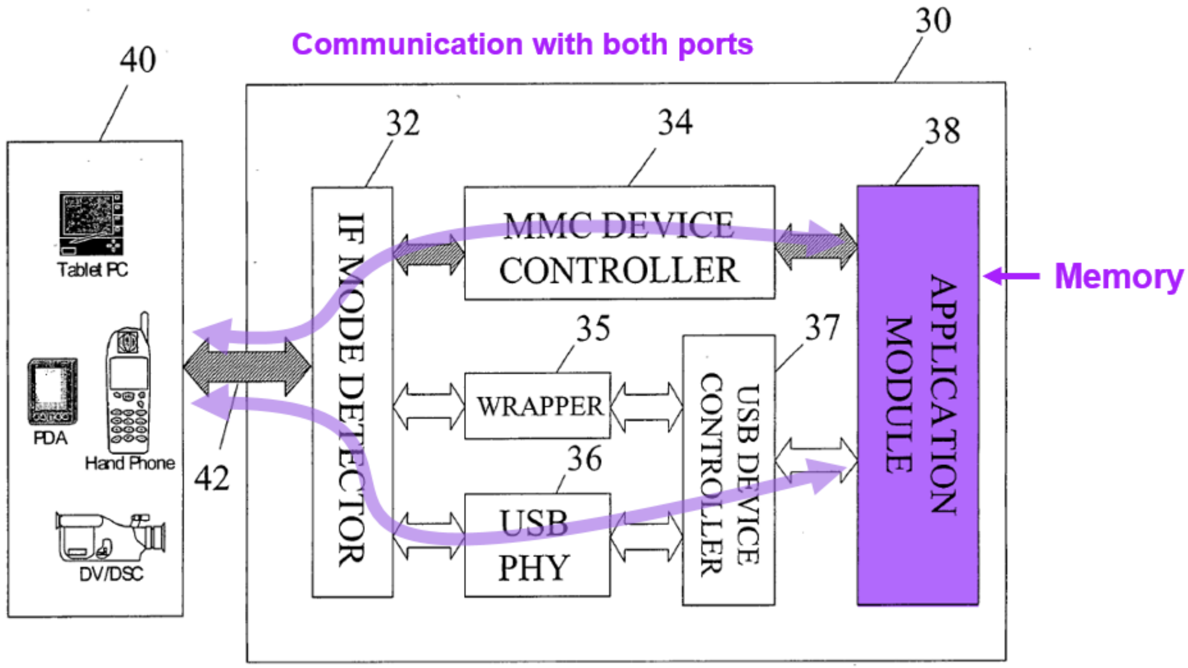


FIG. 1C

Lin, Fig. 1C (annotated).

181. In the USB mode, "USB device controller 37 controls data transfer over a common bus 42 between host 40 and application module 38 via USB PHY circuit 36." Lin, ¶31. Conversely, in the MMC mode, "MMC device controller controls data transfer between host 40 and application module 38." Lin, ¶33; *see also id.*, cls. 5-8 (specifying data transfer between "a host and the memory module," under each operating mode). Accordingly, Lin's disclosed memory is "in communication with the USB port and the I/O port."

g. Element 1[f]: a housing storing the memory and exposing the USB port and the I/O port;

182. In my opinion, Lin discloses Element 1[f]. Referring to Figures 6A and 6B, Lin shows and describes a "housing (not numbered)" for its memory card

(including the application module 38) that "includes a top surface, a bottom surface, and a periphery." Lin, ¶108.

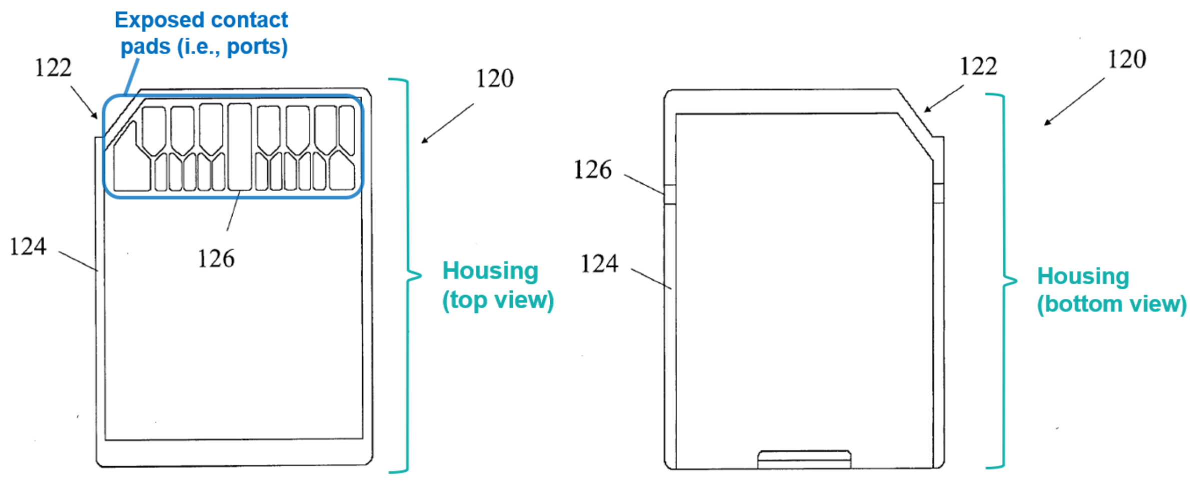


FIG. 6A

FIG. 6B

Lin, Figs. 6A-6B (annotated).

183. As shown in Figure 6A,[10] the top surface of the housing exposes the contact pads that correspond to the pins associated with the USB port and I/O port, as I identified for Elements 1[a] and 1[c] above. Lin further explains that "[t]he contact pads ... are positioned in twenty ***recesses*** on a top surface along a front side 104 and notch 102." Lin, ¶107; *see also id.*, ¶4 ("In general, a memory card includes ***exposed*** electrical contracts on its surface to allow easy connection to and removal from a receptacle of a host electronic system or device, particularly

[10] Based on Lin's description at paragraph 109, in Fig. 6A, the label "126," depicted as indicating a contact pad, appears to be a typo that should instead be "128."

portable devices.”). Accordingly, Lin discloses “a housing storing the memory and exposing the USB port and the I/O port.”

h. Element 1[g]: wherein the USB port and the I/O port are positioned on a same end to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port; and

184. In my opinion, Lin discloses Element 1[g]. As shown in Figures 5 and 6A, Lin’s memory card “includes a plurality of contact pads labeled 1 to 20, which correspond to the pins illustrated in Figure 4A. The interweaving design in the contact pads allows additional pins to be present in the same real estate.” Lin, ¶107. Further, “[t]he contact pads are positioned in twenty recesses on a top surface ***along front side 104*** and notch 102,” where the notch is included “to prevent incorrect insertion of [the] electronic device.” Lin, ¶¶106-107. Accordingly, Lin’s “USB port” and “I/O port”—which correspond to the contact pads on the memory card as explained for Elements 1[a] and 1[c]—“are positioned on a same end to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port.”

185. I note that the position and orientation of the contact pads of Lin’s memory card are substantially similar to Figure 2 of the challenged ’051 Patent, which is described as satisfying the claim element. There, as in Lin, the contact

pads (or pins) are located alongside a "same end"—specifically, the "front 202" of "memory card 200." '051 Patent, Fig. 2, 4:38-42.

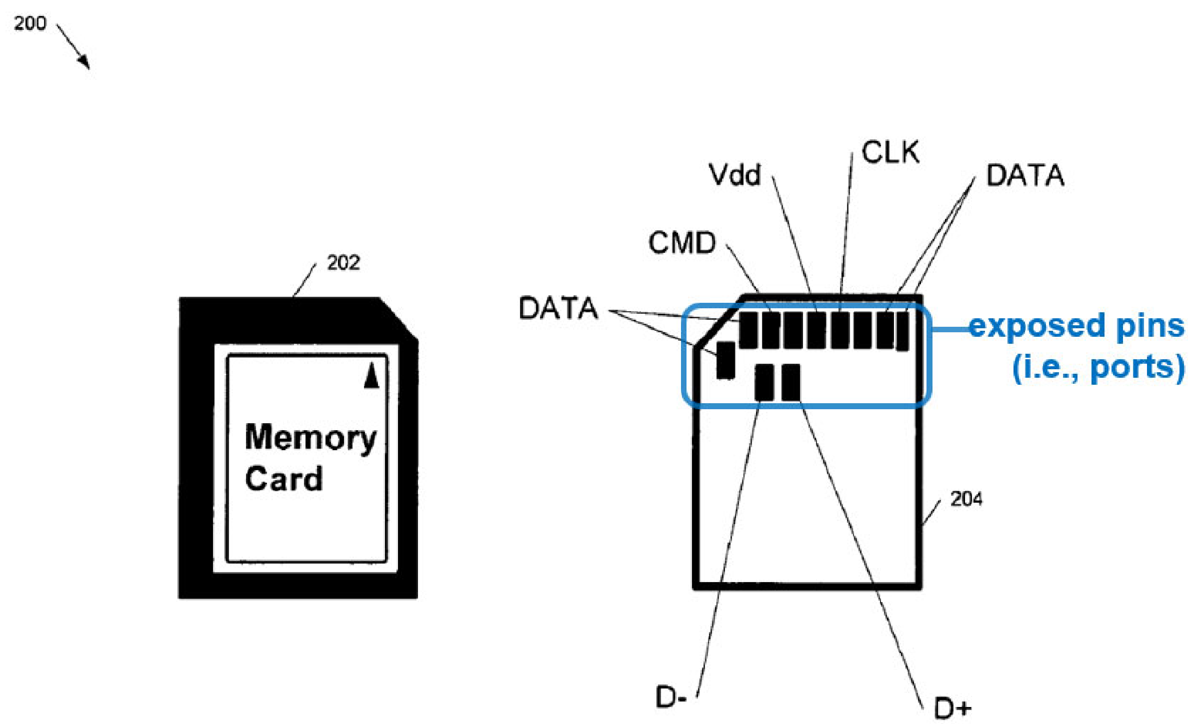


Figure 2

'051 Patent, Fig. 2 (annotated).

186. The '051 Patent explains that "the memory card 200 is ***configured to be inserted in a certain direction*** and orientation so that the SD port interfaces with a mating SD port of a host device. When the memory card 200 is inserted in this fashion, the USB port may also interface with a mating USB port of the host device." '051 Patent, 4:61-66.

i. Element 1[h]: wherein the USB port and the I/O port are positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and

187. In my opinion, Lin discloses Element 1[h]. As discussed for Elements 1[a], 1[c], and 1[g] above, in Lin's memory card, all of the contact pads—including those corresponding to the "USB port" and "I/O port"—are positioned on the front end of the card, which "allow[s] a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port."

188. Further, "IF mode detector 32 detects a mode of operation to distinguish among an MMC mode, a USB mode, or a Mu mode when electronic device 30 is inserted into a host 40." Lin, ¶31. In Figure 1C, for example, "IF mode detector detects that a host 40, to which electronic device 30 is connected, is in compliance with the MMC specifications." Lin, ¶33. As shown and described for Figure 2, this detection or determination is based on the power source voltage level, and the type of command signal received. Lin ¶¶34-35, 37. The pin assignment chart of Figure 4A indicates which pins are used, for example, in the MMC 4.0 mode (corresponding to the "I/O port") and which are used for the USB mode (corresponding to the "USB port"). Lin, ¶38. Pursuant to the MMC specification, "[t]he first pin of the removable electronic device for the MMC 4.0

mode, *i.e.*, DAT 3, is defined to switch the MMC 4.0 mode to the MMC SPI mode." Lin, ¶38. Figure 4A, which I have annotated again below, shows that the MMC 4.0 mode—which corresponds to ***"when the I/O port is electrically connected with the host device"***—does not use two of the pins that are assigned to the USB mode (specifically, pins 14 and 15).

I/O Port connected to host device

Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3	VSS1	VSS1	VSS1	VSS1
4	VDD	VDD	VDD	VDD
5	CLK	SCLK		CLK
6	VSS2	VSS2	VSS2	VSS2
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

Two of the "first set of pins of the USB port" are not electrically connected to host

FIG. 4A

Lin, Fig. 4A (annotated).

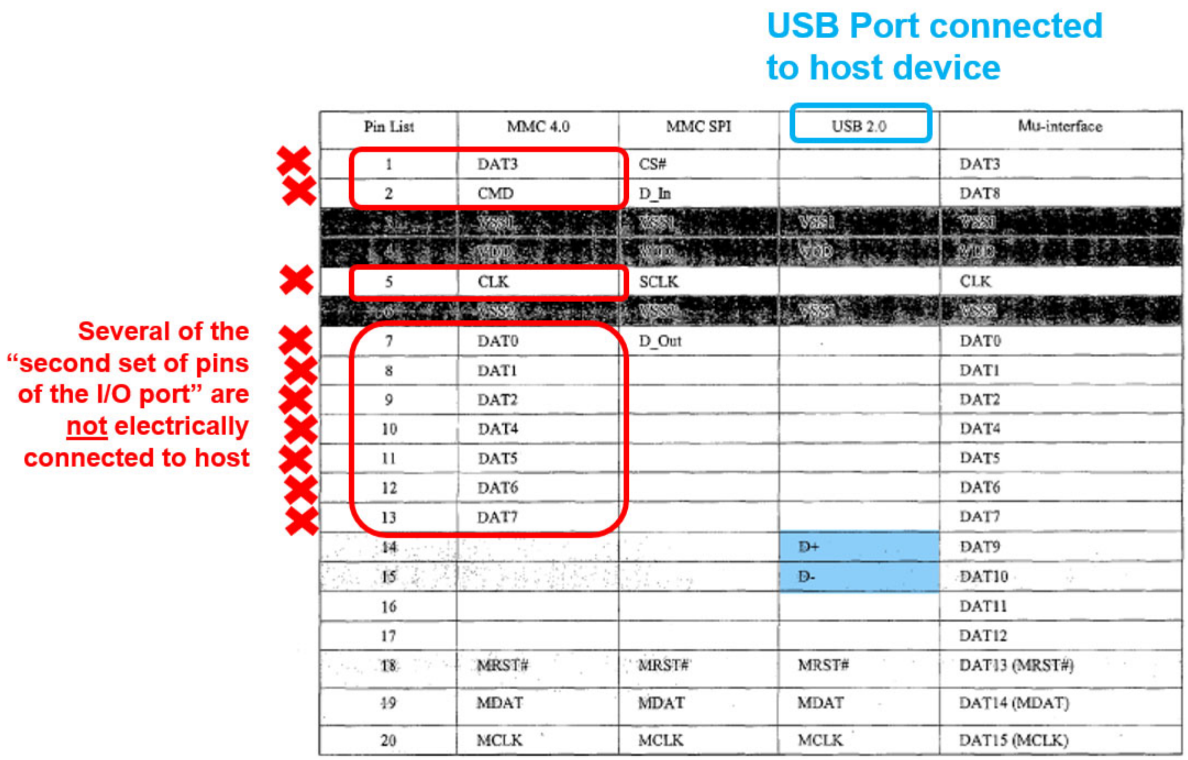
189. Since pins 14 and 15 are not used to transmit electrical signals in the MMC 4.0 mode, these ***"pins of the USB port [are] not electrically connected with the host device"*** in that scenario.

190. Consistent with this understanding, I note that during prosecution, the Applicant referenced Figure 1 of the '051 Patent as "[a]n example of" the scenario

contemplated by Element 1[h]—which was added by amendment to overcome the Kim reference—citing the fact that "in Figure 1, the data line inputs (D+ and D-)" used for the USB mode "are not input to the Host Interface" used for the SD mode, which "allows the pin layout for the USB port to be different from the pin layout for the SD port." Ex-1004 at 46, 52-54 (July 16, 2012 Response at 2, 8-10). Lin's memory card likewise uses a different pin layout for its USB mode (which also uses "D+ and D-" as data inputs) versus its MMC 4.0 mode.

j. Element 1[i]: when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device.

191. In my opinion, Lin discloses Element 1[i]. As discussed for Element 1[h], in Lin's memory card, "IF mode detector 32 detects a mode of operation to distinguish among an MMC mode, a USB mode, or a Mu mode when electronic device 30 is inserted into a host 40." Lin, ¶31. Figure 4A's pin assignment chart, which I have annotated again below, shows that the USB mode—corresponding to ***"when the USB port is electrically connected with the host device"***—does not use several of the pins that are assigned to the MMC 4.0 mode (specifically, pins 1-2, 5, and 7-13).



Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3	VSS1	VSS1	VSS1	VSS1
4	VDD	VDD	VDD	VDD
5	CLK	SCLK		CLK
6	VSS2	VSS2	VSS2	VSS2
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

FIG. 4A

Lin, Fig. 4A (annotated).

192. Since pins 1-2, 5, and 7-13 are not used to transmit electrical signals in the USB mode, these ***"pins of the I/O port [are] not electrically connected with the host device"*** in that scenario.

193. As explained for Element 1[h], I note that this understanding is consistent with Applicant's remarks regarding this limitation, which was added by claim amendment during prosecution. Ex-1004 at 46, 52-54 (July 16, 2012 Response at 2, 8-10).

2. Claim 4: The portable handheld memory card of claim 1 further comprising: a power management unit in communication with the USB controller circuitry.

194. In my opinion, Lin teaches the further requirement of "a power management unit in communication with the USB controller circuitry." Specifically, as I have shown in Figure 1A below, Lin's "IF mode detector 32" (light blue) corresponds to the claimed "power management unit."

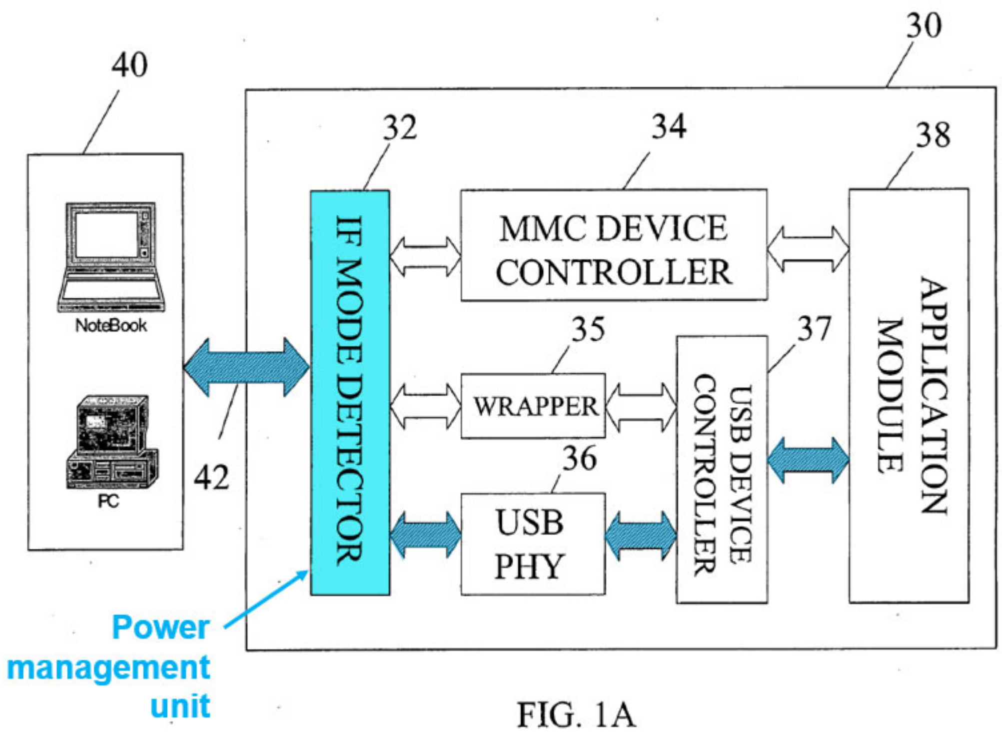


FIG. 1A

Lin, Fig. 1A (annotated).

195. Lin explains that "IF mode detector 32 detects a mode of operation to distinguish among an MMC mode, a USB mode or a Mu mode when electronic device 30 is inserted into a host 40," and that it does so by "determin[ing] whether the [power source voltage] VDD is equal to or greater than a voltage level a USB

application requires." Lin, ¶¶31, 34, Figs. 1A, 2; *see also id.*, ¶30 ("Electronic device 30 includes a 1- 4-, 8-, or 16-bit interface, and provides low voltage support of 5V/3.3V/1.8V, with zero power consumption during standby."). Similarly, the '051 Patent specification discloses a "power management unit 116," and states that it may convert the "bus voltage Vbus … to a suitable voltage for use by components of the memory card 100." '051 Patent, 3:60-63.

196. IF mode detector is further shown and described as being in communication with "USB device controller 37," which is enabled when the host is determined to require the USB mode. *See* Lin, ¶34.[11]

197. Moreover, a POSITA would have been motivated to implement Lin's IF Mode Detector as a power management unit in communication with the USB device controller to ensure that, when Lin's device is in the USB mode, its power source voltage requirements are adjusted to comply with the USB standard.

3. Claim 5: The portable handheld memory card of claim 1 further comprising: a host interface module in communication with the I/O port.

198. In my opinion, Lin discloses the added requirement of "a host interface module in communication with the I/O port." The '051 Patent

[11] I note that the operation of Lin's IF mode detector is analogous to the "level sensing circuit" of the prior art Kim reference cited during prosecution, s*ee* Ex-1022, 6:26-32, Fig. 8. The Applicant did not dispute Examiner's mapping of Kim's level sensing circuit" to the claimed "power management unit." *See* Ex-1004 at 72 (February 14, 2012 Office Action at 4).

specification discloses a "host interface circuit 114" that "may translate data to and from the SD protocol to be transferred via the SD port 104." '051 Patent, 4:4-7.

199. As indicated in orange in Figure 1C below, Lin's "interface (IF) Mode detector 32" and "MMC device controller 34," individually or collectively, corresponds to the "host interface module" as understood from the intrinsic record.[12]

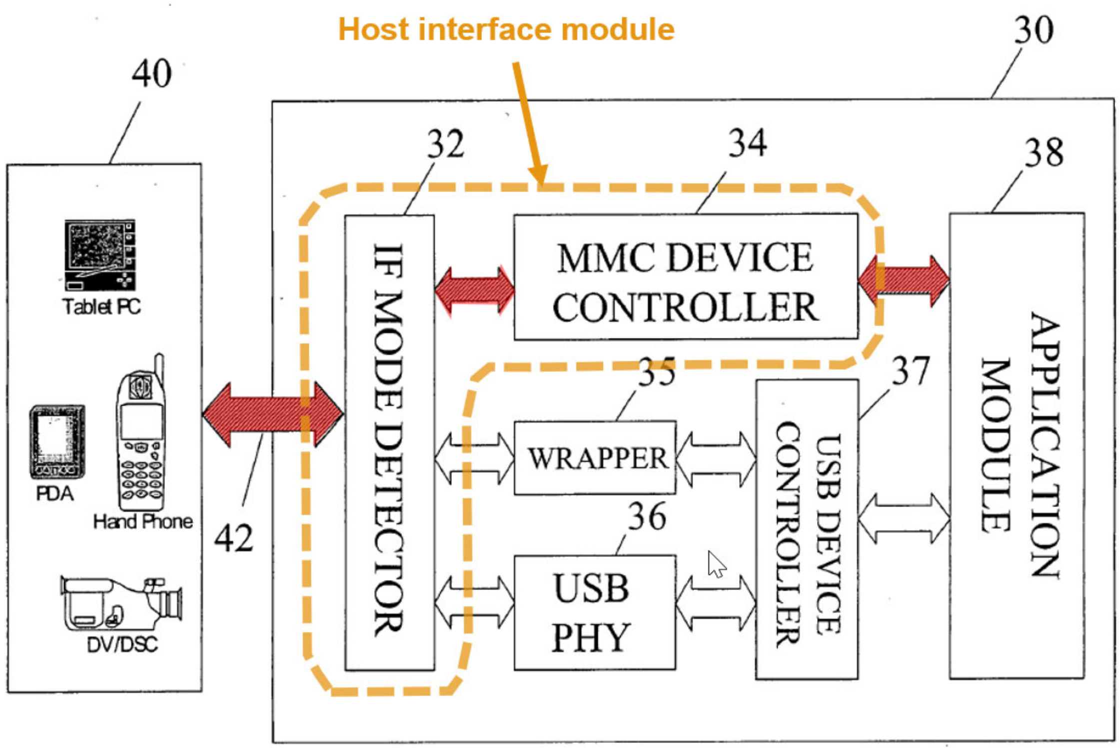


FIG. 1C

Lin, Fig. 1C (annotated).

[12] During prosecution, the Applicant did not dispute Examiner's mapping of the "MMC interface controller" of the prior art Kim reference to the claimed "host interface module," despite also mapping that feature to the "I/O controller circuitry." *See* Ex-1004 at 72 (February 14, 2012 Office Action at 4).

200. Lin teaches that the "MMC device controller 34 controls data transfer between host 40 and application module 38," Lin, ¶33, which entails translating data. Further, both IF mode detector and MMC device controller ***interface*** with the "host 40," either directly or indirectly. *See* Lin, ¶¶31. Finally, both modules also communicate with the "I/O port" (*i.e.*, the assigned pins or contact pads corresponding to the MMC 4.0 mode).

201. Accordingly, either or both of Lin's MMC device controller and IF Mode detector is a "host interface module in communication with the I/O port."

4. Claim 6: The portable handheld memory card of claim 1 further comprising: circuitry configured to control read and write operations to the memory.

202. In my opinion, Lin discloses dependent Claim 6. Specifically, any or all of the USB device controller, USB PHY circuit, or MMC device controller (surrounded in yellow in Figure 1A below) is "circuitry configured to control read and write operations to the memory."

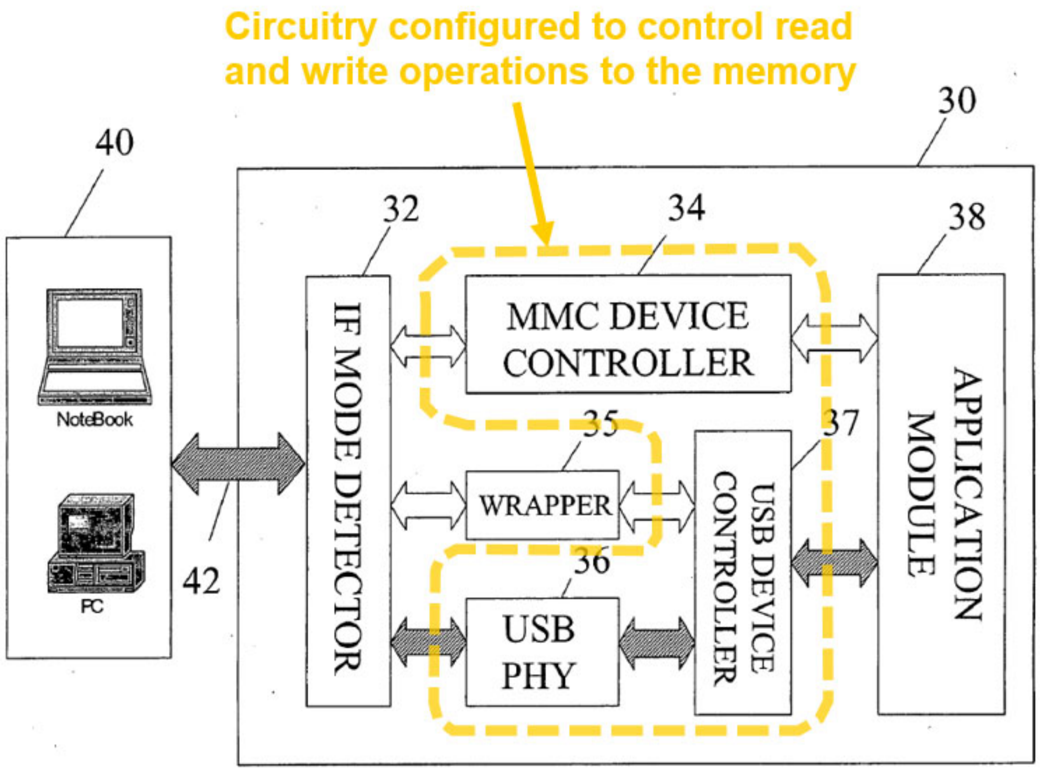


FIG. 1A

Lin, Fig. 1A (annotated).

203. For example, Lin teaches that its "USB device controller 37 ***controls data transfer*** over a common bus 42 ***between*** host 40 and application module 38" (*i.e.*, memory storage) "via USB PHY circuit 36." Lin, ¶31, Fig. 1A. Lin further teaches that its "MMC device controller 34 [also] ***controls data transfer*** between host 40 and application module 38." Lin, ¶33. In the memory storage context, a POSITA would have known that data transfer "between" a memory storage and a host device entails both read and write operations. *See, e.g.*, Ex-1005 (Chen), ¶2 (observing that "a memory device has not only an internal solid-state storage medium but also a controller, which … [w]rites the data from the [external] system

into the solid-state storage medium or read[s] the data stored in the solid-state storage medium").

5. Claim 7: The portable handheld memory card of claim 1, wherein the I/O port comprises a Secure Digital port.

204. In my opinion, Lin teaches Claim 7. As discussed for Element 1[c] above, Lin's memory card ("electronic device") is operable in the MMC 4.0 mode, and the corresponding pins and/or contact pads used for that mode is an "I/O port." *See* Section XII.A.1.d, *supra*. Lin likewise discloses that its "[e]lectronic device 30 ... is [also] able to support modes of operation compatible with ... SD (security digital) applications," and that "[s]killed persons in the art will understand that the present invention is equally applicable" to the "SD mode[]." Lin, ¶29. Pursuant to this teaching, a POSITA would have understood that an obvious design choice would have been to implement an SD mode in place of the MMC 4.0 mode, as shown in the below modification of Lin's Figure 1C, with an "SD Device Controller" in place of the MMC Device Controller.

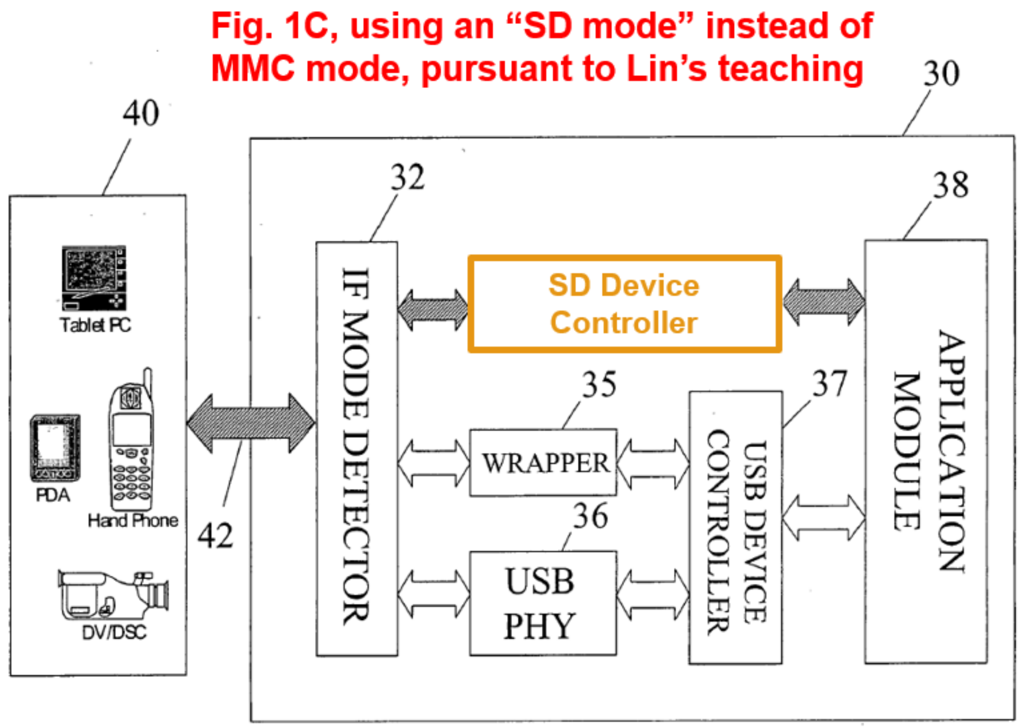


FIG. 1C

Modification of Lin Fig. 1C, to include an "SD Mode."

205. A POSITA would have understood that the above implementation of Lin's memory card features an "SD port" instead of the MMC port discussed for Element 1[c] above, and it uses a different pin assignment for the SD mode than for the USB mode, such that one or more pins assigned to one mode is not assigned to the other. This is reflected, for example, by the below "signal pins" diagram included in the Secure Digital Specification (showing 3 "Data" pins, along with CMD and CLK):

2.4 Signal Pins

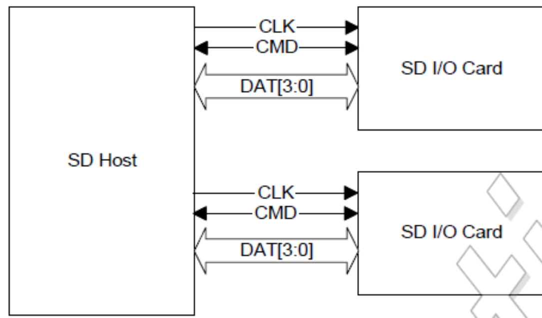


Figure 2-1 Signal connection to two 4-bit SDIO cards

Ex-1028 (Secure Digital Specification) at 12.

6. Claim 8: The portable handheld memory card of claim 1, wherein the memory comprises Flash memory.

206. In my opinion, Lin teaches Claim 8. Lin discloses that its "application module 38 functions to serve as a memory storage." Lin, ¶31. As Lin also recognizes, it is common knowledge that memory cards use "flash memories" for storage. Lin, ¶3. Accordingly, it would have been an obvious design choice to implement Lin's memory card using flash memory in the application module 38, as shown in Figure 1C below.

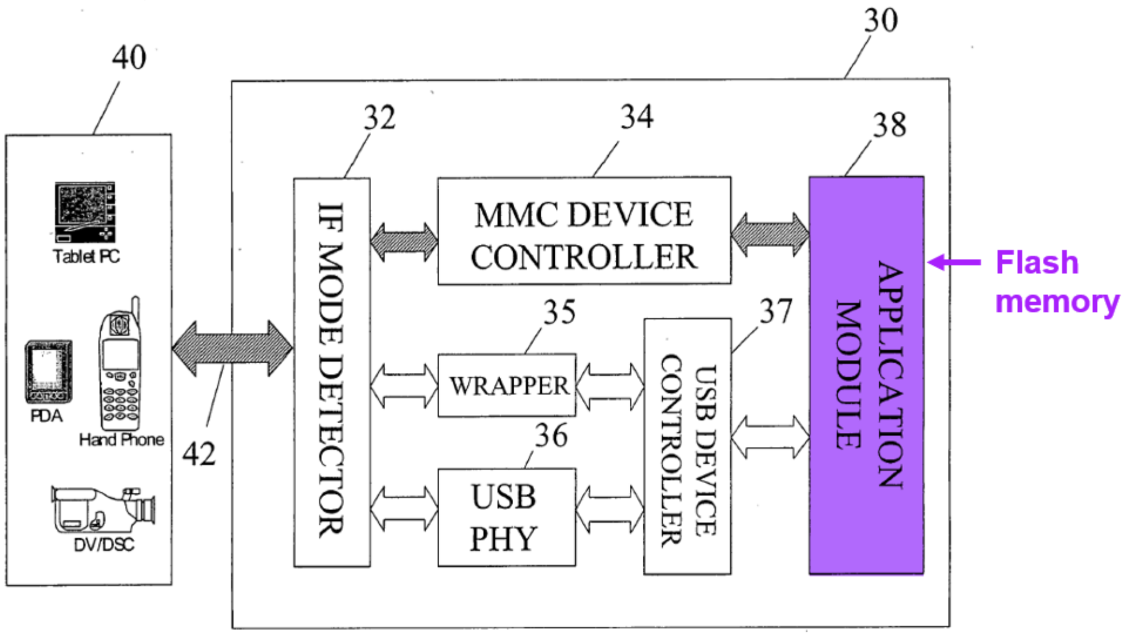


FIG. 1C

Lin, Figure 1C (annotated).

7. **Claim 16:**

a. **Element 16[Preamble]: A method comprising:**

b. **Element 16[a]: with a portable handheld card comprising a Universal Serial Bus (USB) port comprising a first set of pins; USB controller circuitry electrically connected with the first set of pins of the USB port; an input/output (I/O) port comprising a second set of pins; I/O controller circuitry electrically connected with the second set of pins of the I/O port; a memory in communication with the USB port and the I/O port; and a housing storing the memory and exposing the USB port and the I/O port, wherein the USB port and the I/O port are positioned to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port and wherein the USB port and the I/O port are positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not**

electrically connected to the host device, and when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device:

207. In my opinion, Lin teaches Elements 16[preamble]-16[a]. *See* Claim 1, *supra*; Ex-1020 (Claim Mapping Table).

c. Element 16[b]: reading data from the memory;

208. In my opinion, Lin teaches Element 16[b]. As discussed for Claim 6 above, Lin discloses "circuitry configured to control read and write operations to the memory." Such read operations entail "reading data from the memory." *See* Claim 6, *supra*.

d. Element 16[c]: determining whether the data is to be transmitted via the USB port or I/O port; and

209. In my opinion, Lin teaches Element 16[c]. Specifically, "IF mode detector 32 detects a mode of operation to distinguish among an MMC mode, a USB mode or a Mu mode when electronic device 30 is inserted into a host 40," and it does so by "determin[ing] whether the [power source voltage] VDD is equal to or greater than a voltage level a USB application requires." Lin, ¶¶31, 34, Figs. 1A, 2. Accordingly, Lin's memory card, using the IF mode detector, "determin[es] whether the data is to be transmitted" between the application module 38 and host 40 "via the USB port or the I/O port."

e. Element 16[d]: transmitting the data to the host device via the determined port.

210. In my opinion, Lin teaches Element 16[d]. *See* Claim 6 and Element 16[c], *supra*. During a read operation, Lin's memory card "transmit[s] the data to the host device via the determined port."

8. Claim 20: The method of claim 16, wherein the I/O port comprises a Secure Digital port.

211. In my opinion, Lin teaches Claim 20. *See* Claim 7, *supra*.

9. Claim 21: The method of claim 16, wherein the memory comprises Flash memory.

212. In my opinion, Lin teaches Claim 21. *See* Claim 8, *supra*.

10. Claim 23: The portable handheld memory card of claim 1, wherein at least two pins of the USB port are parallel to at least two pins of the I/O port.

213. In my opinion, Lin teaches Claim 23. For example, Figure 5 shows that all of Lin's pins and (and corresponding contact pads) are positioned and oriented to be in parallel with one another. Accordingly, pursuant to the pin assignment chart of Figure 4A, several of the pins of USB port are in parallel to several of the pins of Lin's "I/O port" (*i.e.*, corresponding to the MMC 4.0 mode), as I have shown in the below annotations.

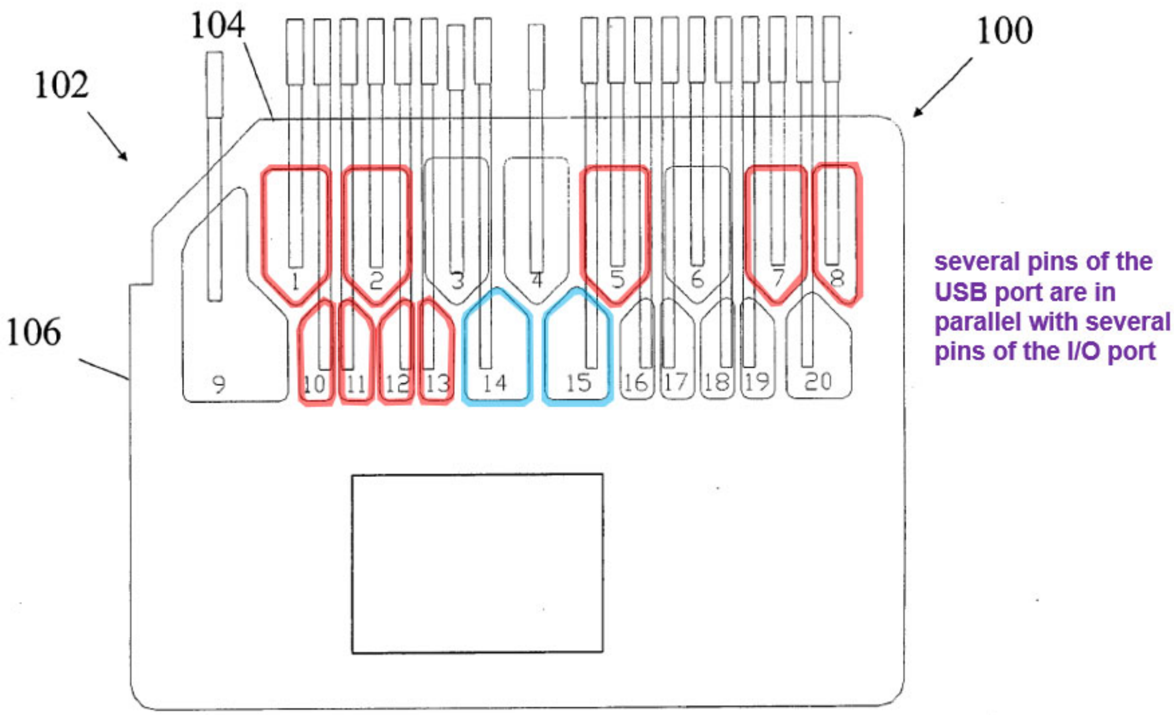
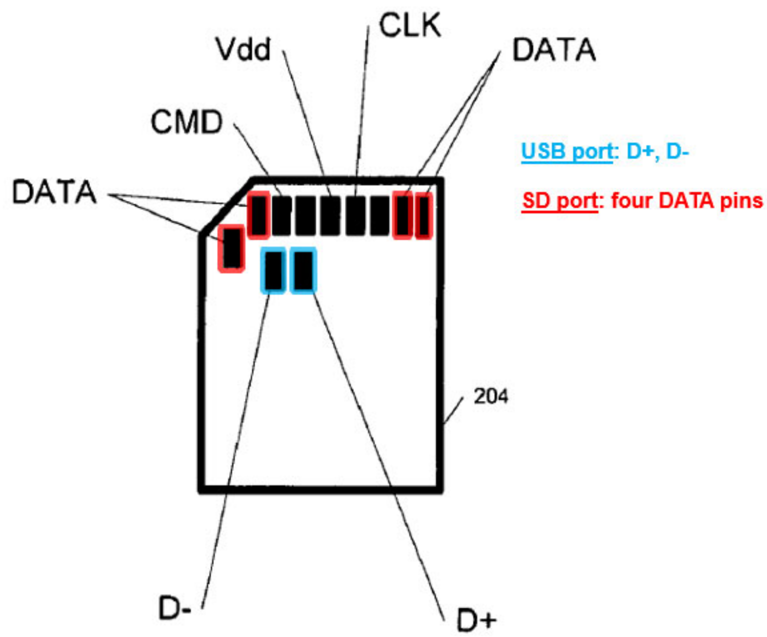


FIG. 5

Lin, Fig. 5 (annotated).

214. I note that the parallel orientation of the above-identified pins in Figure 5 of Lin is the same as in Figure 2 of the ’051 Patent, which—as indicated below—shows that the two data pins (D+, D-) of the USB port are parallel to at least two of the DATA pins of the SD port (*i.e.*, an “I/O port”). *See* ’051 Patent, 4:38-5:9, Fig. 2.



’051 Patent, Fig. 2 (annotated).

215. I further note that the illustration of Figure 2 is the only disclosure of “parallel pins” contained in the ’051 Patent.

11. Claim 24: The portable handheld memory card of claim 1, wherein layout for the USB port is different from layout of the I/O port.

216. In my opinion, Lin discloses Claim 24. Specifically, the pin assignment chart of Figure 4A indicates that two different sets of pins of Lin’s memory card are assigned to the USB mode (corresponding to the claimed “USB port”) and to the MMC 4.0 mode (corresponding to the “I/O port”), respectively. *See* Elements 1[a], 1[c], 1[h]-[i], *supra*.[13]

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[13] I note that, during prosecution, the Examiner similarly concluded—and Applicant did not dispute—that this “different layout” requirement is disclosed in Figure 8 block diagram of the prior art Kim reference, which simply shows *which*

12. Claim 25: The portable handheld memory card of claim 1, wherein the I/O port is configured for mating with an external port.

217. In my opinion, Lin discloses Claim 25. Specifically, Lin's "I/O port"—*i.e.*, the set of pins assigned to the MMC 4.0 mode pursuant to the assignment chart of Figure 4A, or their corresponding "exposed electrical contacts"—is configured for mating with the external port of an MMC 4.0-compliant host device 40 connected to the memory card. *See, e.g.*, Lin, ¶4 ("In general, a memory card includes exposed electrical contacts on its surface to allow ***easy connection to*** and removal from a receptacle of a host electronic system or device."); *id.*, Figs. 1C, 4A, ¶¶31-34, 38.

13. Claim 26: The portable handheld memory card of claim 1, wherein all of the first set of pins electrically connected with the USB controller circuitry is not electrically connected to the I/O controller circuitry.

218. In my opinion, Lin teaches Claim 26. Lin discloses that, in the USB mode, "USB device controller 37 controls data transfer over a common bus 42 between host 40 and application module 38." Lin, ¶38, Fig. 1A. Lin further discloses that the USB mode uses data pins 14 and 15 (*i.e.*, D+ and D-)—the claimed "first set of pins" identified for Element 1[a]—for that purpose. Lin, ¶38.

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pins are connected to the USB and MMC controllers, respectively, but without any indication of the structural layout for the USB and MMC ports. *See* Ex-1004 at 74 (February 14, 2012 Office Action at 6); Ex-1022, Fig. 8.

Accordingly, "all of the first set of pins" are electrically connected to the USB device controller 37, as all such pins are used to transmit electrical signals in the USB mode. Lin's MMC device controller 34, on the other hand, is only used in the MMC mode. *See* Lin, ¶33, Fig. 1C. As shown in the Figure 4A pin assignment chart, the MMC mode does not use either of the "first set of pins" associated with the USB mode.

Pins electrically connected to MMC device controller

Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3	VSS1	VSS1	VSS1	VSS1
4	VDD	VDD	VDD	VDD
5	CLK	SCLK		CLK
6	VSS2	VSS2	VSS2	VSS2
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

All of the "first set of pins of the USB port" are not electrically connected to MMC device controller (used in the MMC mode)

FIG. 4A

Lin, Fig. 4A (annotated).

219. Since neither of the "first set of pins" are used to transmit electrical signals in the MMC mode, those pins "are not electrically connected to the MMC device controller." *See* Lin, Figs. 1A, 4A.

14. Claim 27:

a. Element 27[preamble]: The portable handheld memory card of claim 1,

b. Element 27[a]: wherein the USB port comprises multiple data lines,

220. In my opinion, Lin teaches Elements 27[preamble]-27[a]. According to the pin assignment chart of Figure 4A, "[t]he fourteenth and fifteen pins for the USB mode, *i.e.*, ***D+ and D-, are a pair of data signals***, which may be used to determine whether the USB mode is selected. The pair of data signals (D+, D-) is a complementary pair in which one is at a high level when the other is at a low level." Lin, ¶38, Fig. 4A. Accordingly, Lin's "USB port" (pins and/or corresponding contact pads as shown in Figure 5) comprises multiple data pins and corresponding multiple data lines. Lin, Fig. 5.

c. Element 27[b]: wherein the first set of pins comprise multiple data pins connected to the multiple data lines; and

221. In my opinion, Lin teaches Element 27[b]. *See* Element 27[a], above.

d. Element 27[c]: wherein all of the multiple data pins are not electrically connected to the I/O controller circuitry.

222. In my opinion, Lin teaches Element 27[c]. Specifically, the pin assignment chart of Figure 4A, which I have annotated below, shows that "all of the multiple data pins" used for the USB port—*i.e.*, pins 14 and 15, as discussed

for Element 27[a]—are not used in the MMC 4.0 mode, which corresponds to the claimed "I/O port."

Pins electrically connected to MMC device controller

All of the "first set of pins of the USB port" are not electrically connected to MMC device controller (used in the MMC mode)

Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3	VSS1	VSS1	VSS1	VSS1
4	VDD	VDD	VDD	VDD
5	CLK	SCLK		CLK
6	VSS2	VSS2	VSS2	VSS2
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

FIG. 4A

Lin, Fig. 4A (annotated).

223. As discussed for Claim 26, since neither of the USB port's data pins 14 and 15 are used to transmit electrical signals in the MMC 4.0 mode, these ***"data pins are not electrically connected to"*** Lin's MMC device controller 34 pins (*i.e.*, the claimed "I/O controller circuity").

D. Ground 4: Claims 2 and 17 Are Obvious Over Lin in View of Thorsten

224. As shown below, in my opinion, the subject matter of Claims 2 and 17 are disclosed by Lin in view of Thorsten.

1. A POSITA would have been motivated to combine Lin with Thorsten with a reasonable expectation of success.

225. In my opinion, a POSITA would have been motivated to combine Lin with Thorsten and would have a reasonable expectation of success in doing so, because they are both from the same field and relate to the same well-known issues. Both references disclose memory cards, and external host devices that read data from, and write to, the memory. *Compare* Lin, ¶¶3, 8 *with* Thorsten, ¶3. Like Lin, Thorsten discloses a "memory card comprising a non-volatile memory 2," "a data interface 3 for connecting to a host," and "a controller 5." *E.g.*, Lin, ¶¶7-8, Figs. 1A-1C; Thorsten, ¶13, Fig. 1. A POSITA seeking to store sensitive data in encrypted form, in a manner compatible with different host applications, would have looked to each of these references for teachings of how to reliably store sensitive data.

226. Lin's memory card includes an interface (IF) mode detector, multiple controller circuits, and additional circuity, making it compatible for multiple application standards. *See* Lin, ¶¶ 8, 29, Figs. 1A-C. Lin is silent on the sensitivity of data to be stored in its memory card, or whether its memory card utilizes encryption or decryption.

227. As I discussed for Ground 2 (Section XII.B.1, *supra*), Thorsten's memory card incorporates a "logic component" (*e.g.*, a "programmable circuit") "that is responsible for the encryption and decryption process." Thorsten, ¶¶7, 10,

15, Fig. 1. In Thorsten's configuration, "the card itself handles the encryption and decryption, [so that] it is not necessary to know in advance which applications the memory card is to work with, and it is not necessary to ensure that these applications have the appropriate algorithms." Thorsten, ¶4; *see also* Section XII.B.1 (citing Thorsten, ¶¶8, 10, Fig. 1).

228. Accordingly, a POSITA would have understood and been motivated to incorporate, in Lin's multi-mode removable memory card, (Lin, Abstract, Figs. 1A-1C), data encryption and decryption functionality that is compatible with various host applications, by implementing Thorsten's logic component (*i.e.*, encryption and decryption circuitry) into its design, in order to reap Thorsten's disclosed benefits—*i.e.*, storing sensitive data while remaining compatible with various host applications. *See* Thorsten, ¶¶2-4.

229. Additionally, a POSITA would have had a reasonable expectation of success in achieving the collective objectives of Lin and Thorsten—*e.g.*, obtaining a multiple standard-compliant memory card that can store sensitive data while remaining compatible with various host applications—by combining their teachings with no change in their respective functions, since Lin and Thorsten disclose similar devices, and because Thorsten's encryption and decryption circuitry can be readily incorporated in to Lin's device to achieve predictable results. Lin's memory card features ***two controllers*** (one for USB applications,

another for MMC applications) that "control[] data transfer between host 40 and application module 38" (*i.e.*, the memory storage). Lin, ¶¶31, 33, Figs. 1A, 1C. Thorsten's memory card likewise features a "controller 5" that keys instructions to the logic component. Thorsten, ¶16. According to Thorsten, controller 5 either "connects [to] the logic component" via "third interface 13" as shown in Figure 1 (Thorsten, ¶14), or else "the logic component is designed as an additional module of [the] controller 5" (Thorsten, ¶17). Given that Thorsten teaches flexibility in implementation, a POSITA would have observed that the logic component could be readily implemented in Lin's memory card consistent with Thorsten's teachings, as I have illustrated by the below modification of Lin's Figure 2.[14]

[14] As with the Diggs-Thorsten Modification for Ground 2, the Lin-Thorsten Modification could be implemented slightly differently, where the logic component is situated between the controllers and the IF mode detector, which would still be consistent with the collective teachings of the references.

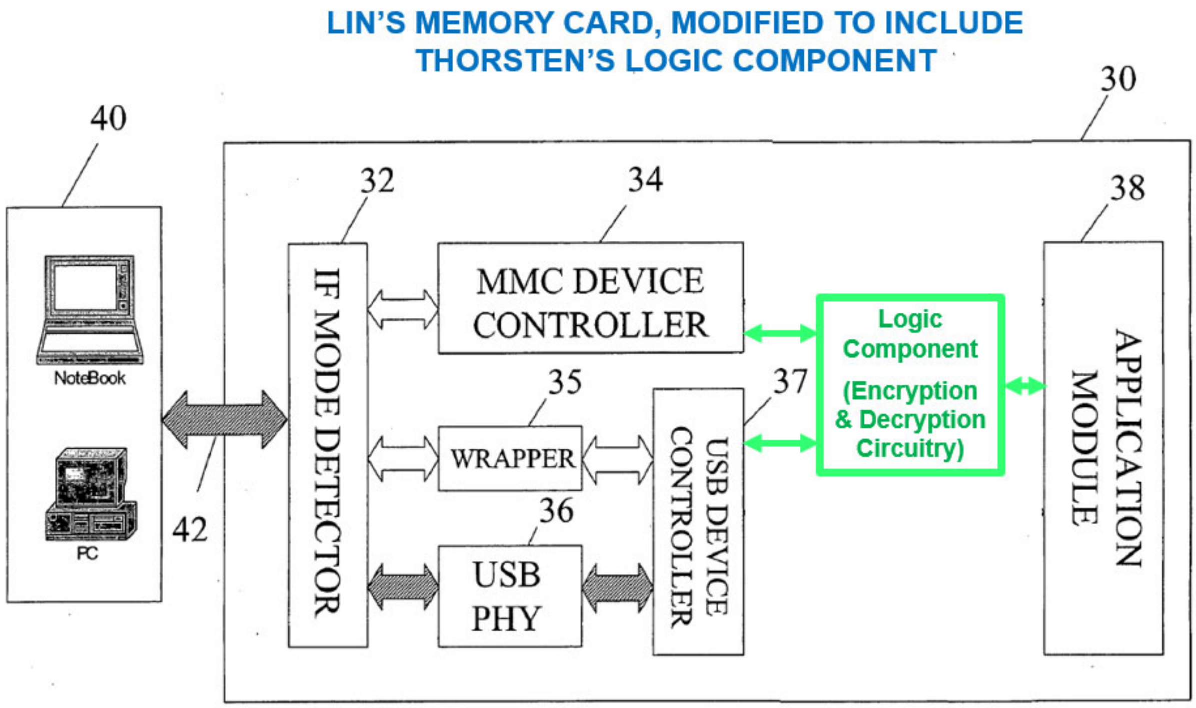

FIG. 1A

Modification of Lin, Fig. 1A (**"Lin-Thorsten Modification"**).

230. In such an implementation, encryption and decryption instructions are keyed into the logic component (*i.e.*, programmable circuitry), which "act under the instructions" of Lin's USB device controller or MMC device controller (depending on the host); "data to be transmitted … to [Lin's] memory … is encrypted in the logic component 6. [Subsequently,] [w]hen reading data from the memory card, data is transmitted from the memory … with decryption being performed by the logic component 6." *See* Thorsten, ¶15. Thus, improving Lin by implementing Thorsten's teachings would have constituted nothing more than the application of a known technique (*e.g.*, encryption and decryption circuity) to a

known device (*e.g.*, Lin's memory card) to obtain predictable results (*e.g.*, storing and retrieving sensitive data in a manner compliant with various host applications).

2. Claim 2: The portable handheld memory card of claim 1 further comprising: decryption circuitry in communication with the memory and configured to decrypt encrypted data stored in the memory.

231. In my opinion, Lin in view of Thorsten teaches Claim 2. As discussed in Ground 3, *supra*, Lin teaches the portable handheld memory card of Claim 1. *See* Section XII.C.1, *supra*.

232. For the reasons discussed in Section XII.D.1, *supra*, Lin-Thorsten includes "decryption circuitry"—*i.e.*, Thorsten's logic component (which I have annotated light green)—that is "in communication with the memory and configured to decrypt encrypted data stored in the memory."

3. Dependent Claim 17: The method of claim 16, wherein the data is encrypted data, and wherein the method further comprises: decrypting the encrypted data to decrypted data.

233. In my opinion, Lin in view of Thorsten teaches Claim 17. As discussed in Ground 3, *supra*, Lin teaches the method of Claim 16. *See* Section XII.A.7, *supra*.

234. As discussed for Section XII.D.1, *supra*, Lin-Thorsten teaches the additional requirement that "the data [to be read from the memory] is encrypted

data, and wherein the method further comprises decrypting the encrypted data to decrypted data."

XIII. CONCLUSION

235. For at least these reasons, Claims 1-2, 4-8, 16-17, 20-21, and 23-27 of the '051 Patent are invalid over the prior art.

236. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

237. I declare that all statements made herein of my knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

238. I declare under penalty of perjury that the foregoing is true and correct.

Respectfully Submitted,

May 30, 2025

R. Jacob Baker, Ph.D., P.E.