

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION**

PALISADE TECHNOLOGIES, LLP,

Plaintiff

v.

MICRON TECHNOLOGY, INC. and
MICRON SEMICONDUCTOR
PRODUCTS, INC.,

Defendants.

Case No. 7:24-cv-00262-DC-DTG

Jury Trial Demanded

**DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS FOR
U.S. PATENT NOS. 8,148,962; 8,327,051; AND 9,281,314**

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I. Introduction

Defendants Micron Technology, Inc. and Micron Semiconductor Products, Inc. (collectively, “Defendants” or “Micron”) submit its Preliminary Invalidity Contentions for U.S. Patent Nos. 8,148,962; 8,327,051; and 9,281,314 (“Invalidity Contentions”) to Plaintiff Palisade Technologies, LLP (“Plaintiff” or “Palisade”) pursuant to the Court’s Order Governing Proceedings in Patent Cases.¹

In Plaintiff’s Preliminary Infringement Contentions (“Infringement Contentions”), served April 16, 2025, Plaintiff asserted the following claims of each patent against Micron.

U.S. Patent No.	Asserted Claim(s)
8,148,962	1, 7-11, 14
8,327,051	1-2, 4-6, 8, 16-17, 21, 23-25, 27
9,281,314	1, 3, 5-6, 13, 17-18

Micron’s Invalidity Contentions address only those claims asserted in Plaintiff’s Infringement Contentions. Micron provides these Invalidity Contentions without waiving any argument about the sufficiency or substance of Plaintiff’s Infringement Contentions.

Based on its investigation to date, Micron hereby: (a) identifies each item of prior art that anticipates each asserted claim or renders it obvious; (b) specifies whether each such item of prior art anticipates each asserted claim or renders it obvious and, if a combination of items of

¹ On May 14, 2025, the Court granted Defendants’ unopposed motion to extend the service deadline for invalidity contentions for U.S. Patent Nos. 8,996,838 and 9,524,974 to July 3, 2025. ECF No. 48.

prior art makes a claim obvious, identifies each such combination and the motivation to combine such items; (c) provides a chart identifying where specifically in each item of prior art each element of each asserted claim is found, including for each element that is governed by pre-AIA 35 U.S.C. § 112 ¶ 6 and/or 35 U.S.C. § 112(f), the identity of the structure(s), act(s), or material(s) in each item of prior art that performs the claimed function; (d) identifies any grounds of invalidity of the asserted claims based on indefiniteness under pre-AIA 35 U.S.C. § 112 ¶ 2 and/or 35 U.S.C. § 112(b), or enablement or written description under pre-AIA 35 U.S.C. § 112 ¶ 1 and/or 35 U.S.C. § 112(a); and (e) identifies any grounds of invalidity of the asserted claims directed to ineligible subject matter under 35 U.S.C. § 101.

In addition, based on its investigation to date, Micron has produced or is producing documents concurrently with these Invalidity Contentions.

II. Reservations

Defendants reserve the right to amend these Invalidity Contentions. The information and documents that Defendants produce are based on information available to date and are subject to further revision.

The information and documents that Defendants produce are based on Defendants' present understanding of Plaintiff's infringement theories as advanced by Plaintiff in its Infringement Contentions. Plaintiff's Infringement Contentions are deficient in numerous respects. For example, although Plaintiff lists hundreds of product models as accused products in its Infringement Contentions, the accompanying claim charts include analysis for only four models. Thus, Plaintiff has failed to identify specifically where each element of each asserted claim is found within each accused instrumentality. If Plaintiff attempts or is permitted to cure such deficiencies, amends its contentions, or provides additional information regarding its

infringement theories, doing so may lead to further grounds for invalidity, and thus Defendants specifically reserve the right to amend or supplement its Invalidity Contentions.

Further, because discovery (including third-party discovery) is at an early stage, Defendants reserve the right to amend or supplement these Invalidity Contentions. For example, Plaintiff has not produced prior art known to it, including information regarding any known prior art products. As discovery proceeds, Defendants may serve subpoenas on third parties believed to have knowledge, documentation, or corroborating evidence relating to invalidity and/or prior art. It is therefore likely that Defendants will discover additional prior art or additional information relating to known prior art, and Defendants reserve the right to supplement these contentions after becoming aware of additional prior art or information. Defendants further reserve the right to introduce and use such supplemental materials at trial.

Defendants' claim charts attached to these Invalidity Contentions cite particular teachings and disclosures of the prior art as applied to limitations of the asserted claims. However, persons having ordinary skill in the art may view an item of prior art generally in the context of other publications, literature, products, and understanding. Accordingly, the cited portions are only exemplary, and Defendants reserve the right to rely on uncited portions of the prior art references and on other publications and expert testimony as aids in understanding and interpreting the cited portions, as providing context thereto, and as additional evidence that a claim limitation is known or disclosed. Defendants reserve the right to establish what was known to a person having ordinary skill in the art through other publications, products, or testimony. Defendants also reserve the right to rely on uncited portions of the prior art references, other publications, and testimony to establish that a person of skill in the art would have been motivated to combine

certain of the cited references so as to render the claims obvious. Citations to figures are inclusive of all discussions of those figures.

Defendants further reserve the right to argue that the asserted claims are invalid under pre-AIA 35 U.S.C. § 102(f) and/or 35 U.S.C §§ 101, 115(a)–(b) if discovery reveals that the named inventor of the Asserted Patents did not invent the subject matter recited in the asserted claims. If Defendants assert invalidity based on inventorship, Defendants will provide the name of the person(s) from whom, and the circumstances under which, the invention or any part of it was derived.

Defendants further intend to rely on inventor admissions concerning the scope of the asserted claims or of the prior art relevant to the asserted claims found in, *inter alia*, the patent prosecution history and/or reexamination history for each of the Asserted Patents and related patents or patent applications; any deposition testimony of a named inventor of the Asserted Patents; and the papers filed and any evidence submitted by Plaintiff in conjunction with this litigation. Defendants reserve the right to contend that the asserted claims are invalid for failure to name the correct inventor(s), or to contend that Plaintiff lacks standing to bring this litigation with respect to such patents.

Furthermore, nothing stated herein shall be treated as an admission or suggestion that Defendants agree with Plaintiff regarding the scope of any asserted claim or the claim constructions in its Infringement Contentions. To the extent that Defendants' Invalidity Contentions reflect claim constructions consistent with or suggested by Plaintiff's Infringement Contentions, no inference is intended nor should any be drawn that Defendants agree with Plaintiff's claim constructions. By applying any of Plaintiff's apparent claim constructions and interpretations, Defendants do not concede in any way that those constructions and

interpretations are correct, but rather assert the fundamental principle that whatever infringes a claim if later in time anticipates if earlier in time. Defendants expressly reserve the right to propose alternative constructions to those that have been or may be advocated by Plaintiff.

Nor shall anything in these Invalidity Contentions be treated as an admission that Defendants' accused products meet any limitation of any asserted claim. Defendants deny that they infringe any claim of the Asserted Patents. To the extent that any prior art contains a claim element that is the same as or similar to an accused product, inclusion of that prior art in Defendants' Invalidity Contentions shall not be deemed a waiver by Defendants of any claim construction or non-infringement position. Defendants expressly reserve the right to contest any claim construction asserted by Plaintiff and expressly reserve all non-infringement arguments.

In its Infringement Contentions, Plaintiff contends that the asserted claims of the Asserted Patents are entitled to the following priority dates.

U.S. Patent No.	Priority Dates
8,148,962	May 12, 2009
8,327,051	Nov. 20, 2007
9,281,314	October 10, 2014

Defendants reserve the right to challenge Plaintiff's alleged priority dates.² Defendants further reserve the right to seek discovery regarding conception and reduction to practice, as appropriate, and to demonstrate earlier invention by other parties under 35 U.S.C. § 102(g), public use or the

² Based on these priority dates, Defendants have applied pre-AIA 35 U.S.C. to the '962 and '051 Patents and post-AIA 35 U.S.C. to the '314 Patent. Throughout these contentions, any citations to either pre-AIA or post-AIA 35 U.S.C. also refer to their corollary, as appropriate.

on-sale bar under 35 U.S.C. § 102(b), or applicants’ failure to comply with 35 U.S.C. § 112. In addition, Defendants rely on Plaintiff’s alleged priority dates in forming these Invalidity Contentions, and to the extent Plaintiff later argues, or it is determined that, any different priority date applies, Defendants reserve the right to amend these Contentions accordingly.

III. U.S. Patent No. 8,148,962 (“’962 Patent”)

A. Invalidity Contentions Under 35 U.S.C. §§ 102 And 103

1. Identification of Prior Art

In addition to the prior art cited on the face of the ’962 Patent and related patents, the admitted prior art in the specifications of the ’962 Patent and related patents, the prior art cited in any file histories, reexaminations, *inter partes* review proceedings, reissue proceedings, or other examination or post-grant proceedings of the ’962 Patent and related patents, and the prior art cited in any invalidity contentions or expert reports submitted in any action or proceedings involving the ’962 Patent or related patents, Defendants identify the following prior art that anticipates each asserted claim or renders it obvious.

a) Prior Art Patents

The following patents and patent publications are prior art to the asserted claims under at least pre-AIA 35 U.S.C. §§ 102(a), (b), (e), and/or (g) and/or pre-AIA 35 U.S.C. § 103. The identification of any patent or patent publication shall be deemed to include any counterpart patent or application filed, published, or issued anywhere in the world.

Patent or Publication Number	Country of Origin	Filing Date	Date of Issue or Publication
U.S. Patent App. Pub. No. 2009/0224737 (“Lou”)	U.S.	3/7/2008	9/10/2009
U.S. Patent App. Pub. No. 2010/0176875 (“Pulijala”)	U.S.	1/14/2009	7/15/2010
U.S. Patent No. 7,151,363 (“Scott”)	U.S.	6/8/2004	12/19/2006

Patent or Publication Number	Country of Origin	Filing Date	Date of Issue or Publication
U.S. Patent No. 6,642,778 ("Opris")	U.S.	2/27/2003	11/4/2003
U.S. Patent No. 6,157,176 ("Pulvirenti")	U.S.	7/13/1998	12/5/2000
U.S. Patent App. Pub. No. 2003/0102851 ("Stanescu")	U.S.	1/10/2003	6/5/2003
U.S. Patent No. 8,044,653 ("Maige")	U.S.	6/4/2007	10/25/2011
U.S. Patent No. 8,080,984 ("Geynet")	U.S.	5/21/2008	12/20/2011
U.S. Patent App. Pub. No. 2006/0197513 ("Tang")	U.S.	6/30/2005	9/7/2006
U.S. Patent No. 7,262,586 ("Gradinariu")	U.S.	03/31/2005	08/28/2007
U.S. Patent App. Pub. No. 2003/0155964 ("Gauthier")	U.S.	02/19/2002	08/21/2003
U.S. Patent App. Pub. No. 2007/0290665 ("Moraveji")	U.S.	06/15/2006	12/20/2007
U.S. Patent App. Pub. No. 2008/0136398 ("Nakashimo")	U.S.	11/05/2007	06/12/2008
U.S. Patent No. 4,158,804 ("Butler")	U.S.	08/10/1977	06/19/1979
U.S. Patent No. 6,188,212 ("Larson")	U.S.	04/28/2000	02/13/2001
U.S. Patent No. 5,867,015 ("Corsi")	U.S.	12/17/1997	02/02/1999
U.S. Patent App. Pub. No. 2002/0130646 ("Zadeh")	U.S.	08/28/2001	09/19/2002
U.S. Patent 7,928,706 ("Do Couto")	U.S.	06/20/2008	04/19/2011
U.S. Patent No. 7,327,125 ("Benbrik")	U.S.	02/17/2005	02/05/2008
U.S. Patent App. Pub. No. 2007/0257644 ("McLeod")	U.S.	05/05/2006	11/08/2007
U.S. Patent No. 6,879,142 ("Chen")	U.S.	08/20/2003	04/12/2005
U.S. Patent App. Pub. No. 2008/0054861 ("Zlatkovic")	U.S.	09/06/2006	03/06/2008

Patent or Publication Number	Country of Origin	Filing Date	Date of Issue or Publication
U.S. Patent App. Pub. No. 2009/0179622 (“Ivanov”)	U.S.	01/11/2008	07/16/2009
U.S. Patent App. Pub. No. 2010/0109435 (“Ahmadi”)	U.S.	09/28/2009	05/06/2010
U.S. Patent App. Pub. No. 2008/0290934 (“Cho”)	U.S.	07/09/2008	11/27/2008
U.S. Patent App. Pub. No. 2007/0236190 (“Kruiskamp”)	U.S.	03/01/2007	10/11/2007
Japanese Patent App. Pub. No. JP2007-004581 (“Norikazu”)	JP	06/24/2005	01/11/2007
U.S. Patent No. 6,104,179 (“Yukawa”)	U.S.	07/21/1999	08/15/2000
Japanese Patent App. Pub. No. JP2002-258954 (“Koji”)	JP	03/05/2001	9/13/2002
Japanese Patent App. Pub. No. JP2004-62329 (“Masahiro”)	JP	07/25/2002	02/27/2004

b) Prior Art Systems

The following systems are prior art under at least 35 U.S.C. §§ 102(a), (b), and/or (g):

1. Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to Qimonda 512 MB DDR4 SGRAM, Device: IDGV51-05A1F1C-40X (“Qimonda DDR4”), as exemplified in the claim chart in Exhibit A9. As part of these Invalidity Contentions, Defendants have produced documents relating to Qimonda DDR4. Based on information available to Defendants, Defendants believes that Qimonda DDR4 was conceived and/or reduced to practice by engineers at Qimonda AG, at least by April 2008, without being abandoned, suppressed, or concealed, and it was in public use or on sale by the dates identified in the claim chart, which are no later than April 2008.
2. Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to Micron V48C SDRAM with QS (“Micron V48C”), as exemplified in the claim chart in Exhibit A10. As part of these Invalidity Contentions, Defendants have produced documents relating to Micron V48C. Based on information available to Defendants, Defendants believes that Micron V48C was conceived and/or reduced to practice by engineers at Micron, at least by September 2007, without being abandoned, suppressed, or concealed, and it was in public use or on sale by the dates identified in the claim chart, which are no later than September 2007.

3. Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to Micron DDR400 MT46V32M8TG-5B (“Micron DDR400”), as exemplified in the claim chart in Exhibit A11. As part of these Invalidity Contentions, Defendants have produced documents relating to Micron DDR400. Based on information available to Defendants, Defendants believes that Micron DDR400 was conceived and/or reduced to practice by engineers at Micron, at least by March 2004, without being abandoned, suppressed, or concealed, and it was in public use or on sale by the dates identified in the claim chart, which are no later than March 2004.
4. Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to Micron V58B (“Micron V58B”), as exemplified in the claim chart in Exhibit A12. As part of these Invalidity Contentions, Defendants have produced documents relating to Micron V58B. Based on information available to Defendants, Defendants believes that Micron V58B was conceived and/or reduced to practice by engineers at Micron, at least by October 2008, without being abandoned, suppressed, or concealed, and it was in public use or on sale by the dates identified in the claim chart, which are no later than October 2008.
5. Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to Micron T48M (“Micron T48M”), as exemplified in the claim chart in Exhibit A13. As part of these Invalidity Contentions, Defendants have produced documents relating to Micron T48M. Based on information available to Defendants, Defendants believes that Micron T48M was conceived and/or reduced to practice by engineers at Micron, at least by June 2007, without being abandoned, suppressed, or concealed, and it was in public use or on sale by the dates identified in the claim chart, which are no later than June 2007.
6. Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to Richtek RT9193 300mA, Ultra-Low Noise, Ultra-Fast CMOS LDO Regulator (“Richtek RT9193”), as exemplified in the claim chart in Exhibit A14. As part of these Invalidity Contentions, Defendants have produced documents relating to Richtek RT9193. Based on information available to Defendants, Defendants believes that Richtek RT9193 was conceived and/or reduced to practice by engineers at Richtek, at least by June 2006, without being abandoned, suppressed, or concealed, and it was in public use or on sale by the dates identified in the claim chart, which are no later than June 2006.

Defendants’ investigation into publicly-available prior art systems that teach and/or render obvious each element of any asserted claims is ongoing. Fact discovery is at an early stage, and Defendants may require discovery from third parties regarding publicly-available prior

art systems. Defendants reserve the right to amend its identification of prior art systems as Defendants become aware of the existence, functionality, and/or characteristics of prior art systems as a result of their investigation and forthcoming discovery.

2. Primary References

Defendants contend that the primary prior art references identified below and described in the charts attached as Exhibits A1 to A22, by themselves, anticipate the asserted claims of the '962 Patent. To the extent that a primary reference is deemed not to anticipate a claim for failing to teach one or more limitations of that claim, Defendants contend that the claim would nonetheless have been obvious to a person of ordinary skill in the art at the time of the invention in view of the prior art reference itself and the knowledge of a person of ordinary skill in the art, as described in the attached charts. Defendants' prior art charts (attached as Exhibits A1 to A22) set forth the particular claims that are anticipated under 35 U.S.C. § 102 and/or rendered obvious under 35 U.S.C. § 103 by each item of prior art and identify where specifically in each item of prior art each element of each asserted claim is found.

Exhibit	Primary References
A1	U.S. Patent App. Pub. No. 2009/0224737 (“Lou”)
A2	U.S. Patent App. Pub. No. 2010/0176875 (“Pulijala”)
A3	U.S. Patent No. 7,151,363 (“Scott”)
A4	U.S. Patent App. Pub. No. 2009/0179622 (“Ivanov”)
A5	U.S. Patent No. 6,157,176 (“Pulvirenti”)
A6	U.S. Patent App. Pub. No. 2003/0102851 (“Stanescu”)
A7	U.S. Patent No. 8,044,653 (“Maige”)
A8	U.S. Patent No. 7,262,586 (“Gradinariu”)

Exhibit	Primary References
A9	Qimonda DDR4
A10	Micron V48C
A11	Micron DDR400
A12	Micron V58B
A13	Micron T48M
A14	Richtek RT9193
A15	U.S. Patent App. Pub. No. 2003/0155964 (“Gauthier”)
A16	U.S. Patent No. 6,188,212 (“Larson”)
A17	U.S. Patent App. Pub. No. 2002/0130646 (“Zadeh”)
A18	U.S. Patent 7,928,706 (“Do Couto”)
A19	U.S. Patent No. 7,327,125 (“Benbrik”)
A20	U.S. Patent App. Pub. No. 2007/0257644 (“McLeod”)
A21	U.S. Patent No. 6,879,142 (“Chen”)
A22	U.S. Patent App. Pub. No. 2008/0054861 (“Zlatkovic”)

3. Secondary References

Exhibit A-A lists secondary prior art references and identifies, on a limitation-by-limitation basis, where specifically each secondary reference teaches the limitations of the asserted claims. To the extent that a primary reference is deemed, by itself, not to anticipate or render obvious a claim for failing to teach one or more limitations, the claim would nonetheless have been obvious to a person of ordinary skill in the art at the time of the invention by the combination of the primary reference with one or more of the other primary references listed above and/or the references listed as disclosing those alleged missing limitations in Exhibit A-A.

4. Obvious Combinations

To the extent that a primary reference is deemed, by itself, not to anticipate or render obvious a claim for failing to teach one or more limitations, the claim would nonetheless have been obvious to a person of ordinary skill in the art at the time of the invention by the combination of the primary reference with one or more other primary references and/or the knowledge of someone skilled in the art. For example, a person of ordinary skill in the art would have been motivated to combine any reference in Exhibits A1 to A22 with any other reference(s) in Exhibits A1 to A22 and A-A. Such combinations would be achieved, for example, by merely combining the disclosures described in the respective claim charts for each reference.

Defendants also contend that any of the primary references (or combination of primary references) could be combined with any of the secondary references (or combination of secondary references) in Exhibit A-A to render obvious the asserted claims. Such combinations would be achieved by merely combining the disclosures described in the respective claim charts for each reference.

The obviousness combinations are provided in the alternative to Defendants' anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not itself anticipatory.

a) Exemplary Combinations

Below are examples of prior art references that would have been combined by one of ordinary skill in the art at the time of the alleged invention. These combinations are merely examples. The asserted claims of the '962 Patent are rendered obvious by:

- Lou alone or in combination with one or more of Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler,

Corsi, Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Lou and Lou in view of one of the following: Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Grandinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Pulijala alone or in combination with one or more of Lou, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler,

Corsi, Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Pulijala and Pulijala in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Gradinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Scott alone or in combination with one or more of Lou, Pulijala, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler,

Corsi, Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Scott and Scott in view of one of the following: Lou; Pulijala; Pulvirenti; Stanescu; Maige; Grandinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Ivanov alone or in combination with one or more of Lou, Pulijala, Scott, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler,

Corsi, Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Lou and Lou in view of one of the following: Lou; Pulijala; Scott; Pulvirenti; Stanescu; Maige; Grandinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, or Benbrik.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Pulvirenti alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler,

Corsi, Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Pulvirenti and Pulvirenti in view of one of the following: Lou; Pulijala; Scott; Ivanov; Stanescu; Maige; Gradinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Stanescu alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler, Corsi,

Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Stanescu and Stanescu in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Maige; Gradinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Maige alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler, Corsi,

Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Maige and Maige in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Grandinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Gradinariu alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler,

Corsi, Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Gradinariu and Gradinariu in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Gauthier alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler, Corsi,

Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Gauthier and Gauthier in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Gradinariu; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Zadeh, Tang; Geynet.
- Larson alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler, Corsi,

Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Larson and Larson in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Gradinariu; Gauthier; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Zadeh alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler, Corsi,

Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Zadeh and Zadeh in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Gradinariu; Gauthier; Larson; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier, Tang; Geynet.
- Do Couto alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler,

Corsi, Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Do Couto and Do Couto in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Gradinariu; Gauthier; Larson; Zadeh; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Gauthier; Zadeh, Tang; Geynet.
- Benbrik alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler, Corsi,

Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Benbrik and Benbrik in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Gradinariu; Gauthier; Larson; Zadeh; Do Couto; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- McLeod alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler, Corsi,

Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over McLeod and McLeod in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Gradinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Chen alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler, Corsi,

Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Chen and Chen in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Gradinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Lou; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Zlatkovic alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Opris, Geynet, Tang, Nakashimo, Butler, Corsi,

Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Zlatkovic and Zlatkovic in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Gradinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Qimonda DDR4 alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo,

Butler, Corsi, Kruiskamp, Masahiro, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Qimonda DDR4 and Qimonda DDR4 in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Gradinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, or Micron V58B.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Micron V48C alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo,

Butler, Corsi, Kruiskamp, Masahiro, Qimonda DDR4, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Micron V48C and Micron V48C in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Grandinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Micron DDR 400 alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo,

Butler, Corsi, Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Micron DDR 400 and Micron DDR 400 in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Grandinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron T48M; Micron V48B; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Micron V58B alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo,

Butler, Corsi, Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Micron V58B and Micron V58B in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Grandinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik, McLeod; Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; Micron T48M; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Micron T48M alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do

Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler, Corsi, Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, and Richtek RT9193. For example:

- Independent claims 1 and 14 are obvious over Micron T48M and Micron T48M in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Grandinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; and Richtek RT9193; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.
- Richtek RT9193 alone or in combination with one or more of Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do

Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler, Corsi, Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, and Micron T48M. For example:

- Independent claims 1 and 14 are obvious over Richtek RT9193 and Richtek RT9193 in view of one of the following: Lou; Pulijala; Scott; Ivanov; Pulvirenti; Stanescu; Maige; Grandinariu; Gauthier; Larson; Zadeh; Do Couto; Benbrik; McLeod, Chen; Zlatkovic; Opris; Geynet; Tang; Nakashimo; Butler; Corsi; Kruiskamp; Masahiro; Qimonda DDR4; Micron V48C; Micron DDR 400; Micron V58B; and Micron T48M; and any of the forgoing combinations further in view of Opris or Scott.
- Dependent claims 7, 8, and 9 are obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Pulvirenti; Geynet; Pulijala; Stanescu; Scott; Tang, Larson, Chen, Micron V48C, Micron V58B, or Qimonda DDR4.
- Dependent claims 10 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Pulijala; Geynet; Stanescu, Chen, Benbrik, or Ivanov.
- Dependent claim 11 is obvious over any of the obviousness grounds listed for independent claim 1 alone and/or further in view of: Lou; Pulijala; Ivanov; Stanescu; Maige; Benbrik; Do Couto; Gauthier; Zadeh, Tang; Geynet.

b) Motivations to Combine and Expectation of Success

To the extent a finder of fact finds that a primary prior art reference does not disclose one or more limitations of an asserted claim, the asserted claim is nevertheless obvious because the

alleged missing limitations contain nothing beyond ordinary improvements that would have been known or obvious to one of ordinary skill in the art. In other words, the claimed subject matter combines known elements to achieve predictable results or chooses between a finite number of clear alternatives known to those of skill in the art, particularly in view of the state of the art as reflected in the relevant prior art.

Moreover, as explained above, it would have been obvious to a person of skill in the art at the time of the alleged invention of the asserted claims to combine any primary reference with any combination of other primary references so as to practice the asserted claims. To the extent that Plaintiff argues that any concept claimed in the asserted claims is not disclosed in a primary reference, it would, at a minimum, have been obvious to adapt the primary reference to include the concept or combine it with other primary references that disclose the concept. Each concept described and claimed in the Asserted Patents was known to those of skill in the art as available design choices for semiconductor memory design and fabrication.

The Supreme Court has held that “[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). “When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.” *Id.* at 417. As the Supreme Court made clear, “[f]or the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *Id.*

To determine whether there is an apparent reason to combine the known elements in the fashion claimed by the patent at issue, a court can “look to interrelated teachings of multiple

patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art.” *Id.* at 418. For example, obviousness can be demonstrated by showing “there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent’s claims.” *Id.* at 420. “[A]ny need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” *Id.* Common sense also teaches that “familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.” *Id.*

However, the Supreme Court in *KSR* held that a claimed invention can be obvious even if there is no explicit teaching, suggestion, or motivation for combining the prior art to produce that invention. In summary, *KSR* holds that patents that are based on new combinations of elements or components already known in a technical field may be found to be obvious. *See, generally, KSR*, 550 U.S. 398. Specifically, the Court in *KSR* rejected a rigid application of the “teaching, suggestion, or motivation [to combine]” test. *Id.* at 418. “In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose of the patentee controls. What matters is the objective reach of the claim.” *Id.* at 419. “Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” *Id.* at 420. A key inquiry is whether the “improvement is more than the predictable use of prior art elements according to their established functions.” *Id.* at 417.

The rationale to combine or modify prior art references is significantly stronger when, as here, the references seek to solve the same problem, come from the same field, and correspond

well to each other. *In re Inland Steel Co.*, 265 F.3d 1354, 1362 (Fed. Cir. 2001). The Federal Circuit has held that two references may be combined as invalidating art under similar circumstances, namely “[the prior art] focus[es] on the same problem that the . . . patent addresses: enhancing the magnetic properties of . . . steel. Moreover, both [prior art references] come from the same field Finally, the solutions to the identified problems found in the two references correspond well.” *Id.* at 1364 (concerning patents and prior art relating to improving the magnetic and electrical properties of steel).

In view of the Supreme Court’s *KSR* decision, the PTO issued a set of Examination Guidelines. Examination Guidelines for Determining Obviousness Under 35 U.S.C. § 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex, Inc.*, 72 Fed. Reg. 57526 (October 10, 2007). Those Guidelines summarized the *KSR* decision and identified various rationales for finding a claim obvious, including those based on other precedents. Those rationales include:

(A) Combining prior art elements according to known methods to yield predictable results;

(B) Simple substitution of one known element for another to obtain predictable results;

(C) Use of known technique to improve similar devices (methods, or products) in the same way;

(D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) “Obvious to try” – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art;

(G) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Id. at 57529. The above rationales likewise apply in rendering obvious the asserted claims of the Asserted Patents.

The references disclosed herein, alone or in combination, contain an explicit and/or implicit teaching or motivation to combine them due to the following: (1) the knowledge generally available to a person of ordinary skill in the art; (2) the prior art references as understood by a person of ordinary skill in the art; (3) the nature of the problem to be solved; (4) the fact that each prior art reference addresses similar problems; and (5) the knowledge of those skilled in the art that the disclosed elements had been or could be used together.

As an example of those reasons and motivations to combine the references, Lou, Pulijala, Scott, Ivanov, Pulvirenti, Stanescu, Maige, Gradinariu, Gauthier, Larson, Zadeh, Do Couto, Benbrik, McLeod, Chen, Zlatkovic, Opris, Geynet, Tang, Nakashimo, Butler, Corsi, Kruiskamp, Masahiro, Qimonda DDR4, Micron V48C, Micron DDR 400, Micron V58B, Micron T48M, and Richtek RT9193 all generally relate to circuit design, and, in particular, voltage regulator design. *See, e.g.*, Lou at ¶2, Fig. 5, Pulijala at ¶8, Fig. 2, Scott at 1:14-23, Ivanov at ¶1, Pulvirenti at 1:7-9, Stanescu at ¶2, Maige at 1:44-55, Gradinariu at 1:11-19, Gauthier at Abstract, Larson at 1:7-14, Zadeh at ¶4, Do Couto at 1:6-8, Benbrik at 3:37-54, McLeod at ¶8, Chen at 2:16-27, Zlatkovic at ¶1, Opris at Abstract, Geynet at 2:40-61, Tang at ¶11, Nakashimo at ¶¶90-99, 118-125, Butler at 3:24-4:2, 4:27-57, Corsi at 1:29-2:21; Kruiskamp at ¶¶18, 38-44, 52-54, and Masahiro at ¶¶11-12, 14. *See also* product prior art circuit diagrams reproduced at Exs. A9-A14. The references disclose using similar components and techniques, such as the use of comparators, feedback loops, and current sources to regulate voltages at different parts of a circuit. *Id.* Thus, combining one or more such references merely involves combining prior art elements according to known methods to yield predictable results, the substitution of one known element for another

to obtain predictable results, the use of a known technique to improve similar devices in the same way, or applying a known technique to a known device ready for improvement to yield predictable results.

In addition, below are additional motivations to combine prior art for particular claim limitations. The following discussion of specific claim limitations merely provides examples, which are not limiting.

For example, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach limitations 1[c] (“a feedback circuit coupled to a first current path and including a feedback transistor, wherein said feedback circuit is constructed to maintain a voltage at a gate of said feedback transistor substantially constant”) and 14[d] (“feedback means for maintaining a voltage at a gate of a feedback transistor substantially constant”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses limitation 1[c]/14[d] in Exhibits A1 to A22 and A-A. For example, the charted prior art references explicitly describe or implicitly suggest a feedback circuit with a feedback transistor that maintains a substantially constant voltage. *See, e.g.*, Ex. Lou, ¶¶ 6-7, 9-10, 19, Figs. 1-5; Pulijala, ¶¶ 5-6, 8, 11, 19, 22, Fig. 2; Opris, 1:22-25, 2:59-3:13, 3:37-52, Figs. 1-5, Scott, 1:64-2:9, 3:24-5:25, Fig. 1; Stanescu, ¶¶4-6, 14, 35, 28, 80, 82, Fig. 3; McLeod, ¶¶4, 8, 10, 19, Fig. 1; Ivanov, ¶17, Figs. 1-2; Chen 2:16-27, 4:34-52, Fig. 7; Do Couto, 2:43-52, 3:23-60, 4:11-24; Zadeh, ¶¶6, 23-24, 46, 65, Fig. 2; Gradinariu, 2:10-24, 4:39-5:247:64-67, Fig. 3, Benbrik at 4:39-65, 5:31-55, 7:14-48, Figs. 2, 4. *See also* product prior art circuit diagrams reproduced at Exs. A9-A14. It would have been obvious to combine any primary reference with any these references or others in Exhibit A to satisfy limitation 1[c]/14[d]. A person skilled in the art would have recognized that having a

“feedback circuit coupled to a first current path and including a feedback transistor wherein said feedback circuit is constructed to maintain a voltage at a gate of said feedback transistor substantially constant” was a common, predictable design for a voltage regulator circuit. Further, a person of ordinary skill in the art would have recognized that including a such a feedback circuit has several benefits. For example, designing voltage regulator circuits using CMOS (complementary metal-oxide-semiconductor) technology (dates back to at least the 1980s and was the industry norm as of the alleged priority date of the '962 Patent. Similarly, using a feedback loop (including a feedback transistor) to compare an output voltage to a reference voltage was also common practice. A person of ordinary skill in the art would have recognized that implementing a current-supply circuit that supplies a current based on either another (more constant) current or on the feedback transistor's voltage would stabilize the output voltage. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would also have had a reasonable expectation of success given that, by the alleged priority date of the '962 Patent, millions of voltage regulator circuits were manufactured each year using components such as comparators to maintain a certain voltage.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach limitation 1[d] (“a first current supply circuit constructed to supply to a second current path a first current that is substantially constant”) or 14[e] (“first current supply means for supplying to a second current path referenced to said input a first current that is substantially constant”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art the discloses limitation 1[d]/14[e] in Exhibits A1 to 23 and A-A. For example, the charted prior art references explicitly

describe or implicitly suggest a first current supply circuit constructed to supply a first current that is substantially constant. *See, e.g.*, Tang, ¶¶6, 19-20, 22, 29-30, Fig. 2; Pulijala at ¶¶4, 8, 19-20, 22, Fig. 2; McLeod at ¶¶4, 8, 10, 19, Fig. 1; Ivanov at ¶17; Stanescu at ¶5, Fig. 3 Chen at 2:16-27, 4:34-52; Scott at 3:62-4:13, 5:39-52; Lou at ¶¶4, 9, 19; Kruiskamp at ¶¶18, 52-54; Geynet at 2:40-61, 4:41-58; Maige at 2:22-44; Corsi at 1:52-2:21; Pulvirenti at 2:1-19, 2:56-63, 3:11-26, Zlatkovic at ¶¶2, 10, 12. *See also* product prior art circuit diagrams reproduced at Exs. A9-A14. It would have been obvious to combine any primary reference with any of these references or others in Exhibit A to satisfy limitation 1[d]/14[e]. A person skilled in the art would have recognized that having a “a first current supply circuit constructed to supply to a second current path a first current that is substantially constant” was a common, predictable design for a voltage regulator circuit. Further, a person of ordinary skill in the art would have recognized that including a such a feedback circuit has several benefits. For example, by supplying a constant current, the voltage drop across the feedback circuit is stabilized leading to more predictable and accurate voltage reference behavior. Moreover, a constant current source has a high output impedance, which hallows the transistor to operate with ahigh intrinsic gain and additional temperature stability, resulting in higher accuracy, better loop regulation, and increased output voltage control. Similarly, a constant current will result in more predictability with respect to the voltage reference node and minimize noise in the feedback loop. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would have had a reasonable expectation of success given that, by the alleged priority date of the '962 patent, voltage regulators current supply circuits supplying a constant current were widely sold and used. A person of ordinary skill in the art would have understood that these references disclose

interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach limitations 1[e] (“a second current supply circuit coupled to said first current supply circuit, said gate of said feedback transistor, and said output of said voltage regulator circuit and constructed to supply a second current to said second current path with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit”) or 14[f] (“second current supply means coupled to said first current supply means, said gate of said feedback transistor, and said output of said voltage regulator circuit for receiving a first voltage reference and a second voltage reference and for supplying a second current to said second current path with a magnitude based on said first voltage reference and said second voltage reference”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses limitation 1[e]/14[f] in Exhibits A1 to A22 and A-A. For example, the charted prior art references explicitly describe or implicitly suggest maintaining current supply circuit that supplies a current to a current path based on the voltage of a gate of a feedback transistor and the output voltage of the voltage regulator circuit. *See, e.g.*, Lou, ¶¶ 7-10, 19, 24; Pulijala, ¶¶ 6, 8-11, 22; Tang at ¶¶7, 11, 19,-21; McLeod at ¶¶8, 10, 19; Ivanov at ¶17; Stanescu at ¶¶5-6, 14, 38, 82; Chen at 2:16-27, 4:34-52; Scott at 3:47-4:13; Do Couto at 1:45-56, 2:7-23; Kruiskamp at ¶¶18, 52-54; Gradinariu at 4:22-38, 6:45-51, 7:50-63; Zadeh at ¶¶23-24, 29, 37-38, 65, 66; Geynet at 2:40-61, 4:41-58, 5:15-35; Pulvirenti at 2:56-3:32; Benbrik at 4:39-65, 5:31-55; Gauthier at ¶¶17, 20-23, 25. *See also* product prior art circuit diagrams reproduced at Exs. A9-A14. It would have been obvious to combine any primary reference with any these references

or others in Exhibit A to satisfy limitation 1[e]/14[f]. A person skilled in the art would have recognized that having a “second current supply means coupled to said first current supply means, said gate of said feedback transistor, and said output of said voltage regulator circuit for receiving a first voltage reference and a second voltage reference and for supplying a second current to said second current path with a magnitude based on said first voltage reference and said second voltage reference;” was a common, predictable design for a voltage regulator circuit. Further, a person of ordinary skill in the art would have recognized that including a such a feedback circuit has several benefits. For example, a stable current source allows the amplifier to operate in its active region with good gain, allowing the amplifier to adjust the gate voltage of the pass transistor to maintain a stable V_{out} even under load changes and temperature drift. A person of ordinary skill would also have understood that this arrangement powers and provides stability to the internal reference and control circuitry. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would have had a reasonable expectation of success given that, by the alleged priority date of the '962 patent, voltage regulators with such second current supply circuits were widely sold and used. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach limitations 1[f] (“a pass device including a gate coupled to said second current path and adapted to receive a signal based on said current of said second current path and supply a load current to said load via said output of said voltage regulator circuit with a magnitude based

on said signal”) and 14[g] (“means for supplying current to said load for receiving a signal based on a magnitude of said first current and a magnitude of said second current and for supplying a load current to said load via said output of said voltage regulator circuit with a magnitude based on a magnitude of said signal;”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses this limitation in Exhibits A1 to A22 and A-A. For example, it was well known at the time that one way to supply a current based on the magnitude of an input signal is through the use of a differential amplifier and voltage divider. Several prior art references explicitly describe or implicitly suggest using components like these in a voltage regulator circuit to control the output voltage of the voltage regulator circuit. *See, e.g.*, Lou, ¶¶ 6, 19, 24; Pulijala, ¶¶ 6, 8-10, Tang at ¶¶6, 11, 19, 20; McLeod at ¶¶4, 8, 10, 18; Ivanov at ¶17; Sanescu at ¶¶6, 14, 39; Chen at 2:16-27, 4:34-52; Scott at 3:24-4:13; Do Couto at 3:61-67, 4:11-24, 4:33-67; Zadeh at ¶¶21, 23-24, 29, 43; Maige at 2:22-56; Corsi at 1:29-2:21; Benbrik at 5:31-38, 6:53-64, 9:41-52; Butler at 3:24-4:2, 4:27-57. *See also* product prior art circuit diagrams reproduced at Exs. A9-A14. It would have been obvious to combine any primary reference with any these references or others in Exhibit A to satisfy limitation 1[f]/14[g]. A person skilled in the art would have recognized that having a “a pass device including a gate coupled to said second current path and adapted to receive a signal based on said current of said second current path and supply a load current to said load via said output of said voltage regulator circuit with a magnitude based on said signal” was a common, predictable design for a voltage regulator circuit. Further, a person of ordinary skill in the art would have recognized that including a such a feedback circuit has several benefits. For example, by directly sensing or mirroring the load current, the regulator can anticipate and rapidly respond to changes in the load faster than waiting for the output voltage to dip and then

correcting it, which a person having ordinary skill in the art would have understood was particularly important in contexts where there are sudden changes in the load current by providing stability and constant output characteristics, even under varying load. In addition, current-mode feedback simplifies compensation, allowing for easier design of stable, high-bandwidth regulators. This arrangement also provides current limiting and protection if the current exceeds a threshold since the gate is pulled in a way that limits or shuts down output, protecting the circuit. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would have had a reasonable expectation of success given that, by the alleged priority date of the '962 patent, voltage regulators with such pass devices were widely sold and used. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach claim limitations 1[pre] (“voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load integrated in the IC under selectively variable load conditions”), 14[pre] (“voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load integrated in the IC under selectively variable load conditions”), 1[h] (“wherein said feedback circuit, said first current supply circuit, said second current supply circuit, and said pass device are integrated in an integrated circuit and referenced to said input of said voltage regulator circuit), 14[i] (“wherein said feedback means, said first current supply means, said second current supply means, and said means for supplying current to said load are integrated in an integrated circuit.”)

it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses these limitation in Exhibits A1 to A22 and A-A. For example, the charted prior art references explicitly describe or implicitly suggest a voltage regulator circuit integrated in an integrated circuit that provides a voltage to a load integrated into the integrated circuit. *See, e.g.*, Lou at ¶¶ 6-7, 9-10, 19, 24, Figs. 4-5; Pulijala at ¶¶ 4, 6, 19, 20-22, Figs. 1-3; Pulvirenti at 2:1-19, 2:42-49, 3:11-19, 4:17-22, Figs. 1-2; Scott at 1:14-23, Ivanov at ¶1, Stanescu at ¶2, Maige at 1:44-55, Gradinariu at 1:11-19, Gauthier at Abstract, Larson at 1:7-14, Zadeh at ¶4, Do Couto at 1:6-8, Benbrik at 3:37-54, McLeod at ¶8, Chen at 2:16-27, Zlatkovic at ¶1, Opris at Abstract, Geynet at 2:40-61, Tang at ¶11, Nakashimo at ¶¶90-99, 118-125, Butler at 3:24-4:2, 4:27-57, Corsi at 1:29-2:21; Kruiskamp at ¶¶18, 38-44, 52-54, and Masahiro at ¶¶11-12, 14. . *See also* product prior art circuit diagrams reproduced at Exs. A9-A14. A person skilled in the art would have understood that a voltage regulator's load connects to a circuit. A person skilled in the art would have known to integrate components of a voltage regulator circuit, such as a load, into an integrated circuit because doing so makes for a simpler circuit design and increases the circuit's reliability. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would also have had a reasonable expectation of success given that, by the alleged priority date of the '962 Patent, millions of voltage regulators were manufactured each year using feedback circuits and current supply circuits to stabilize an output voltage. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations. It

would have been obvious to combine any primary reference with any these references or others in Exhibit A to satisfy these limitations.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach claims 7 (“wherein said second current supply circuit further comprises at least one stability capacitor arrangement”) or 8 (“wherein said at least one stability capacitor arrangement has a capacitance of less than 30 pico-farads”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses claims 7 and 8 in Exhibits A1 to 23 and A-A. For example, the charted prior art references explicitly describe or implicitly suggest utilizing stability capacitors, including small sized capacitors, such as those with a capacitance of less than 30 pico-farads. *See, e.g.*, Tang at ¶¶27-30; Pulijala at ¶¶21-22, 24-26; Ivanov at ¶¶ 27, 33, 40; Stanescu at ¶¶15-16, 40, 82; Chen at 4:34-52, 6:66-7:37, 8:33-9:18; Scott at 3:62-4:33, 4:57-65; Larson at 2:36-50, 6:14-29, 6:48-62, 8:24-31, 10:35-44; Zlatkovic at ¶¶2, 12, 17; Gauthier at ¶¶20-22, 25. *See also* product prior art circuit diagrams reproduced at Exs. A9-A14. It would have been obvious to combine any primary reference with any these references or others in Exhibit A to satisfy claims 7 and 8. A person skilled in the art would have recognized that having a “second current supply circuit further comprises at least one stability capacitor arrangement” was a common, predictable design for a voltage regulator circuit. Further, a person of ordinary skill in the art would have recognized that including a such stability capacitors, including small stability capacitors has several benefits. For example, a person having ordinary skill in the art would have understood that many biasing circuits use high-impedance nodes (e.g. from current mirrors or bandgap references), which are prone to oscillation if not compensated and that a small capacitor adds a dominant pole that slows down fast transitions and prevents high-frequency instability.

Such a capacitor also helps filter out power supply noise or switching transients that could otherwise modulate the bias currents. Moreover, during power-up the current supply needs to stabilize quickly and predictably and a small capacitor helps smooth the voltage ramps and ensures monotonic startup without overshoot or latch-up. In particular, a small capacitor less than 30 pF allows the internal nodes to settle quickly, enabling fast bias stabilization and transient response. A small capacitor also avoids overcompensation, allowing just enough phase lead to stabilize without degrading speed. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would have had a reasonable expectation of success given that, by the alleged priority date of the '962 patent, voltage regulators utilizing stabilizing capacitors current were widely sold and used. Moreover, small capacitors are easily implemented on-chip using minimal die area thus supporting fully integrated regulators without requiring external compensation components. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach claims 9 (“wherein said load current has a magnitude that is at least one order of magnitude greater than a magnitude of a current of said second current path”) or 10 (“wherein said load current has a magnitude of less than one amp, and wherein said current of said second current path has a magnitude of less than one milli-amp”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses claims 9 and 10 in Exhibits A1 to 23 and A-A. For example, the charted prior art references explicitly describe or implicitly suggest a first current supply circuit

constructed to supply a first current that is substantially constant. *See, e.g.*, McLeod at ¶¶4, 8, 17; Ivanov at ¶¶8-9, 13, 21, 27, 40; Stanescu at ¶¶4, 37, 44, 62; Chen at ¶¶4:18-33, 5:22-47, 7:18-37; Scott at 3:47-4:13; Kruiskamp at ¶¶52-54, 56-58; Geynet at 4:59-67, 5:36-46, Maige at 4:21-33, 4:60-5:8, 6:32-39, Nakashimo at ¶¶90-99, Butler at 4:27-57. *See also* product prior art circuit diagrams reproduced at Exs. A9-A14 It would have been obvious to combine any primary reference with any these references or others in Exhibit A to satisfy claims 9 and 10. A person skilled in the art would have recognized that having the ability to handle both large and small load currents compared to the current on the second path was a common, predictable design principle for voltage regulator circuits at the time. Further, a person of ordinary skill in the art would have recognized that including the ability to handle a variety of load currents is a design choice and has several benefits. For example, having a load current an order of magnitude greater than the second current path supports high efficiency, precision control and system robustness by minimizing quiescent power consumption and simplifying compensation. On the other hand, a person having ordinary skill in the art would recognize that having both the load current and the second current path be under one milli-amp would be valuable in ultra-low-power regulators or precision analog circuits to keep the total regulator power consumption low and with reduced die area. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would have had a reasonable expectation of success given that, by the alleged priority date of the '962 patent, voltage adaptable to perform with a wide variety of load current magnitudes were widely sold and used. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations.

B. Invalidity Contentions Under 35 U.S.C. § 112

Defendants include below the grounds on which Defendants contend the asserted claims are invalid for failure to meet the requirements of the first two paragraphs of 35 U.S.C. § 112.

Plaintiff has not yet provided a claim construction for many of the terms and phrases that Defendants anticipate will be in dispute. Defendants, therefore, cannot provide a complete list of its § 112 defenses because Defendants do not know whether Plaintiff will proffer a construction for certain terms and phrases that is broader than, or inconsistent with, the construction that would be supportable by the disclosure set forth in the specification.

To the extent the following contentions reflect constructions of claim limitations consistent with or implicit in Plaintiff's Infringement Contentions, no inference is intended nor should any be drawn that Defendants agree with Plaintiff's claim constructions, and Defendants expressly reserve the right to contest such claim constructions. Defendants offer these contentions in response to Plaintiff's Infringement Contentions and without prejudice to any position it may ultimately take as to any claim construction issues.

Accordingly, Defendants reserve the right to amend or supplement these § 112 Invalidity Contentions as discovery progresses.

1. Indefiniteness Under 35 U.S.C. § 112, ¶ 2

35 U.S.C. § 112, ¶ 2 requires that a patent claim "particularly point[] out and distinctly claim[] the subject matter which the applicant regards as his invention." 35 U.S.C. § 112, ¶ 2. Claim terms that fail to inform those skilled in the art "with reasonable certainty . . . about the scope of the invention" fail the definiteness requirement of 35 U.S.C. § 112, ¶ 2. *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014).

Each of the asserted claims are invalid as indefinite under 35 U.S.C. § 112 because they fail to particularly point out and distinctly claim the subject matter which the applicant regards

as his invention. In particular, the following limitations, read in light of the intrinsic evidence, fail to inform those skilled in the art with reasonable certainty about the scope of the claimed inventions:

- Claims 1 and 14: “adapted to provide a voltage from a power supply to a load under varying load conditions”
- Claims 1 and 14: “an output adapted to be coupled to said load;”
- Claim 1: “a feedback circuit coupled to a first current path and including a feedback transistor, wherein said feedback circuit is constructed to maintain a voltage at a gate of said feedback transistor substantially constant;”
- Claim 1: “a first current supply circuit constructed to supply to a second current path a first current that is substantially constant;”
- Claim 1: “a second current supply circuit coupled to said first current supply circuit, said gate of said feedback transistor, and said output of said voltage regulator circuit and constructed to supply a second current to said second current path;”
- Claim 1: “a pass device including a gate coupled to said second current path and adapted to receive a signal based on said current of said second current path and supply a load current to said load via said output of said voltage regulator circuit with a magnitude based on said signal;”
- Claim 7: “second current supply circuit further comprises at least one stability capacitor arrangement”
- Claim 8: “wherein said at least one stability capacitor arrangement has a capacitance of less than 30 pico-farads.”

- Claim 9: “wherein said load current has a magnitude that is at least one order of magnitude greater than a magnitude of a current of said second current path.”
- Claim 14: “adapted to provide a voltage from a power supply to a load integrated in the IC under selectively variable load conditions”
- Claim 14: “feedback means for maintaining a voltage at a gate of a feedback transistor substantially constant;”
- Claim 14: “ first current supply means for supplying to a second current path referenced to said input a first current that is substantially constant;”
- Claim 14: “second current supply means coupled to said first current supply means”
- Claim 14: “means for supplying current to said load for receiving a signal based on a magnitude of said first current and a magnitude of said second current and for supplying a load current to said load via said output of said voltage regulator circuit with a magnitude based on a magnitude of said signal;”
- Claim 14: “said means for supplying current to said load are integrated in an integrated circuit.”

2. Lack of Enablement/Lack of Written Description Under 35 U.S.C. § 112, ¶ 1

The asserted claims of the '962 Patent are further invalid under 35 U.S.C. § 112, ¶ 1 because the specifications do not contain an adequate written description of the subject matter of these claims and would not enable one of skill in the relevant art to make and use the alleged invention.

For a claim to be valid, the specification must contain a written description of the invention. 35 U.S.C. § 112, ¶ 1. To fulfill the written description requirement, it “must clearly allow persons of ordinary skill in the art to recognize that the inventor invented what is claimed.”

Ariad Pharm., Inc. v. Eli Lilly & Co., 598 F.3d 1336, 1351 (Fed. Cir. 2010) (citation and internal quotation marks omitted). “[T]he applicant must ‘convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,’ and demonstrate that by disclosure in the specification of the patent.” *Carnegie Mellon Univ. v. Hoffmann-La Roche Inc.*, 541 F.3d 1115, 1122 (Fed. Cir. 2008) (quoting *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563–64 (Fed. Cir. 1991)).

The specification must also describe “the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains . . . to make and use the” invention. *Ariad*, 598 F.3d at 1343; *see also* 35 U.S.C. § 112 ¶ 1. “The enablement requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation.” *AK Steel Corp. v. Sollac & Ugine*, 344 F.3d 1234, 1244 (Fed. Cir. 2003) (citation omitted). “[T]he scope of the claims must be less than or equal to the scope of the enablement.” *Nat’l Recovery Tech., Inc. v. Magnetic Separation Sys., Inc.*, 166 F.3d 1190, 1196 (Fed. Cir. 1999).

Each of the asserted claims below are invalid because the specifications fail to provide written description and/or an enabling disclosure of at least the following limitations:

- Claim 1: “a feedback circuit coupled to a first current path and including a feedback transistor, wherein said feedback circuit is constructed to maintain a voltage at a gate of said feedback transistor substantially constant;”
- Claim 1: “a first current supply circuit constructed to supply to a second current path a first current that is substantially constant;”

- Claim 1: “a second current supply circuit coupled to said first current supply circuit, said gate of said feedback transistor, and said output of said voltage regulator circuit and constructed to supply a second current to said second current path;”
- Claim 14: “feedback means for maintaining a voltage at a gate of a feedback transistor substantially constant;”
- Claim 14: “ first current supply means for supplying to a second current path referenced to said input a first current that is substantially constant;”
- Claim 14: “second current supply means coupled to said first current supply means”
- Claim 14: “means for supplying current to said load for receiving a signal based on a magnitude of said first current and a magnitude of said second current and for supplying a load current to said load via said output of said voltage regulator circuit with a magnitude based on a magnitude of said signal;”
- Claim 14: “said means for supplying current to said load are integrated in an integrated circuit.”
- Claim 1: “a pass device including a gate coupled to said second current path and adapted to receive a signal based on said current of said second current path and supply a load current to said load via said output of said voltage regulator circuit with a magnitude based on said signal;”
- Claim 1: “wherein said second current supply circuit is adapted to, via said pass device, cause an increase in magnitude of said load current supplied to said output if a voltage at said output decreases and cause a decrease in magnitude of said load current supplied to said output if a voltage at said output increases;”

IV. U.S. Patent No. 8,327,051 (“’051 Patent”)

A. Invalidity Contentions Under Pre-AIA 35 U.S.C. §§ 102 And 103

1. Identification of Prior Art

In addition to the prior art cited on the face of the ’051 Patent and related patents, the admitted prior art in the specifications of the ’051 Patent and related patents, the prior art cited in any file histories, reexaminations, *inter partes* review proceedings, reissue proceedings, or other examination or post-grant proceedings of the ’051 Patent and related patents, and the prior art cited in any invalidity contentions or expert reports submitted in any action or proceedings involving the ’051 Patent or related patents, Defendants identify the following prior art that anticipates each asserted claim or renders it obvious.

a) Prior Art Patents

The following patents and patent publications are prior art to the asserted claims under at least pre-AIA 35 U.S.C. §§ 102(a), (b), (e), and/or (g) and/or pre-AIA 35 U.S.C. § 103. The identification of any patent or patent publication shall be deemed to include any counterpart patent or application filed, published, or issued anywhere in the world.

Patent or Publication Number	Country of Origin	Filing Date	Date of Issue or Publication
U.S. Patent App. Pub. No. 2004/0136224 (“Hamer”)	U.S.	9/5/2003	7/15/2004
U.S. Patent App. Pub. No. 2006/0053241 (“Lin ’241”)	U.S.	7/27/2005	3/9/2006
U.S. Patent App. Pub. No. 2005/0070157 (“Neo”)	U.S.	9/30/2003	3/31/2005
U.S. Patent App. Pub. No. 2009/0031073 (“Diggs”)	U.S.	7/26/2007	1/29/2009
U.S. Patent App. Pub. No. 2007/0083683 (“Lin ’683”)	U.S.	10/6/2005	4/12/2007
U.S. Patent App. Pub. No. 2007/0263473 (“Raines”)	U.S.	5/14/2007	11/15/2007

Patent or Publication Number	Country of Origin	Filing Date	Date of Issue or Publication
U.S. Patent No. 8,073,985 ("Ni")	U.S.	9/28/2007	12/6/2011
German Patent App. No. DE 102 20 629 ("Boeker")	Germany	8/5/2002	11/27/2003
U.S. Patent App. Pub. No. 2004/0182938 ("Chen '938")	U.S.	8/13/2003	9/23/2004
U.S. Patent App. Pub. No. 2004/0250010 ("Chen '010")	U.S.	10/16/2003	12/9/2004

b) Prior Art Systems

The following systems are prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b) and/or

(g):

1. Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to the Palm Tungsten T5 handheld storage ("Palm Tungsten T5"), as exemplified in the claim chart in Exhibit B6. As part of these Invalidity Contentions, Defendants have produced documents relating to the Palm Tungsten T5. Based on information available to Defendants, Defendants believes that Palm Tungsten T5 was conceived and/or reduced to practice by palmOne, including that identified in the claim chart and its cited publications, at least before October 2004, without being abandoned, suppressed, or concealed, and it was in public use or on sale by the dates identified in the claim chart, which are no later than October 2004.

2. Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to the Sony Network Walkman NW-MS77DR model ("Sony Walkman"), as exemplified in the claim chart in Exhibit B-A. As part of these Invalidity Contentions, Defendants have produced documents relating to the Sony Walkman. Based on information available to Defendants, Defendants believes that the Sony Walkman was conceived and/or reduced to practice by Sony, including that identified in the claim chart and its cited publications, at least before December 2004, without being abandoned, suppressed, or concealed, and it was in public use or on sale by the dates identified in the claim chart, which are no later than December 2004.

Defendants' investigation into publicly-available prior art systems that teach and/or render obvious each element of any asserted claims is ongoing. Fact discovery is at an early stage, and Defendants may require discovery from third parties regarding publicly-available prior

art systems. Defendants reserve the right to amend its identification of prior art systems as Defendants become aware of the existence, functionality, and/or characteristics of prior art systems as a result of their investigation and forthcoming discovery.

2. Primary References

Defendants contend that the primary prior art references identified below and described in the charts attached as Exhibits B1 to B6, by themselves, anticipate the asserted claims of the '051 Patent. To the extent that a primary reference is deemed not to anticipate a claim for failing to teach one or more limitations of that claim, Defendants contend that the claim would nonetheless have been obvious to a person of ordinary skill in the art at the time of the invention in view of the prior art reference itself and the knowledge of a person of ordinary skill in the art, as described in the attached charts. Defendants' prior art charts (attached as Exhibits B1 to B6) set forth the particular claims that are anticipated under 35 U.S.C. § 102 and/or rendered obvious under 35 U.S.C. § 103 by each item of prior art and identify where specifically in each item of prior art each element of each asserted claim is found.

Exhibit	Primary References
B1	U.S. Patent App. Pub. No. 2006/0053241 (“Lin ’241”)
B2	U.S. Patent App. Pub. No. 2009/0031073 (“Diggs”)
B3	U.S. Patent App. Pub. No. 2005/0070157 (“Neo”)
B4	U.S. Patent App. Pub. No. 2004/0182938 (“Chen ’938”)
B5	U.S. Patent App. Pub. No. 2004/0136224 (“Hamer”)
B6	Palm Tungsten T5

3. Secondary References

Exhibit B-A lists secondary prior art references and identifies, on a limitation-by-

limitation basis, where specifically each secondary reference teaches the limitations of the asserted claims. To the extent that a primary reference is deemed, by itself, not to anticipate or render obvious a claim for failing to teach one or more limitations, the claim would nonetheless have been obvious to a person of ordinary skill in the art at the time of the invention by the combination of the primary reference with one or more of the other primary references listed above and/or the references listed as disclosing those alleged missing limitations in Exhibit B-A.

4. Obvious Combinations

To the extent that a primary reference is deemed, by itself, not to anticipate or render obvious a claim for failing to teach one or more limitations, the claim would nonetheless have been obvious to a person of ordinary skill in the art at the time of the invention by the combination of the primary reference with one or more other primary references and/or the knowledge of someone skilled in the art. For example, a person of ordinary skill in the art would have been motivated to combine any reference in Exhibits B1 to B6 with any other reference(s) in Exhibits B1 to B6 and B-A. Such combinations would be achieved, for example, by merely combining the disclosures described in the respective claim charts for each reference.

Defendants also contend that any of the primary references (or combination of primary references) could be combined with any of the secondary references (or combination of secondary references) in Exhibit B-A to render obvious the asserted claims. Such combinations would be achieved by merely combining the disclosures described in the respective claim charts for each reference.

The obviousness combinations are provided in the alternative to Defendants' anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not itself anticipatory.

a) Exemplary Combinations

Below are examples of prior art references that would have been combined by one of ordinary skill in the art at the time of the alleged invention. These combinations are merely examples. The asserted claims of the '051 Patent are rendered obvious by:

- Lin '241 alone or in combination with one or more of Diggs, Neo, Chen '938, Hamer, the Palm Tungsten T5, Boeker, Raines, Ni, Lin '683, and the Sony Walkman. For example:
 - Independent claims 1 and 16 are obvious over Lin '241; Lin '241 in view of Diggs; Lin '241 in view of Neo; Lin '241 in view of Chen '938; Lin '241 in view of Hamer; Lin '241 in view of the Palm Tungsten T5; Lin '241 in view of Raines; Lin '241 in view of Ni; Lin '241 in view of Line '683; and Lin '241 in view of the Sony Walkman.
 - Dependent claims 2 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Boeker.
 - Dependent claim 4 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Diggs; Boeker; Chen '938; Ni; and/or Neo.
 - Dependent claim 5 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Diggs; Boeker; Chen '938; Ni; Neo; Hamer; and/or Lin '683.

- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Diggs; Boeker; Chen '938; Ni; Hamer; and/or Lin '683.
- Dependent claims 8 and 21 are obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Boeker; Diggs; Ni; and/or Lin '683.
- Dependent claim 23 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Diggs; Boeker; Neo; Hamer; and/or Lin '683.
- Dependent claim 24 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Diggs; Boeker; Raines; Chen '938; Ni; Neo; the Palm Tungsten T5; Hamer; Lin '683; and/or the Sony Walkman.
- Dependent claim 25 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Diggs; Neo; Chen '938; Hamer; the Palm Tungsten T5; Raines; Ni; Lin '683; and/or the Sony Walkman.
- Dependent claim 27 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Diggs; Chen '938; Ni; and/or Neo.
- Diggs alone or in combination with one or more of Lin '241, Diggs, Neo, Chen '938, Hamer, the Palm Tungsten T5, Boeker, Raines, Ni, Lin '683, and the Sony Walkman. For example:

- Independent claims 1 and 16 are obvious over Diggs; Diggs in view of Lin '241; Diggs in view of Neo; Diggs in view of Chen '938; Diggs in view of Hamer; Diggs in view of the Palm Tungsten T5; Diggs in view of Raines; Diggs in view of Ni; Diggs in view of Lin '683; and Diggs in view of the Sony Walkman.
- Dependent claims 2 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Boeker.
- Dependent claim 4 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Boeker; Chen '938; Ni; and/or Neo.
- Dependent claim 5 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Boeker; Chen '938; Ni; Neo; Hamer; and/or Lin '683.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Boeker; Chen '938; Ni; Hamer; and/or Lin '683.
- Dependent claims 8 and 21 are obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Boeker; Ni; and/or Diggs in view of Lin '683.
- Dependent claim 23 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Boeker; Neo; Hamer; and/or Lin '683.

- Dependent claim 24 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Boeker; Raines; Chen '938; Ni; Neo; the Palm Tungsten T5; Hamer; Lin '683; and/or the Sony Walkman.
- Dependent claim 25 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Neo; Chen '938; Hamer; the Palm Tungsten T5; Raines; Ni; Lin '683; and/or the Sony Walkman.
- Dependent claim 27 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Chen '938; Ni; and/or Neo.
- Neo alone or in combination with one or more of Lin '241, Diggs, Neo, Chen '938, Hamer, the Palm Tungsten T5, Boeker, Raines, Ni, Lin '683, and the Sony Walkman. For example:
 - Independent claims 1 and 16 are obvious over Neo; Neo in view of Lin '241; Neo in view of Diggs; Neo in view of Chen '938; Neo in view of Hamer; Neo in view of the Palm Tungsten T5; Neo in view of Raines; Neo in view of Ni; Neo in view of Lin '683; and Neo in view of the Sony Walkman.
 - Dependent claims 2 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Boeker.

- Dependent claim 4 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Neo Chen '938; and/or Ni.
- Dependent claim 5 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Chen '938; Ni; Hamer; and/or Lin '683.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Chen '938; Ni; Hamer; and/or Lin '683.
- Dependent claims 8 and 21 are obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Boeker; Diggs; Ni; and/or Lin '683.
- Dependent claim 23 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Hamer; and/or Lin '683.
- Dependent claim 24 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Raines; Chen '938; Ni; the Palm Tungsten T5; Hamer; Lin '683; and/or the Sony Walkman.
- Dependent claim 25 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Chen '938; Hamer; the Palm Tungsten T5; Raines; Ni; Lin '683; and/or the Sony Walkman.

- Dependent claim 27 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Chen '938; and/or Ni.
- Chen '938 alone or in combination with one or more of Lin '241, Diggs, Neo, Chen '938, Hamer, the Palm Tungsten T5, Boeker, Raines, Ni, Lin '683, and the Sony Walkman. For example:
 - Independent claims 1 and 16 are obvious over Chen '938; Chen '938 in view of Lin '241; Chen '938 in view of Diggs; Chen '938 in view of Neo; Chen '938 in view of Hamer; Chen '938 in view of the Palm Tungsten T5; Chen '938 in view of Raines; Chen '938 in view of Ni; Chen '938 in view of Lin '683; and Chen '938 in view of the Sony Walkman.
 - Dependent claims 2 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Boeker.
 - Dependent claim 4 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Ni; and/or Neo.
 - Dependent claim 5 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Ni; Neo; Hamer; and/or Lin '683.
 - Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Ni; Hamer; and/or Lin '683.

- Dependent claims 8 and 21 are obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Boeker; Diggs; Ni; and/or Lin '683.
- Dependent claim 23 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Neo; Hamer; and/or Lin '683.
- Dependent claim 24 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Raines; Ni; Neo; the Palm Tungsten T5; Hamer; Lin '683; and/or the Sony Walkman.
- Dependent claim 25 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Neo; Hamer; the Palm Tungsten T5; Raines; Ni; Lin '683; and/or the Sony Walkman.
- Dependent claim 27 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Ni; and/or Neo.
- Hamer alone or in combination with one or more of Lin '241, Diggs, Neo, Chen '938, Hamer, the Palm Tungsten T5, Boeker, Raines, Ni, Lin '683, and the Sony Walkman. For example:
 - Independent claims 1 and 16 are obvious over Hamer; Hamer in view of Lin '241; Hamer in view of Diggs; Hamer in view of Neo; Hamer in view of Chen '938; Hamer in view of the Palm Tungsten T5; Hamer in view of

Raines; Hamer in view of Ni; Hamer in view of Lin '683; and Hamer in view of the Sony Walkman.

- Dependent claims 2 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Boeker.
- Dependent claim 4 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Chen '938; Ni; and/or Neo.
- Dependent claim 5 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Chen '938; Ni; Neo; and Lin '683.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Chen '938; Ni; and/or Lin '683.
- Dependent claims 8 and 21 are obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Boeker; Diggs; Ni; and/or Lin '683.
- Dependent claim 23 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Neo; and/or Lin '683.
- Dependent claim 24 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241;

Diggs; Boeker; Raines; Chen '938; Ni; Neo; the Palm Tungsten T5; Lin '683; and/or the Sony Walkman.

- Dependent claim 25 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Neo; Chen '938; the Palm Tungsten T5; Raines; Ni; Lin '683; and/or the Sony Walkman.
- Dependent claim 27 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Chen '938; Ni; and/or Neo.
- The Palm Tungsten T5 alone or in combination with one or more of Lin '241, Diggs, Neo, Chen '938, Hamer, Boeker, Raines, Ni, Lin '683, and the Sony Walkman. For example:
 - Independent claims 1 and 16 are obvious over the Palm Tungsten T5; the Palm Tungsten T5 in view of Lin '241; the Palm Tungsten T5 in view of Diggs; the Palm Tungsten T5 in view of Neo; the Palm Tungsten T5 in view of Chen '938; the Palm Tungsten T5 in view of Hamer; the Palm Tungsten T5 in view of Raines; the Palm Tungsten T5 in view of Ni; the Palm Tungsten T5 in view of Lin '683; and the Palm Tungsten T5 in view of the Sony Walkman.
 - Dependent claims 2 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Boeker.

- Dependent claim 4 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Chen '938; Ni; and/or Neo.
- Dependent claim 5 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Chen '938; Ni; Neo; Hamer; and/or Lin '683.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Chen '938; Ni; Hamer; and/or Lin '683.
- Dependent claims 8 and 21 are obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Boeker; Diggs; Ni; and/or Lin '683.
- Dependent claim 23 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Neo; Hamer; and/or Lin '683.
- Dependent claim 24 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Boeker; Raines; Chen '938; Ni; Neo; Hamer; Lin '683; and/or the Sony Walkman.
- Dependent claim 25 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Neo; Chen '938; Hamer; Raines; Ni; Lin '683; and/or the Sony Walkman.

- Dependent claim 27 is obvious over any of the obviousness grounds listed for independent claims 1 and 16 alone and/or further in view of Lin '241; Diggs; Chen '938; Ni; and/or Neo.

b) Motivations to Combine and Expectation of Success

To the extent a finder of fact finds that a primary prior art reference does not disclose one or more limitations of an asserted claim, the asserted claim is nevertheless obvious because the alleged missing limitations contain nothing beyond ordinary improvements. In other words, the asserted claim combines known elements to achieve predictable results or chooses between clear alternatives known to those of skill in the art, particularly in view of the state of the art as reflected in the relevant prior art.

Moreover, as explained above, it would have been obvious to a person of skill in the art at the time of the alleged invention of the asserted claims to combine any primary reference with any combination of other primary references so as to practice the asserted claims. To the extent that Plaintiff argues that any concept claimed in the asserted claims is not disclosed in a primary reference, it would, at a minimum, have been obvious to adapt the primary reference to include the concept or combine it with other primary references that disclose the concept. Each concept described and claimed in the Asserted Patents was known to those of skill in the art as available design choices for semiconductor memory design and fabrication.

The Supreme Court has held that “[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). “When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.” *Id.* at 417. As the Supreme Court made clear, “[f]or the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the

art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *Id.*

To determine whether there is an apparent reason to combine the known elements in the fashion claimed by the patent at issue, a court can “look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art.” *Id.* at 418. For example, obviousness can be demonstrated by showing “there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent’s claims.” *Id.* at 420. “[A]ny need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” *Id.* Common sense also teaches that “familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.” *Id.*

However, the Supreme Court in *KSR* held that a claimed invention can be obvious even if there is no explicit teaching, suggestion, or motivation for combining the prior art to produce that invention. In summary, *KSR* holds that patents that are based on new combinations of elements or components already known in a technical field may be found to be obvious. *See, generally, KSR*, 550 U.S. 398. Specifically, the Court in *KSR* rejected a rigid application of the “teaching, suggestion, or motivation [to combine]” test. *Id.* at 418. “In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose of the patentee controls. What matters is the objective reach of the claim.” *Id.* at 419. “Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the

manner claimed.” *Id.* at 420. A key inquiry is whether the “improvement is more than the predictable use of prior art elements according to their established functions.” *Id.* at 417.

The rationale to combine or modify prior art references is significantly stronger when, as here, the references seek to solve the same problem, come from the same field, and correspond well to each other. *In re Inland Steel Co.*, 265 F.3d 1354, 1362 (Fed. Cir. 2001). The Federal Circuit has held that two references may be combined as invalidating art under similar circumstances, namely “[the prior art] focus[es] on the same problem that the . . . patent addresses: enhancing the magnetic properties of . . . steel. Moreover, both [prior art references] come from the same field Finally, the solutions to the identified problems found in the two references correspond well.” *Id.* at 1364 (concerning patents and prior art relating to improving the magnetic and electrical properties of steel).

In view of the Supreme Court’s *KSR* decision, the PTO issued a set of Examination Guidelines. Examination Guidelines for Determining Obviousness Under 35 U.S.C. § 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex, Inc.*, 72 Fed. Reg. 57526 (October 10, 2007). Those Guidelines summarized the *KSR* decision and identified various rationales for finding a claim obvious, including those based on other precedents. Those rationales include:

(A) Combining prior art elements according to known methods to yield predictable results;

(B) Simple substitution of one known element for another to obtain predictable results;

(C) Use of known technique to improve similar devices (methods, or products) in the same way;

(D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) “Obvious to try” – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art;

(G) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Id. at 57529. The above rationales likewise apply in rendering obvious the asserted claims of the Asserted Patents.

The references disclosed herein, alone or in combination, contain an explicit and/or implicit teaching or motivation to combine them due to the following: (1) the knowledge generally available to a person of ordinary skill in the art; (2) the prior art references as understood by a person of ordinary skill in the art; (3) the nature of the problem to be solved; (4) the fact that each prior art reference addresses similar problems; and (5) the knowledge of those skilled in the art that the disclosed elements had been or could be used together.

As an example of those reasons and motivations to combine the references, Lin '241, Hamer, Neo, Diggs, Lin '683, Raines, Ni, the Palm Tungsten T5, Boeker, Chen '938, and the Sony Walkman, all generally relate to or use memory cards for storing and transferring data between various interfaces. *See, e.g.*, Lin '241, ¶ 7; Diggs, ¶ 8; Neo, ¶ 2; Chen '938, ¶¶ 5-8; Hamer, ¶ 14. The references disclose using similar components and techniques, such as the use of a USB port, along with a corresponding set of pins and controller circuitry; an I/O port, along with a corresponding set of pins and controller circuitry; memory in communication with the ports; a housing that stores the memory and exposes the ports; positioning the ports on the same end to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port; and positioning the ports such that when the I/O port is electrically connected with a host device, at least one of the pins of the USB port is not electrically

connected, and when the USB port is connected to the host device, at least one of the pins of the I/O port is not electrically connected. *See generally* Ex. B1-B6. Thus, combining one or more such references merely involves combining prior art elements according to known methods to yield predictable results, the substitution of one known element for another to obtain predictable results, the use of a known technique to improve similar devices in the same way, or applying a known technique to a known device ready for improvement to yield predictable results.

In addition, below are additional motivations to combine prior art for particular claim limitations. The following discussion of specific claim limitations merely provides examples, which are not limiting.

For example, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach limitations 1[g]/16[g] (“the USB port and the I/O port are positioned to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses limitations 1[g]/16[g] in Exhibits B1 to B6 and B-A. For example, the charted prior art references explicitly describe or implicitly suggest a memory card having a USB port and I/O port positioned to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port. *See, e.g.*, Lin ’241, Figs. 5, 6A, ¶¶ 106-107; Diggs, Fig. 7, ¶¶ 23, 55; Neo, Fig. 1, ¶¶ 24, 29; Hamer, Fig. 2; *see also* Chen ’938, ¶ 16, Boeker, Fig. 1, ¶ 12; Raines, Figs. 3A, 4B, ¶¶ 10-12, 21, 94-95; Ni, 8:43-52. It would have been obvious to combine any primary reference with any of Lin ’241, Hamer, Neo, Diggs, Lin ’683, Raines, Ni, the Palm Tungsten T5, Boeker, Chen ’938, and the Sony Walkman to satisfy limitations 1[g]/16[g]. A person skilled in the art would have recognized that having “USB port and the I/O

port are positioned to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port” was a common, predictable design for a portable handheld memory card. Further, a person of ordinary skill in the art would have recognized that positioning the USB and I/O ports in this manner has several benefits. For example, with such a port positioning, a user need not worry about the orientation of the card when inserting it into different devices, which can prevent damage. It also reduces the risk of inserting the card incorrectly, in turn further minimizes the risk of damage to the device’s ports. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would also have had a reasonable expectation of success given that, by the alleged priority date of the ’051 Patent, storage devices that accommodate different kinds of host devices were widely sold and used. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach limitations 1[h]/16[h] (“the USB port and the I/O port are positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses limitations 1[h]/16[h] in Exhibits B1 to B6 and B-A. For example, the charted prior art references explicitly describe or implicitly suggest a memory card whose USB and I/O

ports are positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device. *See, e.g.*, Lin '241, ¶¶ 31, 33-35, 36-38; Diggs, Figs. 2, 7, ¶¶ 23, 40, 55; Neo, ¶¶ 4, 26; Chen '938, ¶¶ 21, 31; Boeker ¶¶ 1-2; Raines, Figs. 3A, 4A, ¶¶ 12, 34-35, 62, 94-95, 110; Ni at 8:25-52. It would have been obvious to combine any primary reference with any of Lin '241, Neo, Diggs, Raines, Ni, the Palm Tungsten T5, Boeker, Chen '938, and the Sony Walkman to satisfy limitations 1[h]/16[h].

A person skilled in the art would have recognized that having “the USB port and the I/O port ... positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device” was a common, predictable design for a memory card. Further, a person of ordinary skill in the art would have recognized that positioning the USB and I/O ports in this manner has several benefits, such as promoting efficient and convenient memory storage operations. Specifically, a person of ordinary skill in the art would have appreciated that positioning the USB and I/O ports in such a manner would help minimize interference between the two ports when both are connected to a host device. In addition, a person of ordinary skill in the art would have appreciated that such a port positioning promotes design flexibility and compatibility, by allowing the memory card to be easily used with different devices. A person of ordinary skill in the art would have further appreciated that such a port positioning could help minimize wear on the USB and I/O ports, thereby increasing the memory card’s durability and longevity. Thus, a person of ordinary skill in the art would have

been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would also have had a reasonable expectation of success given that, by the alleged priority date of the '051 Patent, storage devices that accommodate different kinds of host devices were widely sold and used. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach claims 2 and 17 (“decryption circuitry in communication with the memory and configured to decrypt encrypted data stored in the memory”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses claims 2 and 17 in Exhibits B1 to B6 and B-A. For example, the charted prior art references explicitly describe or implicitly suggest a memory card having decryption circuitry in communication with the memory and configured to decrypt encrypted data stored in the memory. *See, e.g.*, Boeker at ¶¶ 1-9, 12, 15; Sony Walkman Operating Instructions at 8. It would have been obvious to combine any primary reference with any of Boeker and the Sony Walkman to satisfy claims 2 and 17. A person skilled in the art would have recognized that having “decryption circuitry in communication with the memory and configured to decrypt encrypted data stored in the memory” was a common, predictable design for a memory card. Further, a person of ordinary skill in the art would have recognized that incorporating such circuitry into the memory card has several benefits. For example, a person of ordinary skill in the art would have appreciated that including encryption and decryption on board the memory card enhances security by ensuring that stored information remains confidential

(accessible only to authorized users). Such a position of ordinary skill in the art would have known that circuitry may also help verify the integrity of the data (i.e., ensuring it hasn't been tampered with). Further, hardware-based encryption and decryption (e.g., through circuitry) was known to be generally faster than software-based solutions, thereby reducing latency for accessing data without compromising security. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would also have had a reasonable expectation of success given that, by the alleged priority date of the '051 Patent, storage devices that accommodate different kinds of host devices were widely sold and used. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach claim 4 (“a power management unit in communication with the USB controller circuitry”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses this limitation in Exhibits B1 to B6 and B-A. For example, the charted prior art references explicitly describe or implicitly suggest a power management unit in communication with the USB controller circuitry. *See, e.g.*, Diggs, ¶¶ 4, 29; Chen '938, ¶ 39, Fig. 8; Hamer, ¶¶ 6, 23. It would have been obvious to combine any primary reference with any of Diggs, Chen '938, Neo, and the Sony Walkman to satisfy claim 4. A person skilled in the art would have recognized that having “a power management unit in communication with the USB controller circuitry” was a common, predictable design for a memory card. Further, a person of ordinary skill in the art

would have recognized that managing power of a circuit, including circuitry that controls a USB port, has several benefits. For example, a person of ordinary skill in the art would have appreciated the ability to adjust power to comply with applicable USB standards. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would also have had a reasonable expectation of success given that, by the alleged priority date of the '051 Patent, storage devices that accommodate different kinds of host devices were widely sold and used. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach claims 8 and 21 (“the memory comprises Flash memory”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses this limitation in Exhibits B1 to B6 and B-A. For example, the charted prior art references explicitly describe or implicitly suggest a memory comprises Flash memory. *See, e.g.*, Lin '241, ¶ 3; Diggs, ¶ 30; Neo, ¶¶ 2, 11. It would have been obvious to combine any primary reference with any of Lin '683, Diggs, Boeker, Lin '241, Ni, Neo, and the Sony Walkman to satisfy claims 8 and 21.

A person skilled in the art would have recognized that having “the memory compris[ing] Flash memory” was a common, predictable design for a memory card. Further, a person of ordinary skill in the art would have recognized that the benefits of implementing Flash memory. A person of ordinary skill in the art would have known that Flash memory was an obvious design choice for a type of memory. Thus, a person of ordinary skill in the art would have been motivated

to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would also have had a reasonable expectation of success given that, by the alleged priority date of the '051 Patent, storage devices that accommodate different kinds of host devices were widely sold and used. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach claim 27 (“wherein the USB port comprises multiple data lines; wherein the first set of pins comprise multiple data pins connected to the multiple data lines; and wherein all of the multiple data pins are not electrically connected to the I/O controller circuitry”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses claim 27 in Exhibits B1 to B6 and B-A for the same reasons as for claim limitation 1[h]. Similarly, a person skilled in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed and would also have had a reasonable expectation of success for the same reasons explained for claim limitation 1[h].

B. Invalidity Contentions Under 35 U.S.C. § 112

Defendants include below the grounds on which Defendants contend the asserted claims are invalid for failure to meet the requirements of the first two paragraphs of 35 U.S.C. § 112.

Plaintiff has not yet provided a claim construction for many of the terms and phrases that Defendants anticipate will be in dispute. Defendants, therefore, cannot provide a complete list of its § 112 defenses because Defendants do not know whether Plaintiff will proffer a

construction for certain terms and phrases that is broader than, or inconsistent with, the construction that would be supportable by the disclosure set forth in the specification.

To the extent the following contentions reflect constructions of claim limitations consistent with or implicit in Plaintiff's Infringement Contentions, no inference is intended nor should any be drawn that Defendants agree with Plaintiff's claim constructions, and Defendants expressly reserve the right to contest such claim constructions. Defendants offer these contentions in response to Plaintiff's Infringement Contentions and without prejudice to any position it may ultimately take as to any claim construction issues.

Accordingly, Defendants reserve the right to amend or supplement these § 112 Invalidity Contentions as discovery progresses.

1. Indefiniteness Under 35 U.S.C. § 112, ¶ 2

35 U.S.C. § 112, ¶ 2 requires that a patent claim “particularly point[] out and distinctly claim[] the subject matter which the applicant regards as his invention.” 35 U.S.C. § 112, ¶ 2. Claim terms that fail to inform those skilled in the art “with reasonable certainty . . . about the scope of the invention” fail the definiteness requirement of 35 U.S.C. § 112, ¶ 2. *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014).

Each of the asserted claims are invalid as indefinite under 35 U.S.C. § 112 because they fail to particularly point out and distinctly claim the subject matter which the applicant regards as his invention. In particular, the following limitations, read in light of the intrinsic evidence, fail to inform those skilled in the art with reasonable certainty about the scope of the claimed inventions:

- Claim 1: “the USB port and the I/O port are positioned on a same end to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port;
- Claim 1: “the USB port and the I/O port are positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device.”
- Claim 5: “a host interface module”
- Claim 23: “at least two pins of the USB port are parallel to at least two pins of the I/O port.”
- Claim 24: “layout for the USB port is different from layout of the I/O port.”
- Claim 25: “the I/O port is configured for mating with an external port.”
- Claim 27: “all of the multiple data pins are not electrically connected to the I/O controller circuitry.”

2. Lack of Enablement/Lack of Written Description Under 35 U.S.C. § 112, ¶ 1

The asserted claims of the '051 Patent are further invalid under 35 U.S.C. § 112, ¶ 1 because the specifications do not contain an adequate written description of the subject matter of these claims and would not enable one of skill in the relevant art to make and use the alleged invention.

For a claim to be valid, the specification must contain a written description of the invention. 35 U.S.C. § 112, ¶ 1. To fulfill the written description requirement, it “must clearly allow persons of ordinary skill in the art to recognize that the inventor invented what is claimed.”

Ariad Pharm., Inc. v. Eli Lilly & Co., 598 F.3d 1336, 1351 (Fed. Cir. 2010) (citation and internal quotation marks omitted). “[T]he applicant must ‘convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,’ and demonstrate that by disclosure in the specification of the patent.” *Carnegie Mellon Univ. v. Hoffmann-La Roche Inc.*, 541 F.3d 1115, 1122 (Fed. Cir. 2008) (quoting *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563–64 (Fed. Cir. 1991)).

The specification must also describe “the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains . . . to make and use the” invention. *Ariad*, 598 F.3d at 1343; *see also* 35 U.S.C. § 112 ¶ 1. “The enablement requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation.” *AK Steel Corp. v. Sollac & Ugine*, 344 F.3d 1234, 1244 (Fed. Cir. 2003) (citation omitted). “[T]he scope of the claims must be less than or equal to the scope of the enablement.” *Nat’l Recovery Tech., Inc. v. Magnetic Separation Sys., Inc.*, 166 F.3d 1190, 1196 (Fed. Cir. 1999).

Each of the asserted claims below are invalid because the specifications fail to provide written description and/or an enabling disclosure of at least the following limitations:

- Claim 1: “wherein the USB port and the I/O port are positioned on a same end to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port;
- Claim 1: “when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device.”

- Claim 23: “at least two pins of the USB port are parallel to at least two pins of the I/O port.”
- Claim 24: “layout for the USB port is different from layout of the I/O port.”
- Claim 27: “wherein all of the multiple data pins are not electrically connected to the I/O controller circuitry”

V. U.S. Patent No. 9,281,314 (“’314 Patent”)

A. Invalidity Contentions Under 35 U.S.C. §§ 102 And 103

1. Identification of Prior Art

In addition to the prior art cited on the face of the ’314 Patent and related patents, the admitted prior art in the specifications of the ’314 Patent and related patents, the prior art cited in any file histories, reexaminations, *inter partes* review proceedings, reissue proceedings, or other examination or post-grant proceedings of the ’314 Patent and related patents, and the prior art cited in any invalidity contentions or expert reports submitted in any action or proceedings involving the ’314 Patent or related patents, Defendants identify the following prior art that anticipates each asserted claim or renders it obvious.

a) Prior Art Patents

The following patents and patent publications are prior art to the asserted claims under at least 35 U.S.C. §§ 102(a)(1), (a)(2), and/or 35 U.S.C. § 103. The identification of any patent or patent publication shall be deemed to include any counterpart patent or application filed, published, or issued anywhere in the world.

Patent or Publication Number	Country of Origin	Filing Date	Date of Issue or Publication
U.S. Patent App. Pub. No. 2014/0159132 (“Daycock”)	U.S.	12/6/2012	6/12/2014
U.S. Patent App. Pub. No. 2007/0096202 (“Kang ’202”)	U.S.	10/20/2006	5/3/2007

Patent or Publication Number	Country of Origin	Filing Date	Date of Issue or Publication
U.S. Patent No. 7,598,564 (“Kang ’564”)	U.S.	5/31/2006	10/6/2009
U.S. Patent App. Pub. No. 2013/0193504 (“Kinoshita”)	U.S.	1/24/2013	8/1/2013
U.S. Patent No. 7,759,722 (“Murata”)	U.S.	6/20/2007	7/20/2010
U.S. Patent App. Pub. No. 2011/0309425 (“Purayath”)	U.S.	6/16/2011	12/22/2011
U.S. Patent No. 7,705,392 (“Yonemochi”)	U.S.	4/13/2006	4/27/2010
U.S. Patent App. Pub. No. 2006/0205148 (“Deppe”)	U.S.	3/11/2005	9/14/2006
U.S. Patent App. Pub. No. 2015/0014762 (“Ohnuki”)	U.S.	2/11/2014	1/15/2015
U.S. Patent App. Pub. No. 2015/0380431 (“Kanamori”)	U.S.	3/9/2015; (Claims priority to Korean Application No. 10-2014-0078205, filed on June 25, 2014)	12/31/2015
U.S. Patent App. Pub. No. 2010/0117141 (“Shin”)	U.S.	11/12/2009	5/13/2010
U.S. Patent No. 8,492,797 (“Hwang”)	KR	4/7/2011	7/23/2013

b) Prior Art Non-Patent Publications

The following non-patent publications are prior art to the asserted claims under at least 35 U.S.C. §§ 102(a)(1), (a)(2), and/or 35 U.S.C. § 103.

Title	Author/Publisher	Date of Publication
<i>Memory Detailed Structural Analysis of the Toshiba TC58NVG3D4CTG00 70nm 8Gb MLC NAND Flash</i> , SAR-3843 (“TechInsights SAR-3843”)	Xu Chang, TechInsights	May 31, 2006

Title	Author/Publisher	Date of Publication
<i>Full Electrical Reverse and Reliability Characterization on 8Gb MLC 70nm NAND Toshiba</i>	Dario Romio, Guglielmo Russo & Angelo Visconti, STMicroelectronics	July 2006
<i>Toshiba and SanDisk Develop 8-Gigabit NAND Flash Memory Chip With 70 nm Process Technology (“Toshiba”)</i>	Toshiba, https://www.global.toshiba/ww/news/corporate/2005/02/pr0802.html	Feb. 8, 2005
<i>Toshiba and SanDisk Develop 8-Gigabit NAND Flash Memory Chip (“EETimes”)</i>	EETime, https://www.eetimes.com/toshiba-and-sandisk-develop-8-gigabit-nand-flash-memory-chip/	Mar. 1, 2005
<i>SanDisk, Toshiba to Ship High-Performance NAND Flash Chips (“Channel Insider”)</i>	Channel Insider, https://www.channelinsider.com/news-and-trends/sandisk-toshiba-to-ship-high-performance-nand-flash-chips/	Jan. 23, 2007

c) Prior Art Systems

The following systems are prior art under at least 35 U.S.C. §§ 102(a):

1. Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to Toshiba and SanDisk’s 70nm 8Gb MLC NAND Flash (“Toshiba/SanDisk’s NAND”), as exemplified in the claim chart in Exhibit C9. As part of these Invalidity Contentions, Defendants have produced documents relating to Toshiba/SanDisk’s NAND. Based on information available to Defendants, Defendants believes that Toshiba/SanDisk’s NAND was conceived and/or reduced to practice by engineers at Toshiba Corporation and SanDisk® Corporation, including those identified in the claim chart and its cited publications, at least before May 2006, without being abandoned, suppressed, or concealed, and it was in public use or on sale by the dates identified in the claim chart, which are no later than May 2006.

Defendants’ investigation into publicly-available prior art systems that teach and/or render obvious each element of any asserted claims is ongoing. Fact discovery is at an early stage, and Defendants may require discovery from third parties regarding publicly-available prior art systems. Defendants reserve the right to amend its identification of prior art systems as Defendants become aware of the existence, functionality, and/or characteristics of prior art

systems as a result of their investigation and forthcoming discovery.

2. Primary References

Defendants contend that the primary prior art references identified below and described in the charts attached as Exhibits C1 to C9 by themselves, anticipate the asserted claims of the '314 Patent. To the extent that a primary reference is deemed not to anticipate a claim for failing to teach one or more limitations of that claim, Defendants contend that the claim would nonetheless have been obvious to a person of ordinary skill in the art at the time of the invention in view of the prior art reference itself and the knowledge of a person of ordinary skill in the art, as described in the attached charts. Defendants' prior art charts (attached as Exhibits C1 to C9) set forth the particular claims that are anticipated under 35 U.S.C. § 102 and/or rendered obvious under 35 U.S.C. § 103 by each item of prior art and identify where specifically in each item of prior art each element of each asserted claim is found.

Exhibit	Primary References
C1	U.S. Patent App. Pub. No. 2014/0159132 ("Daycock")
C2	U.S. Patent App. Pub. No. 2007/0096202 ("Kang '202")
C3	U.S. Patent No. 7,598,564 ("Kang '564")
C4	U.S. Patent App. Pub. No. 2013/0193504 ("Kinoshita")
C5	U.S. Patent No. 7,759,722 ("Murata")
C6	U.S. Patent App. Pub. No. 2011/0309425 ("Purayath")
C7	U.S. Patent No. 7,705,392 ("Yonemochi")
C8	U.S. Patent App. Pub. No. 2006/0205148 ("Deppe")
C9	Toshiba and SanDisk's 70nm 8Gb MLC NAND Flash ("Toshiba/SanDisk's NAND")

3. Obvious Combinations

To the extent that a primary reference is deemed, by itself, not to anticipate or render obvious a claim for failing to teach one or more limitations, the claim would nonetheless have been obvious to a person of ordinary skill in the art at the time of the invention by the combination of the primary reference with one or more other primary references and/or the knowledge of someone skilled in the art. For example, a person of ordinary skill in the art would have been motivated to combine any reference in Exhibits C1 to C9 with any other reference(s) in Exhibits C1 to C9. Such combinations would be achieved, for example, by merely combining the disclosures described in the respective claim charts for each reference.

The obviousness combinations are provided in the alternative to Defendants' anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not itself anticipatory.

a) Exemplary Combinations

Below are examples of prior art references that would have been combined by one of ordinary skill in the art at the time of the alleged invention. These combinations are merely examples. The asserted claims of the '314 Patent are rendered obvious by:

- Daycock alone or in combination with one or more of Kang '202, Kang '564, Kinoshita, Murata, Purayath, Yonemochi, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Daycock; Daycock in view of Kang '564; Daycock in view of Yonemochi; Daycock in view of Murata; Daycock in view of Purayath; Daycock in view of Kang '202; Daycock in view of Kinoshita; Daycock in view of Toshiba/SanDisk's NAND.

- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kang '564, Kinoshita, Yonemochi, Deppe, and/or Toshiba/SanDisk's NAND.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Kang '202, and/or Deppe.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kinoshita, Kang '564, Kang '202, and/or Toshiba/SanDisk's NAND.
- Kang '202 alone or in combination with one or more of Kang '564, Daycock, Kinoshita, Murata, Purayath, Yonemochi, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Kang '202; Kang '202 in view of Kang '564; Kang in view of Daycock; Kang '202 in view of Yonemochi; Kang '202 in view of Murata; Kang '202 in view of Purayath; Kang '202 in view of Kinoshita; Kang '202 in view of Toshiba/SanDisk's NAND.
- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kang '564, Kinoshita, Yonemochi, Deppe, and/or Toshiba/SanDisk's NAND.

- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, and/or Deppe.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kinoshita, Kang '564, Daycock, and/or Toshiba/SanDisk's NAND.
- Kang '564 alone or in combination with one or more of Kang '202, Daycock, Kinoshita, Murata, Purayath, Yonemochi, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Kang '564; Kang '564 in view of Daycock; Kang '564 in view of Yonemochi; Kang '564 in view of Murata; Kang '564 in view of Purayath; Kang '564 in view of Kang '202; Kang '564 in view of Kinoshita; Kang '564 in view of Toshiba/SanDisk's NAND.
- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kinoshita, Yonemochi, Deppe, and/or Toshiba/SanDisk's NAND.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, Kang '202, and/or Deppe.

- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kinoshita, Daycock, Kang '202, and/or Toshiba/SanDisk's NAND.
- Kinoshita alone or in combination with one or more of Kang '202, Kang '564, Daycock, Murata, Purayath, Yonemochi, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Kinoshita; Kinoshita in view of Kang '564; Kinoshita in view of Yonemochi; Kinoshita in view of Murata; Kinoshita in view of Purayath; Kinoshita in view of Kang '202; Kinoshita in view of Daycock; Kinoshita in view of Toshiba/SanDisk's NAND.
- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kang '564, Yonemochi, Deppe, and/or Toshiba/SanDisk's NAND.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, Kang '202, and/or Deppe.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kang '564, Daycock, Kang '202, and/or Toshiba/SanDisk's NAND.

- Murata alone or in combination with one or more of Kang '202, Kang '564, Kinoshita, Daycock, Purayath, Yonemochi, Deppe, and Toshiba/SanDisk's NAND. For example:

- Independent claims 1 and 13 are obvious over Murata; Murata in view of Kang '564; Murata in view of Yonemochi; Murata in view of Daycock; Murata in view of Purayath; Murata in view of Kang '202; Murata in view of Kinoshita; Murata in view of Toshiba/SanDisk's NAND.
- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Kinoshita, Kang '564, Yonemochi, Deppe, and/or Toshiba/SanDisk's NAND.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, Kang '202, and/or Deppe.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kinoshita, Kang '564, Daycock, Kang '202, and/or Toshiba/SanDisk's NAND.

- Purayath alone or in combination with one or more of Kang '202, Kang '564, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Purayath; Purayath in view of Kang '564; Purayath in view of Yonemochi; Purayath in view of

Murata; Purayath in view of Daycock; Purayath in view of Kang '202; Purayath in view of Kinoshita; Purayath in view of Toshiba/SanDisk's NAND.

- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kinoshita, Kang '564, Yonemochi, Deppe, and/or Toshiba/SanDisk's NAND.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Daycock, Kang '202, and/or Deppe.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Kinoshita, Kang '564, Daycock, Kang '202, and/or Toshiba/SanDisk's NAND.
- Yonemochi alone or in combination with one or more of Kang '202, Kang '564, Kinoshita, Murata, Purayath, Daycock, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Yonemochi; Yonemochi in view of Kang '564; Yonemochi in view of Daycock; Yonemochi in view of Murata; Yonemochi in view of Purayath; Yonemochi in view of Kang '202; Yonemochi in view of Kinoshita; Yonemochi in view of Toshiba/SanDisk's NAND.

- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kinoshita, Kang '564, Deppe, and/or Toshiba/SanDisk's NAND.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, Kang '202, and/or Deppe.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Kinoshita, Kang '564, Daycock, Kang '202, and/or Toshiba/SanDisk's NAND.
- Deppe alone or in combination with one or more of Kang '202, Kang '564, Kinoshita, Murata, Purayath, Yonemochi, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Deppe; Deppe in view of Kang '564; Deppe in view of Yonemochi; Deppe in view of Murata; Deppe in view of Purayath; Deppe in view of Daycock; Deppe in view of Kang '202; Deppe in view of Kinoshita; Deppe in view of Toshiba/SanDisk's NAND.
- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kinoshita, Kang '564, Yonemochi, and/or Toshiba/SanDisk's NAND.

- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, and/or Kang '202.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kinoshita, Kang '564, Daycock, Kang '202, and/or Toshiba/SanDisk's NAND.
- Toshiba/SanDisk's NAND alone or in combination with one or more of Kang '202, Kang '564, Kinoshita, Murata, Purayath, Yonemochi, Deppe, and Daycock.

For example:

- Independent claims 1 and 13 are obvious over Toshiba/SanDisk's NAND; Toshiba/SanDisk's NAND in view of Kang '564; Toshiba/SanDisk's NAND in view of Yonemochi; Toshiba/SanDisk's NAND in view of Murata; Toshiba/SanDisk's NAND in view of Purayath; Toshiba/SanDisk's NAND in view of Kang '202; Toshiba/SanDisk's NAND in view of Kinoshita; Toshiba/SanDisk's NAND in view of Daycock.
- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kinoshita, Kang '564, Yonemochi, and/or Deppe.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, Kang '202, and/or Deppe.

- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kinoshita, Kang '564, Daycock, and/or Kang '202.

b) Motivations to Combine and Expectation of Success

To the extent a finder of fact finds that a primary prior art reference does not disclose one or more limitations of an asserted claim, the asserted claim is nevertheless obvious because the alleged missing limitations contain nothing beyond ordinary improvements. In other words, the asserted claim combines known elements to achieve predictable results or chooses between clear alternatives known to those of skill in the art, particularly in view of the state of the art as reflected in the relevant prior art.

Moreover, as explained above, it would have been obvious to a person of skill in the art at the time of the alleged invention of the asserted claims to combine any primary reference with any combination of other primary references so as to practice the asserted claims. To the extent that Plaintiff argues that any concept claimed in the asserted claims is not disclosed in a primary reference, it would, at a minimum, have been obvious to adapt the primary reference to include the concept or combine it with other primary references that disclose the concept. Each concept described and claimed in the Asserted Patents was known to those of skill in the art as available design choices for semiconductor memory design and fabrication.

The Supreme Court has held that “[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). “When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.” *Id.* at 417. As the Supreme Court made clear, “[f]or the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the

art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *Id.*

To determine whether there is an apparent reason to combine the known elements in the fashion claimed by the patent at issue, a court can “look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art.” *Id.* at 418. For example, obviousness can be demonstrated by showing “there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent’s claims.” *Id.* at 420. “[A]ny need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” *Id.* Common sense also teaches that “familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.” *Id.*

However, the Supreme Court in *KSR* held that a claimed invention can be obvious even if there is no explicit teaching, suggestion, or motivation for combining the prior art to produce that invention. In summary, *KSR* holds that patents that are based on new combinations of elements or components already known in a technical field may be found to be obvious. *See, generally, KSR*, 550 U.S. 398. Specifically, the Court in *KSR* rejected a rigid application of the “teaching, suggestion, or motivation [to combine]” test. *Id.* at 418. “In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose of the patentee controls. What matters is the objective reach of the claim.” *Id.* at 419. “Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the

manner claimed.” *Id.* at 420. A key inquiry is whether the “improvement is more than the predictable use of prior art elements according to their established functions.” *Id.* at 417.

The rationale to combine or modify prior art references is significantly stronger when, as here, the references seek to solve the same problem, come from the same field, and correspond well to each other. *In re Inland Steel Co.*, 265 F.3d 1354, 1362 (Fed. Cir. 2001). The Federal Circuit has held that two references may be combined as invalidating art under similar circumstances, namely “[the prior art] focus[es] on the same problem that the . . . patent addresses: enhancing the magnetic properties of . . . steel. Moreover, both [prior art references] come from the same field Finally, the solutions to the identified problems found in the two references correspond well.” *Id.* at 1364 (concerning patents and prior art relating to improving the magnetic and electrical properties of steel).

In view of the Supreme Court’s *KSR* decision, the PTO issued a set of Examination Guidelines. Examination Guidelines for Determining Obviousness Under 35 U.S.C. § 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex, Inc.*, 72 Fed. Reg. 57526 (October 10, 2007). Those Guidelines summarized the *KSR* decision and identified various rationales for finding a claim obvious, including those based on other precedents. Those rationales include:

- (A) Combining prior art elements according to known methods to yield predictable results;
- (B) Simple substitution of one known element for another to obtain predictable results;
- (C) Use of known technique to improve similar devices (methods, or products) in the same way;
- (D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- (E) “Obvious to try” – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art;

(G) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Id. at 57529. The above rationales likewise apply in rendering obvious the asserted claims of the Asserted Patents.

The references disclosed herein, alone or in combination, contain an explicit and/or implicit teaching or motivation to combine them due to the following: (1) the knowledge generally available to a person of ordinary skill in the art; (2) the prior art references as understood by a person of ordinary skill in the art; (3) the nature of the problem to be solved; (4) the fact that each prior art reference addresses similar problems; and (5) the knowledge of those skilled in the art that the disclosed elements had been or could be used together.

As an example of those reasons and motivations to combine the references Kang '202, Kang '564, Daycock, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk's NAND all generally relate to semiconductor memory design and, in particular, structures and manufacturing methods for enhancing the speed and reliability and decreasing the parasitic capacitance of semiconductor memory devices including flash/non-volatile memory with minimal space between adjacent gate structures. *See, e.g.*, Daycock ¶ 6; Kang '564 at Abstract, ¶ 6; Kang '202 at Abstract, ¶¶ 5-6; Purayath ¶¶ 7, 12. The references disclose using similar components and techniques, such as using air gaps or other electrical isolation regions between adjacent structures. *See, e.g.*, Daycock at Abstract, ¶¶ 1, 15-17; Kang '202 at Abstract, ¶¶ 3, 14; Purayath at Abstract, ¶¶ 31-33. Thus, combining one or more such references merely involves combining prior art elements according to known methods to yield predictable results, the

substitution of one known element for another to obtain predictable results, the use of a known technique to improve similar devices in the same way, or applying a known technique to a known device ready for improvement to yield predictable results.

In addition, below are additional motivations to combine prior art for particular claim limitations. The following discussion of specific claim limitations merely provides examples, which are not limiting.

For example, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach limitations 1[e] and 13[e] (“[forming] nitride regions that cover the second oxide regions”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses limitation 1[e] and 13[e] in Exhibits C1 to C9. For example, the charted prior art references explicitly describe or implicitly suggest using barrier spacers, such as nitride, to protect a control gate—including a wordline—during cell formation. *See, e.g.,* Kang ’564 at Abstract, 1:65-2:65. It would have been obvious to combine any primary reference with any of Kang ’202, Kang ’564, Daycock, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk’s NAND to satisfy limitations 1[e] and 13[e]. A person skilled in the art would have recognized that having a nitride region covering a control gate and wordline was an effective technique to protect a control gate and wordline during formation of a memory cell. Indeed, using a dielectric layer such as nitride to insulate control gates and wordlines in a semiconductor was a common practice. Further, a person of ordinary skill in the art would have recognized that using a dielectric such as nitride has several benefits. For example, nitride, especially silicon nitride (SiN), has a moderate dielectric constant, which helps in minimizing capacitive coupling between adjacent wordlines. This reduction in capacitive coupling is crucial for preventing interference between

neighboring cells, leading to better data integrity and preventing disturb effects (e.g., unintentional programming or erasing of nearby cells). In addition, using nitride as part of the insulating layers in memory devices can enhance reliability by improving etch resistance and serving as a barrier layer. Further, nitride can facilitate advanced patterning schemes in three-dimensional memory architectures, improving device density and performance. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would also have had a reasonable expectation of success given that, by the alleged priority date of the '314 Patent, millions of semiconductor devices were manufactured each year using dielectric layers for insulation and protection of control gates and wordlines. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach limitations 1[f] and 13[f] (“[forming] electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses limitation 1[f] and 13[f] in Exhibits C1 to C9. For example, the charted prior art references explicitly describe or implicitly suggest a semiconductor device including electrical isolation regions—other than silicon nitride—that are adjacent to the first oxide regions that cover the sidewalls of the charge storage regions. *See, e.g.*, Daycock at Abstract, ¶¶ 1, 15-17; Kang '202 at Abstract, ¶¶ 3, 14; Purayath at Abstract, ¶¶ 31-33. A person skilled in the art would have recognized that the

dielectric constant of an insulating material is a primary factor in determining the capacitance between adjacent floating gates. Kang '202 ¶ 10. For example, “[a]n insulating layer formed from a material having a higher dielectric constant will cause increased parasitic capacitance between adjacent gate structures.” *Id.* And increases in parasitic capacitance reduce the speed of the memory devices while variations in parasitic capacitance between gate structures may cause a variation in the threshold voltage for each gate structure, thereby degrading the reliability of memory devices. *Id.* ¶ 6. A person skilled in the art would, therefore, have recognized that it is desirable to use a dielectric layer from the lowest dielectric constant material possible and that, for example, silicon nitride had a much higher dielectric constant than silicon oxide or air. *See id.* ¶¶ 10, 11. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include this feature. A person of ordinary skill in the art would also have had a reasonable expectation of success given the well-known uses of electrical isolation regions in semiconductor processing. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations. It would, therefore, have been obvious to combine any primary reference with any of Kang '202, Kang '564, Daycock, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk's NAND to satisfy limitations 1[f] and 13[f].

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach claims 3 (“wherein the word lines comprise tungsten”) and 17 (“forming the plurality of word lines from tungsten”) it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses this limitation in Exhibits C1 to C9. For example, the charted prior art references

explicitly describe or implicitly suggest a semiconductor device including having a tungsten word line. *See, e.g.*, Kang '564 at 1:12-57, 6:11-22; Kinoshita ¶¶ 23, 119; Yonemochi at 3:52-64; Deppe ¶ 87. A person skilled in the art would have recognized that tungsten has a low electrical resistance, so forming a word line from tungsten may enhance the speed of a memory device. *See* Kang '564 at 6:10-13, 1:12-30, 6:11-22. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include this feature. A person of ordinary skill in the art would also have had a reasonable expectation of success given the well-known uses of tungsten word lines in memory devices. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations. It would, therefore, have been obvious to combine any primary reference with any of Kang '202, Kang '564, Daycock, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk's NAND to satisfy claims 3 and 17.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach claims 5 (“wherein the charge storage region is a dielectric charge trapping region”) and 18 (“wherein forming the charge storage regions comprising a dielectric charge trapping region”) it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses this limitation in Exhibits C1 to C9. For example, the charted prior art references explicitly describe or implicitly suggest a semiconductor device wherein the charge storage region is a dielectric charge trapping region. *See, e.g.*, Daycock ¶¶ 3, 29, 34; Kang '202 ¶ 32; Purayath ¶¶ 10, 47; Deppe at Abstract, ¶¶ 2, 9. A person skilled in the art would have known that charge-trapping layers store electrons as data state of the memory cell. A person of skill in the art would also

have known that there were advantages to using charge trapping as opposed to other, largely interchangeable methods of storing electrons as a data state of the memory cell (i.e., floating gates), including greater data retention, better scalability to smaller process nodes, and ease of manufacturing. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include this feature. A person of ordinary skill in the art would also have had a reasonable expectation of success given the well-known uses of charge trapping regions in non-volatile memory. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations. It would, therefore, have been obvious to combine any primary reference with any of Kang '202, Kang '564, Daycock, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk's NAND to satisfy claims 5 and 18.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach claim 6 (“wherein the word lines are electrically coupled to the peripheral circuitry”) it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses this limitation in Exhibits C1 to C9. For example, the charted prior art references explicitly describe or implicitly suggest a semiconductor device wherein the word lines are electrically coupled to the peripheral circuitry. *See, e.g.*, Kang '202 ¶¶ 32, 56, 64; Kang '564 at 1:12-30; Kinoshita ¶¶ 14, 99; Purayath ¶¶ 85, 151, 45, 49, Fig. 17; Toshiba/SanDisk's NAND at 53-56, 63-64, 66-68. A person skilled in the art would have known that connecting peripheral circuitry to wordlines plays a crucial role in enabling various functionalities and optimizing performance of memory devices. For example, peripheral circuitry manages data access and handles various operations like

reading, writing, and erasing the memory cells. A person of skill in the art would also have understood that a peripheral circuit would include row control circuitry, such as row decoders and word line drivers, connected to the word lines to select one of the word lines, to apply read voltages, to apply program voltages combined with the bit line potential levels controlled by column control circuit, and to apply an erase voltage, enabling memory access. Accordingly, peripheral circuitry allows for the controlled application of various voltages to wordlines during read, program, and erase operations, which is essential for reducing power consumption through low-power operations, reducing read select delays, reducing wordline-to-wordline interference, and improving data reliability. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would also have had a reasonable expectation of success given that, by the alleged priority date of the '314 Patent, millions of semiconductor devices were manufactured each year using word lines electrically coupled to peripheral circuitry. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations. It would, therefore, have been obvious to combine any primary reference with any of Kang '202, Kang '564, Daycock, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk's NAND to satisfy claim 6.

B. Invalidity Contentions Under 35 U.S.C. § 112

Defendants include below the grounds on which Defendants contend the asserted claims are invalid for failure to meet the requirements of the first two paragraphs of 35 U.S.C. § 112.

Plaintiff has not yet provided a claim construction for many of the terms and phrases that Defendants anticipate will be in dispute. Defendants, therefore, cannot provide a complete list

of its § 112 defenses because Defendants do not know whether Plaintiff will proffer a construction for certain terms and phrases that is broader than, or inconsistent with, the construction that would be supportable by the disclosure set forth in the specification.

To the extent the following contentions reflect constructions of claim limitations consistent with or implicit in Plaintiff's Infringement Contentions, no inference is intended nor should any be drawn that Defendants agree with Plaintiff's claim constructions, and Defendants expressly reserve the right to contest such claim constructions. Defendants offer these contentions in response to Plaintiff's Infringement Contentions and without prejudice to any position it may ultimately take as to any claim construction issues.

Accordingly, Defendants reserve the right to amend or supplement these § 112 Invalidity Contentions as discovery progresses.

1. Indefiniteness Under 35 U.S.C. § 112(b)

35 U.S.C. § 112(b) requires that a patent claim “particularly point[] out and distinctly claim[] the subject matter which the inventor or a joint inventor regards as the invention.” 35 U.S.C. § 112(b). Claim terms that fail to inform those skilled in the art “with reasonable certainty . . . about the scope of the invention” fail the definiteness requirement of 35 U.S.C. § 112(b). *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014).

Each of the asserted claims are invalid as indefinite under 35 U.S.C. § 112 because they fail to particularly point out and distinctly claim the subject matter which the applicant regards as his invention. In particular, the following limitations, read in light of the intrinsic evidence, fail to inform those skilled in the art with reasonable certainty about the scope of the claimed inventions:

- Claim 1: “each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;”
- Claim 1: “first oxide regions that cover the sidewalls of the charge storage regions;”
- Claim 1: “second oxide regions that cover the sidewalls of the word lines;”
- Claim 1: “nitride regions that cover the second oxide regions;”
- Claim 1: “and electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.”
- Claim 3: “wherein the word lines comprise tungsten.”
- Claim 13: “each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;”
- Claim 13: “forming first oxide regions that cover the sidewalls of the charge storage regions;”
- Claim 13: “forming second oxide regions that cover the sidewalls of the word lines;”
- Claim 13: “forming nitride regions that cover the second oxide regions;”
- Claim 13: “forming electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.”
- Claim 17: “wherein the plurality of word lines comprises forming the plurality of word lines from tungsten.”
- Claim 18: “wherein forming the plurality of lines of memory cells comprises forming the charge storage regions comprising a dielectric charge trapping region.”

2. Lack of Enablement/Lack of Written Description Under 35 U.S.C. § 112(a)

The asserted claims of the '314 Patent are further invalid under 35 U.S.C. § 112(a) because the specifications do not contain an adequate written description of the subject matter of these claims and would not enable one of skill in the relevant art to make and use the alleged invention.

For a claim to be valid, the specification must contain a written description of the invention. 35 U.S.C. § 112(a). To fulfill the written description requirement, it “must clearly allow persons of ordinary skill in the art to recognize that the inventor invented what is claimed.” *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (citation and internal quotation marks omitted). “[T]he applicant must ‘convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,’ and demonstrate that by disclosure in the specification of the patent.” *Carnegie Mellon Univ. v. Hoffmann-La Roche Inc.*, 541 F.3d 1115, 1122 (Fed. Cir. 2008) (quoting *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563–64 (Fed. Cir. 1991)).

The specification must also describe “the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains . . . to make and use the” invention. *Ariad*, 598 F.3d at 1343; *see also* 35 U.S.C. § 112(a). “The enablement requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation.” *AK Steel Corp. v. Sollac & Ugine*, 344 F.3d 1234, 1244 (Fed. Cir. 2003) (citation omitted). “[T]he scope of the claims must be less than or equal to the scope of the enablement.” *Nat'l Recovery Tech., Inc. v. Magnetic Separation Sys., Inc.*, 166 F.3d 1190, 1196 (Fed. Cir. 1999).

Each of the asserted claims below are invalid because the specifications fail to provide written description and/or an enabling disclosure of at least the following limitations:

- Claim 1: “each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;”
- Claim 1: “first oxide regions that cover the sidewalls of the charge storage regions;”
- Claim 1: “second oxide regions that cover the sidewalls of the word lines;”
- Claim 1: “nitride regions that cover the second oxide regions;”
- Claim 1: “and electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.”
- Claim 3: “wherein the word lines comprise tungsten.”
- Claim 5: “wherein the charge storage region is a dielectric charge trapping region.”
- Claim 6: “further comprising peripheral circuitry, wherein the word lines are electrically coupled to the peripheral circuitry.”
- Claim 13: “each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;”
- Claim 13: “forming first oxide regions that cover the sidewalls of the charge storage regions;”
- Claim 13: “forming second oxide regions that cover the sidewalls of the word lines;”
- Claim 13: “forming nitride regions that cover the second oxide regions;”
- Claim 13: “forming electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.”

- Claim 17: “wherein the plurality of word lines comprises forming the plurality of word lines from tungsten.”
- Claim 18: “wherein forming the plurality of lines of memory cells comprises forming the charge storage regions comprising a dielectric charge trapping region.”

VI. Document Production

Pursuant to the Court’s Standing Order Governing Patent and Scheduling Order (Dkt. No. 38), Defendants are concurrently producing the prior art identified in these Invalidity Contentions.

In addition, based on its investigations to date, Defendants are concurrently producing technical documents, sufficient to show the operation of the Accused Instrumentalities identified by Plaintiff in its Infringement Contentions. Defendants further make available source code for inspection at Micron’s facilities in Boise, Idaho, as soon as a protective Order is entered.

Defendants reserve the right to supplement these productions with additional documentation, in accordance with the Federal Rules of Civil Procedure, the Local Rules, the Court’s Orders and other applicable rules and statutes.

Dated: June 11, 2025

Respectfully submitted,

/s/ John Kappos

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CERTIFICATE OF SERVICE

Pursuant to the Federal Rules of Civil Procedure, I hereby certify that, on June 11, 2025, all counsel of record who have appeared in this case are being served with a copy of the foregoing via the electronic mail.

/s/ John Kappos
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