

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS, LLC,
Petitioner

v.

PALISADE TECHNOLOGIES, LLP,
Patent Owner.

Case No. IPR2025-01008
U.S. Patent No. 8,327,051

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,327,051**

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LIST OF EXHIBITS¹

Ex-1001	U.S. Patent No. 8,327,051 (“the ’051 Patent”)
Ex-1002	Declaration of Dr. R. Jacob Baker
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Ex-1004	Prosecution History of U.S. Patent No. 8,327,051 (App. No. 11/986,389)
Ex-1005	U.S. Patent Application Pub. No. US2009/0031073 to Diggs et al. (“Diggs”)
Ex-1006	U.S. Patent Application Pub. No. US2004/0250010 to Chen et al. (“Chen”)
Ex-1007	U.S. Patent Application Pub. No. US 2006/0053241 to Lin et al. (“Lin”)
Ex-1008	German Patent Application Publication No. DE 10220629A1 to Thorsten
Ex-1009	Certified translation of German Patent Application Publication No. DE 10220629A1 (“Thorsten”)
Ex-1010	[Intentionally left blank]
Ex-1011	[Intentionally left blank]
Ex-1012	[Intentionally left blank]
Ex-1013	[Intentionally left blank]
Ex-1014	[Intentionally left blank]
Ex-1015	[Intentionally left blank]
Ex-1016	[Intentionally left blank]
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Ex-1019	[Intentionally left blank]
Ex-1020	Claim Mapping Table
Ex-1021	Amended Complaint, <i>Palisade Techs., LLP v. Micron Tech., Inc. et al.</i> , No. 24-cv-00262-DC-DTG (W.D. Tex. Dec. 19, 2024), ECF No. 20
Ex-1022	U.S. Patent No. 7,376,773 to Kim et al. (“Kim”)
Ex-1023	Keun S. Yim et al., <i>A Flash Compression Layer for SmartMedia Card Systems</i> , 50 IEEE Transactions on Consumer Electronics 120

¹ Four-digit pin citations that begin with 0 are the page stamps added by Micron in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

	(2004)
Ex-1024	U.S. Patent No. 7,433,994 to Petersen (“Petersen”)
Ex-1025	<i>On-The-Go Supplement to the USB 2.0 Specification</i> , Revision 1.0a (June 24, 2003) (“USB mini-A specification”)
Ex-1026	Newton’s Telecom Dictionary (23d ed. 2007) (“port”)
Ex-1027	Microsoft Computer Dictionary (5th ed. 2002) (“port”)
Ex-1028	PartE1 SDIO Simplified Specification ver. 2.00 (Feb. 2007) (“Secure Digital Specification”)
Ex-1029	IEEE Standard for a High Performance Series Bus—Amendment 1 (Mar. 30, 2000) (“IEEE-1394 four-pin Specification”)
Ex-1030	U.S. Patent No. 7,082,483 to Poo (“Poo”)
Ex-1031	U.S. Patent Application Pub. No. 2005/0102471 to Tsai et al. (“Tsai”)
Ex-1032	Wolfgang Rankl et al., <i>Smart Card Handbook</i> (3d ed. 2003)
Ex-1033	Universal Serial Bus Specification 2.0 (April, 2000)

I. INTRODUCTION

Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC (collectively, “Petitioner”) request *inter partes* review (“IPR”) of Claims 1-2, 4-8, 16-17, 20-21, and 23-27 of U.S. Patent No. 8,327,051 (“the ’051 Patent”) (Ex-1001), currently assigned to Palisade Technologies, LLP (“PO”).

II. MANDATORY NOTICES, STANDING, AND FEES

A. Mandatory Notices Under 37 C.F.R. §42.8

Real Parties-in-Interest: Petitioner identifies the following real parties-in-interest: Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC.

Related Matters: PO has asserted the ’051 Patent against the real parties-in-interest in *Palisade Technologies, LLP v. Micron Tech., Inc*, No. 7-24-cv-00262 (W.D. Tex. Oct. 16, 2024).

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B. Grounds for Standing

Petitioner certifies that the '051 Patent is available for review, and Petitioner is not barred or estopped from requesting review.

C. Fee Authorization

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-0639.

III. RELIEF REQUESTED

Petitioner requests cancellation of the challenged claims based on the following grounds:

Ground	Summary
1	Claims 1, 4-8, 16, 20-21, and 23-27 are obvious over Diggs (Ex-1005).
2	Claims 2 and 17 are obvious over Diggs in view of Thorsten (Ex-1008).
3	Claims 1, 4-8, 16, 20-21, and 23-27 are obvious over Lin (Ex-1007).
4	Claims 2 and 17 are obvious over Lin in view of Thorsten.

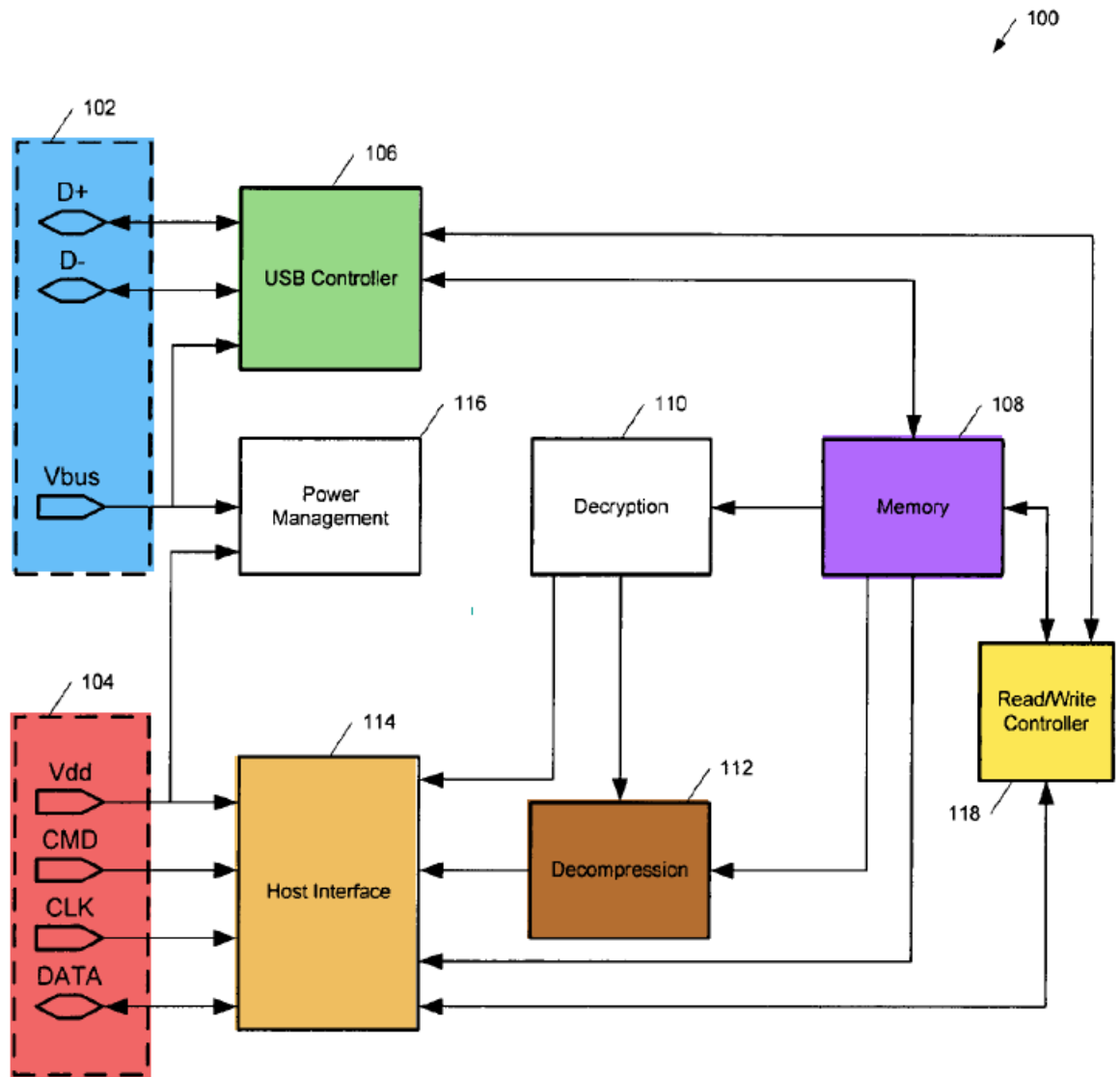
IV. THE CHALLENGED PATENT

A. The '051 Patent

“The [*'051 Patent*] relates to memory devices, and particularly, to portable handheld memory cards configured to transfer data over various interfaces” to a host electronic device. Ex-1001 (*'051 Patent*), 1:6-16. The disclosed memory cards feature “a Universal Serial Bus (USB) port, USB controller circuitry, an input/output (I/O) port, a memory,” and “a housing storing the memory and exposing the USB port and the I/O port,” where “[t]he USB port and I/O port [are] positioned to allow a same-card insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port.” *'051 Patent*, 1:61-2:4; *see also id.*, Abstract.

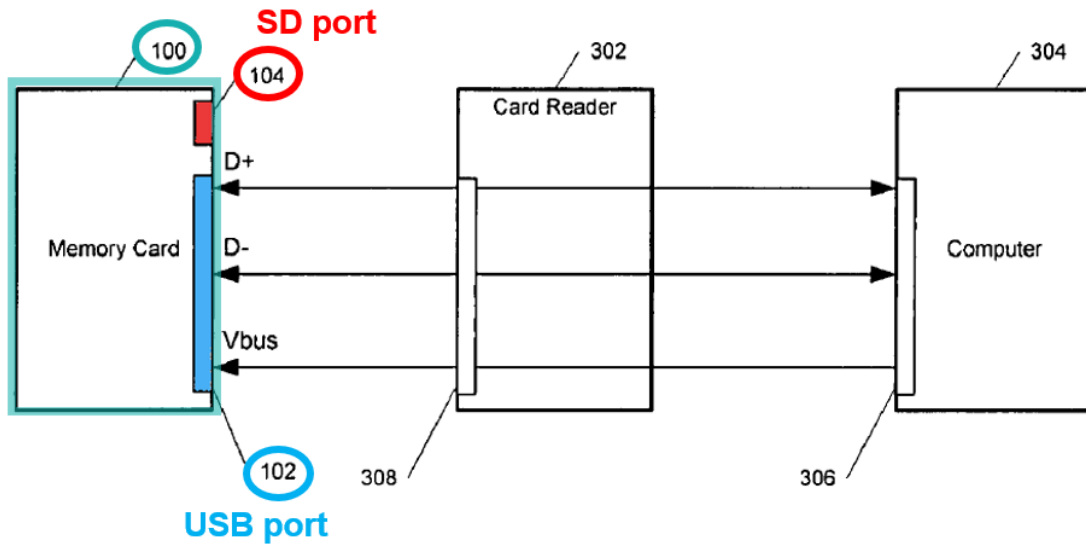
Figure 1 (annotated) illustrates “an embodiment of a memory card 100.” *'051 Patent*, 2:57-62. In operation, data is “transferred between the memory 108” (purple) “and an external device directly via the USB port 102” (blue). *Id.*, 3:32-35. The USB port includes “serial data lines D+ and D- and a bus voltage Vbus,” where the D+ and D- lines are “in communication with the USB controller 106” (green). *Id.*, 3:33-35, 45-48. “The memory card 100 may also communicate with external devices using an input/output (I/O) port, such as the SD port 104” (red). *Id.*, 3:64-66. The SD port “include[s] a voltage Vdd, a command line CMD, a clock line CLK, and a data bus DATA, all of which [are] in communication with the host interface circuit 114” (orange). *Id.*, 4:1-4. “The memory card 100 may also decompress compressed

data” stored in memory 108 “with the decompression circuit 112 [(brown)] so that a connected device does not need to include potentially costly and complex decompression circuitry.” *Id.*, 3:12-16. “Data flow to and from the memory 108 may be a managed by the read/write controller 118” (yellow), which “may be in communication with the USB controller 106 and the host interface 114 to control and coordinate read and write operations between” the memory and either of the two ports. *Id.*, 3:23-29.



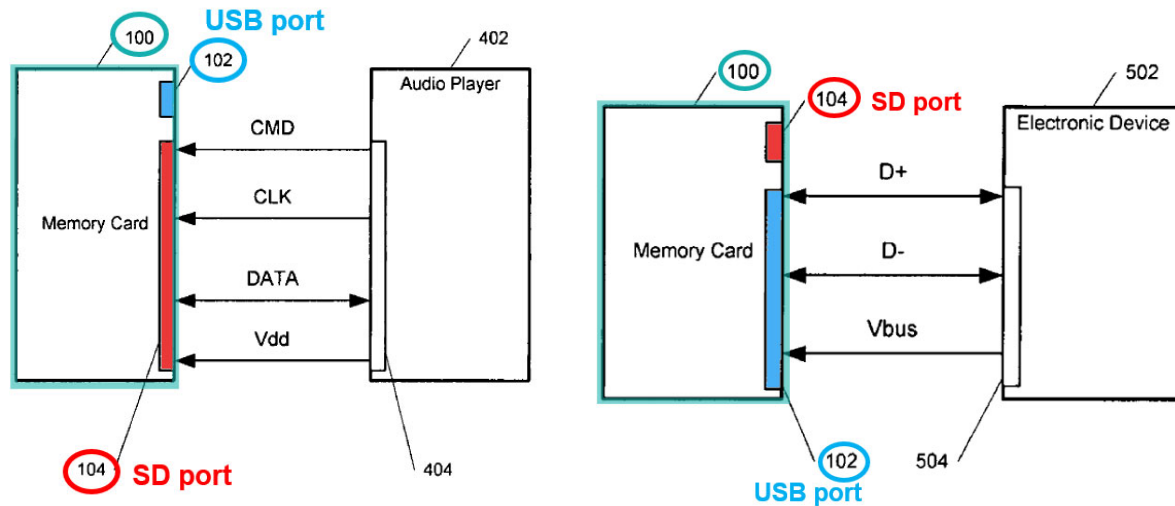
'051 Patent, Fig. 1 (annotated).

Figure 2 shows “an exemplary pinout of an embodiment of a memory card 200 ... that complies with the Secure Digital standard,” where “the SD port shown in Fig. 2 ... includ[es] pins for the voltage Vdd, the command line CMD, the clock link CLK, and the data bus DATA,” whereas “the USB port shown in Fig. 2 includes serial data pins D+ and D-.” '051 Patent, 4:38-61, Fig. 2.



'051 Patent, Fig. 3 (annotated).

Likewise, in Figure 5, data is “transferred between the electronic device 502 and the memory card 100 using the USB protocol” via USB port 102, since “the electronic device 502 does not include a mating SD port.” '051 Patent, 6:3-23. Conversely, in Figure 4, memory card 100’s “SD port 104 interfaces with”—and is “electrically connected to”—“a mating SD port 404 of [an] audio player 402,” whereas “the USB port 102 of the memory card 100 is not electrically connected.” *Id.*, 5:43-53; Ex-1002 ¶¶67-71.



'051 Patent, Figs. 4-5 (annotated).

B. Priority Date

The '051 Patent was filed November 20, 2007, and PO has not alleged an earlier priority date. Petitioner applies this as the priority date. Accordingly, pre-AIA 35 U.S.C. §103 applies and the '051 Patent was never eligible for PGR.

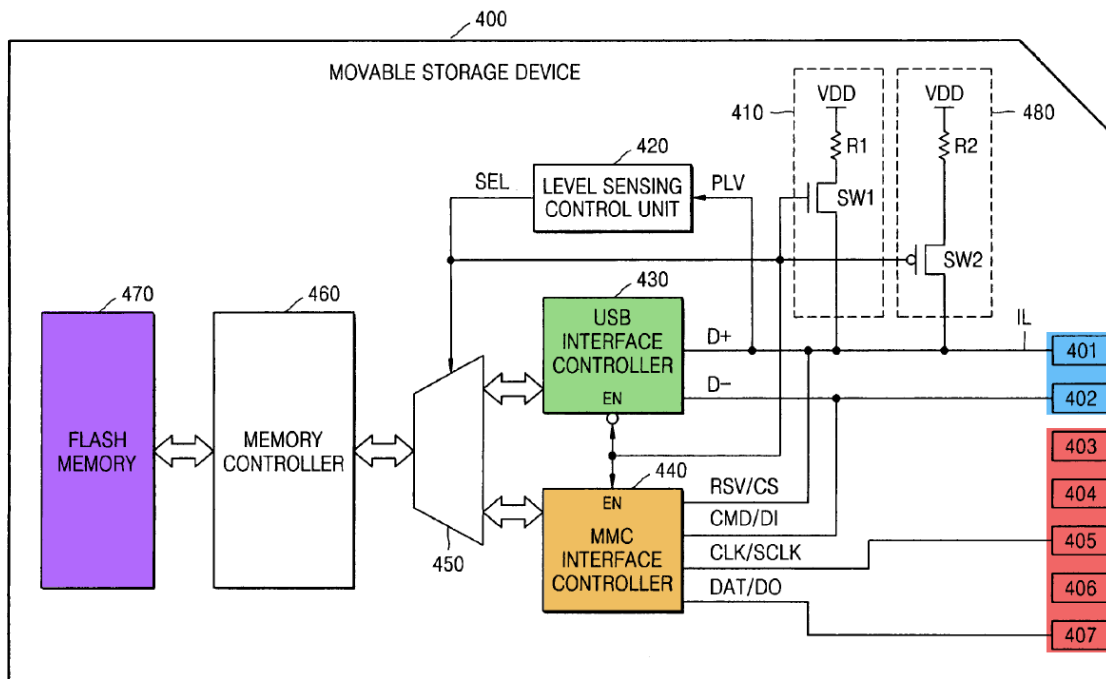
C. Prosecution History of the '051 Patent

The '051 file history is submitted as Ex-1004. Over the course of prosecution, the Examiner issued five rejections, prompting the Applicant to make successive amendments to the pending claims to eventually obtain issuance. Notably, the Examiner relied on the prior art Kim reference (Ex-1022), arguing that Kim's Figure 8 (below) discloses the majority of the '051 Patent's claim elements, including:

- a USB port comprising a first set of pins, and associated “USB controller circuitry” (Kim’s pins 401 and 402, and USB interface controller);
- an I/O port comprising a second set of pins, and associated “I/O controller circuitry” (pins 402, 405, 407, and MMC interface controller);
- a memory in communication with both ports (flash memory 470);
- a housing storing the memory and exposing both ports (movable storage device 400); and
- the ports being “positioned on a same end ... to allow a same-card insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port”

See Ex-1004 at 70-75 (Feb. 14, 2012 Office Action at 2-7).

FIG. 8



Ex-1022, Fig. 8 (annotated); Ex-1004 at 70-75.

The Applicant did not dispute Examiner’s identification of these features in Kim. Instead, the Applicant distinguished Kim—thereby obtaining allowance—by amending the claims to further specify that **“the USB port and the I/O port are positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device.”** Ex-1004 at 46-53 (July 16, 2012 Amendment at 2-9). Applicant emphasized that this feature is consistent with Figure 1 of the ’051 Patent, and beneficially “allow[s] the pin layout for the USB port to be

different from the pin playout for the SD port”—*i.e.*, the USB port’s pinout “does not need to be forced into a particular layout (which may not be compatible with USB standards) in order to conform with the pinout of the second port.” *Id.* at 52-54.

D. Level of Ordinary Skill in the Art

A person of ordinary skill in the art at the relevant time (“POSITA”) would have had a bachelor’s degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory systems, with additional education substituting for experience and vice versa. Ex-1002 ¶74.

V. BRIEF DESCRIPTION OF THE APPLIED PRIOR ART REFERENCES

This petition presents three references, none of which were of record during prosecution. *See* Ex-1004.

A. Diggs (Ex-1005)

Diggs (U.S. Patent Application Pub. No. US2009/0031073) was filed July 26, 2007, and published January 29, 2009. Diggs qualifies as prior art at least under pre-AIA §102(e). Ex-1002 ¶¶91-94.

Diggs discloses “[a] solid-state storage subsystem, such as a non-volatile memory card or drive, [that] includes multiple interfaces”—*i.e.*, “multiple physical connectors and bus structures for different signal interfaces”—“and a memory area

[for] storing information.” Diggs, Abstract ¶10. Diggs’s storage subsystem may be “simultaneously connected across multiple host systems, using ... a priority management scheme for handling multiple data access commands.” Diggs ¶12; *see also id.*, 9. Figure 2 shows multiple host systems (210, 211, and 212), each “utiliz[ing] a different signal interface to communicate with storage subsystem 100”—including a “USB interface 220” and “an IEEE-1394 interface 221.” Diggs, ¶¶39, 26, Fig. 2. “Each recording system”—*i.e.*, host—“may be connected to the storage subsystem 100 with a corresponding physical connector 223, 234, and 235 and over a bus structure 236, 237, and 238.” Diggs ¶40. In Figure 2, “audio recording system 210 is connected to USB controller 230 [while] video recording system 211 is connected to IEEE-1394 controller 231 ... Accordingly, physical connector 233 may be a USB mini-A connector [while] physical connector 234 may be a four-pin Firewire connector,” and “[b]us structures 236 [and] 237 ... correspond to USB [and] IEEE-1394, bus structures ... respectively.” Diggs ¶40.

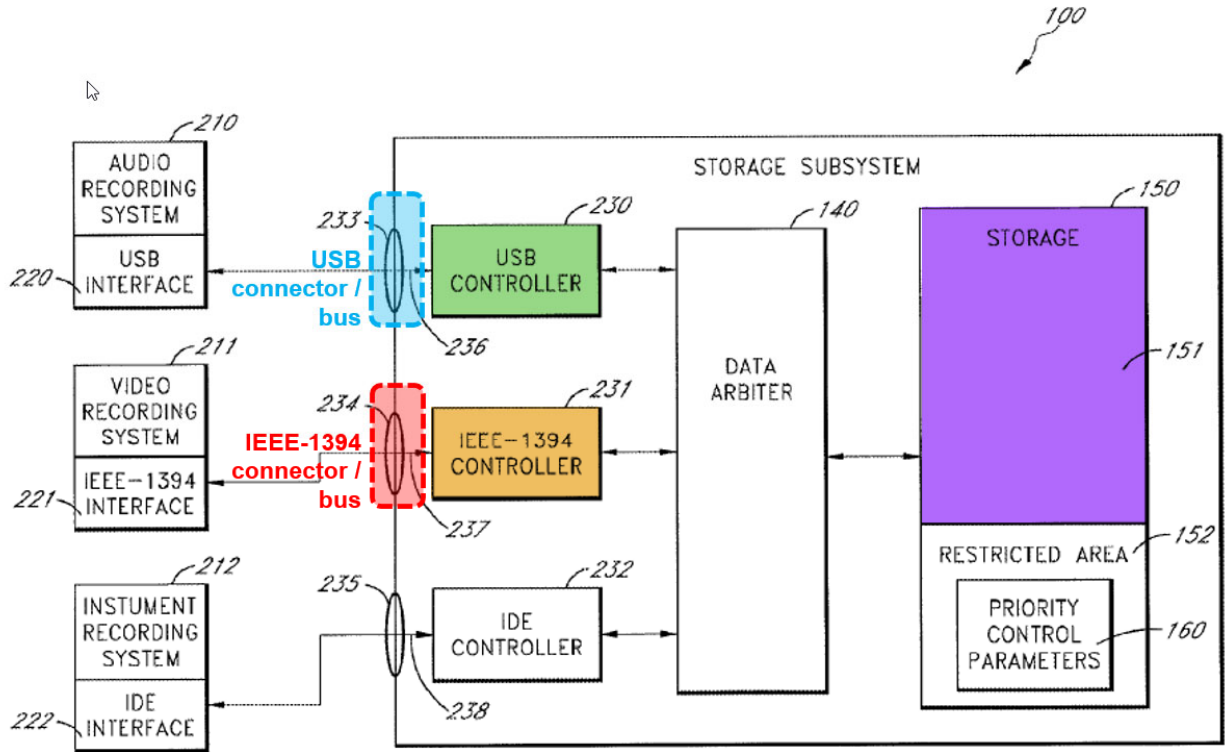


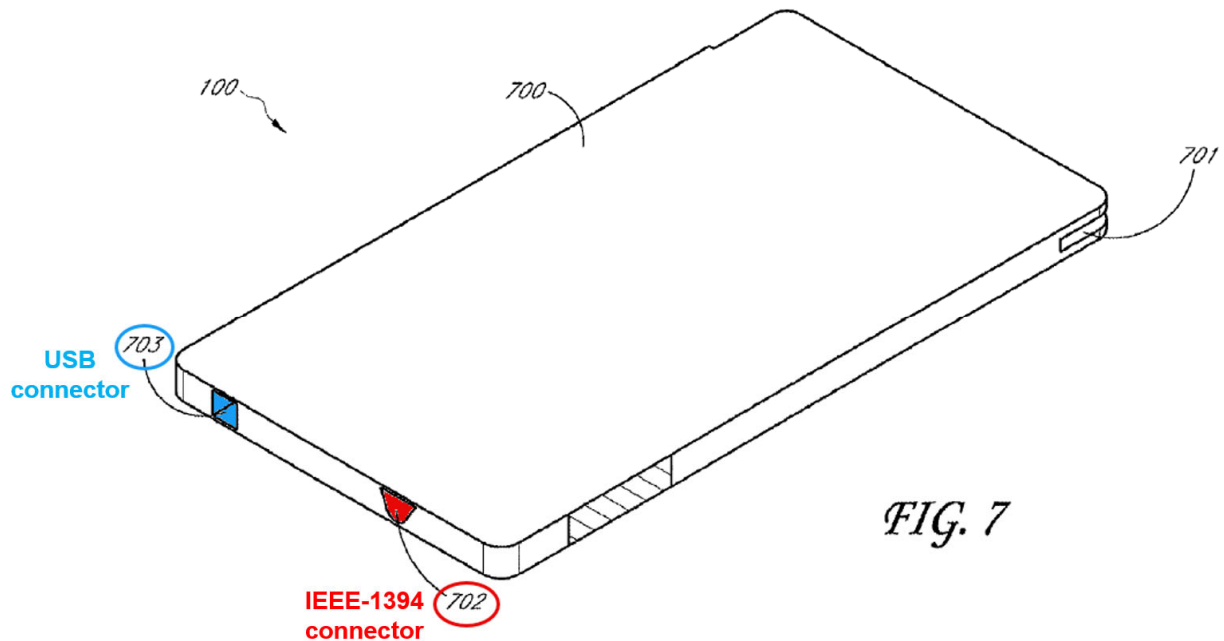
FIG. 2

Diggs, Fig. 2 (annotated).

“The storage subsystem 100 further comprises a storage 150,” which includes “user data memory area 151 that is generally accessible by the operating systems of [the] host systems.” Diggs ¶¶30, 38. “Data arbiter 140 is responsible for prioritizing read/write commands received simultaneously from [the] multiple controllers,” and does so based on “priority control parameters 160” that are stored in “a restricted memory area 152 of the storage 150.” Diggs ¶¶32-34.

The storage subsystem 100 of Figure 2 may have the “PC Card form factor” shown in Figure 7. Diggs ¶55. The subsystem includes “three [separate] physical

connectors 701, 702, and 703. . . Physical connector 702 comprises a USB mini-A connector and is connected to a USB con[troller] over a USB bus structure. Physical connector 7[0]3 comprises an IEEE-1394 four-pin connector, and is connected to an IEEE-1394 controller using IEEE-1394 bus structure.” Diggs ¶55.²



Diggs, Fig. 7 (annotated).

B. Lin (Ex-1007)

Lin (U.S. Patent Application Pub. No. US 2006/0053241) was filed on July 27, 2005, and was published on March 9, 2006. Lin qualifies as prior art under at least pre-AIA §102(b). Ex-1002 ¶¶95-98.

² Paragraph 55 of Diggs appears to include two typos: “793” should instead read “703,” and “USB connector” should instead read “USB controller.” See Ex-1002 ¶94, n.1.

Lin discloses “a removable memory card standard and method thereof.” Lin, ¶2. Lin’s memory card—referred to as “electronic device 30”—“is able to support modes of operations compatible with” different standard applications. Lin ¶29. As illustrated in Fig. 1A, “electronic device 30 includes an interface (IF) mode detector 32” that “detects a mode of operation to distinguish among an MMC [(multi-media card)] mode, a USB mode[,], or a Mu mode when electronic device 30 is inserted into a host 40.” Lin ¶31. Device 30 also features an MMC “device controller 34, a wrapper 35, a universal serial bus (USB) physical layer (PHY) circuit 36, [and] a USB device controller 37.” Lin ¶31. Finally, the device includes an “[a]pplication module 38 [that] functions to serve as a memory storage or an input/output (I/O) interface, depending on the operation mode detected.” Lin ¶31.

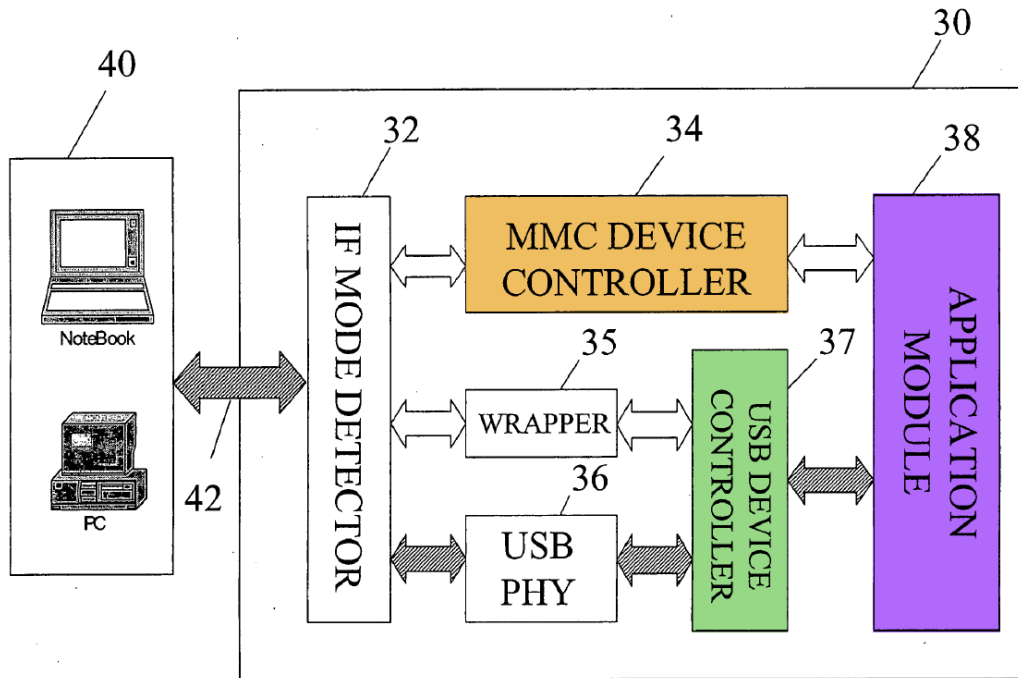


FIG. 1A

Lin, Fig. 1A (annotated).

“Fig. 4A is a proposed pin assignment chart” for Lin’s electronic device. Lin ¶38. For example, “[t]he fourteenth and fifteenth pins for the USB mode, *i.e.*, D+ and D-, are a pair of data signals, which may be used to determine whether the USB mode is selected.” Lin ¶38. The Fig. 4A assignment chart also features “MMC 4.0 [and] MMC SPI (serial-peripheral interface) applications,” as well as “Mu-interface applications.” Lin ¶¶29, 38.

	I/O Port		USB Port	
Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3	VDD	VDD	VDD	VDD
4	VDD	VDD	VDD	VDD
5	CLK	SCLK		CLK
6	VSS	VSS	VSS	VSS
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

second set of pins

first set of pins

FIG. 4A

Lin, Fig. 4A (annotated).

Lin’s electronic device, as further depicted in the Fig. 5, features “a notch 102 on the upper left-hand corner to prevent incorrect insertion of electronic device 100,” and “a plurality of interweaving contact pads labeled 1 to 20, which correspond to the pins illustrated in Fig. 4A.” Lin, ¶¶106-107.

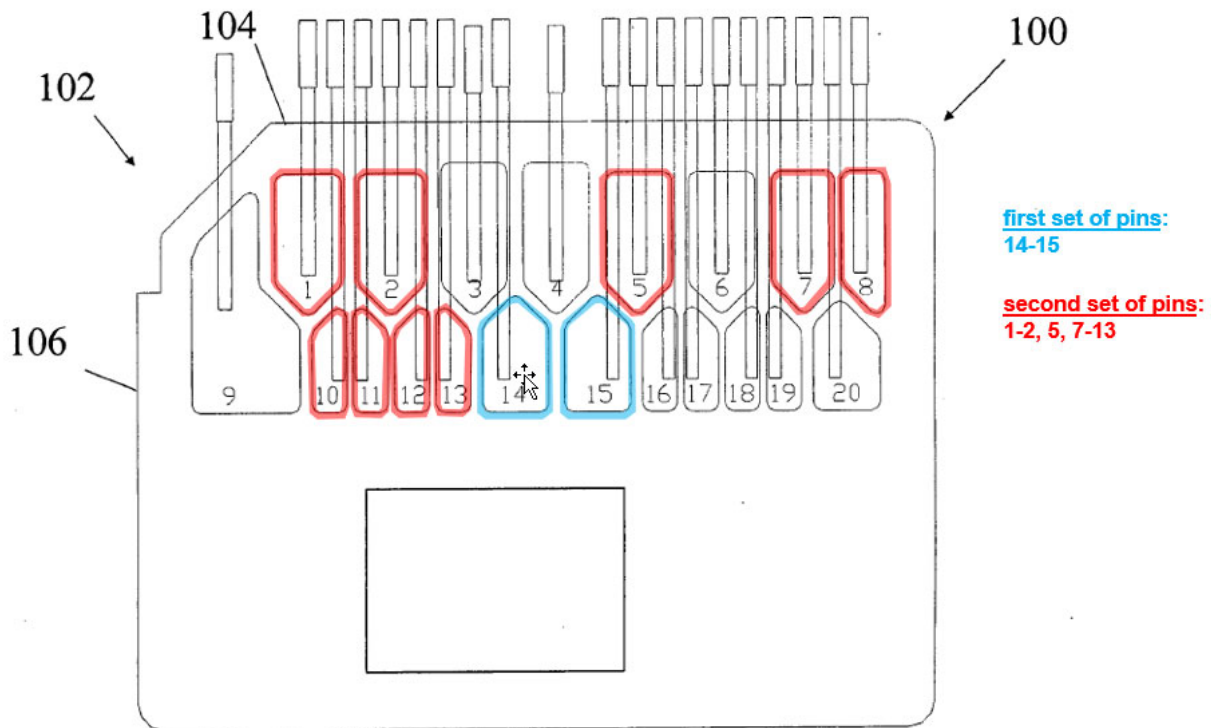


FIG. 5

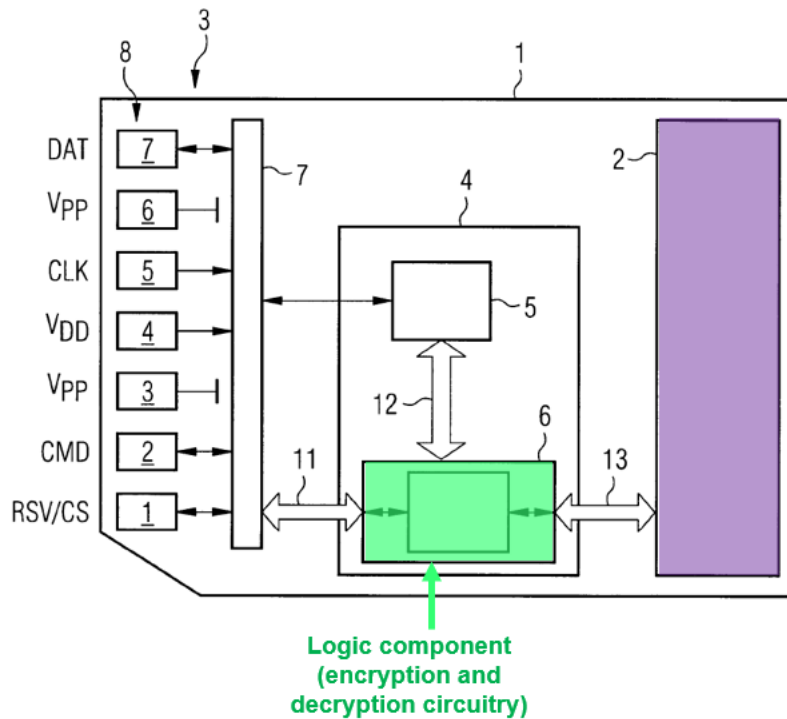
Lin, Fig. 5 (annotated).

C. Thorsten (Ex-1009)

German Patent Application Publication No. DE 10220629A1 to Thorsten (Ex-1008) (certified translation, Ex-1009 (“Thorsten”)) was filed on August 5, 2002, and was published on November 27, 2003. Thorsten qualifies as prior art under at least pre-AIA §102(b). Ex-1002 ¶¶99-102.

Thorsten discloses a “data carrier”—e.g., memory card—“comprising a non-volatile memory, a data interface via which data can be written to and read from the non-volatile memory, and an interface module which is connected between the data interface and the memory and by way of which the data can be encrypted and/or

decrypted.” Thorsten ¶1. As shown in Figure 1, “the interface module comprises a logic component” (light green) “that is responsible for the encryption and/or decryption process.” Thorsten ¶8.



Thorsten, Fig. 1 (annotated).

Specifically, “[d]ata to be transmitted from the data interface 3 to the memory 2 is encrypted in the logic component 6. When reading data from the memory card, data is transmitted from the memory 2 to the data interface 3, with decryption being performed by the logic component 6.” Thorsten ¶15. Thorsten explains that the logic component may be provided “by means of a function-programmable logic circuit.” Thorsten ¶10. Figure 1 shows that “the data path for encryption and decryption runs exclusively via the logic component 6, but not via the controller 5,” Thorsten ¶15,

but Thorsten also states that “[i]n an advantageous implementation, the logic component 6 is designed as an additional module of a chip card controller 5. This enables a compact and cost-effective implementation.” Thorsten ¶17.

Thorsten acknowledges that “[i]f the data is sensitive, the data is usually stored in encrypted form,” Thorsten ¶2, but also teaches “it is advantageous if the card itself”—rather than the host device—“handles the encryption and decryption, since in this case it is not necessary to know in advance which applications the memory card is to work with, and it is not necessary to ensure that these applications have the appropriate algorithms.” Thorsten ¶4.

VI. CLAIM CONSTRUCTION

Petitioner interprets the ’051 Patent’s claims according to the *Phillips* claim construction standard. 37 C.F.R. §42.100(b). To resolve this Petition, Petitioner does not believe that any term requires express construction because the prior art teaches the claims under the plain meaning of all of the recited claim terms.³ CTPG, 44; Ex-1002 ¶¶75-76.

Of note, the claims recite a “USB port” and an “I/O port” that “*are positioned such that* when the I/O port is electrically connected with the host device, at least

³ Petitioner respectfully reserves all rights to raise claim construction and other arguments in district court. Additionally, Petitioner will request leave to submit the district court’s claim construction as soon as it becomes available. Moreover, should PO raise implied claim construction arguments in its Preliminary Response, Petitioner will respectfully seek a Preliminary Reply to respond. CTPG, 44-45.

one of the first set of pins of the USB port is not electrically connected to the host device, and when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device.” See ’051 Patent, Cls. 1, 9, 16. That is, each port has distinct positioning requirements.

Grounds 1-2, involving the Diggs reference, render the claims obvious by teaching two ports positioned as physically separate ports. Additionally, Grounds 3-4, involving the Lin reference, *also* render the claims obvious by teaching a memory card having two subsets of pins corresponding to logically separate ports.

VII. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS

The ’051 Patent contains 27 claims. This Petition challenges independent Claims 1, 9, and 16 (directed to “a portable handheld memory card” or method of using the same), as well as dependent Claims 2, 4-8, 17-21, and 23-27. The subject matter of the challenged claims is disclosed by the prior art as shown below. Ex-1002 ¶¶103, 235.

A. Ground 1: Claims 1, 4-8, 16, 20-21, and 23-27 Are Obvious Over Diggs

As shown below, the subject matter of Claims 1, 4-8, 16, 20-21, and 23-27 are taught by Diggs alone. Ex-1002 ¶¶104-150.

1. Claim 1

a. Element 1[preamble]: A portable handheld memory card comprising:

If Claim 1's preamble is limiting, Diggs discloses it. Ex-1002 ¶¶105-106. Diggs discloses a “a solid state storage subsystem, such as a *memory card*” (below, teal). See, e.g., Diggs, Abstract; see also *id.* ¶¶60; Figs. 2, 7 (“storage subsystem 100”).

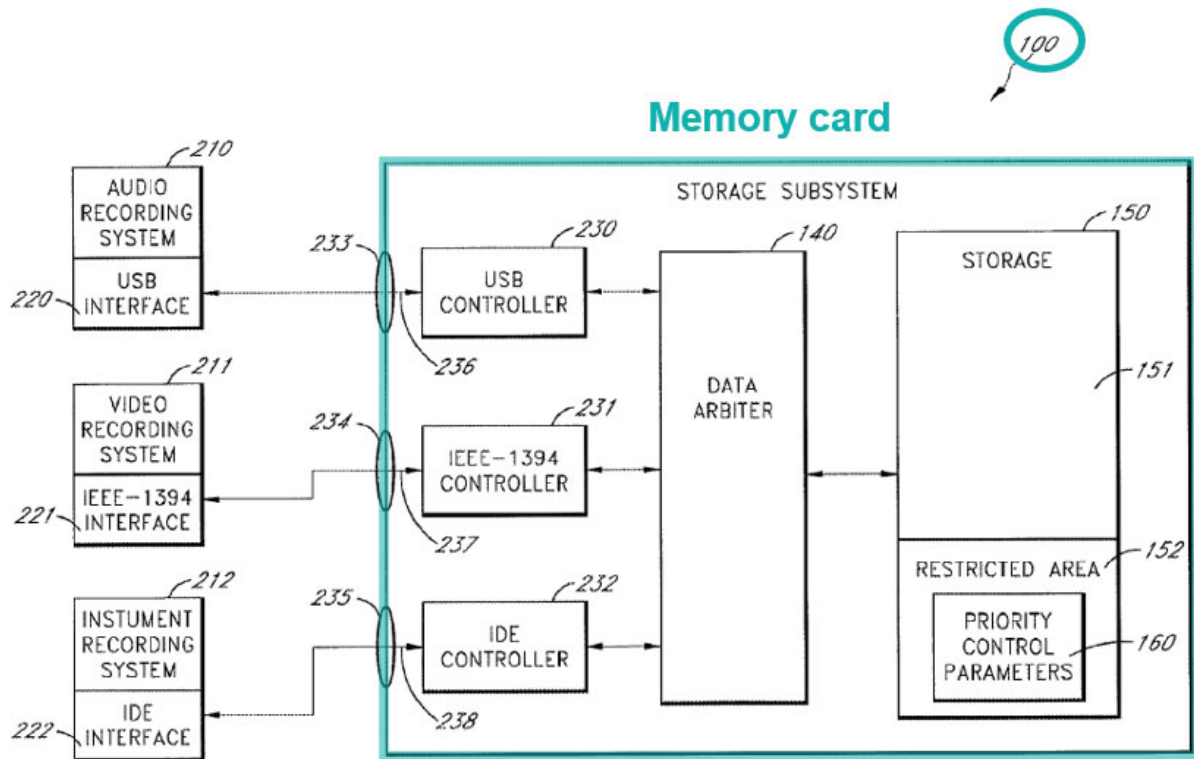
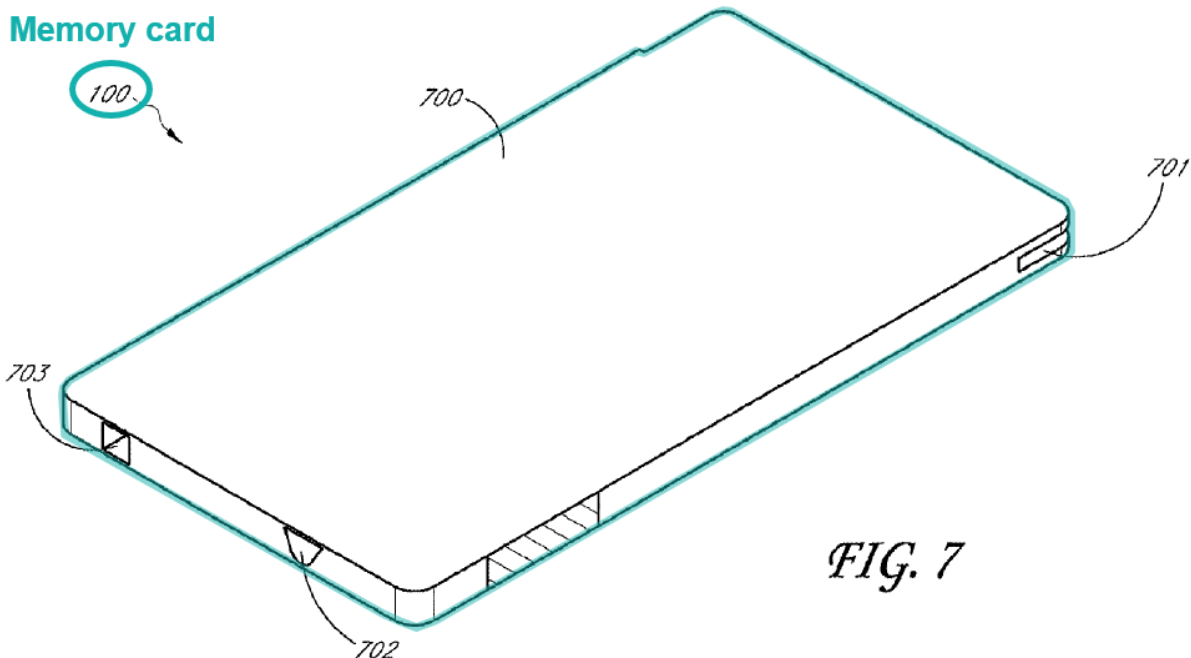


FIG. 2

Diggs, Fig. 2 (annotated).



Diggs, Fig. 7 (annotated).

Diggs further characterizes “[s]torage subsystem 100” as a “*portable* memory device having a card type form factor,” Diggs ¶49, and explains that it is “a *detachable* device” that may be “*inserted* into a PC Card slot on a host system,” Diggs ¶¶10, 55. A POSITA would have understood that a user that “inserts” or “detaches” the card does so with his hands, such that the memory card is “handheld” while the user is holding it before or after such actions. Diggs’ memory card includes a housing 700 (see Element 1[f], *infra*), which a POSITA would have recognized as protecting internal components from dust, moisture, or impact, thus further confirming the “handheld” nature of the card. Ex-1002 ¶106.

b. Element 1[a]: a Universal Serial Bus (USB) port comprising a first set of pins;

Diggs discloses Element 1[a]. Ex-1002 ¶¶107-110. Diggs’s solid-state storage subsystem “includes multiple physical connectors and bus structures for different signal interfaces.” Diggs ¶10. In Figure 2, an external host “audio recording system 210 is connected to USB controller 230... Accordingly, **physical connector 233** may be a USB mini-A connector” and “[b]us structure[] 236” corresponds to a USB bus structure. Diggs ¶40. The USB mini-A connector 233, alone or in combination with the USB bus structure 236, collectively form a “**Universal Serial Bus (USB) port,**” as annotated in Figure 2 (blue).

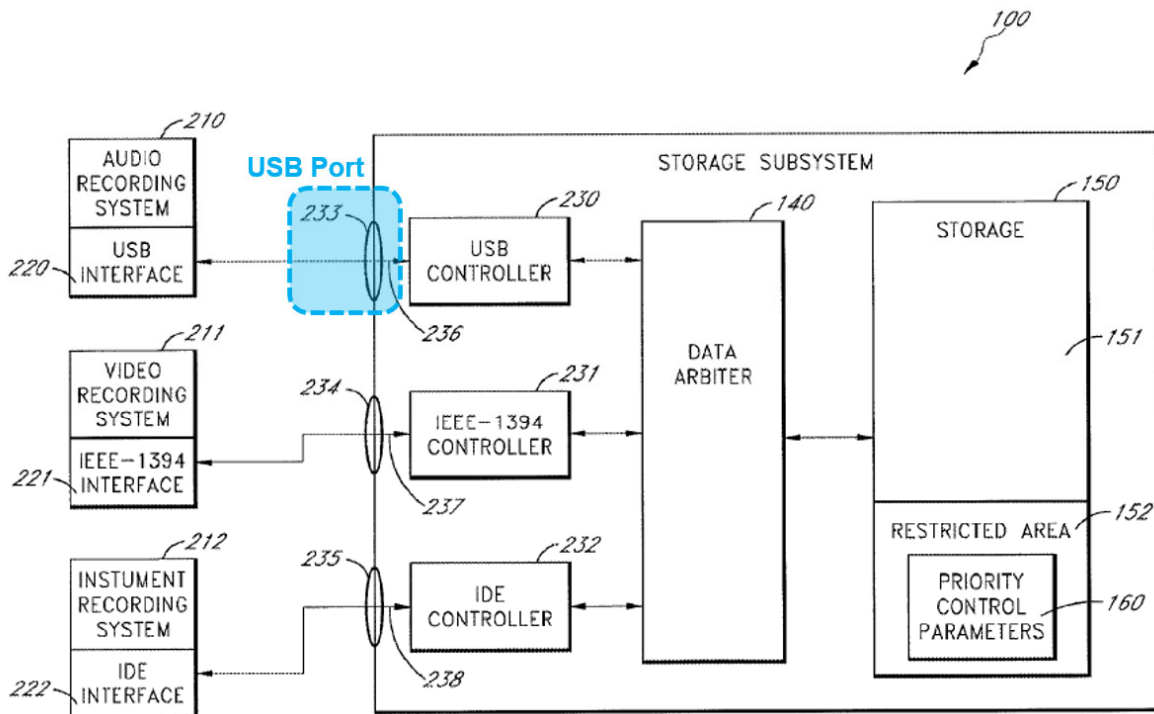
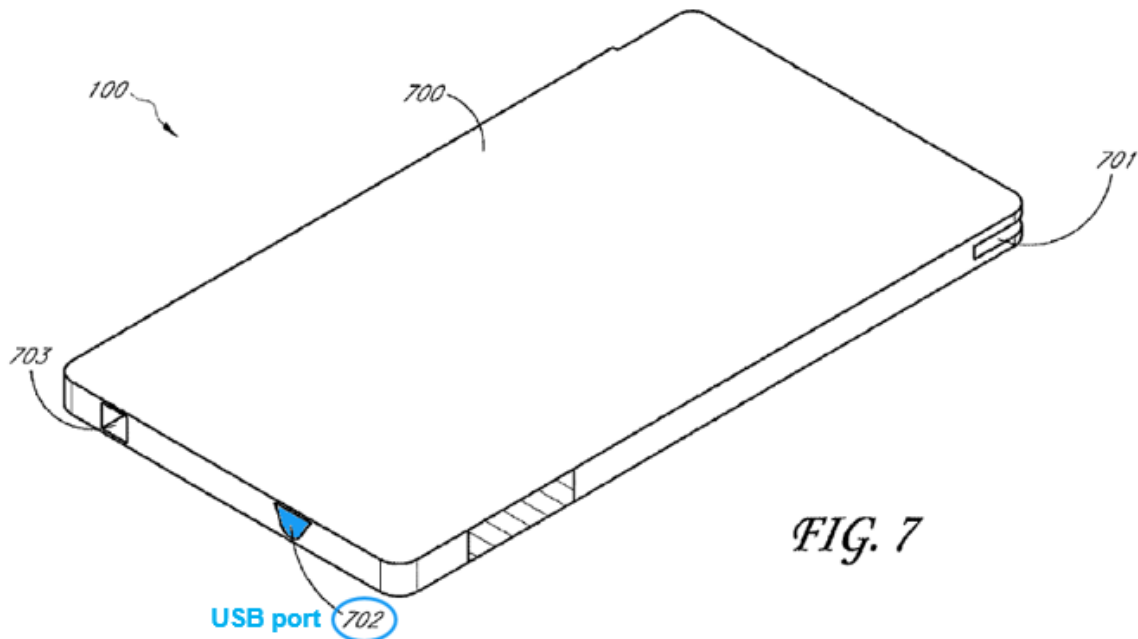


FIG. 2

Diggs, Fig. 2 (annotated).

Diggs’s Figure 7 also shows the USB port (blue). Diggs explains that “[p]hysical connector 702 comprises a USB mini-A connector and is connected to a USB con[troller] over a USB bus structure.” Diggs ¶55.



Diggs, Fig. 7 (annotated).

Further, while Diggs does not explicitly identify the electrical pins associated with its physical connectors (*i.e.*, ports), it was well-understood to POSITAs that the USB mini-A standard is implemented with a set of five pins. This demonstrated in the “On-The-Go” Supplement to the USB 2.0 Specification (Ex-1025, “USB mini-A Specification”),⁴ where the following “Pin Assignment” table shows “[t]he usage

⁴ Retrieved from https://web.archive.org/web/20060114004406/http://www.usb.org/developers/onthego/OTG1_0a%28PDFs%29.zip (captured on Jan. 14, 2006) on March 24, 2025.

and wiring assignments of the five pins in the Mini-A plug.” Ex-1025 at 10; Ex-1002 ¶¶109-110.

Table 4-2. Mini-A Plug Pin Assignments

Contact Number	Signal Name	Typical Wiring Assignment
1	VBUS	Red
2	D-	White
3	D+	Green
4	ID	< 10 Ω to GND
5	GND	Black
Shell	Shield	Drain Wire

Ex-1025 at 10.

As reflected above, the USB mini-A includes data pins D- and D+ for pins 2 and 3, respectively. Ex-1025 at 10. Thus, Diggs’s USB port comprises a corresponding “first set of pins” (e.g., data pins 2 and 3).⁵ Ex-1002 ¶110.

⁵ The three remaining power pins—*i.e.*, pin 1 (connected to VBUS) and pins 4 and 5 (connected to GND)—are not required to satisfy the claim’s recitation of a “first set of pins,” but they are each additional pins that comprise a “set of pins” under the applicable USB specifications. Ex-1002 ¶110, n.3.

c. **Element 1[b]: USB controller circuitry electrically connected with the first set of pins of the USB port; and**

Diggs discloses Element 1[b]. Ex-1002 ¶¶111-112. As discussed for Element 1[a], Diggs’s memory card includes a “USB controller 230,” as shown in Figure 2 (green). Diggs ¶40, Fig. 2.

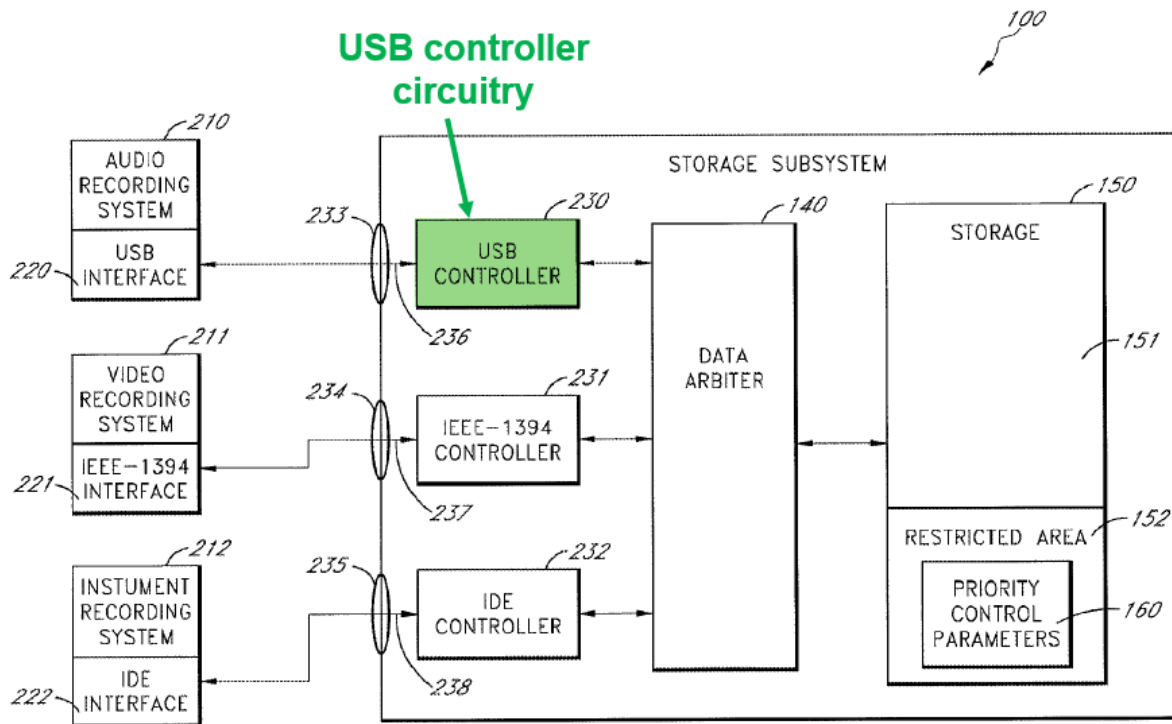


FIG. 2

Diggs, Fig. 2 (annotated).

Diggs explains that USB controller 230 “may receive storage access commands from a host system and translate these signals to access storage 150.” Diggs ¶40; *see also id.* ¶29. In Figure 2, the host “audio recording system 210 is *connected to* USB controller 230,” in order to facilitate these commands, which are

received over the USB mini-A connector 233. Diggs ¶40. Accordingly, the USB controller 230 circuitry is “electrically connected with the first set of pins of the USB port.” Ex-1002 ¶112.

d. Element 1[c]: an input/output (I/O) port comprising a second set of pins; and

Diggs discloses this Element 1[c]. Ex-1002 ¶¶113-115. In addition to its USB physical connector and corresponding USB bus structure, Diggs’s storage subsystem includes “**physical connector 234** [that] may be a four-pin Firewire connector,” **and corresponding bus structure 237** which is “IEEE-1394” compliant. Diggs ¶40; *see also id.* ¶4 (“[T]he IEEE-1394 signal interface is commonly used for video applications because of the high data rates involved”). The physical connector 234, alone or in combination with the IEEE-1394 bus structure 237, collectively form “**an input/output (I/O) port,**” as annotated in Figure 2 (red); Ex-1002 ¶113.

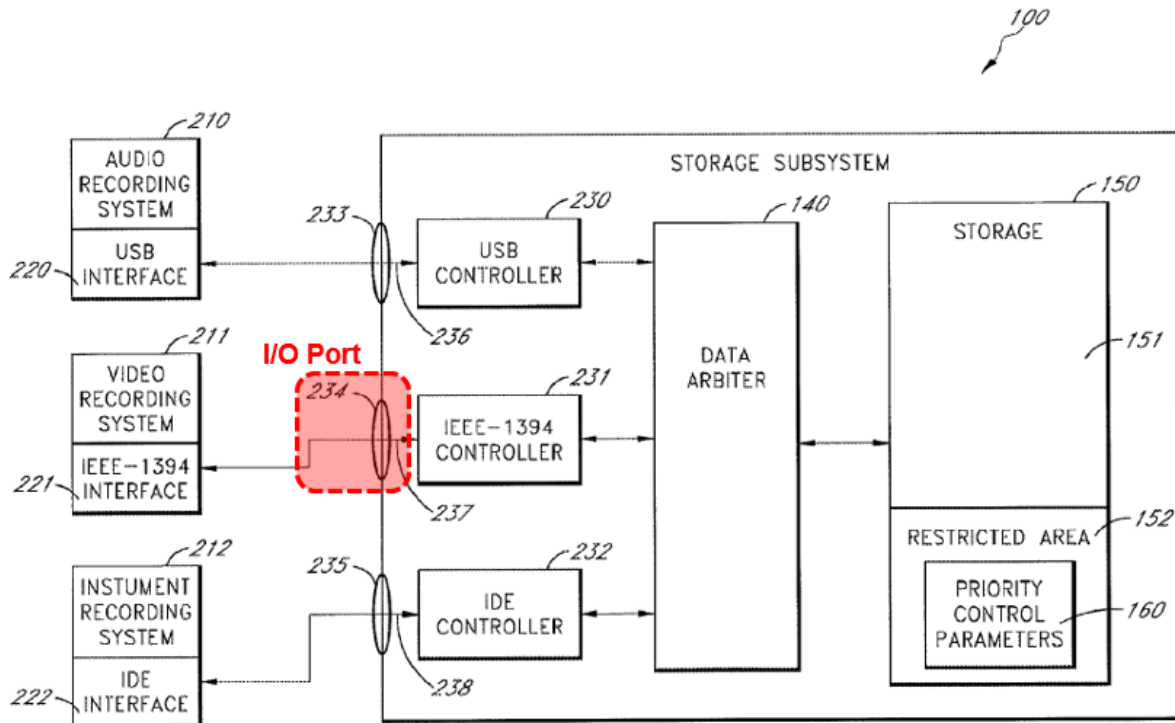
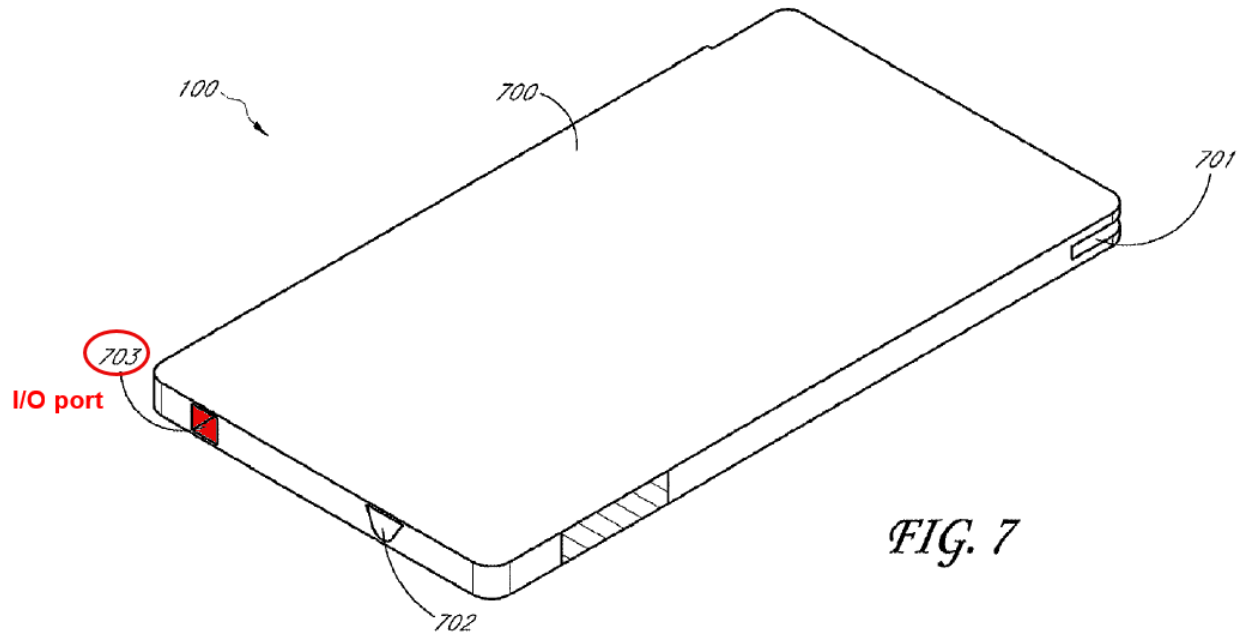


FIG. 2

Diggs, Fig. 2 (annotated).

Figure 7 also shows the I/O port (red). Diggs explains that “[p]hysical connector 7[0]3 comprises an IEEE-1394 four-pin connector, and is connected to an IEEE-1394 controller using [an] IEEE-1394 bus structure.” Diggs ¶55.



Diggs, Fig. 7 (annotated).

The *four pins* associated with Diggs’s IEEE-1394 physical connector 233 constitute the claimed “second set of pins” of the I/O port.⁶ Diggs ¶¶40, 55. Further, a POSITA would have understood that Diggs’s second set of pins would have the signal assignment shown in the following table, from the IEEE-1394 four-pin Specification (Ex-1029). Ex-1002 ¶115.

⁶ It was well-understood by POSITAs that the “four-pin Firewire connector” associated with the IEEE-1394 carries only data, not power. Ex-1002 ¶115, n.4; Ex-1029 at 27.

Table 4-11A — Connector socket signal assignment

Contact number	Signal name	Comment
1	TPB*	Strobe on receive, data on transmit (differential pair)
2	TPB	
3	TPA*	Data on receive, strobe on transmit (differential pair)
4	TPA	
Shell	VG	Necessary for ground reference

Ex-1029 at 35.

e. Element 1[d]: I/O controller circuitry electrically connected with the second set of pins of the I/O port;

Diggs discloses Element 1[d]. Ex-1002 ¶¶116-117. As discussed for Element 1[a], Diggs’s memory card includes an “IEEE-1394 controller 231,” as shown in Figure 2 (orange). Diggs ¶40, Fig. 2.

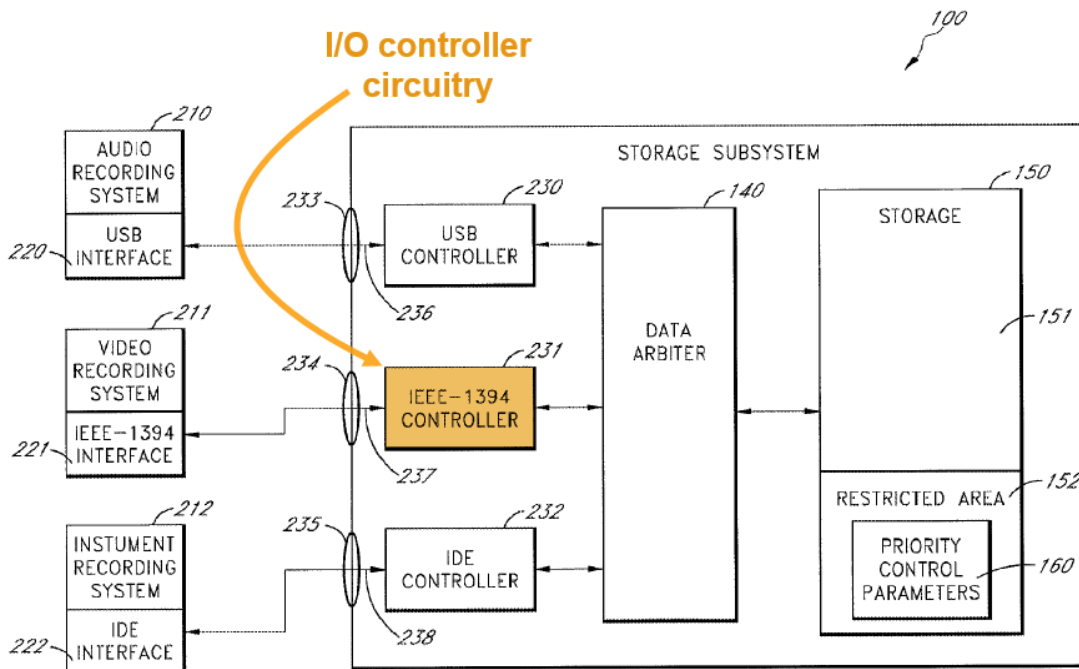


FIG. 2

Diggs, Fig. 2 (annotated).

As with USB controller 230, the IEEE-1394 controller 231 “may receive storage access commands from a host system and translate these signals to access storage 150.” Diggs ¶40; *see also id.* ¶29. In Figure 2, the host “video recording system 211 is *connected to* IEEE-1394 controller 231,” in order to facilitate these commands, which are received over the IEEE-1394 four-pin Firewire connector 234. Diggs ¶40. Accordingly, the IEEE-1394 controller 231 circuitry is “electrically connected with the second set of pins of the I/O port.” Ex-1002 ¶117.

f. Element 1[e]: a memory in communication with the USB port and the I/O port; and

Diggs discloses Element 1[e]. Diggs discloses that “[t]he storage subsystem 100 comprises a storage 150” that in turn “may comprise a plurality of solid-state storage devices.” Diggs ¶30. Storage 150 is separated into “a restricted memory area 152 [that] stores priority control parameters 160” and a “user data memory area 151 that is generally accessible by the operating systems of [the] host systems.” Diggs ¶¶34, 38; *see also id.* ¶26 (“The host systems ... execute driver programs ... that provide functionality for communicating with the subsystem 100.”). Further, the Figure 2 storage subsystem is “simultaneously connected across multiple host systems”—*i.e.*, “audio recording system 210” and “video recording system 211—via the “USB port” and “I/O port” identified for Elements 1[a] and 1[c]. Thus, Diggs’s storage 150—or, specifically, user data memory area 151—is “a memory in

communication with the USB port and I/O port.” Ex-1002 ¶118.

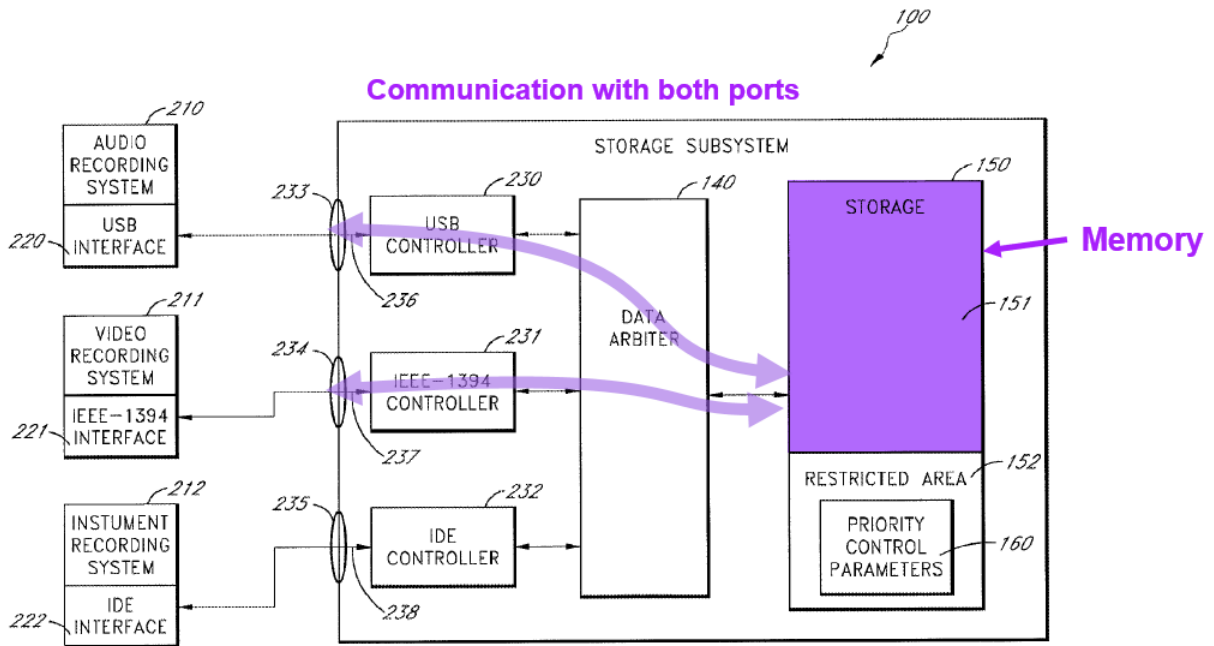
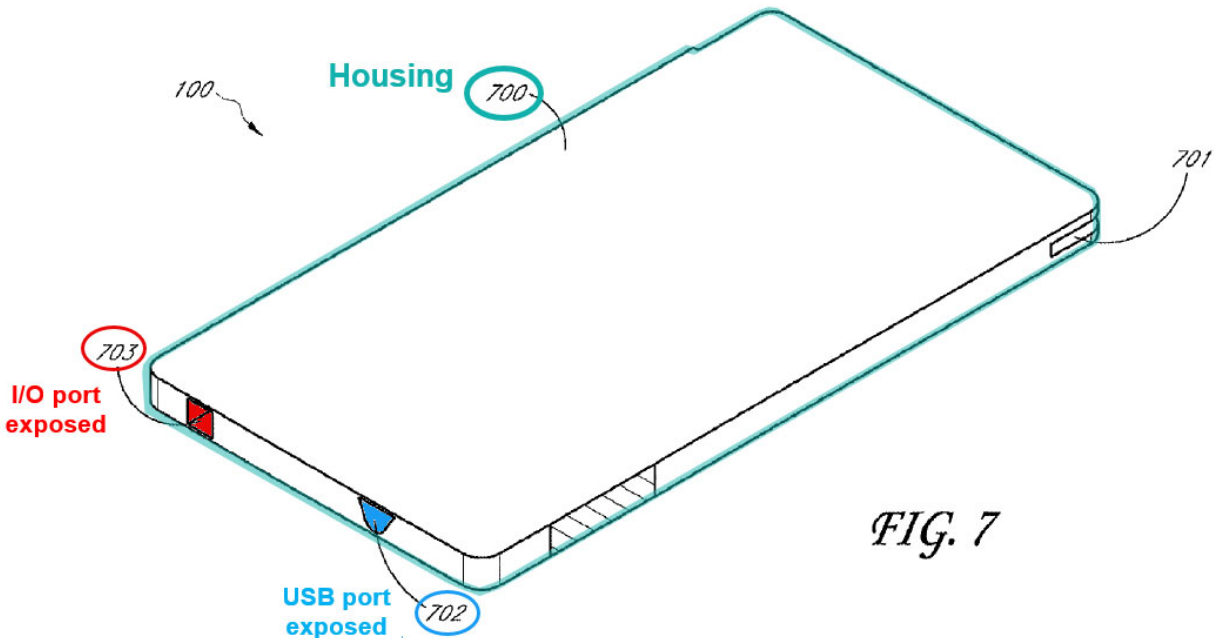


FIG. 2

Diggs, Fig. 2 (annotated).

- g. **Element 1[f]: a housing storing the memory and exposing the USB port and the I/O port;**

Diggs discloses Element 1[f]. In Figure 7, for example, “[s]torage subsystem 100 is shown with a PC Card *housing* 700,” which houses the storage 150. Diggs ¶155, Cl. 1.



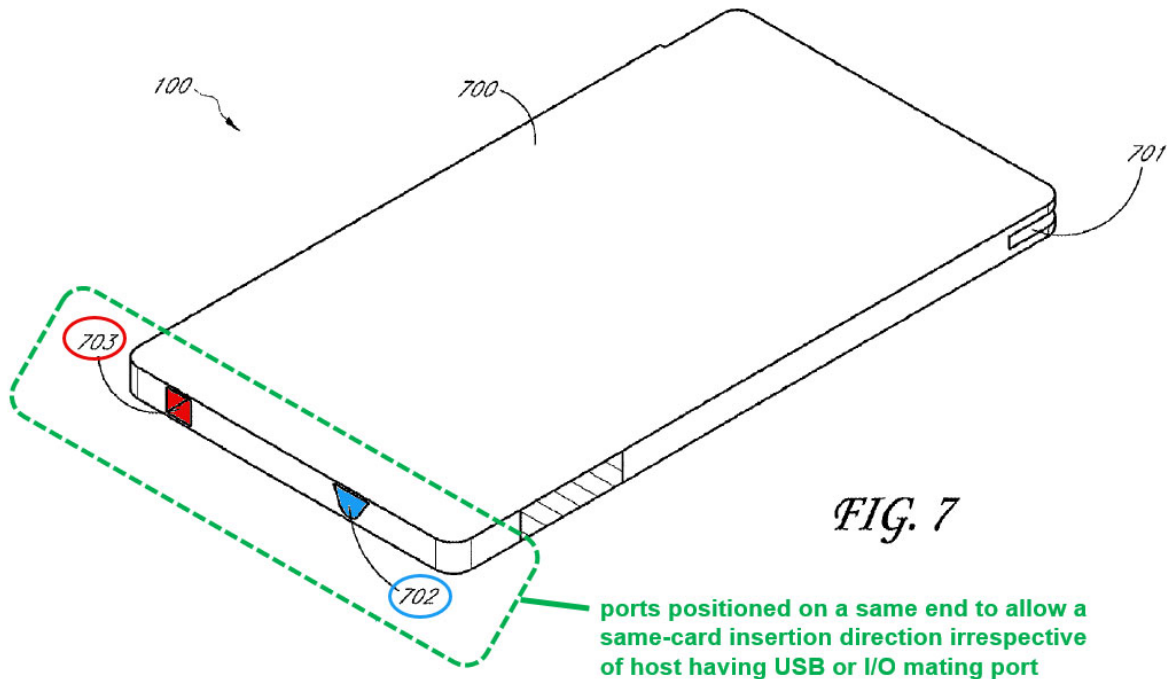
Diggs, Fig. 7 (annotated).

Figure 7 features a “[p]hysical connector 702” (*i.e.*, “a USB mini-A connector”) and a “[p]hysical connector 7[0]3” (*i.e.*, “an IEEE-1394 four-pin connector”). Diggs ¶55. As shown in Figure 7, “[p]hysical connector 702 and 703 are further *accessible to be connected* to USB and IEEE-1394 cable connections from additional host systems”—*i.e.*, those USB and I/O ports are *exposed* by the housing 700. Ex-1002 ¶¶119-120.

- h. Element 1[g]: wherein the USB port and the I/O port are positioned on a same end to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port; and**

Diggs discloses Element 1[g]. In Diggs’s memory card (*i.e.*, storage subsystem 100), the USB port and I/O port (702 and 703, respectively) are

positioned on the “same end”—*i.e.*, the near, left end of the card in the perspective view of Figure 7. Diggs ¶55, Fig. 7.



Diggs, Fig. 7 (annotated).

Further, this positioning “allow[s] a same-card insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port,” because, as Diggs explains, the “[p]hysical connector[s] 702 and 703 are [] accessible to be connected” in that direction—*i.e.*, the near, left end-direction of the card—“to USB and IEEE-1394 cable connections from additional host systems.” Diggs ¶55; Ex-1002 ¶¶121-122.

- i. **Element 1[h]: wherein the USB port and the I/O port are positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and**

Diggs discloses Element 1[h]. As shown and described for Figures 2 and 7, Diggs's USB port 702 and I/O port 703 are separate "physical connector" receptacles. Diggs, Figs. 2, 7, ¶¶40, 55. Accordingly, their corresponding "first" and "second" sets of pins (identified for Elements 1[a] and 1[c], respectively) are likewise physically separate. Thus the positioning of these ports are such that "when the I/O port is electrically connected with the host device"—e.g., with video recording system 211, using an IEEE-1394 cable connection (Diggs ¶¶39, 55)—"at least one of the first set of pins of the USB port is *not electrically connected* to the host device" because, in that circumstance, none of the USB mini-A pins (*see* Element 1[a], *supra*) are electrically connected with that IEEE-1394-compatible video recording system 211. Indeed, since the "host device" to which the I/O port is connected (video recording system 211) only has an IEEE-1394 interface, and no USB interface, it is not designed to connect to the USB port. *See* Diggs ¶39 ("Each [host] system may utilize a **different** signal interface to communicate with storage subsystem 100."). Ex-1002 ¶123.

- j. Element 1[i]: when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device.**

Diggs discloses Element 1[i]. As discussed for Element 1[h], Diggs's USB port 702 and I/O port 703 are separate "physical connector" receptacles. Diggs, Figs. 2, 7, ¶¶40, 55. Accordingly, their corresponding "first" and "second" sets of pins (identified for Elements 1[a] and 1[c], respectively) are likewise physically separate. Thus the positioning of these ports are such that "when the USB port is electrically connected with the host device"—*e.g.*, with audio recording system 210, using a USB cable connection (Diggs ¶¶39, 55)—"at least one of the second set of pins of the I/O port is *not electrically connected* to the host device" because, in that circumstance, none of the four IEEE-1394 Firewire connector pins (*see supra* Element 1[c]) are electrically connected with that USB-compatible audio recording system 210. Indeed, since the "host device" to which the USB port is connected (audio recording system 210) only has a USB interface, and no IEEE-1394 interface, it is not designed to connect to the I/O port. *See* Diggs ¶39 ("Each [host] system may utilize a **different** signal interface to communicate with storage subsystem 100."). Ex-1002 ¶124.

- 2. Claim 4: The portable handheld memory card of claim 1 further comprising: a power management unit in communication with the USB controller circuitry.**

Diggs teaches the further requirement of "a power management unit in

communication with the USB controller circuitry.” For example, Diggs acknowledges “power consumption” as a design constraint for solid-state storage subsystems generally. Diggs ¶4. Further, “[e]ach controller ... may be configured to write data to, and read data from, the storage 150 in response to memory/storage access commands from hosts,” which entails “translat[ing] control, address, and data signals into storage access commands to storage 150. Controllers ... may also access and transmit data from storage 150 to host systems.” Diggs ¶29. Further, the USB mini-A Specification (Ex-1025) confirms that Diggs’s USB mini-A port (*i.e.*, physical connector 230 (Fig. 2) or 702 (Fig. 7)) includes a “VBUS” pin that is connected to power management circuitry on the memory card, as required for USB mini-A compliance. *See* Ex-1025, 41-44 (“A-device electrical requirements”); Ex-1002 ¶125.

Moreover, as shown in the below modification of Diggs’s Figure 2, a POSITA would have been motivated to implement, in Diggs’s memory card, a power management unit in communication with each of the controllers (including USB controller 230) to ensure that, when Diggs’s device is connected to respective host devices like those shown in Figure 2, its power source voltage requirements are adjusted to comply with each of the applicable standards. Ex-1002 ¶126.

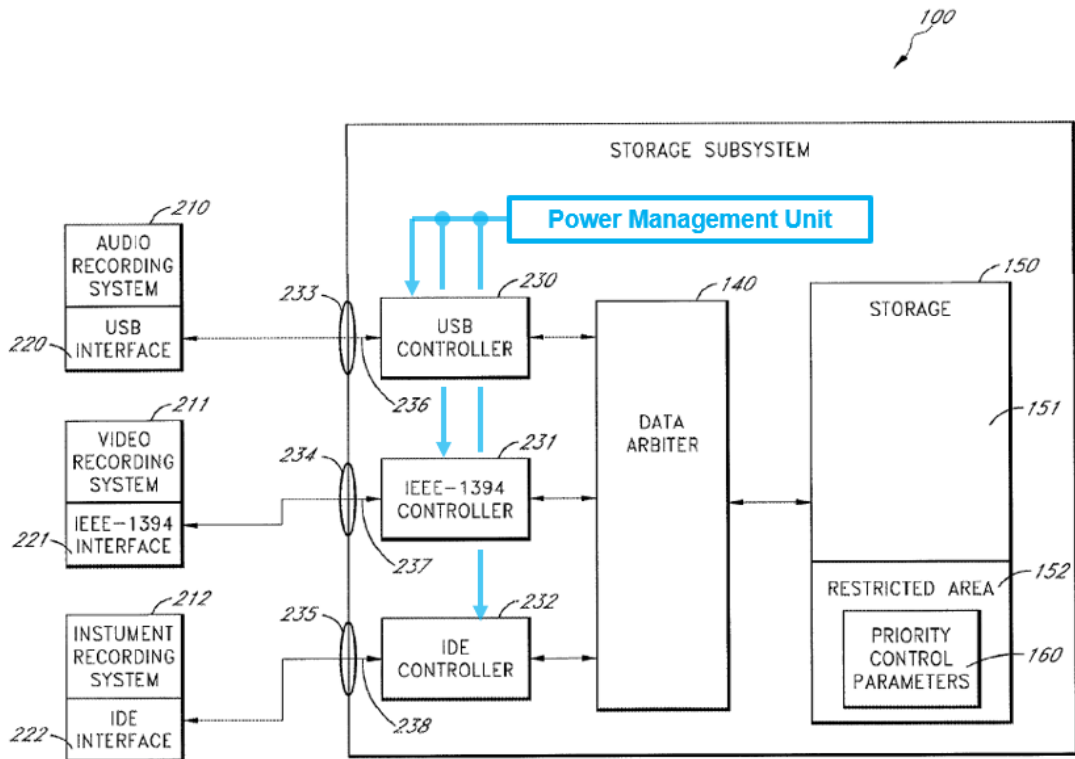


FIG. 2

Modification of Diggs Fig. 2 (showing power management unit).

3. Claim 5: The portable handheld memory card of claim 1 further comprising: a host interface module in communication with the I/O port.

Diggs discloses the added requirement of “a host interface module in communication with the I/O port.” The ’051 Patent specification discloses a “host interface circuit 114” that “may translate data” in order to be transferred via a given port. ’051 Patent, 4:4-7.

As indicated in Figure 2 (orange), Diggs’s “IEEE-1394 controller 231”

corresponds to the “host interface module” as understood from the intrinsic record.⁷

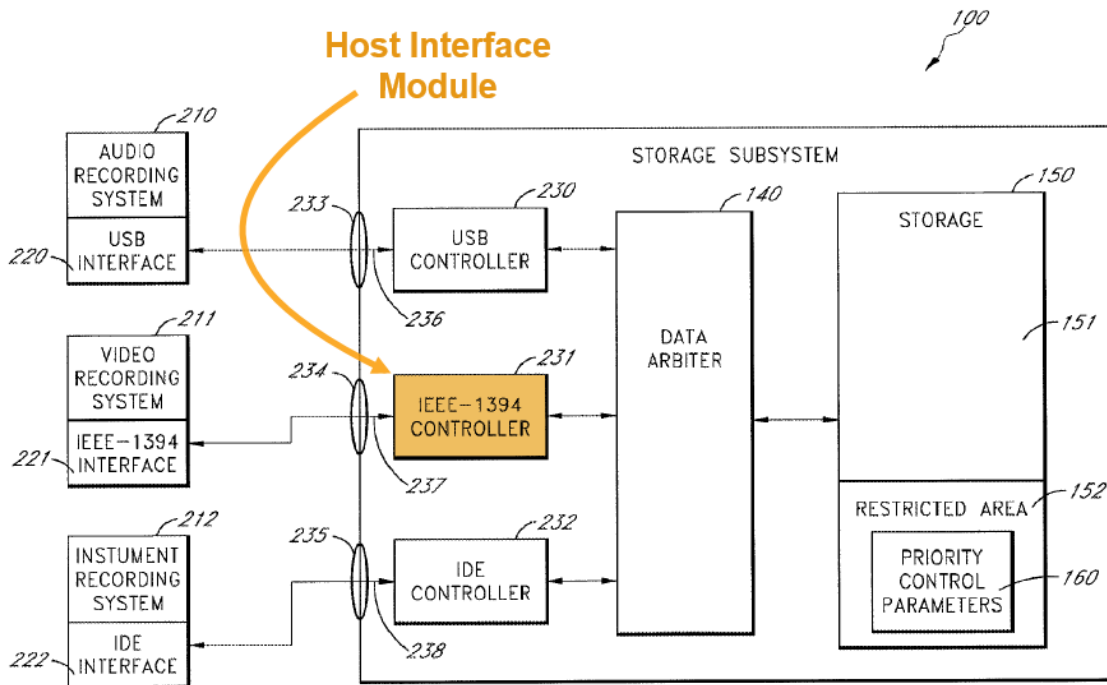


FIG. 2

Diggs, Fig. 2 (annotated).

Diggs discloses that “[e]ach controller may receive storage access commands from a host system and *translate these* signals to access storage 150,” Diggs ¶40, and that the host “video recording system 211 is connected to”—*i.e.*, *interfaces* with—“IEEE-1394 controller 231.” *Id.* Accordingly, IEEE-1394 controller 231 is a host interface module. Ex-1002 ¶¶127-129.

⁷ During prosecution, the Applicant did not dispute Examiner’s mapping of the “MMC interface controller” of the prior art Kim reference to the claimed “host interface module,” despite also mapping that feature to the “I/O controller circuitry.” See Ex-1004 at 72 (Feb. 14, 2012 Office Action at 4).

Diggs further teaches that IEEE-1394 controller 231 communicates with the “I/O port”—*i.e.*, “physical connector 234 [that] may be a four-pin Firewire connector.” Diggs ¶40; Ex-1002 ¶130.

4. Claim 6: The portable handheld memory card of claim 1 further comprising: circuitry configured to control read and write operations to the memory.

Diggs discloses Claim 6. Diggs states that “[e]ach controller ... may be configured to write data to, and read data from, the storage 150 in response to memory/storage access commands from hosts,” which entails “translat[ing] control, address, and data signals into storage access commands to storage 150. Controllers ... may also access and transmit data from storage 150 to host systems.” Diggs ¶29. Further, “[d]ata arbiter 140 is responsible for prioritizing read/write commands received simultaneously from multiple controllers,” and may do so “according to a priority ranking.” Diggs ¶33; *see also id.* ¶40. Thus, as indicated in Figure 2 (yellow), any or all of Diggs’s controllers 230, 231, and 222, and “data arbiter 140,” qualify as “circuitry configured to control read and write operations to the memory.” Ex-1002 ¶131.

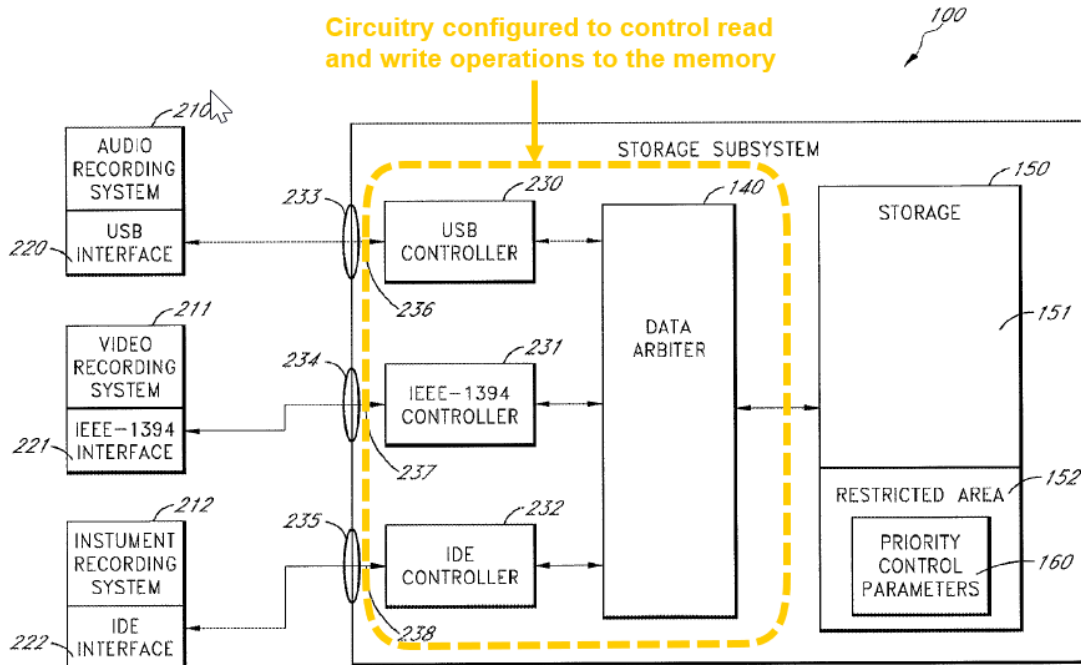


FIG. 2

Diggs, Fig. 2 (annotated).

5. Claim 7: The portable handheld memory card of claim 1, wherein the I/O port comprises a Secure Digital port.

Diggs teaches Claim 7. As discussed for Element 1[c], Diggs's Figure 2 memory card ("storage subsystem 100") includes an "input/output (I/O) port" in the form of a "physical connector 234 [that] may be a four-pin Firewire connector" and corresponding bus structure 237 which is "IEEE-1394" compliant. Diggs ¶¶40, 4; *supra* Element 1[c]. Diggs discloses that alternatively, "the storage subsystem 100 may, for example, be a solid-state memory card that connects to" a host according to the "SecureDigital" specification. Diggs ¶60. Pursuant to this teaching, a POSITA would have understood that an alternative embodiment would have been the below

modification of Diggs's Figure 2, which shows an "SD Device Controller" and corresponding host interface, in place of IEEE-1394 controller 231 and interface 221. Ex-1002 ¶132.

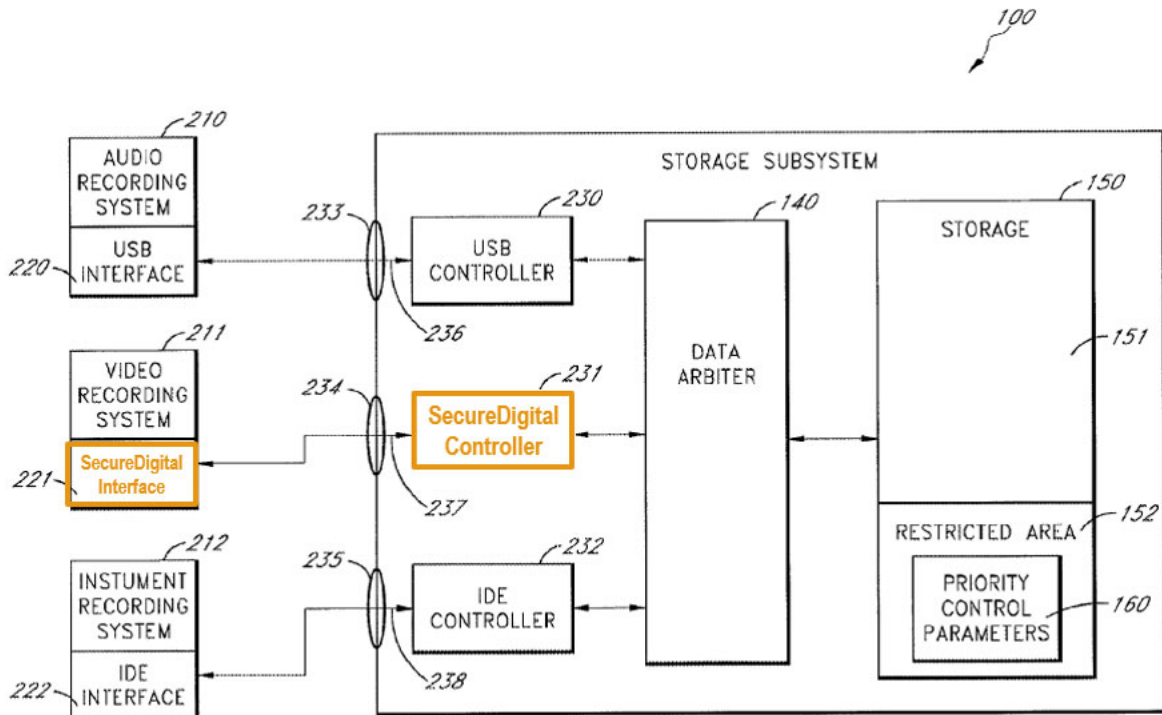


FIG. 2

Modification of Diggs Fig. 2 (including a "SecureDigital Controller" and interface instead of an IEEE-1394 controller / interface).

A POSITA would have understood that, in the above implementation of Diggs's memory card, physical connector 234 and corresponding bus structure 237 would be Secure-Digital compliant, and would therefore collectively form an "SD port." Further, as shown in Figure 7, the separate "[p]hysical connector[s] 702 and 703" would now correspond to an USB port and SD port, respectively, and the

positioning of these ports is such that, when the “set of pins” for one port is electrically connected to a host device, the other “set of pins” for the other port is not electrically connected to that host device. Ex-1002 ¶133.

6. Claim 8: The portable handheld memory card of claim 1, wherein the memory comprises Flash memory.

Diggs discloses that “[s]torage 150 may comprise a plurality of solid-state storage devices,” and that such “device[s] may comprise, for example, flash integrated circuits.” Diggs ¶30; Ex-1002, ¶134.

7. **Claim 16:**

- a. **Element 16[Preamble]: A method comprising:**
- b. **Element 16[a]: with a portable handheld card comprising a Universal Serial Bus (USB) port comprising a first set of pins; USB controller circuitry electrically connected with the first set of pins of the USB port; an input/output (I/O) port comprising a second set of pins; I/O controller circuitry electrically connected with the second set of pins of the I/O port; a memory in communication with the USB port and the I/O port; and a housing storing the memory and exposing the USB port and the I/O port, wherein the USB port and the I/O port are positioned to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port and wherein the USB port and the I/O port are positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device:**

Diggs teaches Elements 16[Preamble]-[a] for the reasons it teaches Claim 1.

See supra Section VII.A.1 (Claim 1); Ex-1020 (Claim Mapping Table); Ex-1002

¶135.

- c. **Element 16[b]: reading data from the memory;**

As discussed for Claim 6, Diggs discloses “circuitry configured to control read and write operations to the memory,” which entails “reading data from the memory.” *See* Claim 6, *supra*; Ex-1002 ¶136.

d. Element 16[c]: determining whether the data is to be transmitted via the USB port or I/O port; and

Diggs discloses Element 16[c]. Diggs explains that “[e]ach controller ... may be configured to write data to, and read data from, the storage 150 in response to memory/storage access commands from hosts,” which entails “translat[ing] control, address, and data signals into storage access commands to storage 150. Controllers ... may also access and transmit data from storage 150 to host systems.” Diggs ¶29. Diggs further teaches that “[d]ata arbiter 140 is responsible for prioritizing read/write commands received simultaneously from multiple controllers,” and may do so “according to a priority ranking.” Diggs ¶33; *see also id.*, ¶40. “For instance, the data arbiter 140 may determine that the priority control parameters 160 designate that commands received from the first host system []are of highest priority, and are therefore processed before commands received from the second host system.” Diggs ¶34. Based on these descriptions, and as reflected in Figure 2, a POSITA would have understood that during a “read” operation, data arbiter 140 would determine whether the data accessed from the memory 150 “is to be transmitted via the USB port” (*i.e.*, through USB controller 230 and bus structure 236) “or I/O port” (*i.e.*, through IEEE-1394 controller 231 and bus structure 237). Ex-1002 ¶137.

e. Element 16[d]: transmitting the data to the host device via the determined port.

See Claim 6 and Element 16[c], *supra*. During a read operation, Diggs’s

memory card “transmit[s] the data to the host device via the determined port.” Ex-1002 ¶138.

- 8. Claim 20: The method of claim 16, wherein the I/O port comprises a Secure Digital port.**

See Claim 7, *supra*; Ex-1002 ¶139.

- 9. Claim 21: The method of claim 16, wherein the memory comprises Flash memory.**

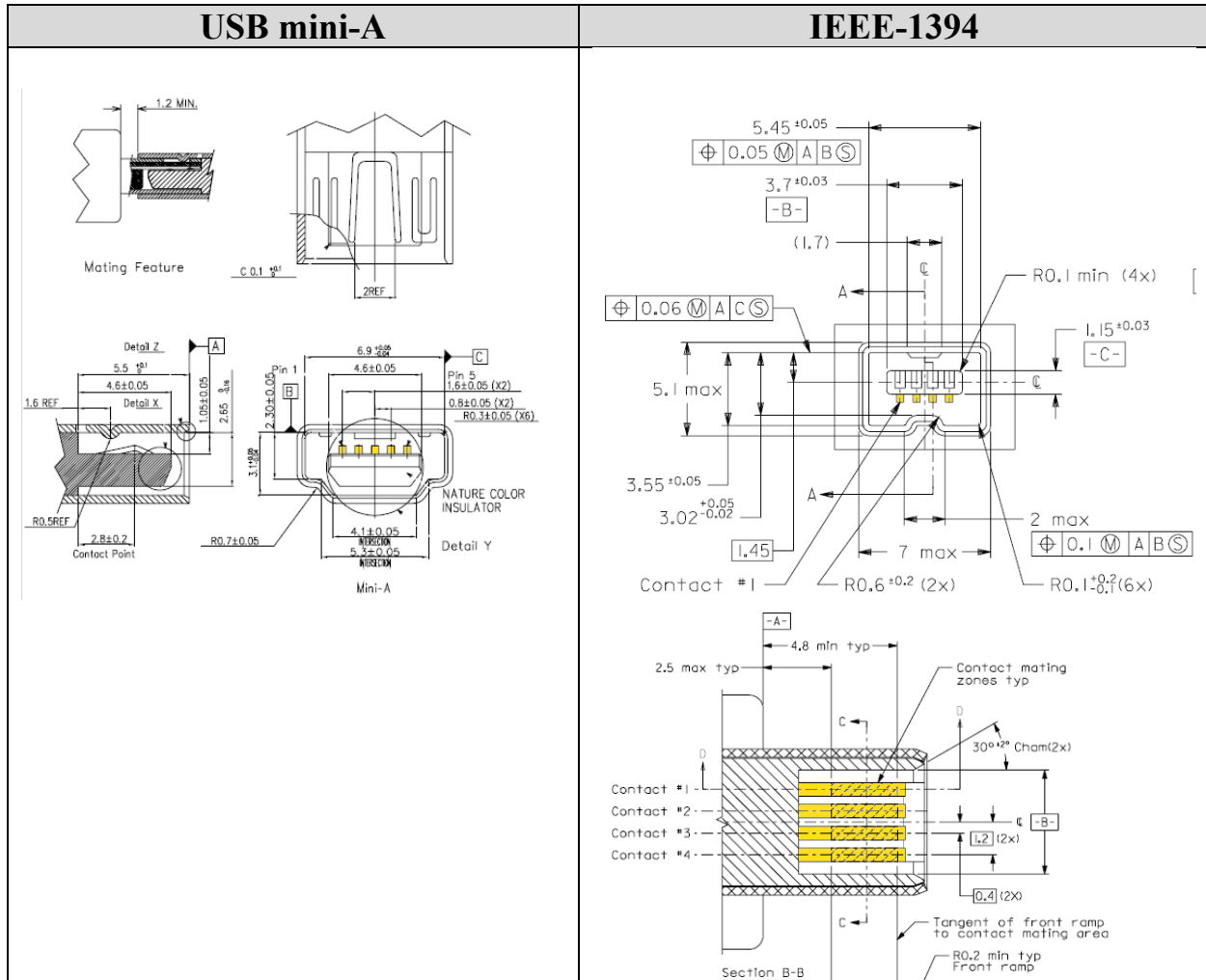
See Claim 8, *supra*; Ex-1002 ¶140.

- 10. Claim 23: The portable handheld memory card of claim 1, wherein at least two pins of the USB port are parallel to at least two pins of the I/O port.**

Diggs teaches Claim 23. As discussed for Element 1[g] above, Diggs discloses a USB port and I/O port—a USB mini-A port and IEEE-1394, respectively—which are positioned and oriented on the same end of the memory card as shown in Figure 7 (*i.e.*, as separate physical connectors 702 and 703, respectively, which are both located the near, left end). *See* Element 1[g], *supra*; Diggs ¶55, Fig. 7.

While not explicitly shown in Figure 7, a POSITA would have understood that the respective sets of pins associated with the USB port and I/O port—*i.e.*, the five USB mini-A pins, and the four IEEE-1394 Firewire pins—would have been implemented such that they are parallel to one another. Ex-1002 ¶¶141-142. This is supported, for example, by the specifications for USB mini-A and the four-pin IEEE-1394 applications, which include the below receptacle interface drawings. *See* Ex-

1025 at 21 (USB mini-A drawing); Ex-1029 at 35 (IEEE-1394 four-pin drawings);
 Ex-1002 ¶¶142-143.



These drawings, when considered against the positioning and orientation of the physical connector receptacle ports 702 and 703 in Figure 7 below, confirm that at least two of the pins of the USB port are in parallel to at least two of the pins of the I/O port.

11. Claim 24: The portable handheld memory card of claim 1, wherein layout for the USB port is different from layout of the I/O port.

Diggs discloses Claim 24. Diggs explains, and Figure 7 shows, that the USB port and I/O port are *separate physical connectors*: one having five pins, compliant with USB mini-A; the other having four pins, compliant with IEEE-1394. Diggs ¶¶40, 55, Fig. 7. Accordingly, the respective layouts for these two ports are different from one another. Ex-1002 ¶144.

12. Claim 25: The portable handheld memory card of claim 1, wherein the I/O port is configured for mating with an external port.

Diggs discloses Claim 25. Diggs’s “I/O port” (IEEE-1394 “four-pin Firewire” physical connector 234) is configured for mating with an external port—e.g., with the corresponding IEEE-1394-compliant port located at the “IEEE-1394 interface 221” of “video recorder system 211” as shown in Figure 2. Diggs ¶¶27, 39-40, Fig. 2; *see also id.*, ¶55 (stating that physical connector 703—the I/O port of Figure 7—is “further accessible to be connected to [an] IEEE-1394 cable connection[] from [an] additional host system[]”). Ex-1002 ¶145.

13. Claim 26: The portable handheld memory card of claim 1, wherein all of the first set of pins electrically connected with the USB controller circuitry is not electrically connected to the I/O controller circuitry.

Diggs discloses Claim 26. In Diggs’s card, all of the “first set of pins” (*i.e.*, both of the data pins D+ and D- of USB mini-A physical connector 233, as explained

for Element 1[a]) are electrically connected with USB controller 230. Further, both pins are “not electrically connected to the I/O controller circuitry” (IEEE-1394 controller 231); instead, the IEEE-1394 controller is connected to an entirely separate physical connector—the “four-pin Firewire connector” 234, which is compliant with IEEE-1394 instead of USB mini-A. Diggs ¶¶40, 55, Figs. 2, 7. Ex-1002 ¶146.

14. Claim 27:

- a. Element 27[preamble]: The portable handheld memory card of claim 1,**
- b. Element 27[a]: wherein the USB port comprises multiple data lines,**

Diggs discloses Elements 27[preamble]-27[a]. The below pin assignment table in the USB mini-A specification shows two data pins: D- and D+ for pins 2 and 3, respectively.

Table 4-2. Mini-A Plug Pin Assignments

Contact Number	Signal Name	Typical Wiring Assignment
1	VBUS	Red
2	D-	White
3	D+	Green
4	ID	< 10 Ω to GND
5	GND	Black
Shell	Shield	Drain Wire

Ex-1025 at 10.

Accordingly, in Diggs’s memory card, “USB mini-A” physical connector 233 and corresponding bus structure 236 (*i.e.*, “USB port”) includes multiple data pins and corresponding data lines. Diggs ¶40, Fig. 2; Ex-1002 ¶¶147-148.

- c. Element 27[b]: wherein the first set of pins comprise multiple data pins connected to the multiple data lines; and**

See Element 27[a], above; Ex-1002 ¶149.

- a. Element 27[c]: wherein all of the multiple data pins are not electrically connected to the I/O controller circuitry.**

See Claim 26 above, explaining that, in Diggs’s memory card, none of the “first set of pins” of the USB port—including the “multiple data pins”—are connected to the IEEE-1394 controller 231. Ex-1002 ¶150.

B. Ground 2: Claims 2 and 17 Are Obvious Over Diggs in View of Thorsten

As shown below, the subject matter of Claims 2 and 17 are disclosed by Diggs in view of Thorsten. Ex-1002 ¶¶151-163.

1. A POSITA would have been motivated to combine Diggs with Thorsten with a reasonable expectation of success.

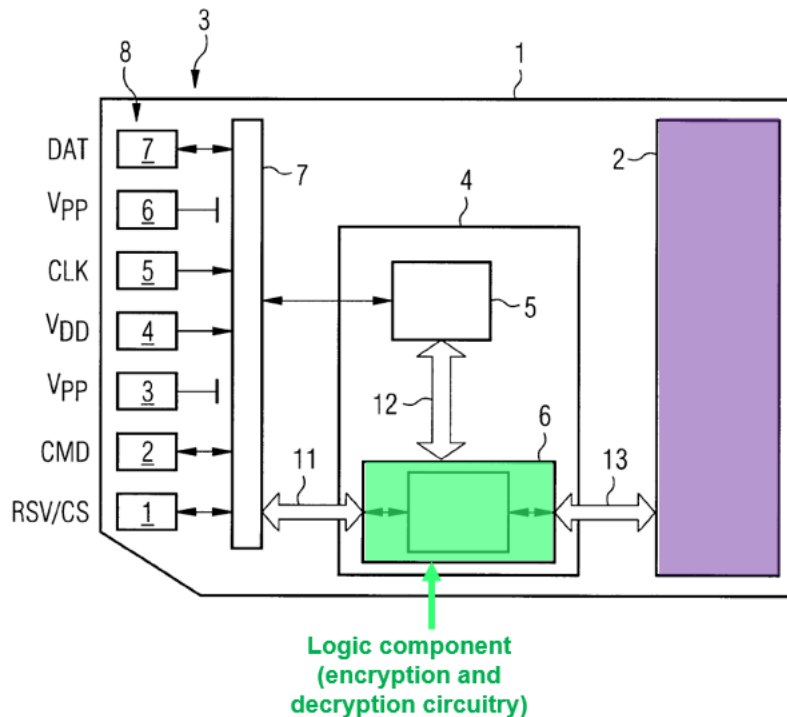
A POSITA would have been motivated to combine Diggs with Thorsten and would have a reasonable expectation of success in doing so, because they are both from the same field and relate to the same well-known issues. Both references disclose memory cards, and external host devices that read data from, and write to, the memory. *Compare* Diggs ¶¶29, 33 *with* Thorsten ¶3. Like Diggs, Thorsten discloses a “memory card comprising a non-volatile memory 2,” “a data interface 3 for connecting to a host,” and “a controller 5.” *E.g.*, Diggs ¶¶29-30, Fig. 2; Thorsten ¶13, Fig. 1. A POSITA seeking to store sensitive data in encrypted form, in a manner compatible with different host applications, would have looked to each of these references for teachings of how to reliably store sensitive data. Ex-1002 ¶152.

Diggs’s memory card is capable of receiving read and write commands simultaneously from multiple connected external host devices compliant with different standards, including USB and IEEE-1394, and it includes separate corresponding physical connectors, bus structures, and controller circuits corresponding to those multiple standards. *See* Diggs ¶¶39, 40, Figs. 2, 7. Diggs is

silent on the sensitivity of data to be stored in its memory card, or whether its memory card utilizes encryption or decryption. However, at the time of the '051 Patent, encryption and decryption techniques were a common feature of solid-state memory cards. *See* Ex-1002 ¶¶86-87, 153.

Thorsten, for example, acknowledges that sensitive data is usually stored in encrypted form, but recognizes that conventional “memory cards are designed in such a way that almost all hosts, which may belong to different applications, ... [s]o if a first application stores a data record that it has previously encrypted using a specific algorithm, the host of a second application ... again must also have this algorithm, otherwise the data cannot be decrypted again.” Thorsten ¶3. To resolve this, Thorsten proposes a configuration in which “the card itself handles the encryption and decryption, [so that] it is not necessary to know in advance which applications the memory card is to work with, and it is not necessary to ensure that these applications have the appropriate algorithms.” Thorsten ¶4.

Thorsten’s “data carrier 1” (“memory card”) incorporates a “logic component 6” (light green) “that is responsible for the encryption and/or decryption process,” Thorsten ¶8, and which may be “a function-programmable logic circuit.” Thorsten ¶10.



Thorsten, Fig. 1 (annotated).

“Data to be transmitted from the data interface 3 to the memory 2 is encrypted in the logic component 6. When reading data from the memory card, data is transmitted from the memory 2 to the data interface 3, with decryption being performed by the logic component 6.” Thorsten ¶15. Figure 1 shows that “the data path for encryption and decryption runs exclusively via the logic component 6, but not via the controller 5” (Thorsten ¶15), but “[i]n an advantageous implementation, the logic component 6 is designed as an additional module of a chip card controller 5. This enables a compact and cost-effective implementation.” Thorsten ¶17.

Accordingly, a POSITA would have understood and been motivated to incorporate, in Diggs’ memory card, data encryption and decryption functionality

that is compatible with various host applications, by implementing Thorsten’s logic component (*i.e.*, encryption and decryption circuitry), to reap Thorsten’s disclosed benefits—*i.e.*, storing sensitive data while remaining compatible with various host applications. Ex-1002 ¶¶154-157; *see* Thorsten ¶¶2-4; *Dystar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006) (A motivation to combine exists when the “improvement” results in a product or process that is “stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient.”).

Additionally, a POSITA would have had a reasonable expectation of success in achieving the collective objectives of Diggs and Thorsten—*e.g.*, obtaining a multiple standard-compliant memory card that can store sensitive data while remaining compatible with various host applications—by combining their teachings with no change in their respective functions, since Diggs and Thorsten disclose similar devices, and because Thorsten’s encryption and decryption circuitry can be readily incorporated in to Diggs’ device to achieve predictable results. Ex-1002 ¶158. As discussed in Ground 1 above, Diggs discloses a memory card featuring *multiple controllers*, where “[e]ach controller . . . may be configured to write data to, and read data from, the storage 150 in response to memory/storage access commands from hosts,” which entails “translat[ing] control, address, and data signals into storage access commands to storage 150.” Diggs ¶29. Diggs further

teaches that its “[d]ata arbiter 140 is responsible for prioritizing read/write commands received simultaneously from multiple controllers,” and may do so “according to a priority ranking.” Diggs ¶¶33, 40, Fig 2. Thorsten’s memory card likewise features a “controller 5” that keys instructions to the logic component. Thorsten ¶16. According to Thorsten, controller 5 either “connects [to] the logic component” via “third interface 13” (Thorsten ¶14, Fig. 1), or else “the logic component 6 is designed as an additional module of [the] controller 5” (Thorsten ¶17). Given that Thorsten teaches flexibility in implementation, a POSITA would have observed that the logic component could be readily implemented in Diggs’s memory card consistent with Thorsten’s teachings, as illustrated by the following modification of Diggs’ Figure 2. Ex-1002 ¶158.⁸

⁸ As Dr. Baker explains, the Diggs-Thorsten Modification could be implemented slightly differently, where the logic component is situated between the controllers and the data arbiter, consistent with the collective teachings of the references. Ex-1002 ¶158, n.6.

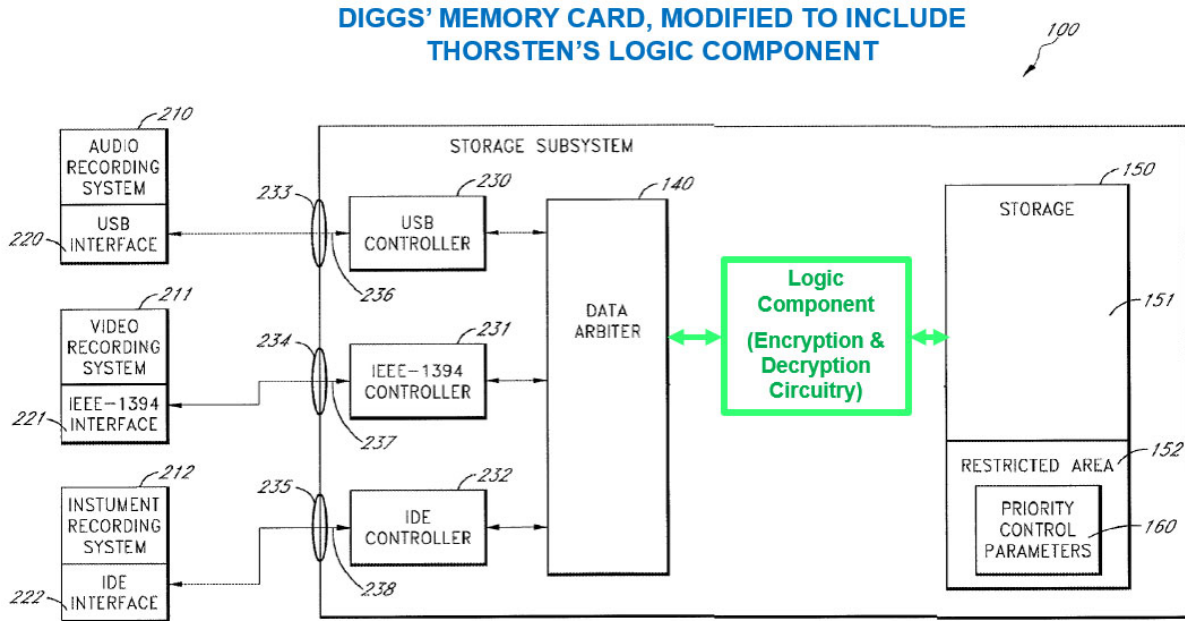


FIG. 2

Modification of Diggs, Fig. 2 (“**Diggs-Thorsten Modification**”).

In such an implementation, encryption and decryption instructions are keyed into the logic component (*i.e.*, programmable circuitry) by one of Diggs’s controllers 230, 231, or 232, along with the data arbiter 140 (based on a priority ranking for simultaneously-received commands); depending on priority, “[d]ata to be transmitted ... to [Diggs’s] memory ... is encrypted in the logic component 6. [Subsequently,] [w]hen reading data from the memory card, data is transmitted from the memory ... with decryption being performed by the logic component 6.” See Thorsten ¶15; Ex-1002 ¶159. Thus, improving Diggs by implementing Thorsten’s teachings would have constituted nothing more than the application of a known technique (*e.g.*, encryption and decryption circuitry) to a known device (*e.g.*, Diggs’

memory card) to obtain predictable results (*e.g.*, storing and retrieving sensitive data in a manner compliant with various host applications). *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

2. Dependent Claim 2: The portable handheld memory card of claim 1 further comprising: decryption circuitry in communication with the memory and configured to decrypt encrypted data stored in the memory.

Diggs in view of Thorsten teaches Claim 2. As discussed in Ground 1, *supra*, Diggs teaches the portable handheld memory card of Claim 1. *See* Section VII.A.1, *supra*.

As discussed in Section VII.B.1, *supra*, Diggs-Thorsten teaches “decryption circuitry”—*i.e.*, Thorsten’s logic component (annotated light green)—that is “in communication with the memory and configured to decrypt encrypted data stored in the memory.” Ex-1002 ¶¶160-161.

3. Dependent Claim 17: The method of claim 16, wherein the data is encrypted data, and wherein the method further comprises: decrypting the encrypted data to decrypted data.

Diggs in view of Thorsten teaches Claim 17. As discussed in Ground 1, *supra*, Diggs teaches the method of Claim 16. *See* Section VII.A.7, *supra*.

As discussed in Section VII.B.1, *supra*, Diggs-Thorsten teaches that “the data [to be read from the memory] is encrypted data, and wherein the method further comprises decrypting the encrypted data to decrypted data.” Ex-1002 ¶¶162-163.

C. Ground 3: Claims 1, 4-8, 16, 20-21, and 23-27 Are Obvious Over Lin

As shown below, the subject matter of Claims 1, 4-8, 16, 20-21, and 23-27 are taught by Lin alone. Ex-1002 ¶¶164-223.

1. Claim 1

a. Element 1[preamble]: A portable handheld memory card comprising:

If Claim 1’s preamble is limiting, Lin discloses it. Ex-1002 ¶¶165-166. Lin discloses “a removable memory card” (below, teal), also shown and described as a “removable electronic device.” *See, e.g.*, Lin ¶¶2, 21, 29, Fig 1A, 6A. (“removable electronic device 30”), Fig. 6A (“removable electronic device 120”).

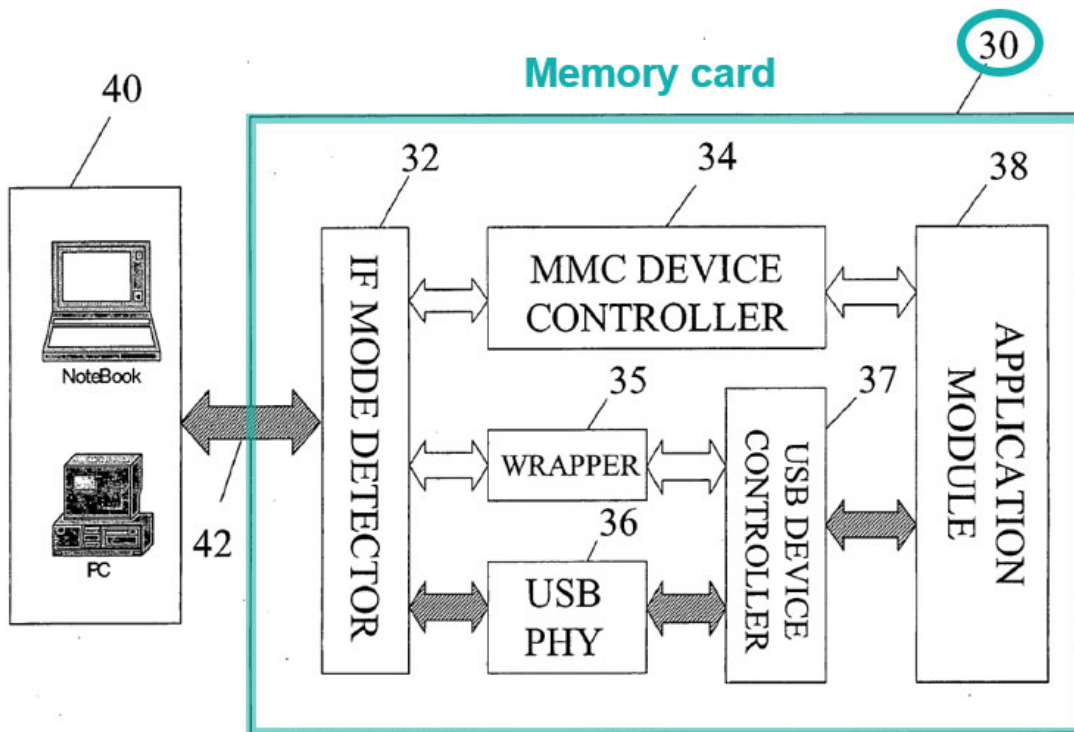


FIG. 1A

Lin, Fig. 1A (annotated).

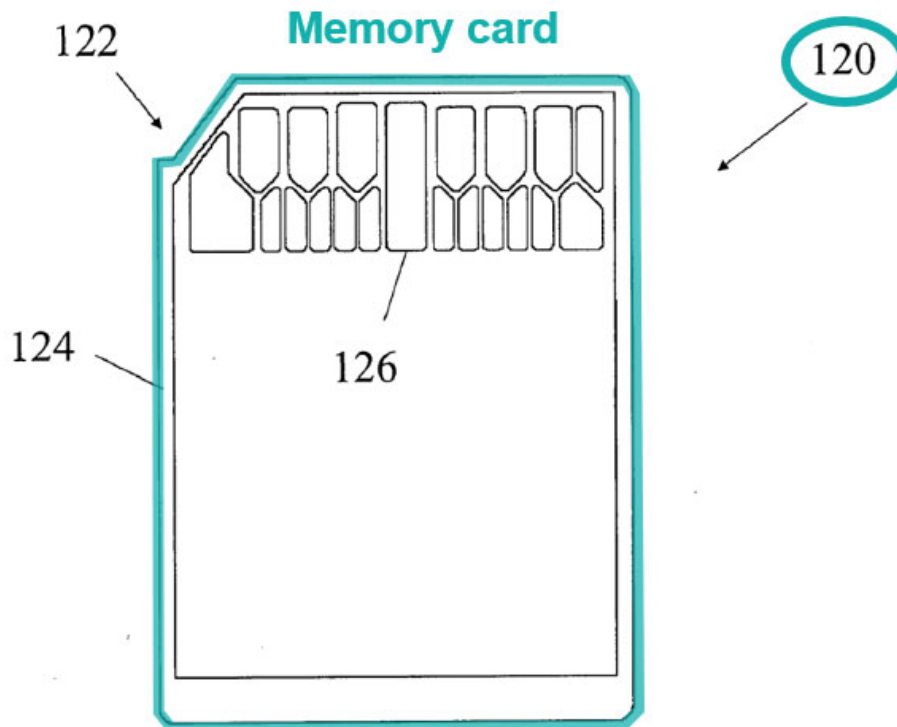


FIG. 6A

Lin, Fig. 6A (annotated).

Lin states that “[a] memory card is commonly known as a small *portable* package containing [a] digital memory,” and is used to store data from various host “electronic devices that support removable data storage.” Lin ¶¶3-4. Lin also explains that its memory card is “*inserted* into a host ... for example, a notebook, a personal computer (PC), a cell phone, a tablet PC,” Lin ¶¶31, 106, and is “removable,” *id.* ¶¶2, 29. A POSITA would have understood that a user that “inserts” or “removes” the card does so with his hands, such that the memory card is

“handheld” while the user is holding it before or after such actions. Lin’s memory card includes a housing (*see* Element 1[f], *infra*), which a POSITA would have recognized as protecting internal components from dust, moisture, or impact, thus further confirming the “handheld” nature of the card. Ex-1002 ¶166.

b. Element 1[a]: a Universal Serial Bus (USB) port comprising a first set of pins;

Lin discloses Element 1[a]. Ex-1002 ¶¶167-170. Lin’s removable electronic device is compatible with different modes of operation, including “a universal serial bus (USB) compatible mode.” Lin ¶8; *see also id.* ¶5 (describing the USB standard). Fig. 1A (annotated) shows “electronic device 30 operating in a USB mode,” as indicated by the blue bi-directional arrows. Lin ¶31.

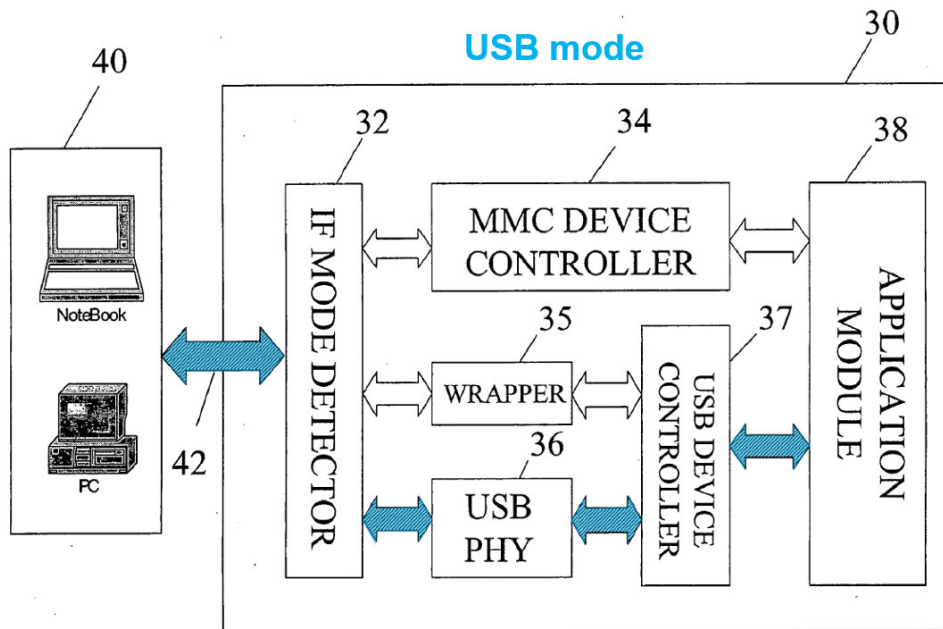


FIG. 1A

Lin, Fig. 1A (annotated).

Figure 4A shows “a proposed pin assignment chart” of an electronic device with USB compatibility. “The fourteenth and fifteenth pins for the USB mode, *i.e.*, D+ and D-, are a pair of data signals, which may be used to determine whether the USB mode is selected.” Lin ¶38. Specifically, D+ and D- are “a complementary pair in which one is at a high level when the other is at a low level.” *Id.*

USB Port

Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3	VSS1	VSS1	VSS1	VSS1
4	VDD1	VDD1	VDD1	VDD1
5	CLK	SCLK		CLK
6	VSS2	VSS2	VSS2	VSS2
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

first set of pins

FIG. 4A

Lin, Fig. 4A (annotated).

Further, Figure 5, also annotated below, shows “a diagram of a removable electronic device 100” that “includes a plurality of interweaving contact pads labeled 1 to 20, which correspond to the pins illustrated in Fig. 4A.” Lin ¶¶106-107.

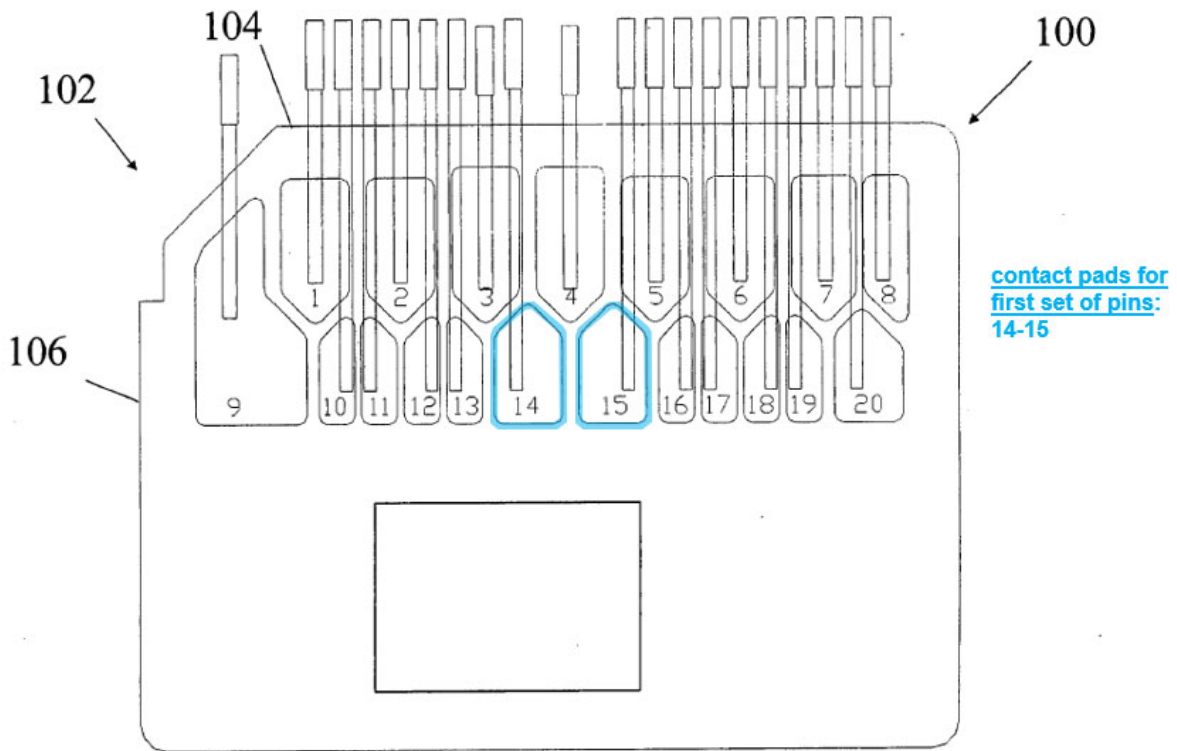


FIG. 5

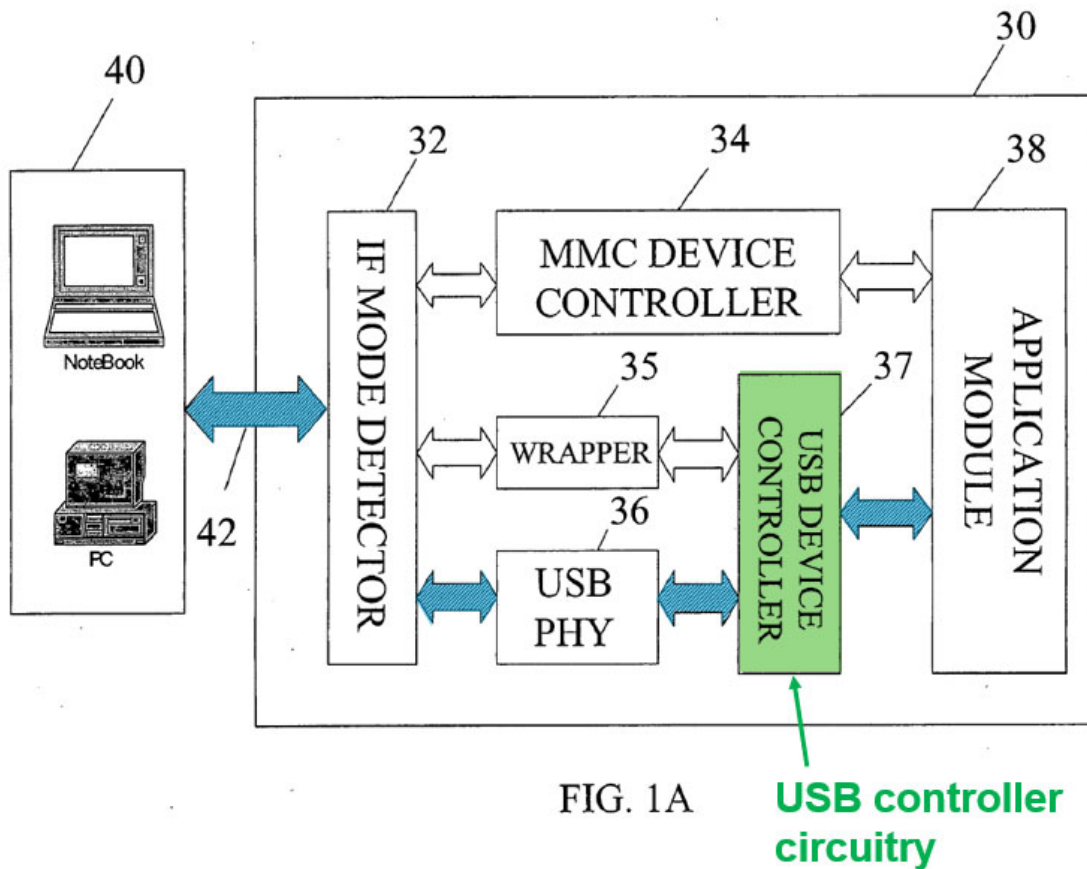
Lin, Fig. 5 (annotated).

The claimed “USB port” is met by the set of pins, or else the corresponding set of contact pads, that are assigned to the USB mode according to Lin’s Figure 4A. As shown in the Figure 4A and Figure 5 annotations above, the corresponding “first set of pins” includes pins 14-15 associated with the USB mode of the device.⁹ Ex-1002 ¶170.

⁹ Pins 3, 4, and 6, which provide power levels VSS1, VDD, and VSS2, respectively, while not required for Petitioner’s mapping to the claimed “first set of pins,” could optionally be included. Ex-1002 ¶170, n.7.

c. **Element 1[b]: USB controller circuitry electrically connected with the first set of pins of the USB port; and**

Lin discloses Element 1[b]. Ex-1002 ¶¶171-172. Lin’s memory card includes “a USB compatible device controller for controlling data transfer in the USB compatible mode.” Lin ¶8. Specifically, Fig. 1A (annotated below) shows a “USB device controller 37” (green).



Lin, Fig. 1A (annotated).

The USB device controller is “electrically connected with the first set of pins of the USB port,” for example, by way of the USB PHY circuit 36 and the IF mode

detector 32 as reflected by the bi-directional arrows (annotated in blue) in Fig. 1A.

Ex-1002 ¶172.

d. Element 1[c]: an input/output (I/O) port comprising a second set of pins; and

Lin discloses Element 1[c]. Ex-1002 ¶¶173-176. Lin's removable electronic device features an "MMC compatible mode" that includes the "MMC 4.0 or MMC SPI (serial peripheral interface) applications." Lin, ¶¶7-8, 29; *see also id.* ¶4 (describing "the MultiMedia Card ('MMC')" standard). Fig. 1C (annotated) shows "electronic device 30 operating in a MMC mode," as indicated by the red bi-directional arrows. Lin ¶31.

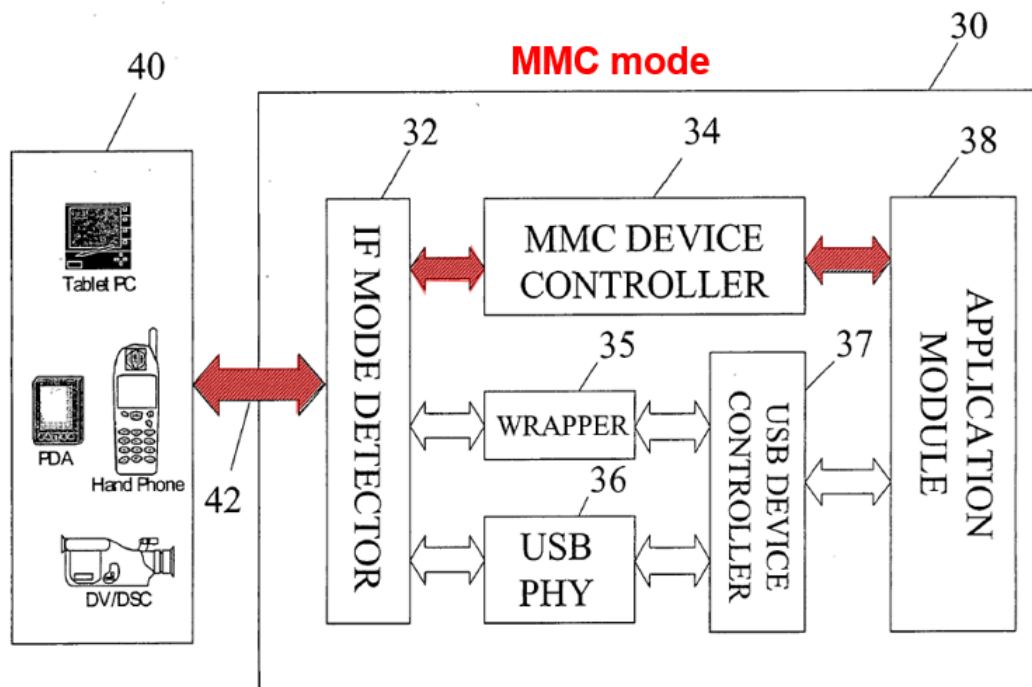


FIG. 1C

Lin, Fig. 1C (annotated).

The “pin assignment chart” of Fig. 4A shows how the electronic device features MMC compatibility. As shown in the below Figure 4A annotation, the “MMC 4.0” standard uses pins 1-13 and 18-20. *See* Lin, Fig. 4A, ¶¶36, 38.

I/O Port

Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3			VDD	VDD
4			VDD	VDD
5	CLK	SCLK		CLK
6			VDD	VDD
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

second set of pins

FIG. 4A

Lin, Fig. 4A (annotated).

Further, Figure 5, also annotated below, shows “a diagram of a removable electronic device 100” that “includes a plurality of interweaving contact pads labeled 1 to 20, which correspond to the pins illustrated in Fig. 4A.” Lin ¶¶106-107.

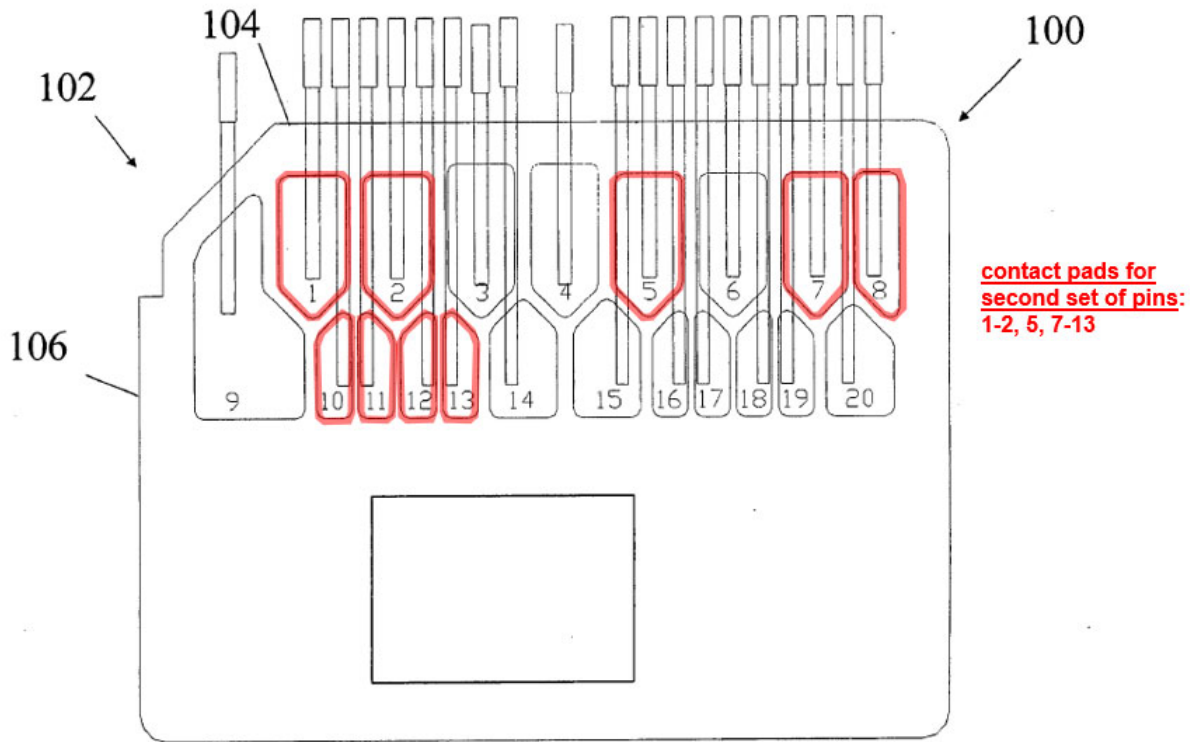


FIG. 5

Lin, Fig. 5 (annotated).

The claimed “I/O port” is met by the set of pins, or else the corresponding set of contact pads, that are assigned to the MMC 4.0 mode according to Lin’s Figure 4A. As shown in the Figures 4A and 5 annotations above, the corresponding “second set of pins” includes pins 1-2, 5, and 7-13 associated with the MMC 4.0 mode of the device.¹⁰ Ex-1002 ¶176.

¹⁰ Pins 3, 4, and 6, which provide power levels VSS1, VDD, and VSS2, respectively, while not required for Petitioner’s mapping to the claimed “second set of pins,” could optionally be included. Ex-1002 ¶176, n.8.

e. **Element 1[d]: I/O controller circuitry electrically connected with the second set of pins of the I/O port;**

Lin discloses Element 1[d]. Ex-1002 ¶¶177-179. Specifically, Lin’s memory card includes “a multi-media card (MMC) device controller 34” (orange) that “controls data transfer between host 40 and application module 38” when “electronic device 30 is operating in an MMC mode.” Lin ¶¶31, 33.

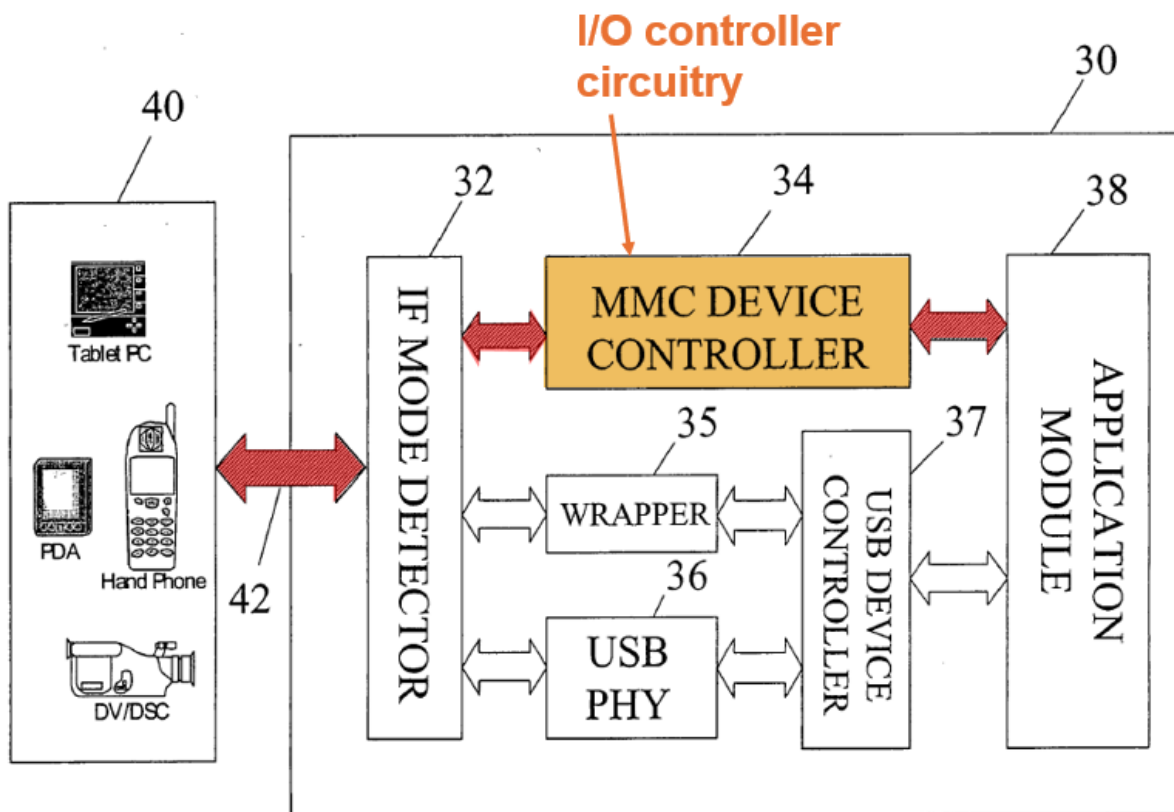


FIG. 1C

Lin, Fig. 1C (annotated).

A POSITA would have understood Lin’s “MMC device controller 34” is “I/O

controller circuitry” because a controller operates through circuitry.¹¹ Ex-1002

¶178.

The MMC device controller is “electrically connected with the second set of pins of the I/O port,” for example, by way of the IF mode detector 32 as reflected by the bi-directional arrows (annotated in red) in Figure 1C. Ex-1002 ¶179.

f. Element 1[e]: a memory in communication with the USB port and the I/O port; and

Lin discloses Element 1[e]. Lin discloses an “[a]pplication module 38,” shown for example in Fig. 1C below (purple), that “functions to serve as a memory storage or an input/output (I/O) interface, depending on the operation mode detected.” Lin ¶31.

¹¹ As discussed in Section IV.B, during prosecution, the Applicant did not dispute the Examiner’s mapping of the claimed “I/O controller circuitry” to the “MMC interface controller” disclosed in the prior art Kim reference. *See* Ex-1004 at 73 (Feb. 14, 2012 Office Action at 3).

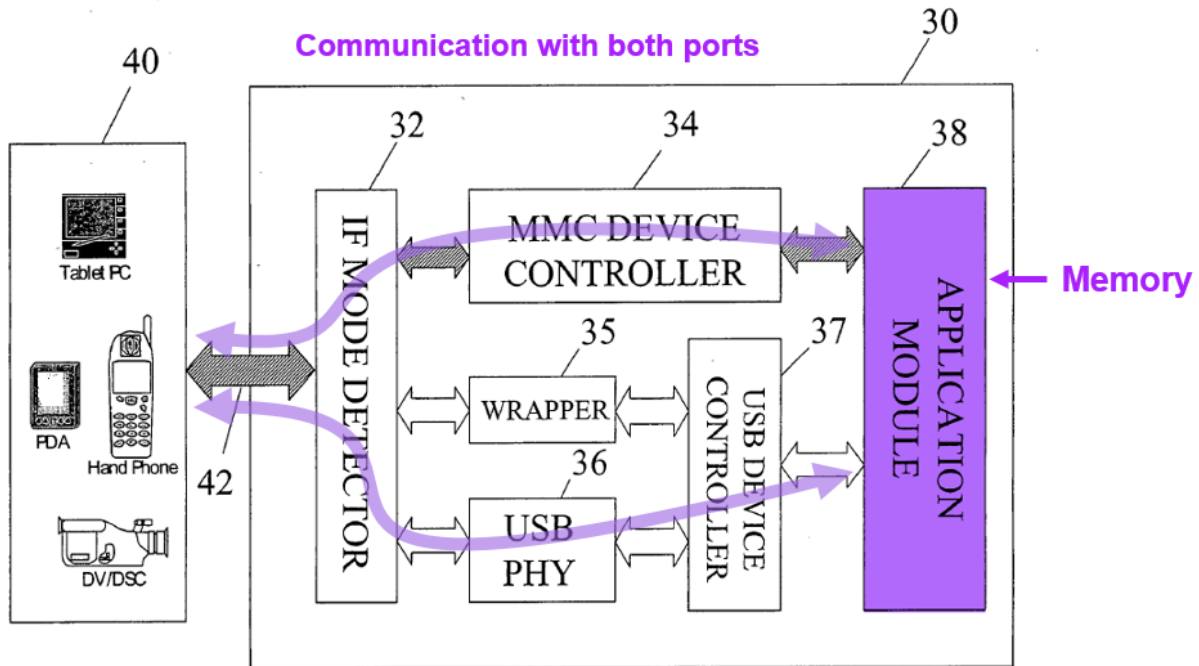


FIG. 1C

Lin, Fig. 1C (annotated).

In the USB mode, “USB device controller 37 controls data transfer over a common bus 42 between host 40 and application module 38 via USB PHY circuit 36.” Lin ¶31. Conversely, in the MMC mode, “MMC device controller 34 controls data transfer between host 40 and application module 38.” Lin ¶33; *see also id.* Cls. 5-8 (specifying data transfer between “a host and the memory module,” under each operating mode). Accordingly, Lin’s disclosed memory is “in communication with the USB port and the I/O port.” Ex-1002 ¶¶180-181.

- g. Element 1[f]: a housing storing the memory and exposing the USB port and the I/O port;**

Lin discloses Element 1[f]. In Figures 6A and 6B, Lin shows and describes a “housing (not numbered)” for its memory card (including application module 38)

that “includes a top surface, a bottom surface, and a periphery.” Lin ¶108.

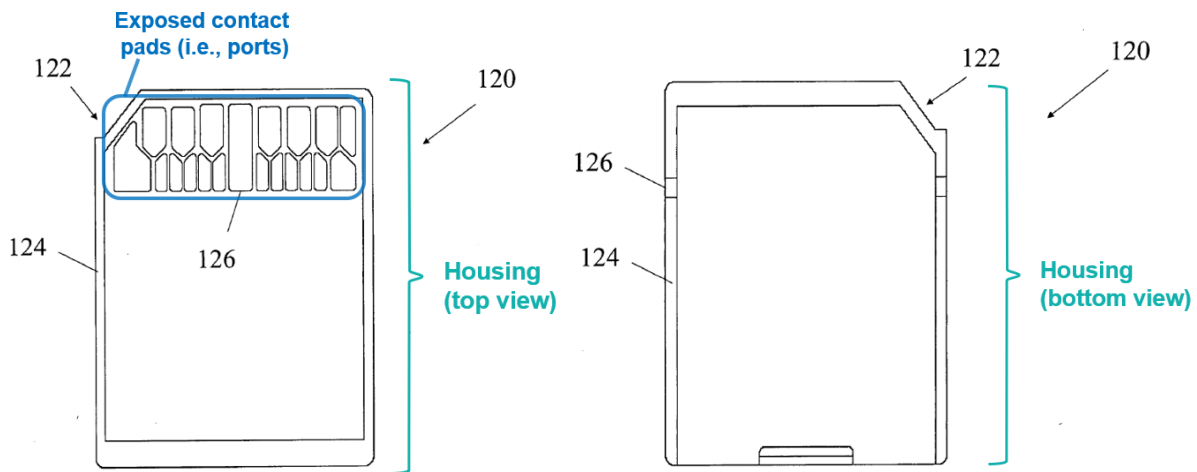


FIG. 6A

FIG. 6B

Lin, Figs. 6A-6B (annotated).

As shown in Figure 6A,¹² the top surface of the housing exposes the contact pads that correspond to the pins associated with the USB port and I/O port, as identified for Elements 1[a] and 1[c]. Lin further explains that “[t]he contact pads ... are positioned in twenty *recesses* on a top surface along [a] front side 104 and notch 102.” Lin ¶107; *see also id.* ¶4 (“In general, a memory card includes *exposed* electrical contracts on its surface to allow easy connection to and removal from a receptacle of a host electronic system or device, particularly portable devices.”). Ex-1002 ¶¶182-183. Accordingly, Lin discloses “a housing storing the memory and exposing the USB port and the I/O port.”

¹² Based on Lin’s description at paragraph 109, in Fig. 6A, label “126,” depicted as indicating a contact pad, appears to be a typo that should instead be “128.”

- h. Element 1[g]: wherein the USB port and the I/O port are positioned on a same end to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port; and**

Lin discloses Element 1[g]. As shown in Figures 5 and 6A, Lin's memory card "includes a plurality of interweaving contact pads labeled 1 to 20, which correspond to the pins illustrated in Fig. 4A. The interweaving design in the contact pads allows additional pins to be present in the same real estate." Lin ¶107. Further, "[t]he contact pads ... are positioned in twenty recesses on a top surface *along front side 104* and notch 102," where the notch is included "to prevent incorrect insertion of [the] electronic device." Lin ¶¶106-107. Accordingly, Lin's "USB port" and "I/O port"—which correspond to the memory card's contact pads as explained for Elements 1[a] and 1[c]—"are positioned on a same end to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port." Ex-1002 ¶¶184-186.

Notably, the position and orientation of the Lin's contact pads are substantially similar to Figure 2 of the challenged '051 Patent, which is described as satisfying the claim element. There, as in Lin, the contact pads (or pins) are located alongside a "same end"—the "front 202" of "memory card 200." Ex-1001, Fig. 2, 4:38-42.

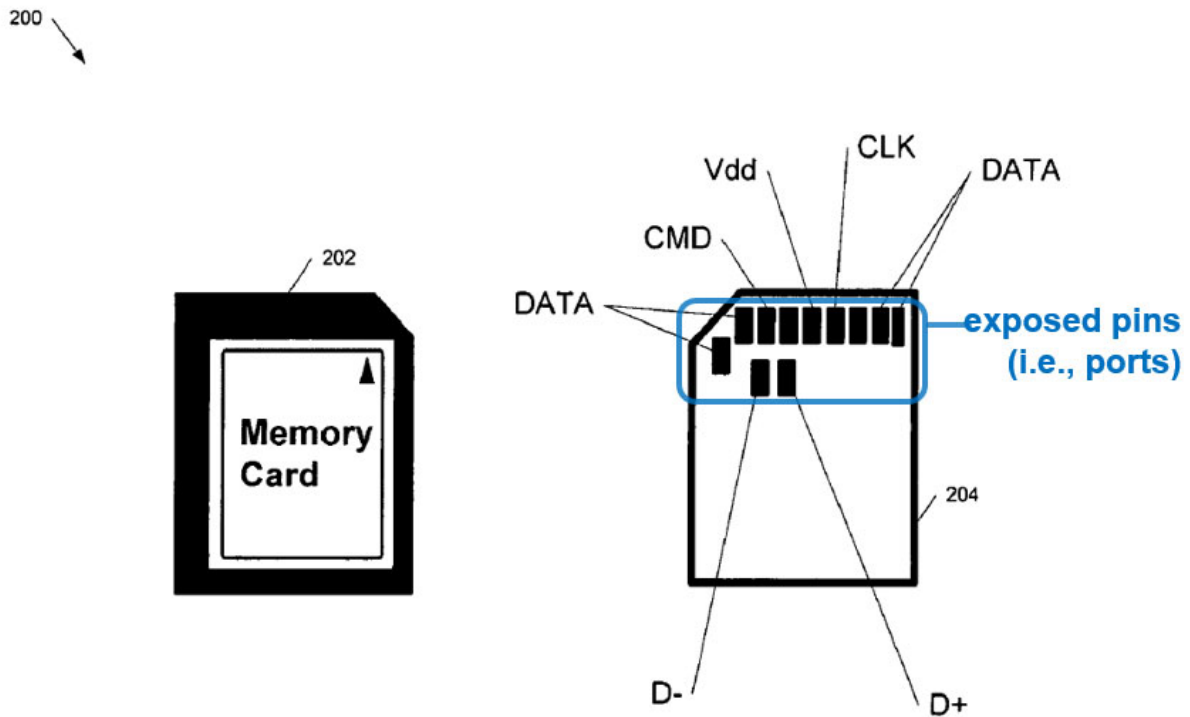


Figure 2

'051 Patent, Fig. 2 (annotated).

The '051 Patent explains that “the memory card 200 is *configured to be inserted in a certain direction* and orientation so that the SD port interfaces with a mating SD port of a host device. When the memory card 200 is inserted in this fashion, the USB port may also interface with a mating USB port of the host device.”

'051 Patent, 4:61-66. Ex-1002 ¶186.

- i. **Element 1[h]: wherein the USB port and the I/O port are positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and**

Lin discloses Element 1[h]. Ex-1002 ¶¶187-190. As discussed for Elements 1[a], 1[c], and 1[g], in Lin’s memory card, all of the contact pads—including those corresponding to the “USB port” and “I/O port”—are positioned on the front end of the card, which “allow[s] a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port.”

Further, “IF mode detector 32 detects a mode of operation to distinguish among an MMC mode, a USB mode[,] or a Mu mode when electronic device 30 is inserted into a host 40.” Lin ¶31. In Figure 1C, for example, “IF mode detector 32 detects that a host 40, to which electronic device 30 is connected, is in compliance with the MMC specifications.” Lin ¶33. As shown and described for Figure 2, this detection or determination is based on the power source voltage level, and the type of command signal received. Lin ¶¶34-35, 37. The Figure 4A pin assignment chart indicates which pins are used, for example, in the MMC 4.0 mode (corresponding to the “I/O port”) and which are used for the USB mode (corresponding to the “USB port”). Lin ¶38. Pursuant to the MMC specification, “[t]he first pin of the removable electronic device for the MMC 4.0 mode, *i.e.*, DAT 3, is defined to switch the MMC 4.0 mode to the MMC SPI mode.” Lin ¶38. Figure 4A (annotated below) shows that

the MMC 4.0 mode—which corresponds to “*when the I/O port is electrically connected with the host device*”—does not use two of the pins that are assigned to the USB mode (specifically, pins 14 and 15).

I/O Port connected to host device

Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3				
4				
5	CLK	SCLK		CLK
6				
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

Two of the “first set of pins of the USB port” are not electrically connected to host

FIG. 4A

Lin, Fig. 4A (annotated).

Since pins 14 and 15 are not used to transmit electrical signals in the MMC 4.0 mode, these “*pins of the USB port [are] not electrically connected with the host device*” in that scenario. Ex-1002 ¶189. Consistent with this understanding, during prosecution, the Applicant referenced Figure 1 of the ’051 Patent as “[a]n example of” the scenario contemplated by Element 1[h]—which was added by amendment to overcome the Kim reference—citing the fact that “in Figure 1, the data line inputs (D+ and D-)” used for the USB mode “are not input to the Host Interface” used for

the SD mode, which “allow[s] the pin layout for the USB port to be different from the pin layout for the SD port.” Ex-1004 at 46, 52-54 (July 16, 2012 Response at 2, 8-10). Lin’s memory card likewise uses a different pin layout for its USB mode (which also uses “D+ and D-” as data inputs) versus its MMC 4.0 mode. Ex-1002 ¶190.

- j. Element 1[i]: when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device.**

Lin discloses Element 1[i]. As discussed for Element 1[h], in Lin’s memory card, “IF mode detector 32 detects a mode of operation to distinguish among an MMC mode, a USB mode[,] or a Mu mode when electronic device 30 is inserted into a host 40.” Lin ¶31. Figure 4A’s pin assignment chart (annotated again below) shows that the USB mode—corresponding to “*when the USB port is electrically connected with the host device*”—does not use several of the pins that are assigned to the MMC 4.0 mode (specifically, pins 1-2, 5, and 7-13).

**USB Port connected
 to host device**

Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3				
4				
5	CLK	SCLK		CLK
6				
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

Several of the
 “second set of pins
 of the I/O port” are
 not electrically
 connected to host

FIG. 4A

Lin, Fig. 4A (annotated).

Since pins 1-2, 5, and 7-13 are not used to transmit electrical signals in the USB mode, these “pins of the I/O port [are] not electrically connected with the host device” in that scenario. Ex-1002 ¶¶191-193. As explained for Element 1[h], this understanding is consistent with Applicant’s remarks regarding this limitation, which was added by claim amendment during prosecution. Ex-1004 at 46, 52-54 (July 16, 2012 Response at 2, 8-10).

2. **Claim 4: The portable handheld memory card of claim 1 further comprising: a power management unit in communication with the USB controller circuitry.**

Lin teaches the further requirement of “a power management unit in

communication with the USB controller circuitry.” Specifically, as shown in Figure 1A below, Lin’s “IF mode detector 32” (light blue) corresponds to the claimed “power management unit.”

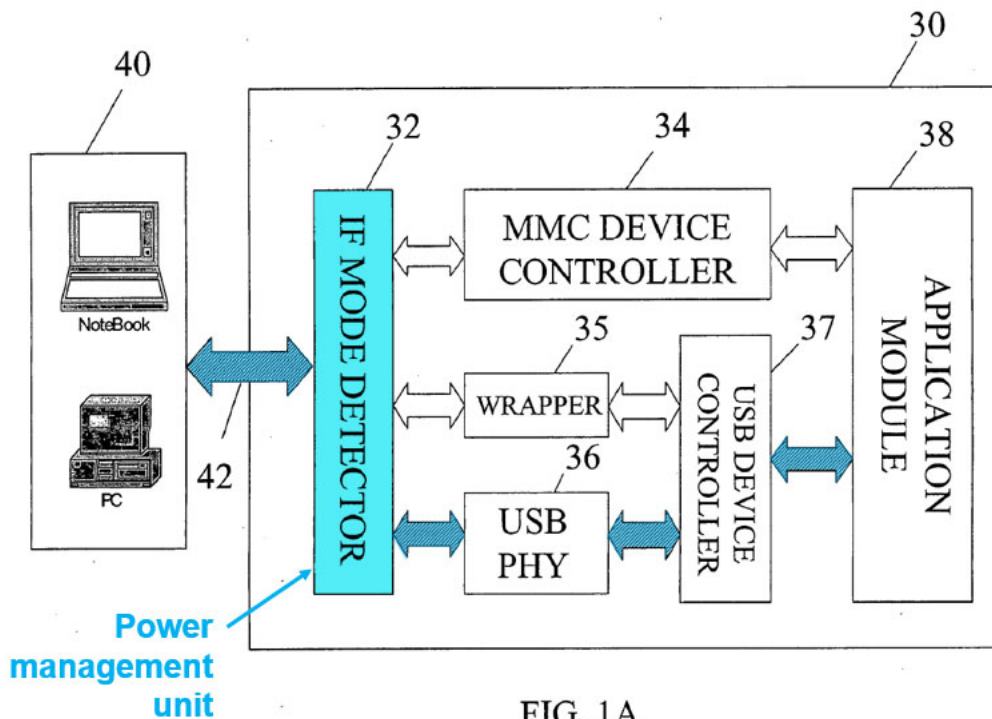


FIG. 1A

Lin, Fig. 1A (annotated).

Lin explains that “IF mode detector 32 detects a mode of operation to distinguish among an MMC mode, a USB mode or a Mu mode when electronic device 30 is inserted into a host 40,” and that it does so by “determin[ing] whether the [power source voltage] VDD is equal to or greater than a voltage level a USB application requires.” Lin ¶¶31, 34, Figs. 1A, 2; *see also id.* ¶30 (“Electronic device 30 includes a 1-, 4-, 8-, or 16-bit interface, and provides low voltage support of 5V/3.3V/1.8V, with zero power consumption during standby.”). Similarly, the ’051

Patent specification discloses a “power management unit 116,” and states that it may convert the “bus voltage Vbus ... to a suitable voltage for use by components of the memory card 100.” ’051 Patent, 3:60-63.

IF mode detector is further shown and described as being in communication with “USB device controller 37,” which is enabled when the host is determined to require the USB mode. *See* Lin ¶34; Ex-1002 ¶¶194-196.¹³

Moreover, a POSITA would have been motivated to implement Lin’s IF Mode Detector as a power management unit in communication with the USB device controller to ensure that, when Lin’s device is in USB mode, its power source voltage requirements are adjusted to comply with the USB standard. Ex-1002 ¶197.

3. Claim 5: The portable handheld memory card of claim 1 further comprising: a host interface module in communication with the I/O port.

Lin discloses “a host interface module in communication with the I/O port.” The ’051 Patent specification discloses a “host interface circuit 114” that “may translate data to and from the SD protocol to be transferred via the SD port 104.” ’051 Patent, 4:4-7.

As indicated in orange in Figure 1C, Lin’s “interface (IF) Mode detector 32”

¹³ The operation of Lin’s IF mode detector is analogous to the “level sensing circuit” of the prior art Kim reference cited during prosecution, *see* Ex-1022, 6:26-32, Fig. 8. The Applicant did not dispute Examiner’s mapping of Kim’s level sensing circuit” to the claimed “power management unit.” *See* Ex-1004 at 72 (Feb. 14, 2012 Office Action at 4). Ex-1002 ¶196, n.11.

and “MMC device controller 34,” individually or collectively, corresponds to the “host interface module” as understood from the intrinsic record.¹⁴

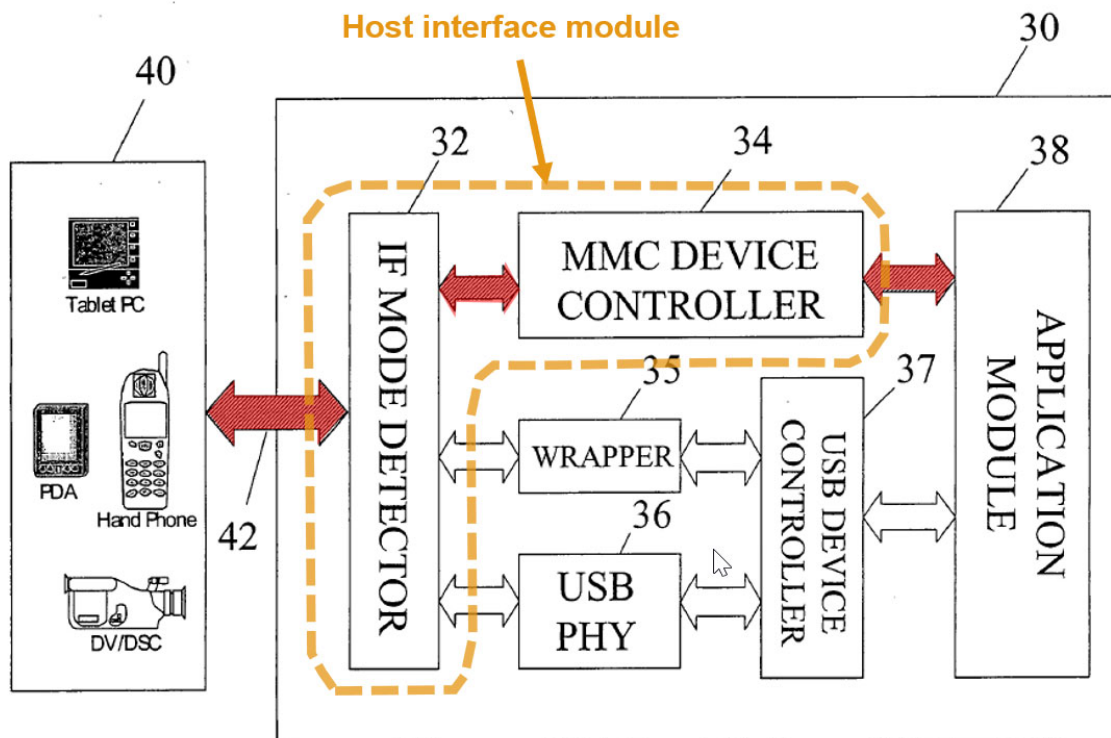


FIG. 1C

Lin, Fig. 1C (annotated).

Lin teaches that “MMC device controller 34 controls data transfer between host 40 and application module 38,” Lin ¶33, which entails translating data. Further, both IF mode detector and MMC device controller *interface* with the “host 40,” either directly or indirectly. *See* Lin ¶¶31. Finally, both modules communicate with

¹⁴ During prosecution, the Applicant did not dispute Examiner’s mapping of the “MMC interface controller” of the prior art Kim reference to the claimed “host interface module,” despite also mapping that feature to the “I/O controller circuitry.” *See* Ex-1004 at 72 (Feb. 14, 2012 Office Action at 4).

the “I/O port” (*i.e.*, the pins or contact pads corresponding to the MMC 4.0 mode).

Accordingly, either or both of Lin’s MMC device controller and IF Mode detector is a “host interface module in communication with the I/O port.” Ex-1002 ¶¶198-201.

4. Claim 6: The portable handheld memory card of claim 1 further comprising: circuitry configured to control read and write operations to the memory.

Lin discloses dependent Claim 6. Specifically, any or all of the USB device controller, USB PHY circuit, or MMC device controller (surrounded in yellow in Figure 1A below) is “circuitry configured to control read and write operations to the memory.”

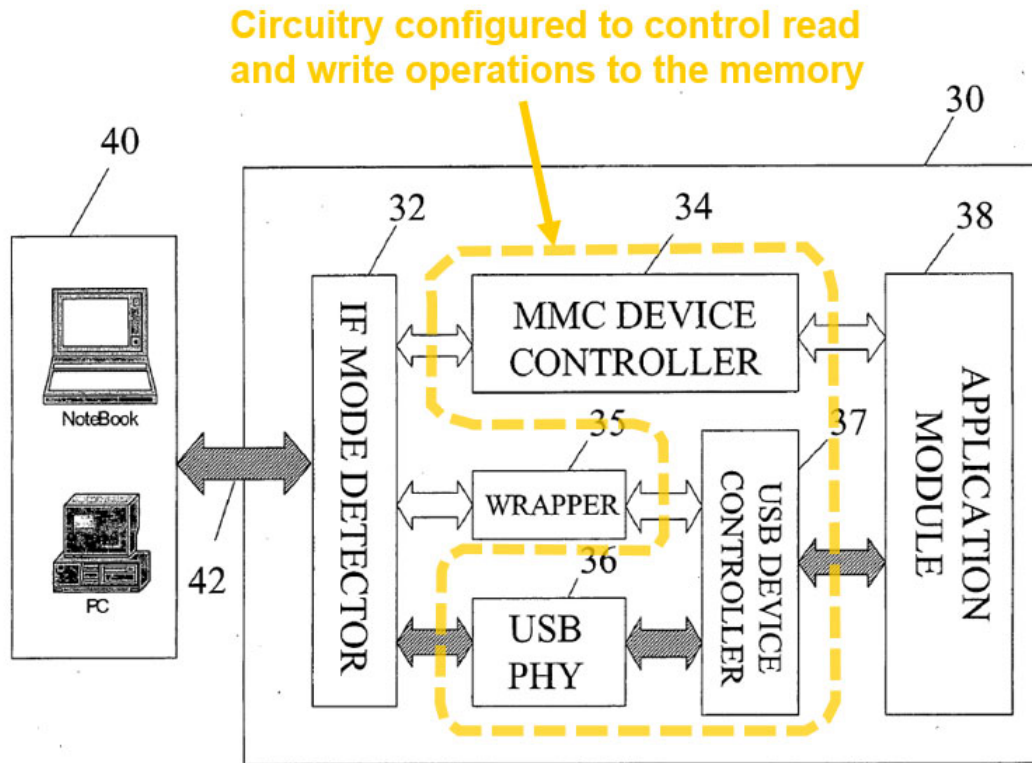


FIG. 1A

Lin, Fig. 1A (annotated).

For example, Lin teaches that its “USB device controller 37 *controls data transfer* over a common bus 42 *between* host 40 and application module 38” (*i.e.*, memory storage) “via USB PHY circuit 36.” Lin ¶31, Fig. 1A. Lin further teaches that its “MMC device controller 34 [also] *controls data transfer* between host 40 and application module 38.” Lin ¶33. In the memory storage context, a POSITA would have known that data transfer “between” a memory storage and a host device entails both read and write operations. Ex-1002 ¶¶202-203; *see, e.g.*, Ex-1006 (Chen) ¶2 (“a memory device has not only an internal solid-state storage medium but also a controller, which ... [w]rites the data from the [external] system into the

solid-state storage medium or read[s] the data stored in the solid-state storage medium”).

5. Claim 7: The portable handheld memory card of claim 1, wherein the I/O port comprises a Secure Digital port.

Lin teaches Claim 7. As discussed for Element 1[c] above, Lin’s memory card (“electronic device”) is operable in the MMC 4.0 mode, and the corresponding pins and/or contact pads used for that mode is an “I/O port.” *See* Section VII.A.1.d, *supra*. Lin likewise discloses that “[e]lectronic device 30 ... is [also] able to support modes of operation compatible with ... SD (security digital) applications,” and that “[s]killed persons in the art will understand that the present invention is equally applicable” to the “SD mode[.]” Lin ¶29. Pursuant to this teaching, an obvious design choice would have been to implement an SD mode in place of the MMC 4.0 mode, as shown in the below modification of Lin’s Figure 1C, with an “SD Device Controller” in place of the MMC Device Controller.

Fig. 1C, using an “SD mode” instead of MMC mode, pursuant to Lin’s teaching

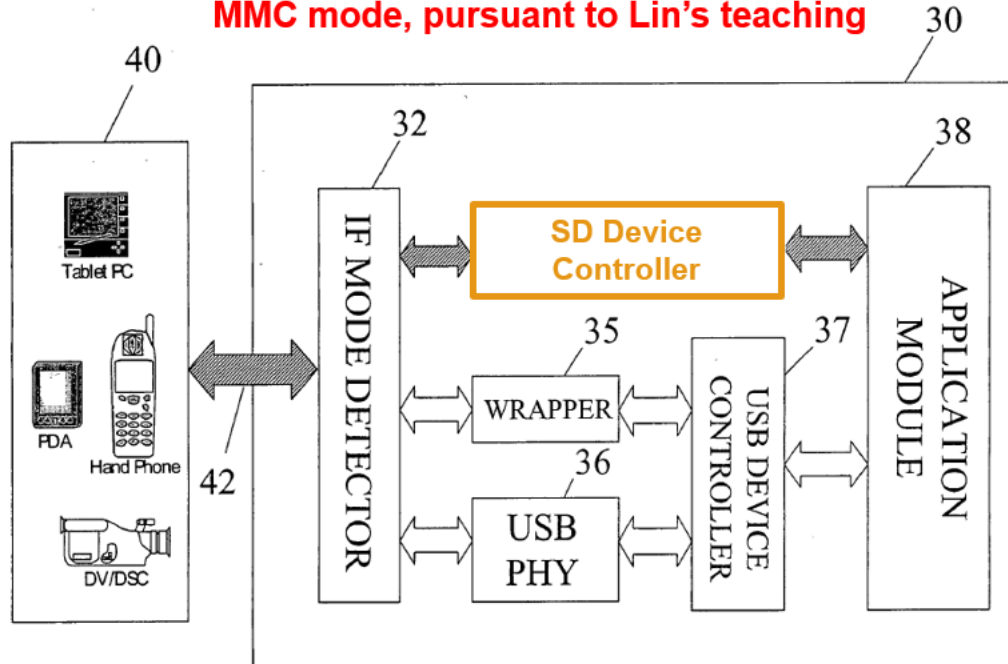


FIG. 1C

Modification of Lin Fig. 1C, to include an “SD Mode.”

A POSITA would have understood that the above implementation of Lin’s memory card features an “SD port” instead of the MMC port discussed for Element 1[c] above, and uses a different pin assignment for the SD mode than for the USB mode, such that one or more pins assigned to one mode is not assigned to the other. Ex-1002 ¶¶204-205; Ex-1028 at 12.

6. Claim 8: The portable handheld memory card of claim 1, wherein the memory comprises Flash memory.

Lin discloses that its “[a]pplication module 38 functions to serve as a memory storage.” Lin ¶31. As Lin also recognizes, it is common knowledge that memory

cards use “flash memories” for storage. Lin ¶3. Accordingly, it would have been an obvious design choice to implement Lin’s memory card using flash memory in the application module 38, as shown below. Ex-1002 ¶206.

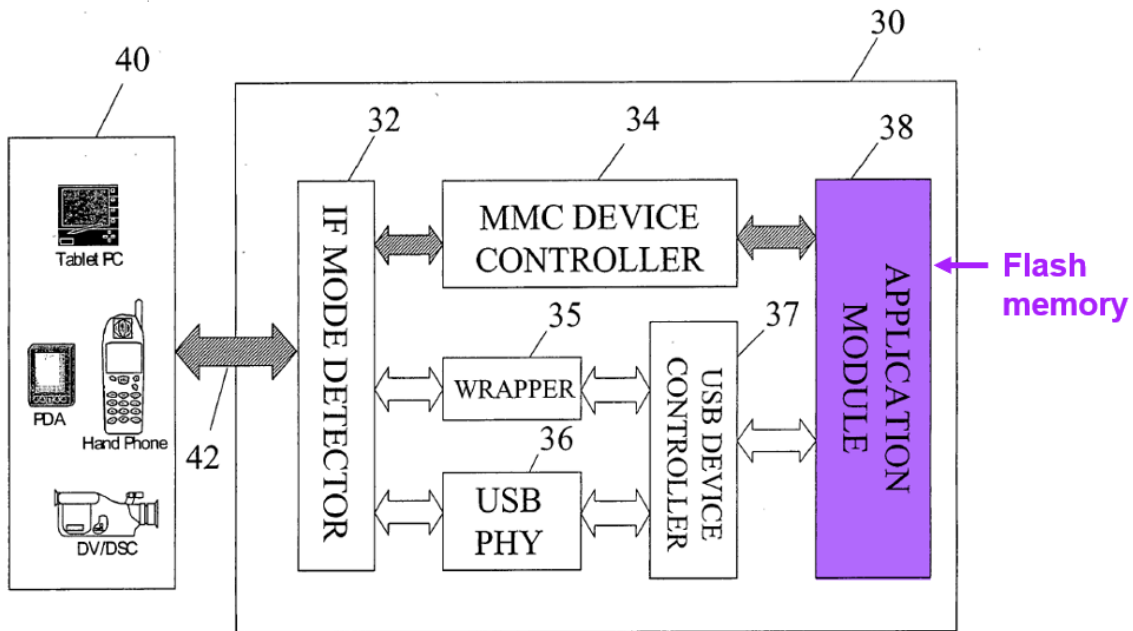


FIG. 1C

Lin, Figure 1C (annotated).

7. **Claim 16:**

- a. **Element 16[Preamble]: A method comprising:**
- b. **Element 16[a]: with a portable handheld card comprising a Universal Serial Bus (USB) port comprising a first set of pins; USB controller circuitry electrically connected with the first set of pins of the USB port; an input/output (I/O) port comprising a second set of pins; I/O controller circuitry electrically connected with the second set of pins of the I/O port; a memory in communication with the USB port and the I/O port; and a housing storing the memory and exposing the USB port and the I/O port, wherein the USB port and the I/O port are positioned to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port and wherein the USB port and the I/O port are positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device:**

See Claim 1, *supra*; Ex-1020 (Claim Mapping Table); Ex-1002 ¶207.

- c. **Element 16[b]: reading data from the memory;**

As discussed for Claim 6 above, Lin discloses “circuitry configured to control read and write operations to the memory.” Such read operations entail “reading data from the memory.” *See* Claim 6, *supra*; Ex-1002 ¶208.

- d. **Element 16[c]: determining whether the data is to be transmitted via the USB port or I/O port; and**

Lin teaches Element 16[c]. Specifically, “IF mode detector 32 detects a mode

of operation to distinguish among an MMC mode, a USB mode or a Mu mode when electronic device 30 is inserted into a host 40,” and it does so by “determin[ing] whether the [power source voltage] VDD is equal to or greater than a voltage level a USB application requires.” Lin ¶¶31, 34, Figs. 1A, 2. Accordingly, Lin’s memory card, using the IF mode detector, “determin[es] whether the data is to be transmitted” between the application module 38 and host 40 “via the USB port or the I/O port.” Ex-1002 ¶209.

e. Element 16[d]: transmitting the data to the host device via the determined port.

See Claim 6 and Element 16[c], *supra*. During a read operation, Lin’s memory card “transmit[s] the data to the host device via the determined port.” Ex-1002 ¶210.

8. Claim 20: The method of claim 16, wherein the I/O port comprises a Secure Digital port.

See Claim 7, *supra*; Ex-1002 ¶211.

9. Claim 21: The method of claim 16, wherein the memory comprises Flash memory.

See Claim 8, *supra*; Ex-1002 ¶212.

10. Claim 23: The portable handheld memory card of claim 1, wherein at least two pins of the USB port are parallel to at least two pins of the I/O port.

Lin discloses Claim 23. For example, Figure 5 shows that all of Lin’s pins and (and corresponding contact pads) are positioned and oriented to be in parallel with

one another. Accordingly, pursuant to the pin assignment chart of Figure 4A, several of the pins of USB port are in parallel to several of the pins of Lin's "I/O port" (*i.e.*, corresponding to the MMC 4.0 mode), as shown below. Ex-1002 ¶¶213-215.

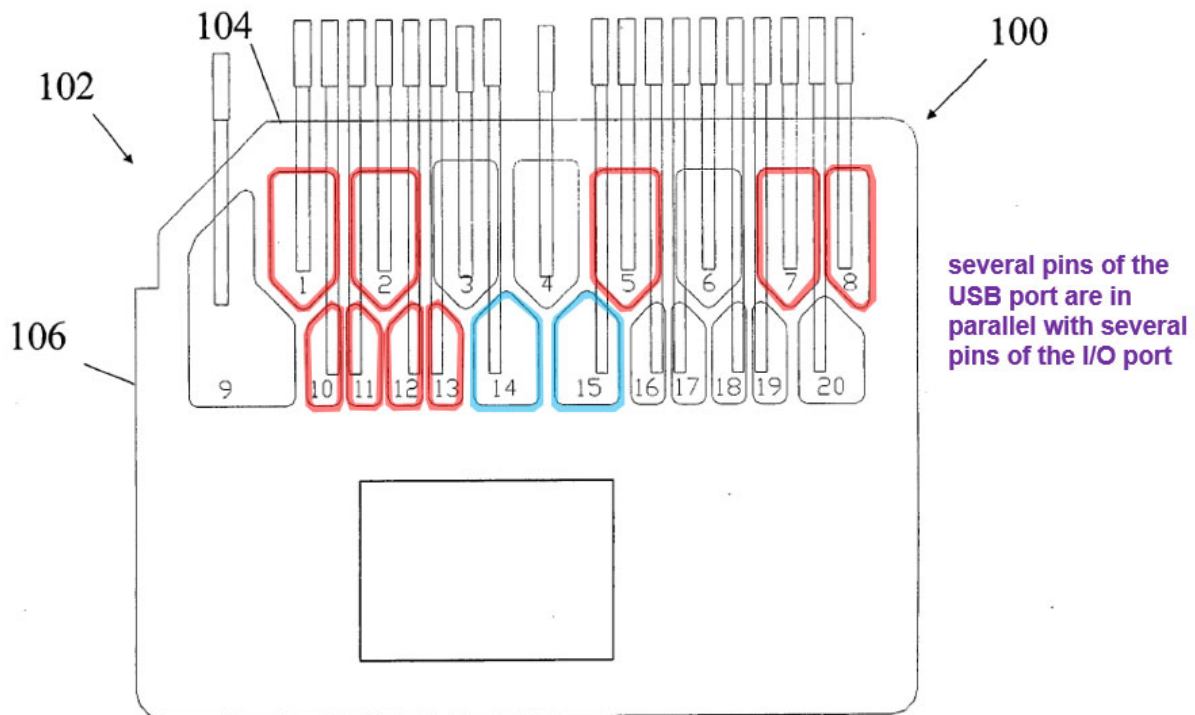
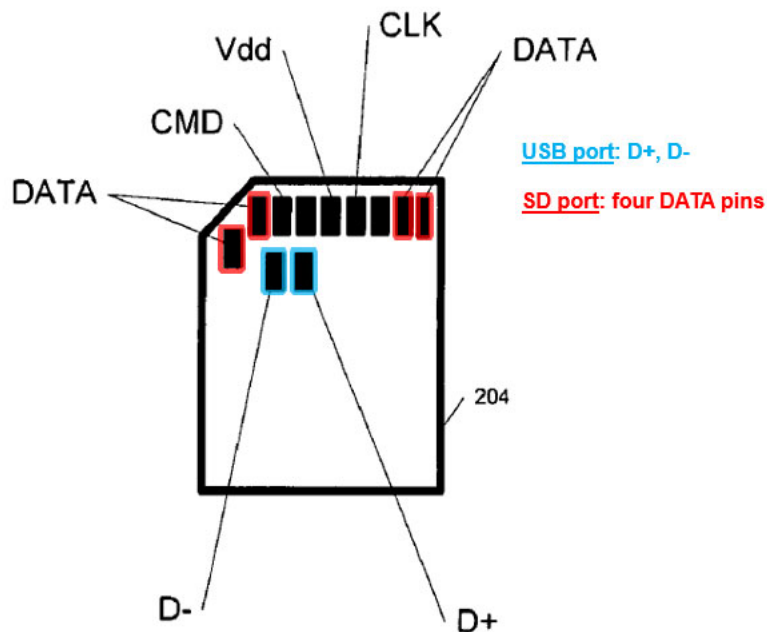


FIG. 5

Lin, Fig. 5 (annotated).

The parallel orientation of the pins in Lin's Figure 5 is the same as in Figure 2 of the '051 Patent, which—as indicated below—shows that the two data pins (D+, D-) of the USB port are parallel to at least two of the DATA pins of the SD port (*i.e.*, "I/O port"). See '051 Patent, 4:38-5:9, Fig. 2.



'051 Patent, Fig. 2 (annotated).

The illustration of Figure 2 is the only disclosure of “parallel pins” contained in the '051 Patent.

11. Claim 24: The portable handheld memory card of claim 1, wherein layout for the USB port is different from layout of the I/O port.

Lin discloses Claim 24. Specifically, the pin assignment chart of Figure 4A indicates that two different sets of pins of Lin’s memory card are assigned to the USB mode (corresponding to the claimed “USB port”) and to the MMC 4.0 mode (corresponding to the “I/O port”), respectively. *See* Elements 1[a], 1[c], 1[h]-[i],

*supra.*¹⁵ Ex-1002 ¶216.

12. Claim 25: The portable handheld memory card of claim 1, wherein the I/O port is configured for mating with an external port.

Lin discloses Claim 25. Specifically, Lin’s “I/O port”—*i.e.*, the set of pins assigned to the MMC 4.0 mode pursuant to the assignment chart of Figure 4A, or their corresponding “exposed electrical contacts”—is configured for mating with the external port of an MMC 4.0-compliant host device 40 connected to the memory card. *See, e.g.*, Lin ¶4 (“In general, a memory card includes exposed electrical contacts on its surface to allow *easy connection to* and removal from a receptacle of a host electronic system or device.”); *id.*, Figs. 1C, 4A, ¶¶31-34, 38; Ex-1002 ¶217.

13. Claim 26: The portable handheld memory card of claim 1, wherein all of the first set of pins electrically connected with the USB controller circuitry is not electrically connected to the I/O controller circuitry.

Lin discloses Claim 26. In the USB mode, “USB device controller 37 controls data transfer over a common bus 42 between host 40 and application module 38.” Lin ¶38, Fig. 1A. The USB mode uses data pins 14 and 15 (*i.e.*, D+ and D-)—the “first set of pins” for Element 1[a]—for that purpose. Lin ¶38. Accordingly, “all of

¹⁵ During prosecution, the Examiner similarly concluded—and Applicant did not dispute—that this “different layout” requirement is disclosed in Figure 8 of the prior art Kim reference, which simply shows *which pins are connected* to the USB and MMC controllers, respectively, but without any indication of the structural layout for those ports. *See* Ex-1004 at 74; Ex-1022, Fig. 8.

the first set of pins” are electrically connected to USB device controller 37, as all such pins are used to transmit electrical signals in the USB mode. Lin’s MMC device controller 34, on the other hand, is only used in the MMC mode. *See* Lin, ¶33, Fig. 1C. As shown in Figure 4A , the MMC mode does not use either of the “first set of pins” associated with the USB mode.

Pins electrically connected to MMC device controller

Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3				
4				
5	CLK	SCLK		CLK
6				
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

All of the “first set of pins of the USB port” are not electrically connected to MMC device controller (used in the MMC mode)

FIG. 4A

Lin, Fig. 4A (annotated).

Since neither of the “first set of pins” are used to transmit electrical signals in the MMC mode, those pins “are not electrically connected to the MMC device controller.” *See* Lin, Figs. 1A, 4A. Ex-1002 ¶¶218-219.

14. Claim 27:

- a. Element 27[preamble]: The portable handheld memory card of claim 1,**
- b. Element 27[a]: wherein the USB port comprises multiple data lines,**

Lin discloses Elements 27[preamble]-27[a]. According to Lin's Figure 4A pin assignment, "[t]he fourteenth and fifteenth pins for the USB mode, *i.e.*, ***D+ and D-***, ***are a pair of data signals***, which may be used to determine whether the USB mode is selected. The pair of data signals (D+, D-) is a complementary pair in which one is at a high level when the other is at a low level." Lin ¶38, Fig. 4A. Accordingly, Lin's "USB port" (pins and/or corresponding contact pads in Figure 5) comprises multiple data pins and corresponding multiple data lines. Lin, Fig. 5; Ex-1002 ¶220.

- c. Element 27[b]: wherein the first set of pins comprise multiple data pins connected to the multiple data lines; and**

See Element 27[a], above. Ex-1002 ¶221.

- d. Element 27[c]: wherein all of the multiple data pins are not electrically connected to the I/O controller circuitry.**

Lin discloses Element 27[c]. Specifically, the pin assignment chart of Figure 4A (annotated below) shows that "all of the multiple data pins" used for the USB port—*i.e.*, pins 14 and 15, as discussed for Element 27[a]—are not used in the MMC 4.0 mode, which corresponds to the "I/O port."

Pins electrically connected to MMC device controller

Pin List	MMC 4.0	MMC SPI	USB 2.0	Mu-interface
1	DAT3	CS#		DAT3
2	CMD	D_In		DAT8
3				
4				
5	CLK	SCLK		CLK
6				
7	DAT0	D_Out		DAT0
8	DAT1			DAT1
9	DAT2			DAT2
10	DAT4			DAT4
11	DAT5			DAT5
12	DAT6			DAT6
13	DAT7			DAT7
14			D+	DAT9
15			D-	DAT10
16				DAT11
17				DAT12
18	MRST#	MRST#	MRST#	DAT13 (MRST#)
19	MDAT	MDAT	MDAT	DAT14 (MDAT)
20	MCLK	MCLK	MCLK	DAT15 (MCLK)

All of the “first set of pins of the USB port” are not electrically connected to MMC device controller (used in the MMC mode)

FIG. 4A

Lin, Fig. 4A (annotated).

As discussed for Claim 26, since neither of the USB port’s data pins 14 and 15 are used to transmit electrical signals in the MMC 4.0 mode, these “*data pins are not electrically connected to*” Lin’s MMC device controller 34 (*i.e.*, the claimed “I/O controller circuitry”). Ex-1002 ¶¶222-223.

D. Ground 4: Claims 2 and 17 Are Obvious Over Lin in View of Thorsten

As shown below, the subject matter of Claims 2 and 17 are disclosed by Lin in view of Thorsten. Ex-1002 ¶¶224-234.

1. A POSITA would have been motivated to combine Lin with Thorsten with a reasonable expectation of success.

A POSITA would have been motivated to combine Lin with Thorsten and would have a reasonable expectation of success in doing so, because they are both from the same field and relate to the same well-known issues. Both references disclose memory cards, and external host devices that read data from, and write to, the memory. *Compare* Lin ¶¶3, 8 *with* Thorsten ¶3. Like Lin, Thorsten discloses a “memory card comprising a non-volatile memory 2,” “a data interface 3 for connecting to a host,” and “a controller 5.” *E.g.*, Lin ¶¶7-8, Figs. 1A-1C; Thorsten ¶13, Fig. 1. A POSITA seeking to store sensitive data in encrypted form, in a manner compatible with different host applications, would have known of and consulted these references. Ex-1002 ¶225.

Lin’s memory card includes an interface (IF) mode detector, multiple controller circuits, and additional circuitry, making it compatible for multiple application standards. *See* Lin ¶¶8, 29, Figs. 1A-C. Lin is silent on the sensitivity of data to be stored in its memory card, or whether its memory card utilizes encryption or decryption. As discussed for Ground 2 (Section VII.B.1, *supra*), Thorsten’s memory card incorporates a “logic component” (*e.g.*, a “programmable circuit”) “that is responsible for the encryption and decryption process.” Thorsten, ¶¶7, 10, 15, Fig. 1. In Thorsten’s configuration, “the card itself handles the encryption and decryption, [so] it is not necessary to know in advance which applications the

memory card is to work with, and it is not necessary to ensure that these applications have the appropriate algorithms.” Thorsten ¶4; *see* Section VII.B.1.

Accordingly, a POSITA would have understood and been motivated to incorporate, in Lin’s memory card, data encryption-decryption functionality that is compatible with various host applications, by implementing Thorsten’s logic component (*i.e.*, encryption-decryption circuitry), to reap Thorsten’s disclosed benefits—*i.e.*, storing sensitive data while remaining compatible with various host applications. Ex-1002 ¶¶226-228; *see* Thorsten ¶¶2-4; *Dystar*, 464 F.3d at 1368.

Additionally, a POSITA would have had a reasonable expectation of success in achieving the collective objectives of Lin and Thorsten—*e.g.*, a multiple standard-compliant memory card that can store sensitive data while remaining compatible with various host applications—by combining their teachings with no change in their respective functions, since Lin and Thorsten disclose similar devices, and because Thorsten’s encryption-decryption circuitry can be readily incorporated into Lin’s device to achieve predictable results. Ex-1002 ¶229. Lin’s memory card features **two controllers** (one for USB applications, another for MMC applications) that “control[] data transfer between host 40 and application module 38” (*i.e.*, memory storage). Lin ¶¶31, 33, Figs. 1A, 1C. Thorsten’s memory card likewise features a “controller 5” that keys instructions to the logic component. Thorsten ¶16. Controller 5 either “connects [to] the logic component” via “third interface 13” as shown in

Figure 1 (Thorsten ¶14), or else “the logic component 6 is designed as an additional module of [the] controller 5” (Thorsten ¶17). Given that Thorsten teaches flexibility in implementation, a POSITA would have observed that the logic component could be readily implemented in Lin’s memory card consistent with Thorsten’s teachings, as illustrated below. Ex-1002 ¶229.¹⁶

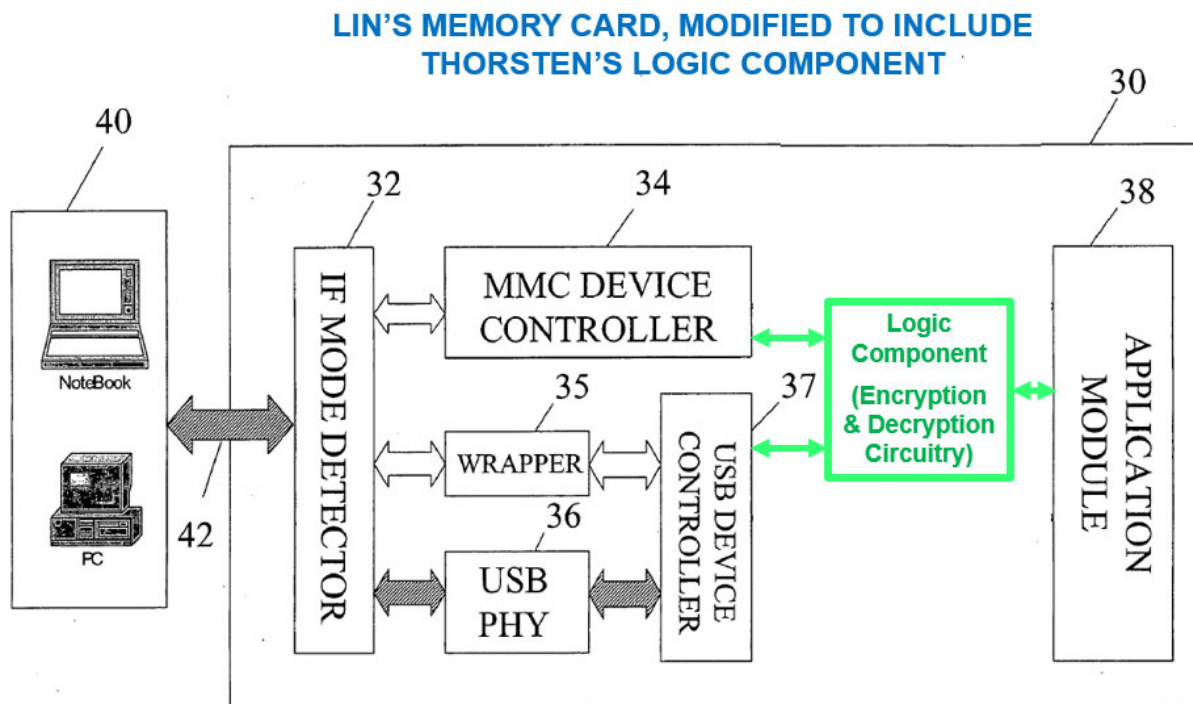


FIG. 1A

Modification of Lin, Fig. 1A (“**Lin-Thorsten Modification**”).

¹⁶ As Dr. Baker explains, the Lin-Thorsten Modification could be implemented slightly differently, where the logic component is situated between the controllers and the IF mode detector, consistent with the collective teachings of the references. Ex-1002 ¶229, n.14.

In such an implementation, encryption and decryption instructions are keyed into the logic component (*i.e.*, programmable circuitry), which “act under the instructions” of Lin’s USB device controller or MMC device controller (depending on the host); “[d]ata to be transmitted ... to [Lin’s] memory ... is encrypted in the logic component 6. [Subsequently,] [w]hen reading data from the memory card, data is transmitted from the memory ... with decryption being performed by the logic component 6.” *See* Thorsten ¶15; Ex-1002 ¶230. Thus, improving Lin by implementing Thorsten’s teachings would have constituted nothing more than the application of a known technique (*e.g.*, encryption-decryption circuitry) to a known device (*e.g.*, Lin’s memory card) to obtain predictable results (*e.g.*, storing and retrieving sensitive data in a manner compliant with various host applications). *See KSR*, 550 U.S. at 416.

2. Claim 2: The portable handheld memory card of claim 1 further comprising: decryption circuitry in communication with the memory and configured to decrypt encrypted data stored in the memory.

Lin in view of Thorsten teaches Claim 2. As discussed in Ground 3, *supra*, Lin teaches the portable handheld memory card of Claim 1. *See* Section VII.C.1, *supra*.

As discussed in Section VII.D.1, *supra*, Lin-Thorsten includes “decryption circuitry”—*i.e.*, Thorsten’s logic component (annotated light green)—that is “in communication with the memory and configured to decrypt encrypted data stored in

the memory.” Ex-1002 ¶¶231-232.

3. **Dependent Claim 17: The method of claim 16, wherein the data is encrypted data, and wherein the method further comprises: decrypting the encrypted data to decrypted data.**

Lin in view of Thorsten teaches Claim 17. As discussed in Ground 3, *supra*, Lin teaches the method of Claim 16. *See* Section VII.A.7, *supra*.

As discussed for Section VII.D.1, *supra*, Lin-Thorsten teaches that “the data [to be read from the memory] is encrypted data, and wherein the method further comprises decrypting the encrypted data to decrypted data.” Ex-1002 ¶¶233-234.

VIII. CONCLUSION

The unpatentability grounds presented above are reasonably likely to prevail, and IPR should be instituted for Claims 1-2, 4-8, 16-17, 20-21, and 23-27 of the '051 Patent based on each of the grounds specified in this Petition.

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CERTIFICATE OF WORD COUNT

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