Invited Paper

Process Flow Innovations for Photonic Device Integration in CMOS

Mark Beals, J. Michel, J.F. Liu, D.H. Ahn, D. Sparacin, R. Sun, C.Y. Hong and L. C. Kimerling
Massachusetts Institute of Technology, 77 Mass. Avenue, Cambridge, Massachusetts 02139

A. Pomerene, D. Carothers, and J. Beattie
BAE Systems, 9300 Wellington Rd, Manassas, VA 20110

A. Kopa and A. Apsel
Cornell University, 412 Phillips Hall, Ithaca, NY 14850

M. S. Rasras, D. M. Gill, S. S. Patel, K.Y. Tu, Y. K. Chen, and A. E. White
Lucent Technologies Bell Laboratories, 600 Mountain Avenue, Murray Hill, New Jersey 07974

ABSTRACT

Multilevel thin film processing, global planarization and advanced photolithography enables the ability to integrate complimentary materials and process sequences required for high index contrast photonic components all within a single CMOS process flow. Developing high performance photonic components that can be integrated with electronic circuits at a high level of functionality in silicon CMOS is one of the basic objectives of the EPIC program sponsored by the Microsystems Technology Office (MTO) of DARPA. Our research team consisting of members from: BAE Systems, Alcatel-Lucent, Massachusetts Institute of Technology, Cornell University and Applied Wave Research reports on the latest developments of the technology to fabricate an application specific, electronic-photonic integrated circuit (AS_EPIC).

Now in its second phase of the EPIC program, the team has designed, developed and integrated fourth order optical tunable filters, both silicon ring resonator and germanium electro-absorption modulators and germanium pin diode photodetectors using silicon waveguides within a full 150nm CMOS process flow for a broadband RF channelizer application. This presentation will review the latest advances of the passive and active photonic devices developed and the processes used for monolithic integration with CMOS processing. Examples include multilevel waveguides for optical interconnect and germanium epitaxy for active photonic devices such as p-i-n photodiodes and modulators.

Keywords: waveguides, modulators, detectors, filters, EPIC, CMOS, integration, photonics

1. INTRODUCTION

The basis and benefit derived from migrating from an electronic based signal system to an optical one is clearly established for telecom and datacom networks. The introduction of optical fiber into the system resulted in a significant shift in network capacity enabling data rate growth at an even faster rate. A figure of merit for communication system performance is the distance-bandwidth product. The transition point for communication systems switching from electrons to photons is found to be >10Mb/s•km. When applied to chip-scale silicon semiconductor interconnects, the key figure of merit is >1 Tb/s•cm. High performance computer systems are one of the leading technology drivers for increasing data communication rates to these levels. Supercomputers are forecasted by the Top500 Supercomputer site (www.top500.org) to operate at 6 petaflops by 2010. Current interconnect technology can support this level of performance in a single system using 2.5 million fiber connections operating at 10 Gb/s[1]. The budget for optical transceivers alone used in this system is in the 10's of millions of dollars. Efforts by DARPA and DOE are already underway to design and create an exascale (10^{18} FLOPS) supercomputer system for 2015. Performance at this level will require increased clustering of CPU's and will help drive the development of single chip multicore processors from the 8 core designs available today to 1000 core processors operating at 4.5TFlops by 2014[2].

Silicon Photonics III, edited by Joel A. Kubby, Graham T. Reed
Proc. of SPIE Vol. 6898, 689804, (2008) · 0277-786X/08/$18 · doi: 10.1117/12.774576

There are significant challenges to realize these levels of performance using electrons alone[3]. The ITRS technology roadmap supports the ability to physically layout these designs by the 22nm node. Power loss increases with the square of the operating frequency and plays a key role in limiting CPU operation to <5GHz. In order to address power loss, electrical interconnect designs require incorporation of low k dielectric materials, k<2.0 including air gap designs that incrementally improve performance but with reduced processing flexibility and greater risk to yield and long term reliability. Operation at higher frequencies and longer interconnect path length will drive circuit designs to use traveling wave transmission lines which will require increased footprint and processing complexity.

Advances in the development of photonic components using high index contrast design is enabling the integration of these devices in CMOS processes leading to creation of monolithic electronic photonic integrated circuits[4,5,6,7]. Drivers for the further development and use of this technology include: increasing demand for high frequency mixed signal processing, ability to operate at high bandwidths in chip-to-chip as well as within the chip for multicore applications with greater power efficiency and lower manufacturing cost. Developing this capability within the silicon CMOS technology would leverage the semiconductor industry's expertise in design, materials processing and integration with the global infrastructure of semiconductor fabs lowering the cost of manufacturing.

There are two general approaches when considering photonic device integration into the CMOS process. The first assumes that no changes are allowed to the CMOS design and/or process flow. This is driven by the capital intensive investment of building a semiconductor fab and the need to avoid risks for products committed to the semiconductor manufacturing process. EPIC designs using this approach are limited in the degree of photonic functionality that can in integrated monolithically into the process flow. In this work, the 180nm CMOS technology node is leveraged to use as much of the existing design and process flow as possible for fabrication of photonic devices; however, the process flow is also adapted for photonic design approaches that maximize incorporating as much photonic functionality into the circuit design as possible.

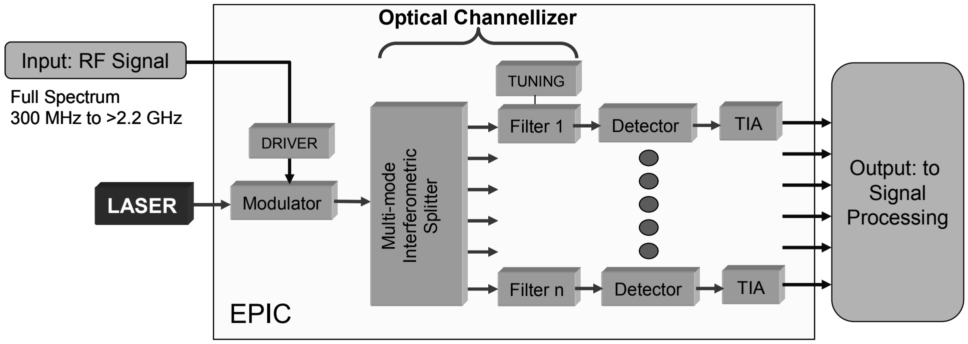
2. EPIC TECHNOLOGY

2.1 Photonic components for monolithic integration in CMOS

EPIC technology includes active photonic devices responsible for the conversion of electronic signals to photonic signals and vice versa in a synergistic system using electronic circuits for signal processing that is monolithically integrated for fabrication in a silicon semiconductor fab. A RF channelizer serves as the objective for this research and provides an excellent application to develop EPIC. The primary functional elements are shown in Figure 1. In this chip, a broadband RF input signal ranging from 300 MHz to over 2.2 GHz must be processed and analyzed. The RF input is first modulated into the optical domain and then split into channels where the components of the spectrum are filtered, detected and output digitally via a transimpedance amplifiers (TIA). The chip operates as a fast Fourier transform device. EPIC in this application enables the simultaneous partitioning of a very wide band RF input before conversion to the digital domain all within a single silicon chip. The benefits of integrated photonics include the high operating speed and bandwidth utilizing a THz signal carrier modulated into a form that is free from EMI, is less susceptible to crosstalk, uses less power in a very small footprint.

Photonic device designs in the EPIC RF Channelizer program are based on using tunable diode laser light sources operating at a nominal wavelength of 1550nm. Cost is always a key factor in any design; however, the precision needed for the optical component functionality dictates light source selection and impacts the appropriate material that is compatible. Light emitting diode sources are low in cost; however, they are less reliable and do not provide the precise wavelength control as are available to tunable diode lasers. Tunable diode lasers are essential when utilizing a wavelength division multiplexing approach.

For minimum device size and lowest optical loss, waveguide devices were made using silicon-on-insulator (SOI) substrates. Channel and ridge waveguide device designs were evaluated using silicon layer thicknesses of 200nm and 250nm, respectively. The bottom oxide thickness was 3.0 um thick and served as the lower cladding to waveguide devices. In the ridge waveguide approach, the ridge height was nominally 200nm leaving a 50nm slab thickness. Channel waveguides are a preferred approach for CMOS processing due to the difficulty in controlling etch to depth processes based on time with across wafer etch uniformity typically >3% 1 sigma. Channel waveguides can be etched using a process that includes an overetch step. Overetching ensures the waveguide structure is completely defined and improves process reproducibility and is not an option with ridge waveguide formation.



Functions
- Optical power source
- Signal Encoding
- Routing
- MUX/DEMUX
- Tuning
- Signal decoding

Design Elements
- Mode transformer
- Modulator w/Driver
- Waveguides
- Splitters
  - MMI
  - Directional Couplers
- Filters
  - Interferometers
  - Resonators
- Detector w/TIA
- Phase shifters
- OE conversion

Fig. 1. Primary components of the EPIC RF Channelizer Chip – Application of active and passive photonics with silicon CMOS electronics.

Silicon CMOS processing provides clear boundary conditions for process integration at each technology node. Some of these include: limits for physical size (in 3D), processing temperatures and time, limits in minimum feature size and cross contamination of both devices being fabricated and/or the process equipment. These are driven by the design rules for transistor formation including junction depths, layout, isolation and the layer thickness of materials forming contacts and the electrical interconnect. The integration strategy for photonics must take into account the total scope of device functionality to be included and the CMOS compatible materials that can be used for that function. Figure 2 is a schematic representation of the CMOS device cross section. The integration of active and passive photonic devices in a monolithic EPIC process can be considered for several areas including: the front end of line (FEOL) transistor device area, the backend of line (BEOL) interconnect layers, last metal before ball grid array (BGA) packaging or backside of the die. Of these choices, monolithic integration of photonics into CMOS is the most viable with FEOL processes.

An alternative to collocating photonics on the same plane as electronics would be to utilize a separate layer for the optical components. 3D chip stacking is one method that would support an EPIC approach utilizing CMOS. In this approach separate chips are created for electronics and photonics. The substrates are thinned, through vias for electrical interconnect are created and then stacked on top of each other. The bonded chips are then packaged in a single module. A monolithically integrated approach might consider placement of the optical plane within the interconnect structure, i.e. between local and global electrical interconnect layers; however, this would require the development of active photonic materials with lower processing temperatures along with added complexity in the routing the electrical interconnect.

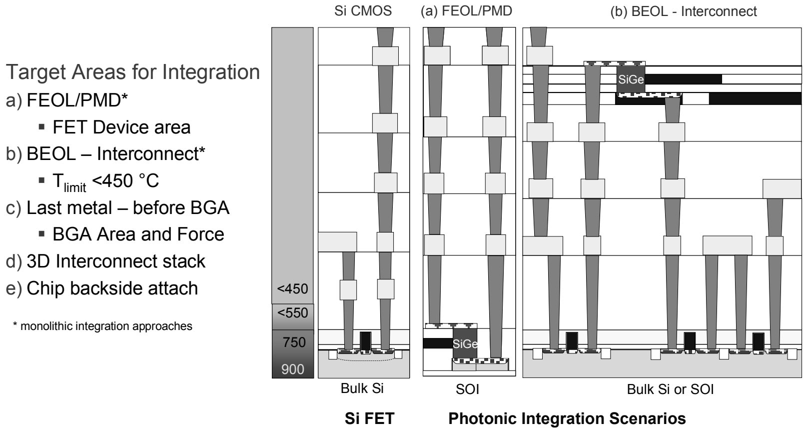


Fig. 2. Monolithic integration of active and passive photonic devices in a silicon CMOS process can be considered for insertion into (a) FEOL/PMD process flow regime where high temperature CVD processes can be supported and (b) BEOL interconnect with the development of low processing temperature materials.

2.2 Passive Photonic Materials

Passive devices for EPIC include: waveguides for transport and routing of optical signals, filters, couplers, splitters, and mode transformers. Passive devices do not require direct electrical signal integration for their function; however, there may be indirect electrical systems such as heaters, both local and global, that serve to set, maintain and control the optical properties needed for proper device operation.

CMOS compatible materials for the waveguides include: silicon oxides, silicon oxynitrides, silicon nitride and silicon. From this selection, only silicon nitride with an index of refraction, n>2.05, and silicon, n>3.5, are possible candidates. The index contrast Δn of >0.6 for nitride and >2.0 for silicon enables the waveguide dimensions to be compatible with the multilayer planarization thickness used for the CMOS chip. Single mode channel waveguides of silicon nitride or silicon using silicon dioxide as the cladding are best designed for TE mode due to the thinner layer requirement compared to TM for confinement and routing. The single mode TE channel waveguide dimensions for silicon nitride and silicon in oxide operating in the 1550nm regime are 400 x 900 nm^2 and 200 x 500 nm^2 (height x width), respectively. Although it is well established that TM mode propagation losses are generally lower, the height of the optical mode exceeds a tolerable thickness (>400nm) in the interconnect making it an unsuitable candidate. The TM mode also suffers from excessive bend loss with tight bend radii (<15um) needed for efficient routing within the chip.

An important design consideration for waveguide material selection is the optical wavelengths to be used. Silicon nitride films can be produced that are optically transparent over a wide free spectral range (FSR), ranging from 600nm to over 1500nm; however, high temperature anneals of 1100°C are required to produce waveguide losses <1.0dB/cm[8]. In CMOS, low pressure CVD (LPCVD) and PECVD nitrides are used in both FEOL and BEOL process flows. These nitride processes have broad absorption loss in the 1400 to 1550nm range due to the presence of N-H bonds limiting its useful range as a waveguide in photonics. LPCVD nitride process temperatures or 750°C limit this application to FEOL processing. PECVD silicon nitride deposition temperatures are less than 450°C making it compatible with low temperature applications such as the metallization processes of the interconnect.

Waveguides have been fabricated at MIT using a modified PECVD silicon nitride process with transmission losses of 1.2-1.6 dB/cm for TE mode channel waveguides fully cladded in silicon dioxide at 1550nm. Single mode waveguides are 400nm thick x 900nm wide. Although SiN waveguides are thicker than silicon waveguides due to the lower index contrast in oxide, integration into CMOS is still possible within the contact region located between the top of polysilicon gates and the first level of metal where the gap in the interlevel dielectric is ~600nm. TE mode silicon nitride waveguides can be used as the global optical interconnect in chip integration for passive devices such as add/drop filters and/or evanescently top coupled to germanium based detectors in a receiver.

Single crystal silicon is transparent above 980nm and suffers no intrinsic loss mechanisms above 1300nm. Optical losses are primarily due to scattering along sidewall interfaces due the sidewall roughness associated with patterning and etching. Control of line edge roughness is an important process consideration for producing low loss TE mode waveguides. CMOS processing provides the means to add both treatment steps and materials that aid in the reduction of sidewall roughness. These include: the use of hardmasks for patterning waveguides, wet chemical treatment of etched sidewalls in oxidation reduction processes and furnace oxidation. Incorporation of these techniques into the CMOS process flow has resulted in the fabrication of silicon crystal waveguides using SOI substrates with <1.0 dB/cm for single mode channel guides and 0.35 dB/cm for hybrid waveguides[9].

PECVD amorphous silicon is another material option for waveguides. The low deposition temperature of ≤450°C makes the material compatible with BEOL interconnect processes and can be used for short optical interconnects of <100um with minimum overall loss in optical signal. Optical losses for single mode TE channel waveguides fabricated using PECVD deposited amorphous silicon films on oxide were measured at 3.5-4.0 dB/cm making the material unsuitable for long optical interconnect. Post deposition temperatures of >625°C should be avoided in order to prevent formation of polycrystalline silicon where optical losses will exceed 10dB/cm[10].

The advantages of using silicon for waveguide devices in CMOS is in the transparency above 980nm, significantly smaller 200nm thickness for highly confined single mode TE mode waveguides and the increasing use of SOI substrates for semiconductor devices. Optical losses of <1.0 dB/cm and the small waveguide cross section make silicon the most attractive material for integration as the global optical interconnect and use in photonic devices such as high order filters[11], couplers, splitters, MZI structures and mode transformers.

2.3 Active Photonic Materials

The greatest challenge for EPIC is the development and integration of CMOS compatible active photonic devices. In order to create this family of components, such as modulators, crystalline materials are typically required to maximize EO conversion efficiency by minimizing defect induced absorption and carrier recombination processes. Crystalline materials can be introduced using chemical vapor deposition (CVD) epitaxy processes. These LPCVD processes typically require temperatures that exceed 900°C and must be grown on crystalline surfaces that are ideally lattice matched to the grown film. Due to the high growth temperatures, the use of CVD EPI films is not considered viable once the CMOS process has formed the transistor gate level with source, drain and graded junction implants.

Silicon is the only crystalline material already in the CMOS process that is available via the substrate. Silicon, an indirect bandgap material, is not an ideal candidate for active photonic devices such as detectors and modulators due to the limitation in ideal responsivity from the band gap transition of 1.11 eV limiting usefulness to detection in the 980nm range[12]. This limitation has been overcome by the use of carrier injection designs[13]. As a semiconductor, silicon can be doped via ion implantation to create a device that can generate free carriers with an applied electric field. The ability to generate and remove carriers in the waveguide by an electric field can be used to control the absorption characteristics of waveguides for switching and modulation functions. Michal Lipson of Cornell University has demonstrated carrier injection modulation using silicon ring resonator structures in a pin diode configuration. Ring resonant modulators of 10 to 15 μm diameter were fabricated in SOI using a ridge waveguide structure. Modulation speeds of over 10Gbps have been demonstrated; however, operation of over 5GHz requires operating at ≥3 volts[14.] Speeds are limited to the rate at which carriers can be injected or removed from the ring. As a coupled resonant device, the FSR of the ring modulator is controlled by ring diameter. Its operation is sensitive to temperature and must be accurately controlled.

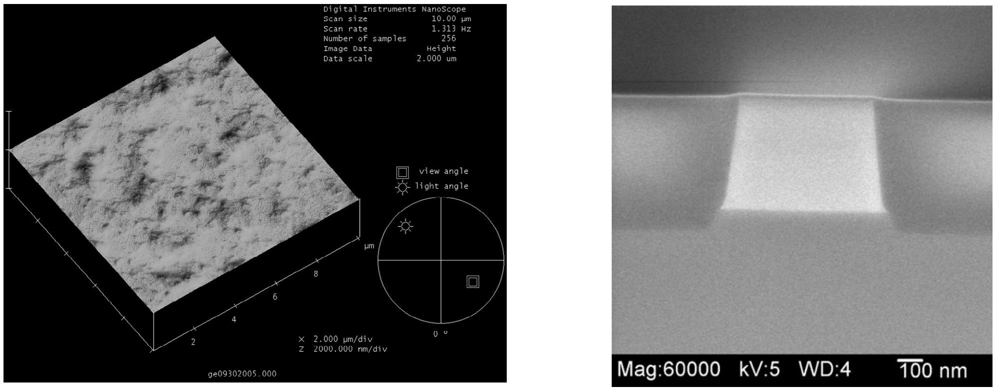
Mach-Zehnder interferometer designs have been the most common approach for modulation due to their excellent linearity in response[15]; however, these designs are fairly large for the CMOS chip, requiring up to 4mm in length to achieve the necessary field induced phase shift in the arms. In both cases, voltages in excess of ≥1.5 Volt are required for operation at ≥10 Gbps[16,17, 18].

Germanium and alloys of silicon with germanium may prove to be the best material for use in fabricating high speed detectors and/or modulators in a p-i-n diode configuration[19,20]. Germanium can be grown epitaxially in thin films on silicon substrates or SOI using a thin, strain relieving buffer layer to produce a crystal with defect dislocation densities on the order of 10^7/cm^2. Epitaxial growth temperatures are 700-750°C using an UHVCVD system. At this temperature germanium can be grown as a blanket film on silicon or selectively in etched oxide trenches over silicon. The Ge CVD process can be inserted in the CMOS flow after polysilicon gate and CoSi2 formation but before tungsten cvd for contacts.

Thin, vertical p-i-n diodes are used as the basis for device design and operation. Germanium is used for the intrinsic layer. Concentration of the carriers in the p and n regions must be sufficiently high to support ohmic behavior with electrical contacts; however the lower contact region must be low enough to minimize damage to the silicon crystal needed for good quality germanium growth. For this reason, the lower electrical contact of the diode is doped via ion implantation using boron forming the p-type region with a dose matching the level used for lightly doped drains (l_{dd}). The vertical pin diode configuration is completed by depositing an amorphous silicon layer over the germanium and implanted with n-type carriers to form the top electrode.

AFM of blanket Ge films grown on a boron doped (p-type) silicon substrates were measured to be <4nm rms roughness indicating good film quality (Figure 3.a). A SEM cross section of an integrated process using blanket germanium film is is shown in Figure 3.b. Germanium was patterned and reactive ion etched followed by blanket deposition with HDPCVD oxide and planarized with CMP to 400nm thickness.

Ge Processing
- UHV-CVD
- Temperature 700°C
  - 4.5 hrs
- Growth rate
  - 2.4 nm/min
- Film roughness
  - < 4nm rms



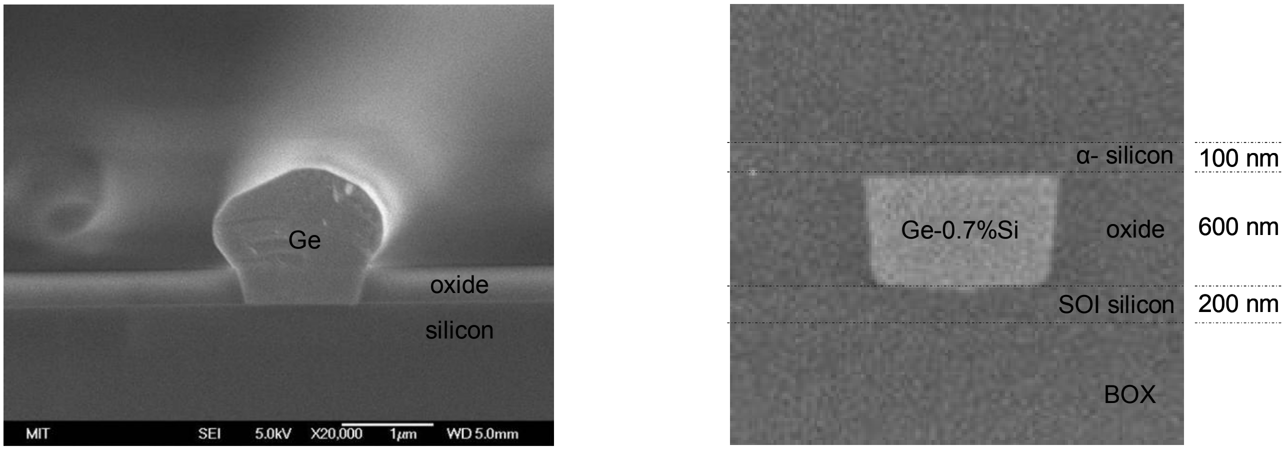
a.) AFM of as grown Ge Film on silicon

b.) RIE patterned Ge on silicon, oxide deposition fill & CMP

Fig. 3. Blanket Ge film processing and integration: a.) smooth blanket Germanium EPI Film on silicon measured by AFM and b.) demonstration of fabricating Ge structures defined using a patterned reactive ion etch process followed by oxide deposited fill and CMP.

In the selective germanium process, Ge is overgrown in etched oxide trenches and then planarized to the oxide surface using a CMP process modified for use with germanium. Complete filling is observed particularly along the oxide trench sidewall as shown in Figure 4.a. Faceting is noted on the overgrown material and is an indicator that the germanium is crystalline. After Ge growth, the structure is planarized using a modified CMP process. For both approaches, a thin 100nm layer of amorphous silicon is deposited in preparation of defining the upper electrode of the pin diode. The integrated result is shown in Figure 4.b.

Waveguide integration to the germanium diode improves responsivity the performance of detectors compared to free space designs. In free space designs the absorption length is limited to the film growth thickness and also defines the path length and transit time for carriers generated. In a lateral waveguide integrated design, the absorption length can be defined independently of the carrier path length defined between the p and n electrodes enhancing responsivity at minimal capacitance. A vertical pin diode configuration allows the use of thin germanium films to be used in TE mode waveguide which have short 400-600nm vertical carrier path lengths and absorption lengths as needed based on the FSR required.



a.) UHVCVD Ge overgrown in etched oxide on silicon

b.) Trench grown Ge-0.7%Si on p-implanted SOI, CMP Planarization, & n-implanted polysilicon top electrode

Fig. 4 Selective, trench filled germanium processing: a.) germanium overgrown in patterned oxide trenches on silicon and b.) process integrated structure of a p-i-n diode using germanium-0.7%siliocn on SOI substrate.

Coupling to the germanium can be achieved using two methods. In the first approach, light is routed in the SOI waveguides and evanescently coupled into the bottom of the germanium device. For fabrication, this is the simplest approach. To minimize loss to the substrate and avoid scattering from the Ge buffer layer interface, a second PECVD silicon waveguide layer is added to create a butt coupled design that ensures incoming light is launched into the center of the germanium structure. The germanium device cross section is enlarged to enhance mode confinement and minimizing edge effects. A vertical coupler is used to evanescently couple light from the SOI silicon waveguide to the upper PECVD silicon waveguide. The multilayer waveguide stack is designed to use evanescent vertical couplers of silicon crystal and amorphous silicon. The waveguides of the coupler are tapered in the coupling region to improve the device tolerance to pattern variations caused by processing. Figure 6 shows a cross section schematic of a Ge based detector using a butt coupled waveguide and an SEM of the device fabricated in the integrated CMOS process.

Modulators are the key device for realizing high level photonic integration in CMOS. Using a similar device configuration as the Ge pin diode detector, an electro-absorption modulator using the Franz-Keldysh effect[21] can be designed to operate at very high speeds in the 1550nm region. In the Franz-Keldysh affect the absorption band edge of the material shifts under the application of an applied electric field. The magnitude change in absorption with respect to absorption, $\Delta\alpha/\alpha$, is the figure of merit corresponding to modulation performance. In order minimize insertion loss while maximizing modulation depth; the lower edge of the absorption tail is used. Figure 9.a is a graph of the FK simulation for low 8kV/cm and 40kV/cm electric fields. The use of higher electric fields produces larger period oscillation as a function of wavelength and is the key to using this effect for a modulator. The ability to provide high electric fields at the Ge diode in a CMOS process depends on having a device with low leakage current and low resistivity ohmic electrical contacts. Strained Ge has shown increases in the absorption coefficient from 62 cm^{-1} to 230 cm^{-1} using an applied field of 70kV/cm at 1647nm. In order to work at 1550nm an alloy of germanium-0.8% silicon is used[20].

A critical requirement for any modulator is that the optical signal must be able to pass through the device in the off state with low insertion loss. The butt coupled waveguide used for the detector is easily modified with the addition of an output waveguide that is matched to the input waveguide of the Ge device. The same vertical coupler is also used to route light from the upper silicon output waveguide to the lower SOI silicon waveguide. A schematic cross section of the waveguide integrated modulator design and an SEM of the actual germanium pin diode is shown in Figure 8 a. and b., respectively. These layers are easily fabricated in the FEOL and PMD CMOS process using CVD, DUV photolithography, reactive ion etch and CMP processes.

3. CMOS FABRICATION

3.1 CMOS Processing

Based on the design and physical sizes of the photonic components reviewed, the 180nm CMOS technology node provides an excellent entry point for integration. The use of 248nm DUV photolithography provides the pattern resolution and overlay accuracy needed for critically designed optical devices such as couplers and resonators while CVD and chemical mechanical planarization (CMP) processes provide excellent layer thickness control enabling additional waveguide layers and structures to be positioned with excellent layer to layer thickness control and smoothness. The maturity of the CMOS process allows the process flow to be tailored for the addition of photonic components with the ability to compensate for the electronics.

EPIC designs were processed using BAE Systems 150nm CMOS foundry located in Manassas, Virginia. Designs are based on the 180 nm CMOS technology node in silicon using 150mm silicon wafers. Germanium films were prepared and grown at MIT's Substrate Engineering Laboratory located in Cambridge, Massachusetts. The CMOS process has a minimum feature size of 150nm and provides dual gate thickness and drive voltage options of 26Å and 70Å operating at up to 1.5V and 3.3V, respectively. Polysilicon and diffusion contacts are based on using CoSi2 with a 7 level planarized BEOL interconnect using AlCu metal and silicon dioxide dielectric. The maturity and robustness of the CMOS process technology enabled a wide range of considerations for photonic integration and an excellent feedback on its impact on electronic device performance. The fundamental design requirements of the CMOS were held constant and provided the basis for photonic device design and integration into the process flow. The primary considerations driving the design of photonic devices were:

- device size – minimization of footprint area and thicknesses of inserted layers
- processing temperatures - stability of materials and proper sequencing in the flow and impact on transistor performance and
- material cross contamination – impacting processes and device performance

Monolithic integration of photonics with CMOS is ideally achieved using SOI substrates; however, a bulk silicon process can be considered. In order to use bulk silicon and include an active photonic device such as a germanium photodiode, a top coupled waveguide scheme is used. For this approach a low deposition temperature material is required due to the insertion of the waveguide into the interconnect layer. PECVD nitride is an ideal candidate based on its deposition temperature of <450°C. The use of silicon nitride in oxide requires the waveguide to be 500 nm thick and 900 nm wide for single mode confinement of TE polarization due to its index contrast of 0.5. Optical isolation of silicon nitride waveguides requires at least a 2.0 um cladding thickness. Oxide filled silicon trenches of ≥1.0um are required below waveguide regions with an additional oxide layer used to minimize substrate coupling losses.

For SOI Substrates, the top crystalline silicon layer of 200 to 250nm thickness is suitable for use as both low loss waveguides and the gate and junctions regions used by transistors for electrical circuits. The oxide layer below the silicon surface (BOX) provides both optical isolation of waveguides and the electrical circuits from the substrate. Above the waveguide, design rules limit routing of first level of metal interconnect near waveguides to minimize loss. The isolation requirements for silicon waveguides are much less than nitride due to the smaller optical mode profile and is an advantage for integration in CMOS.

3.2 EPIC Process Flow in CMOS

Fabrication of photonic device elements occurs in the same sequence as the CMOS flow and minimizes the requirement for additional process steps. The sequence used for EPIC is summarized below.

Wafer Preparation

SOI Substrates are used with 3.0 um bottom oxide thickness. SOI substrates were undoped and had an as received silicon layer thickness of 270 to 280nm. Silicon layers were thinned to 200nm thickness for channel waveguide designs by thermal oxidation. The oxide formed is removed in a Mercury FSI tool with dilute hydrofluoric acid.

First level waveguide formation

After silicon surface preparation for transistor devices regions with pad oxide and nitride depositions, the primary waveguides are formed using the same shallow trench isolation process used for electrical isolation. Additional steps are added for sidewall smoothing of the waveguides. An SC1 wet etch CMOS processing was used to reduce sidewall smoothing by chemical oxidation[12]. A single SC1 process consists of 3 successive steps. The first step uses a dilute 50:1 HF:H_2O solution to remove an initial oxide layer. The second step uses a solution of ammonium hydroxide in hydrogen peroxide and water (1:1:5) to oxidize the exposed silicon sidewall surfaces. This is followed by a second dilute HF treatment to remove the oxide. The SC1 process was found to be most effective at reducing waveguide transmission loss when repeated three times. The remaining trenches are filled with additional oxide and planarized to the nitride surface using CMP.

Nwell & Pwell Implants

A sacrificial oxide is deposited to set up for the n+ and p+ well regions used by the CMOS electronics. Well implant doses exceed requirements for the ge pin diodes and are not used for the photonic devices.

Gate formation

Transistor gate oxide is formed via thermal oxidation of exposed silicon regions following removal of the sacrificial oxides. Gate oxide thicknesses are 26Å for this technology node. LPCVD polysilicon of 250nm is then deposited and etched to form the transistor gate electrodes. Implants for lightly doped drains, l_{dd}, are formed using sequential resist masked processes for p-type and n-type regions. The l_{dd} p-type implant dose of boron is used for the formation of p doped regions of the vertical p-i-n diode structures used for detectors and modulators. Annealing activation of the implant will yield a concentration of 1E19/cm3 enabling low resistivity contacts with the photonics devices.

Sidewall spacers are formed on polysilicon gate electrodes using a deposited conformal oxide followed by an anisotropic reactive ion etch. Graded junction implants for n+ and p+ regions are then formed for transistors followed by deposition of a capping oxide and source/drain anneal.

Salicided junctions of $CoSi_2$ are formed using sputter deposited cobalt reacted with silicon in masked source drain regions of the transistors. Contact windows are defined for active photonic devices to utilize the same process. $TiSi_2$ can also be used and was evaluated as a mitigation risk for cross contamination with subsequent germanium cvd processes.

Second level waveguide formation

Formation of butt coupled waveguides for germanium devices requires the addition of a second level pecvd silicon layer. A dual layer stack of 200nm PECVD TEOS oxide followed by 200nm PECVD a-silicon is formed. The 200nm oxide film defines the coupling gap used for evanescently coupling light vertically from the first level SOI waveguide to the PECVD Silicon local waveguide. Light coupled into the pecvd silicon waveguides is then launched into and through germanium pin diodes for detectors and modulator devices, respectively. The PECVD silicon waveguides are formed using RIE silicon etch.

After etching the PECVD silicon waveguides, a 300nm HDPCVD oxide layer is deposited followed by oxide CMP defining a total stack height of 600nm. The planarized stack is then capped with a thin LPCVD silicon nitride film.

Ge Device Structures

The oxide/silicon/oxide stack is then patterned and etched for the germanium based detector and modulator devices. The exposed regions of the stack are etched using a reactive ion etch process for oxide. The exposed area is too small for endpoint techniques. As a result, the etch is based on time and designed to stop just at endpoint. The residual oxide is then removed in a quick dilute HF etch which also serves to prepare the silicon surface prior to Ge CVD. Germanium or germanium -0.7% silicon films are over grown in trenches to ensure a complete fill. Growth rate on the facetted planes located at the edges of the defined structure is lower and must be accounted for by allowing additional time in growth process.

Ge Top Electrode Formation

After germanium growth, the film is planarized to the oxide layer using a modified CMP process. A 100nm thick PECVD a-silicon film is deposited for the top electrode. The film is then doped with the equivalent of an n-type l_{dd} implant of arsenic. The target carrier concentration is 1E19/cm3 after anneal. The film is patterned and etched using a silicon RIE process defining the top electrodes.

BEOL Processing -the interconnect

At this point all of the major photonic components have been defined within a 610nm height above the silicon surface containing all electronics. The next step is to complete the formation of the premetal dielectric layer with the deposition of an undoped HDPCVD oxide to the required contact height. The height for metal contacts in this technology node is 1.0 micron and defines the position of the first metal layer of interconnect. All steps after the start of the first layer of metal interconnect follow the process of record. The 180nm CMOS process defines interconnect with 6 levels of metal comprised of 4 levels for local interconnect and 2 levels for the global interconnect.

Heater element option

Increasing the contact height to >1.6 microns allows the insertion of one additional component for photonics, micro-heater elements made of silicided polysilicon positioned above or near temperature controlled or tuned structures such as couplers and phase shifters used in MZI devices. The increased contact height minimizes losses due to evanescent field coupling from the waveguide structures. Before tungsten is deposited for the contact metalization, processes with temperatures over 550C, such as silicide formation, can be used; however, temperatures are limited to the thermal budget adjusted to maintain the design performance for the FET's.

Packaging

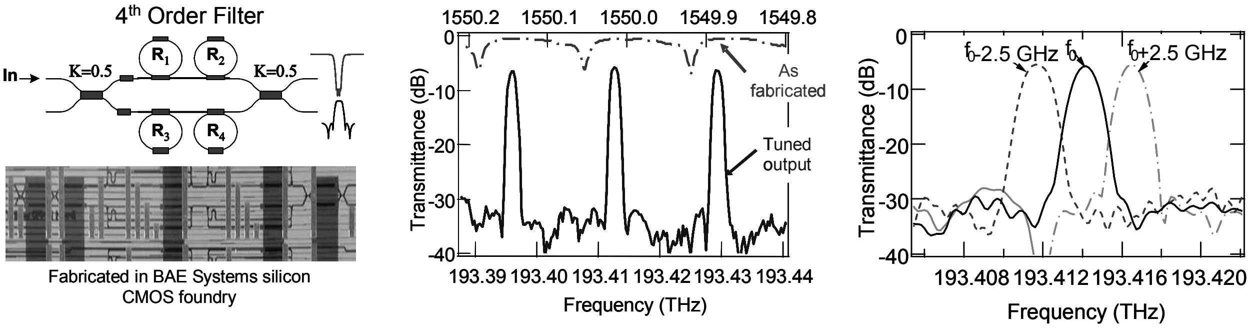
Device designs reported in this work were limited to prototype testing of discrete elements in photonic circuits. Active photonic devices were tested using 3 point GSG electrical probes. Device probe pads were 100um^2 using 150 um pitch. Fiber chip I/O used free space tapered and lens tipped fibers on polished waveguides facets located along the edges of EPIC chips. As a result, Fabry-Perot fringing is observed in the raw data (Figure 8a).

4. INTEGRATED DEVICE RESULTS

4.1 Waveguide devices –Tunable Narrow Band Filter

For the channelizer, a tunable narrowband fourth order pole-zero optical filters were designed and fabricated using the CMOS process described. The filter utilizes silicon channel waveguides in oxide and consists of a Mach-Zehnder interferometer with two ring resonator all pass filters (APFs) on each arm. Operation of the filter is based on splitting the input optical power equally between the upper and lower APF's using a 3dB splitter, routing the split power past two cascaded all-pass filters on each arm. A 3db combiner is used at the filters output. The filter response can be tailored by tuning the zeros and the poles of the individual resonators and is accomplished by changing the coupling strength of the coupling into each resonator while tuning the resonant frequency by the resonator phase. The schematic for a single channel and fabricated layout of a 3 channel device is shown in figure 5 a.

As fabricated and tuned filter response is shown in figure 5b. Roundtrip loss for all APFs was measured to be 0.78 dB. A narrow passband of 3dB bandwidth of 1 GHz, 25dB bandwidth of 2.9GHz is obtained with tuning with >25dB stopband rejection and filter insertion loss of <6dB. The result showed excellent agreement with simulated passbands analysis.



Fabricated in BAE Systems silicon CMOS foundry

a.) Filter design & fabricated layout

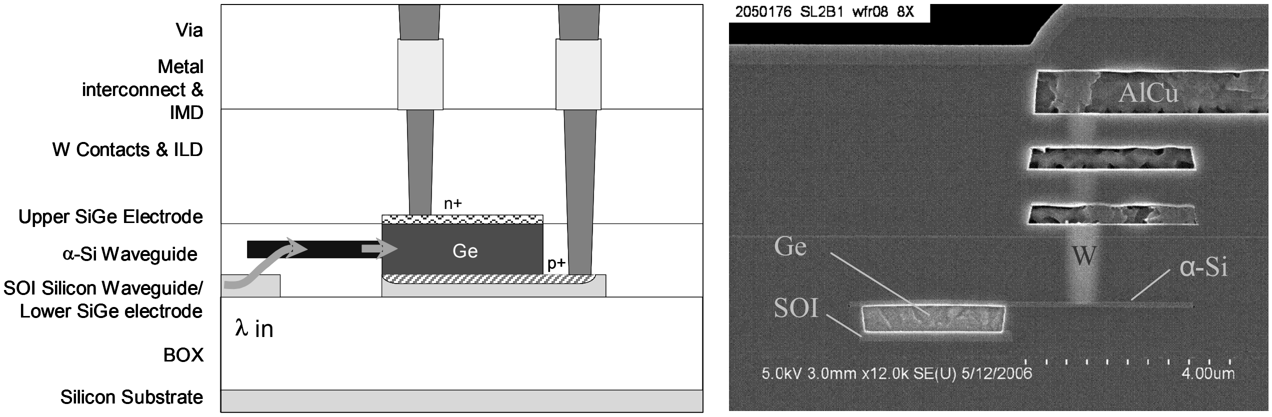
b.) As built and tuned response

c.) Single channel tunability

Fig. 5. 4th order zero pole filters using TE mode silicon waveguides a.) 4th order filter schematic and fabricated chip, b.) as fabricated and tuned filter response showing narrow 3dB bandwidth of 1.0GHz and stopband rejection of 25dB, c.) wide channel frequency tuning of +/-2.5GHz with no loss in filter shape

4.2 Waveguide integrated Ge Detectors

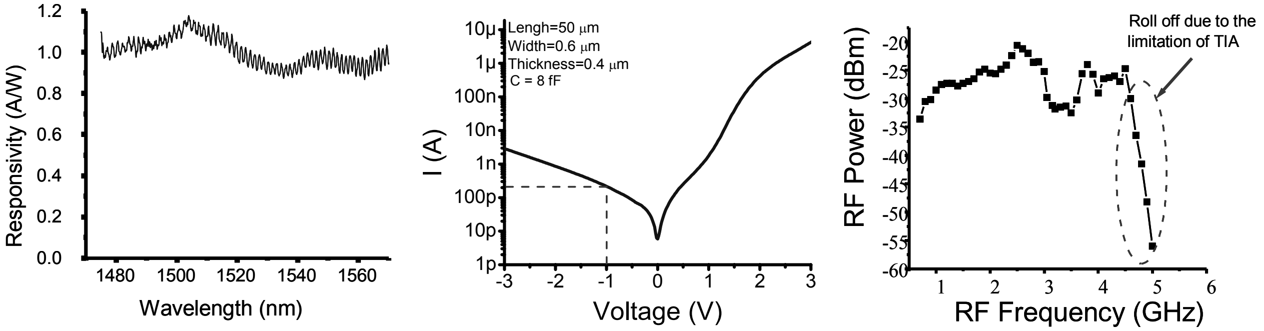
Butt coupled silicon waveguide integrated detectors were fabricated using Ge-0.8%Si selective trench grown films in a fully integrated CMOS process. Responsivity for 50um long devices was >1.0 A/W over a wide FSR of 1460-1570nm demonstrating >90% external quantum efficiency. FSR range is measurement limited. Detector operation beyond 1600nm due can be achieved by modifying the device length to compensate for the decrease in absorption coefficient. Dark current was measured to be <10nA at -1.0 volt bias. In a p-i-n diode configuration, photodetector devices have achieved 8.5 GHz with responsivity of >1 Amp/watt at a bias of 1.0 Volt [10]. The 3dB bandwidth for the waveguide integrated devices was measured at 4.5 GHz. The decreased roll off performance is attributed to the limitation of the TIA. Improvements in the electrical contact scheme to lower resistivity are expected to improve device performance to ≥30 GHz.



a.) Butt coupled Ge p-i-n photodiode

b.) EPIC Ge Device Cross Section

Figure 6. Waveguide integrated vertical Ge pin detector in CMOS process flow with butt coupled silicon waveguides using SOI silicon substrates.



a.) High 1 A/W responsivity at full BW

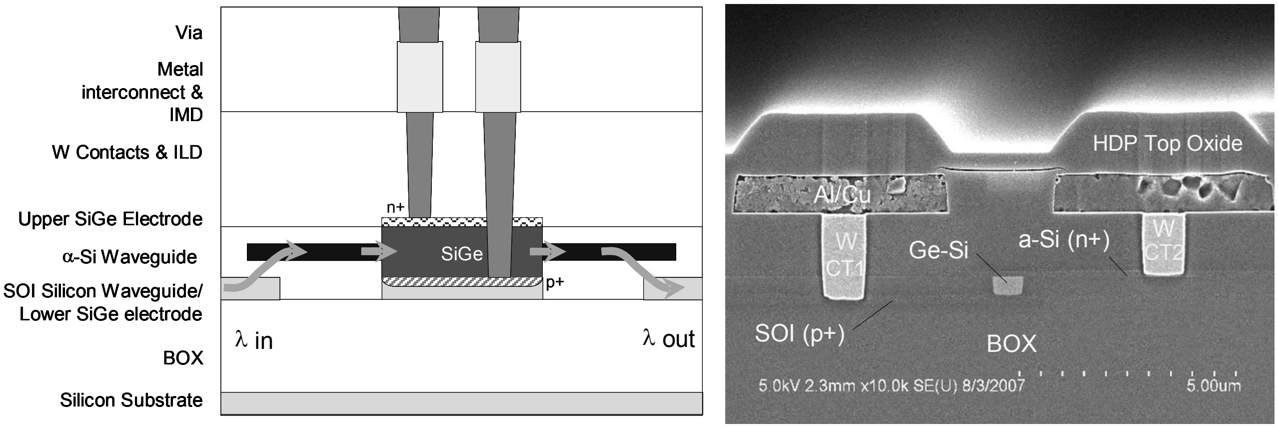
b.) Dark current: 0.2nA at full BW bias (1V)
- RC_{device} = 12 ps

c.) Detector bandwidth >4.5GHz

Fig. 7. Measured performance of silicon waveguide integrated Ge-0.8%Si detectors. a.) high >1.0 A/W responsivity , b.) low 0.2nA dark current at -1V reverse bias, and c.) 3dB bandwidth of >4.5GHz

4.3 SiGE EA Modulators

EA modulators were fabricated using the same butt coupled design and CMOS process as the GeSi detectors. The use of Ge-0.8% silicon alloy enables operation of the modulator in the C band regime targeting 1550nm using the Franz Keldysh effect. Process integration into CMOS is simplified by using the same Ge-Si alloy for both modulators and detectors requiring only one additional CVD growth step. Through coupling of light is accomplished by using an output waveguide matched to the input. Figure 8 shows a cross section schematic of the EA modulator structure and an SEM of the fabricated device.

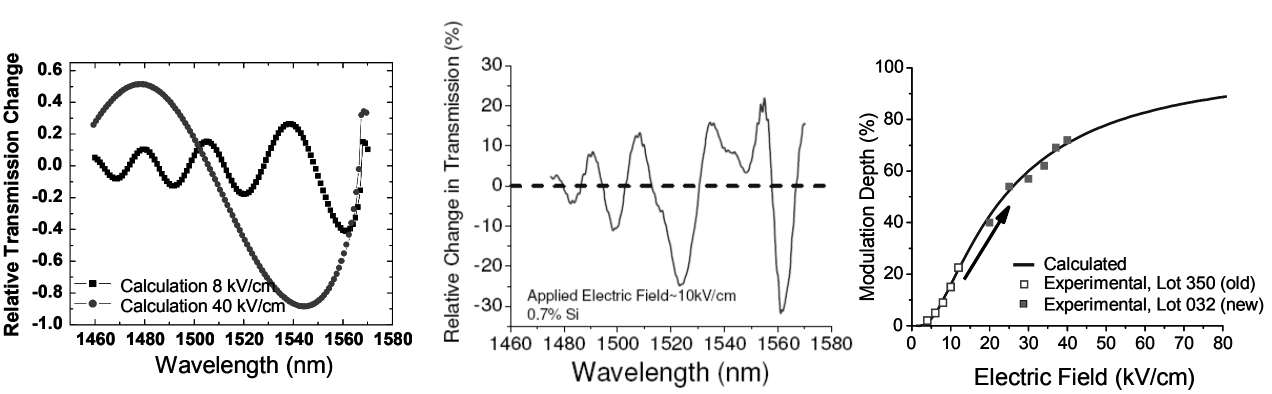


a.) Butt coupled SiGe device

b.) EPIC SiGe Device Cross Section

Fig. 8. Waveguide integrated vertical p-i-n SiGe modulator in CMOS Process flow with butt coupled silicon waveguides using SOI silicon substrates.

EA modulator simulation and fabricated device measurements are shown in figure 9. The relative transmission measurement for low 10kV/cm field shows excellent agreement with the FK simulation in the range of 1460 to 1580nm. Modulation depth of 70% has been achieved with an electric field of 40kV/cm in the wavelength range of 1550-1560nm corresponding to an extinction ratio of >7dB. Higher electric fields were obtained through process improvements that lowered electrical contact resistance. This result confirms our expectations for results previously reported for silicon germanium alloy devices[20]. At these levels of performance and the linear regime observed as a function of field, the FK effect looks to be a very effective method for ultra small, low power, high performance modulators fabricated in a monolithically integrated silicon CMOS process.



a.) FK Simulations b.) EA Modulator measured response c.) Modulation Depth

Figure 9. SiGe EA modulator results

5. CONCLUSIONS

The essential elements of the EPIC technology include: low loss, multilayer waveguides of silicon for signal routing, coupling; high order tunable filters; Si ring and SiGe modulators; and SiGe and Ge detectors. Tunable narrow band optical filters have been fabricated in the EPIC CMOS flow yielding a 3dB bandwidth of 1 GHz at 1.55um and an out of band rejection of >25dB. These devices were fabricated in a CMOS process flow including germanium detectors, amorphous silicon butt coupled modulators and TIA in a channelizer configuration demonstrating the basic integrated capability of EPIC technology.

Information system performance levels approaching the >1 Tb/s•cm level will drive the need for integrated photonics at the chip level. The drivers include increasing demand for high frequency mixed signal processing and the ability to operate at high bandwidths for interchip communication links. Increasing core count in multicore processors will require migration from bus, cluster and mesh based point to point electrical architectures to one that enables true all –to-all broadcast capability. Photonics is seen as the technology that can provide that capability.

In addition to improving device designs and processes for integration, design tools are needed that will enable system designers to translate functional specs into design layouts for masks used in CMOS fabrication. As the technology matures, reliability data will be needed to back additional investment for commitments to manufacture.

Increasing component density and competition for silicon real estate will drive the development of a separate photonic device plane. This could be realized by inserting the optical plane within an upper layer region of the BEOL interconnect. It will require development of new materials compatible with the low temperature processing conditions associated with the copper and low κ dielectric.

The technology for HIC photonics is progressing rapidly. The DARPA sponsored EPIC program resulted in the demonstration of integrated photonic components successfully fabricated in a silicon CMOS process using SOI. Development efforts continue and promise to deliver higher levels of performance and integration with improved designs. The factors enabling integration with CMOS include high resolution 193nm photolithography, CMP, PECVD film deposition, etching and post process treatments combined with the new performance capabilities established for silicon based waveguides and active photonics using germanium EPI in the CMOS process flow.

Based on the advances and implementation of photonic technology from long haul telecom networks to datacom servers, photonics will play an increasing role in supporting communication requirements to the chip level because of its immunity from EMI and high operational data rates enable by wavelength division multiplexing (WDM) designs. Adoption of photonics to the chip level will lead to the creation of new computing architectures and system designs that will be able to take full advantage of the performance gain provided by photonics. There is a significant opportunity to support the need for increased system performance but with an economically attractive alternative.

ACKNOWLEDGEMENT

This work was sponsored under the Defense Advanced Research Projects Agency's (DARPA) EPIC program supervised by Dr. Jagdeep Shah. The program is executed by the Microsystems Technology Office (MTO) under Contract No. HR0011-05-C-0027.

REFERENCES

1. Benner, Ignatowski, Kash, Kuchta, Ritter, “Exploitation of Optical Interconnects in future server architectures”, *IBM Journal of R&D*, Vol. **49**, number 4/5, 2005
2. C.A. Mortiz, D. Young, A. Agarwal, “SimpleFit: A Framework for Analyzing Design Trade-Offs in Raw Architectures”, *IEEE Transactions on Parallel and Distributed Systems*, Vol **12**, No. 7, July 2001
3. Agarwal, “Limits on Interconnection Network Performance”, *IEEE Transactions on parallel and distributed systems*, pp. 398-412, October 1991
4. C. Gunn, “10Gb/s CMOS Photonics Technology”, *Proc. SPIE 6125*, 612501, 2006
5. M. Morse, O. I. Dosunmu, G. Sarid, and Y. Chetrit, “Performance of Ge-on-Si p-i-n Photodetectors for Standard Receiver modules”, *IEEE. Photon. Technol. Lett*. Vol. **18**, 2442-2444 (2006).
6. C. L. Schow, S. J. Koester, L. Scharesa, G. Dehlinger and R. A. John, “High Speed, Low Voltage Optical Receivers Consisting of Ge-on-SOI photodiodes paired with CMOS IC’s”, *Proc. SPIE,* Vol. 6477, 647705, 2007.
7. Michel, Liu, Ahn, Sparacin, Sun, Hong, Giziewicz, Beals, Kimerling, Kopa, Apsel, Rasras, Gill, Patel, Tu, Chen, White, Pomerene, Carothers, Grove, “Advances in fully CMOS integrated photonic devices”, *Proc. SPIE* Vol. 6477*,* 64770P, 2007
8. Shaw, Guo, Vawter, Habermehl, Sullivan, “Fabrication techniques for low-loss silicon nitride waveguides”, *Proc. SPIE*, Vol. 5720, pp. 109-118, 2004
9. D.K. Sparacin, S. Spector, Lionel Kimerling, “Silicon Sidewall Smoothing by Wet Chemical Oxidation”, Journal of Lightwave Technology, Vol. **23**, No. 8, 2005
10. Agarwal, A.M. Ling Liao; Foresi, J.S.; Black, M.R.; Xiaoman Duan; Kimerling, “L.C. Low-loss polycrystalline silicon waveguides for silicon photonics”,Journal of Applied Physics, v **80**, n 11, p.6120-3,1 Dec. 1996
11. M.S. Rasras, D.M. Gill, S.S. Patel, K.-Y. Tu, Y.-K. Chen, A.E. White, A.T.S. Pomerene, D.N. Carothers, M.J. Grove, D.K. Sparacin, J. Michel, M.A. Beals, and L.C. Kimerling, “Demonstration of a Fourth-Order Pole-Zero Optical Filter Integrated Using CMOS Processes”, *IEEE Journal of Lightwave Technology*, **25**, 87-92, (Jan 2007)
12. Saleh, Teich, *Fundamentals of Photonics*, pp. 573-576, 660-661, John Wiley & Sons, Ney York, 1991
13. Q. Xu, B. Schmidt, S. Pradhan, M. Lipson, “Micrometer-scale silicon electro-optic modulator”, Nature, **435** (7040), p. 325-327, 2005.
14. Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, M. Lipson, 12.5 Gbit/s carrier-injection-based silicon microring silicon modulators“, Opt. Express **15**, 430-436, 2007
15. Xie, Khurgin, Kang, Chow, “Linearized Mach-Zehnder Intersity Modulator”, IEEE Phot. Tech. Lett, **15(**4), p.531-533, 2003
16. Gunn, “CMOS Photonics^{TM} – SOI learns a new trick”, 2005 SOI Conference Proceedings, IEEE, p.7-13, 3-6 Oct 2005
17. Ling Liao, Samara-Rubio, Morse, Liu, Hodge, Rubin, Kell, Franck, “High speed silicon Mach-Zehnder modulator”, Optics Express, v 13, n 8, 18 April 2005
18. Liao, Liu, Rubin, Basak, Chetrit, Nguyen, Cohen, Izhaky, Panicca, “40 Gbit/s Silicon Optical Modulator for High-Speed Applications”, Elect. Lett. **43**(22), 2007
19. D. Ahn, C.-Y. Hong, J. Liu, W. Giziewicz, M. Beals, L. C. Kimerling, J. Michel, J. Chen, and F. X. Kärtner, “ High performance, waveguide integrated Ge photodetectors”, *Optics Express* **15**, 3916, 2007
20. J. Liu, D. Pan, S. Jongthammanurak, K. Wada, L.C. Kimerling, and J. Michel, “Design of monolithically integrated GeSi electroabsorption modulators and photodetectors on an SOI platform”, *Optics Express* **15**, 623, 2007.
21. S. Jongthammanurak, J. Liu, K. Wada, D. D. Cannon , D. T. Danielson, D. Pan, L. C. Kimerling, and J. Michel, “Large Electro-optic Effect in Tensile Strained Ge-on-Si Films”, *Appl. Phys. Lett*. **89**, 161115-1-3, Oct. 2006.