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(54) **SOLAR BLIND ULTRA VIOLET (UV) DETECTOR AND FABRICATION METHODS OF THE SAME**

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Publication Classification

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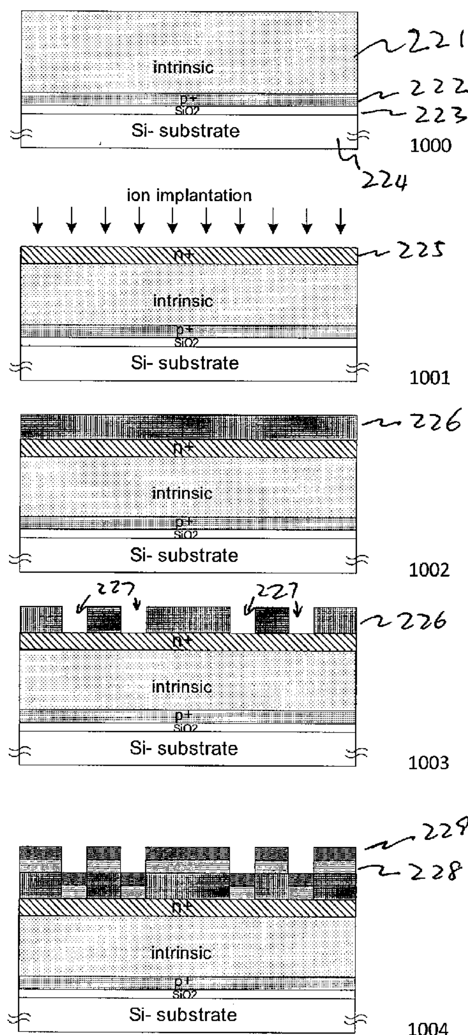
H01L 31/105 (2006.01)
H01L 31/18 (2006.01)
H01L 31/107 (2006.01)

(52) **U.S. Cl.** **257/21**; 438/73; 257/E31.063; 257/E31.061

(57) **ABSTRACT**

Described herein is device configured to be a solar-blind UV detector comprising a substrate; a plurality of pixels; a plurality of nanowires in each of the plurality of pixel, wherein the plurality of nanowires extend essentially perpendicularly from the substrate.



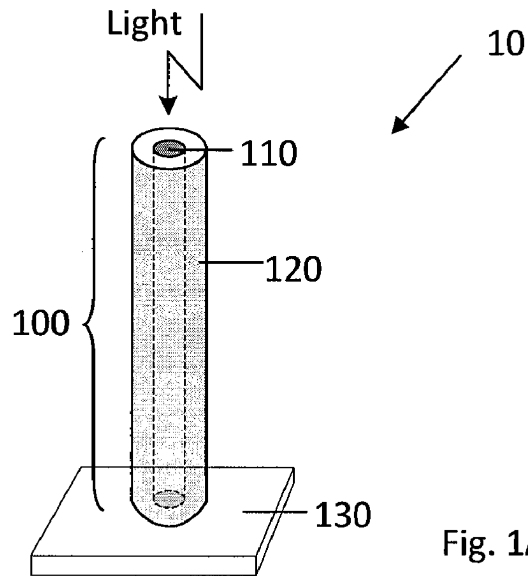


Fig. 1A

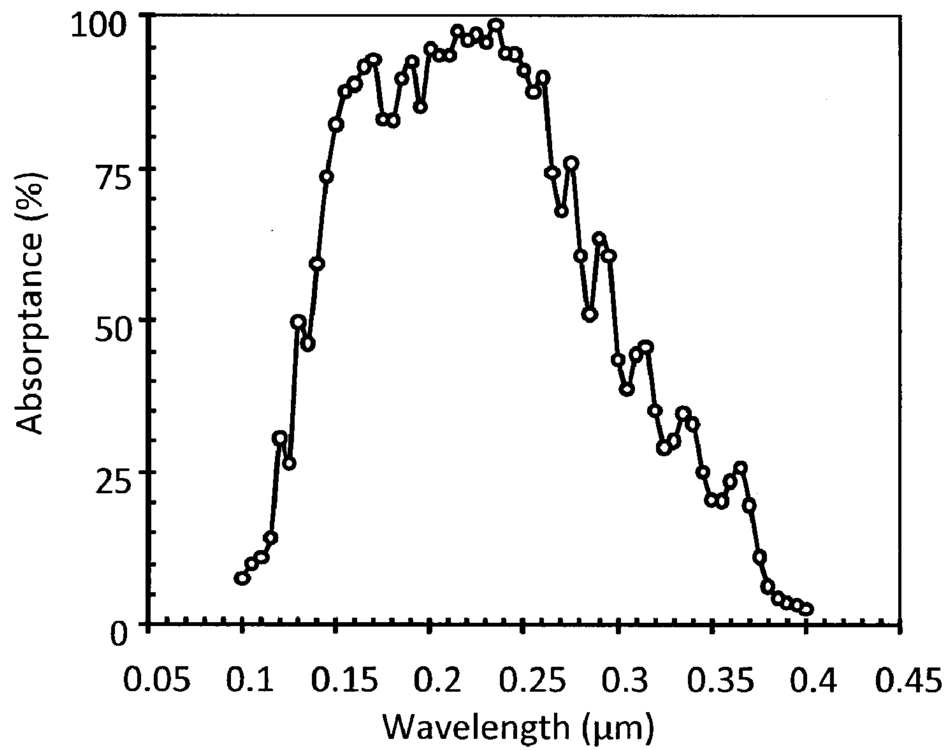


Fig. 1B

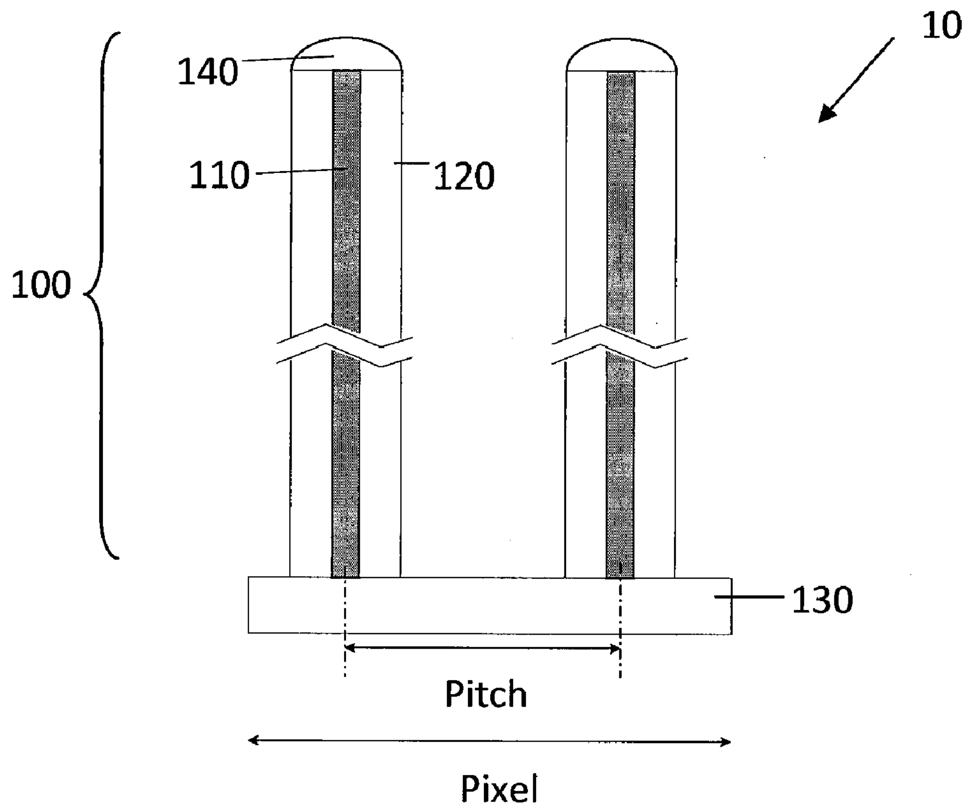


Fig. 1C

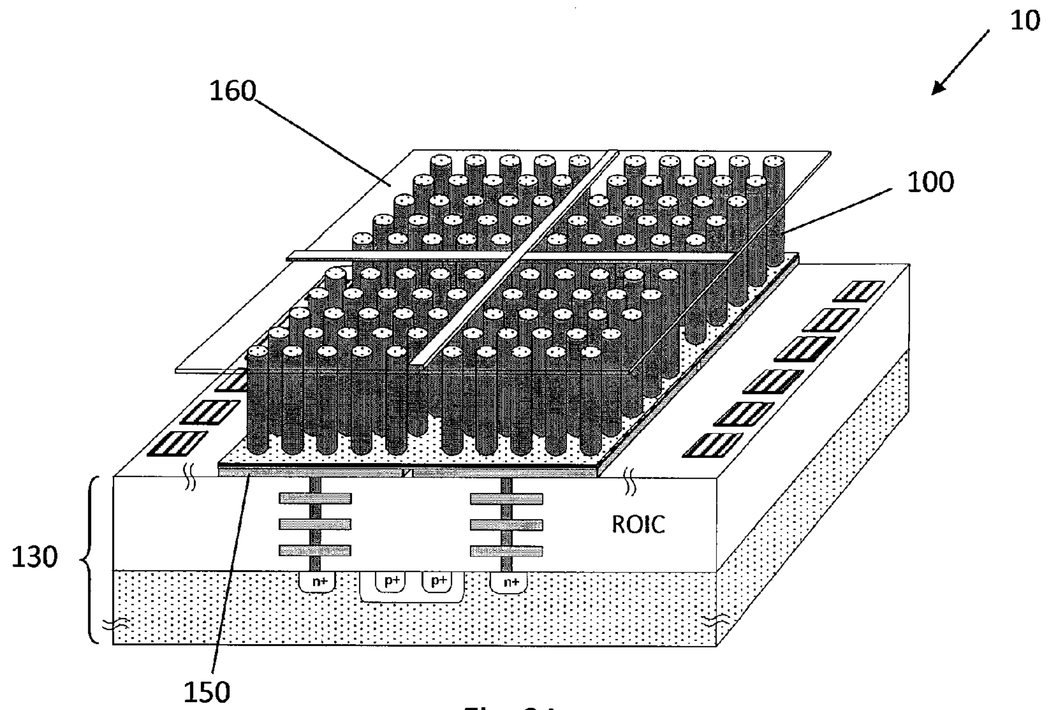


Fig. 2A

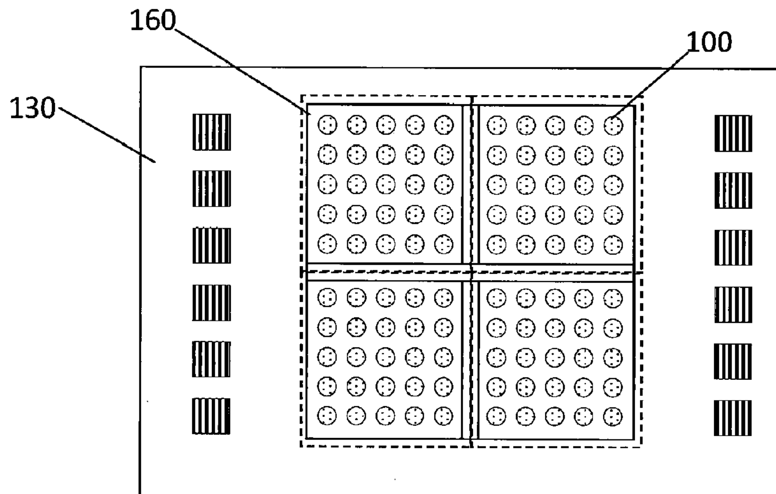


Fig. 2B

Fig. 3

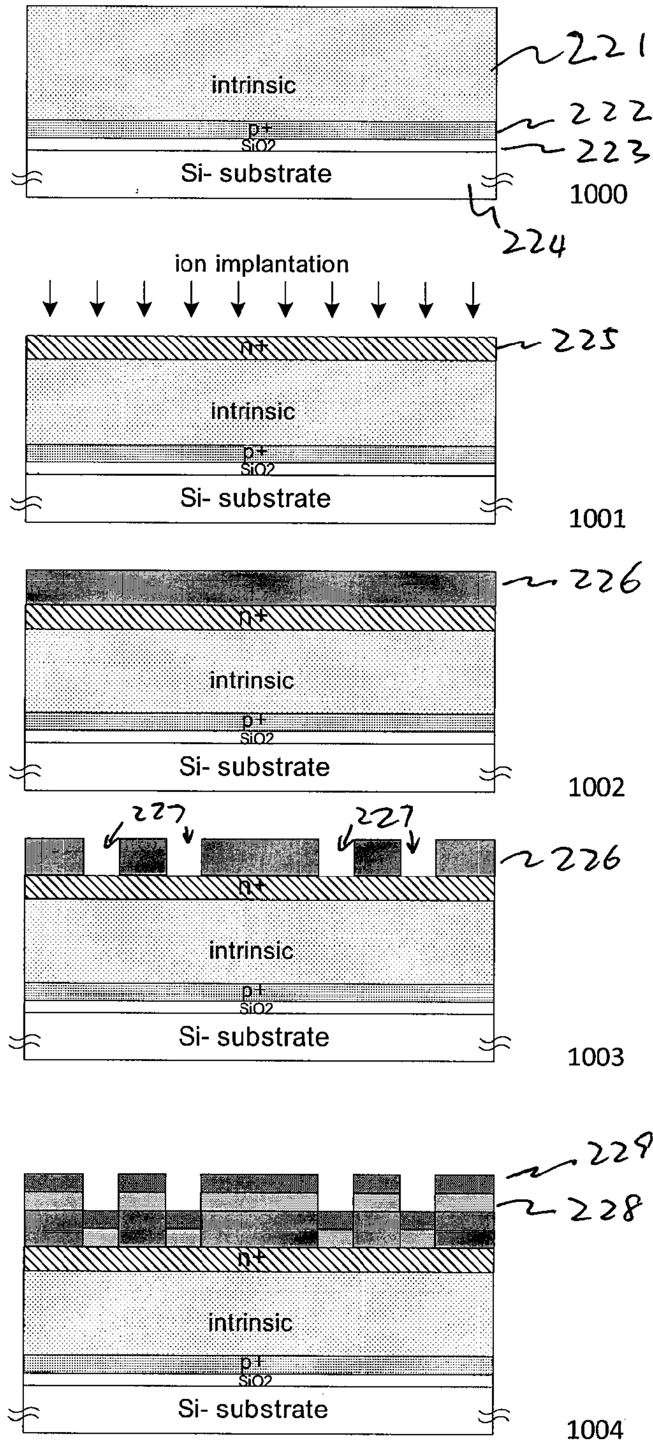
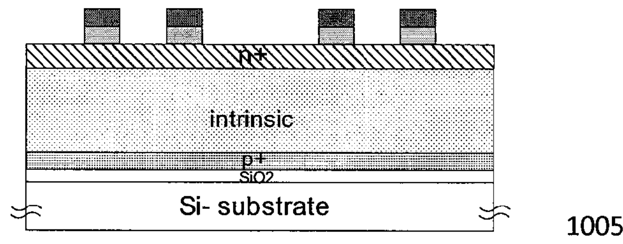
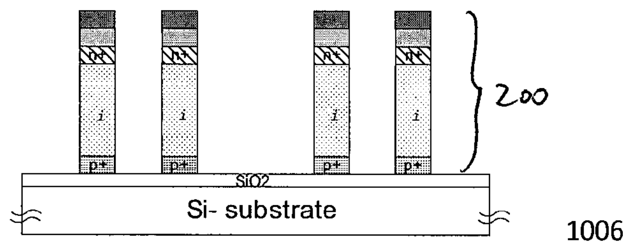
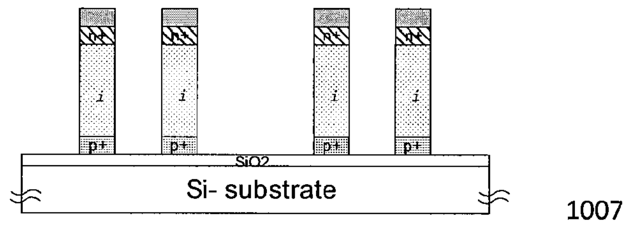


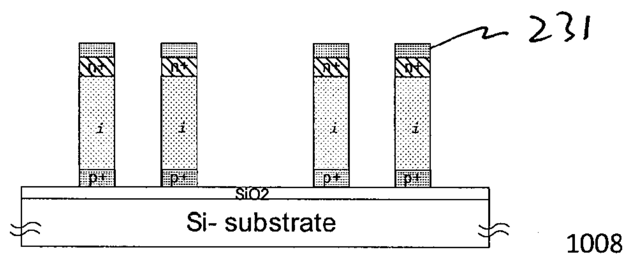
Fig. 4

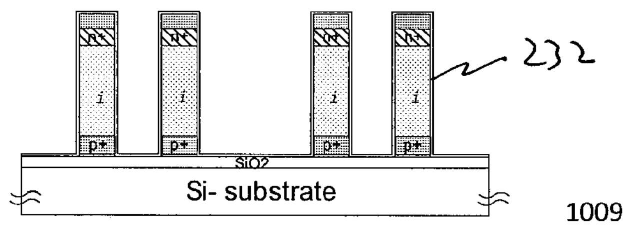
Fig. 4 cont'd











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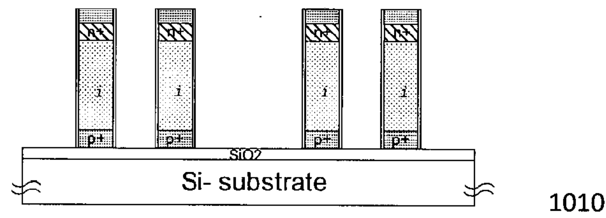

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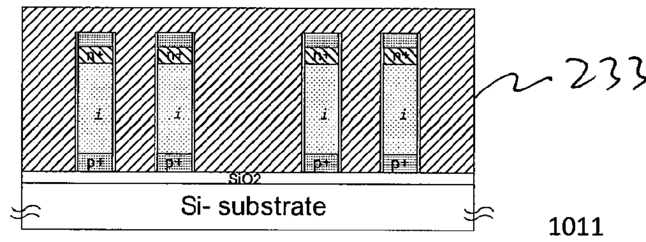

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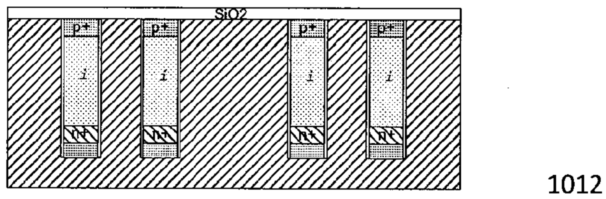

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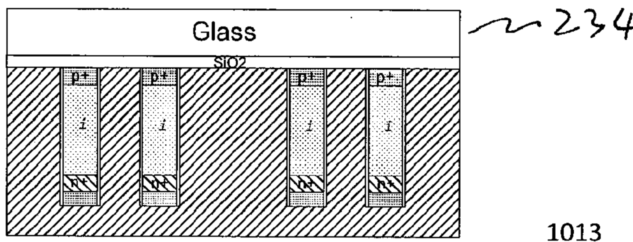

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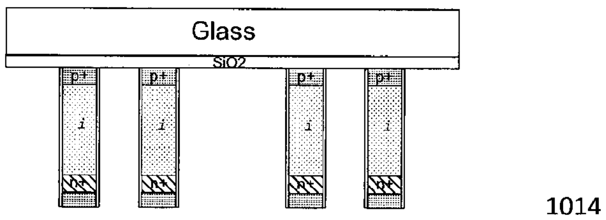

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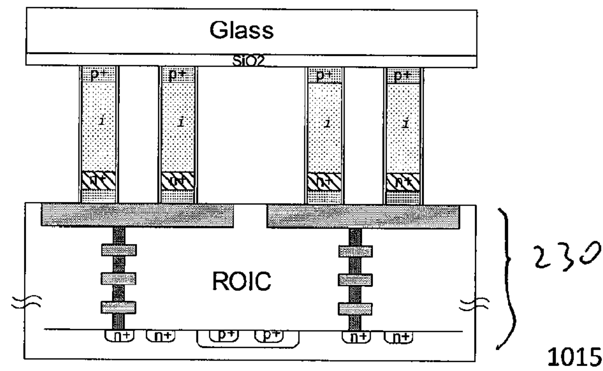

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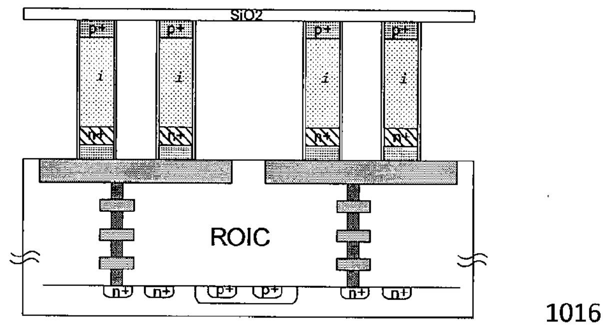

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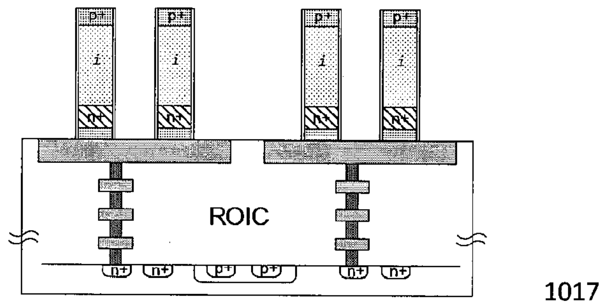

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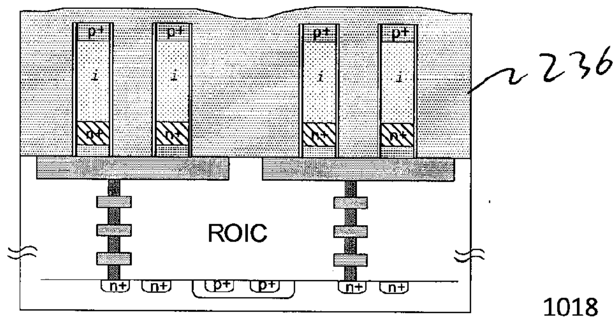

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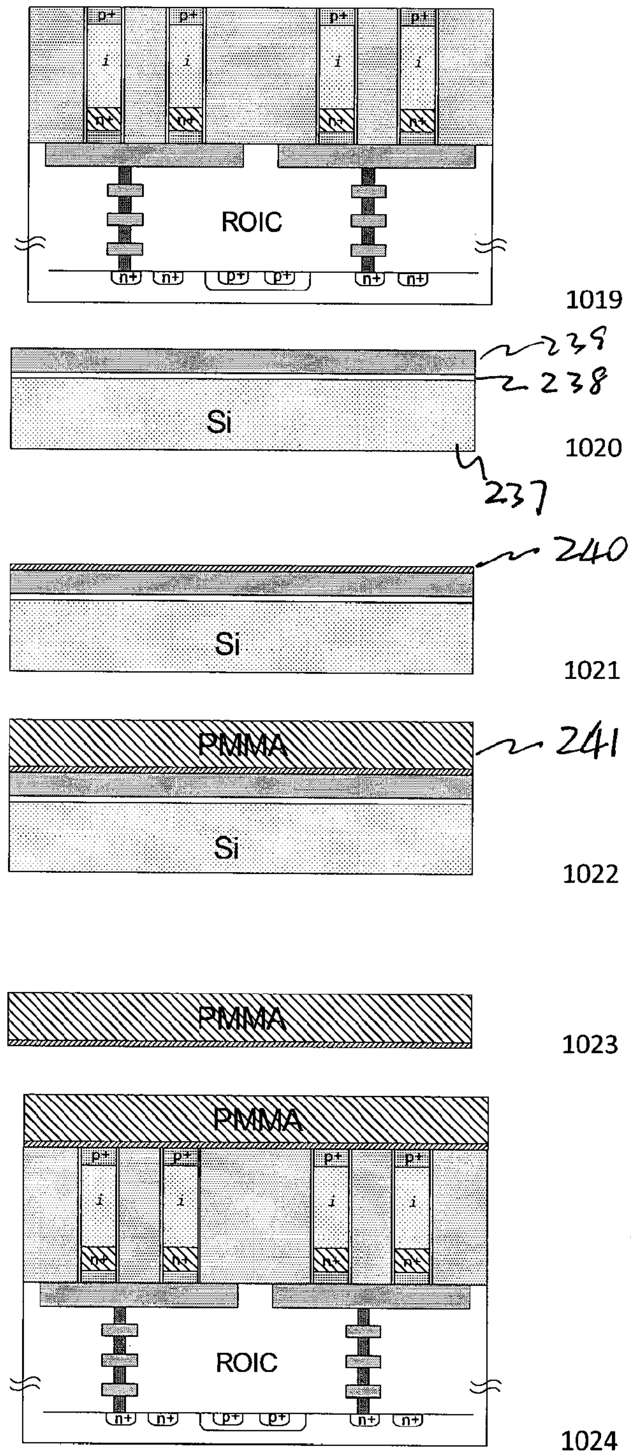

Fig. 4 cont'd

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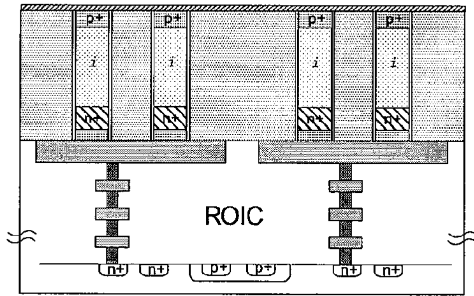

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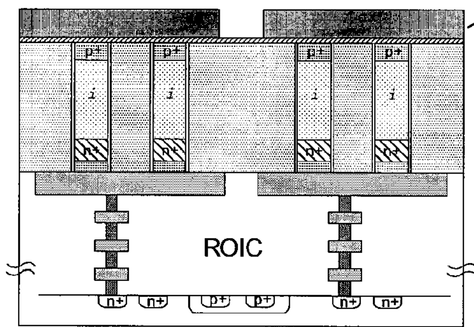

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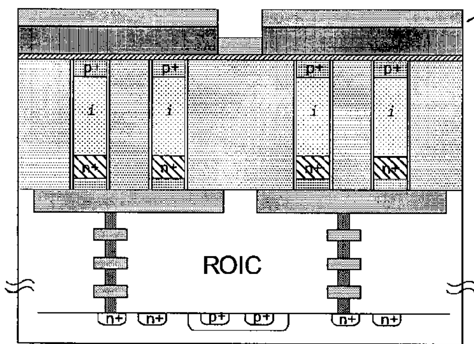

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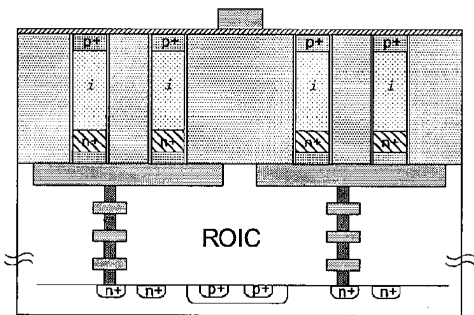

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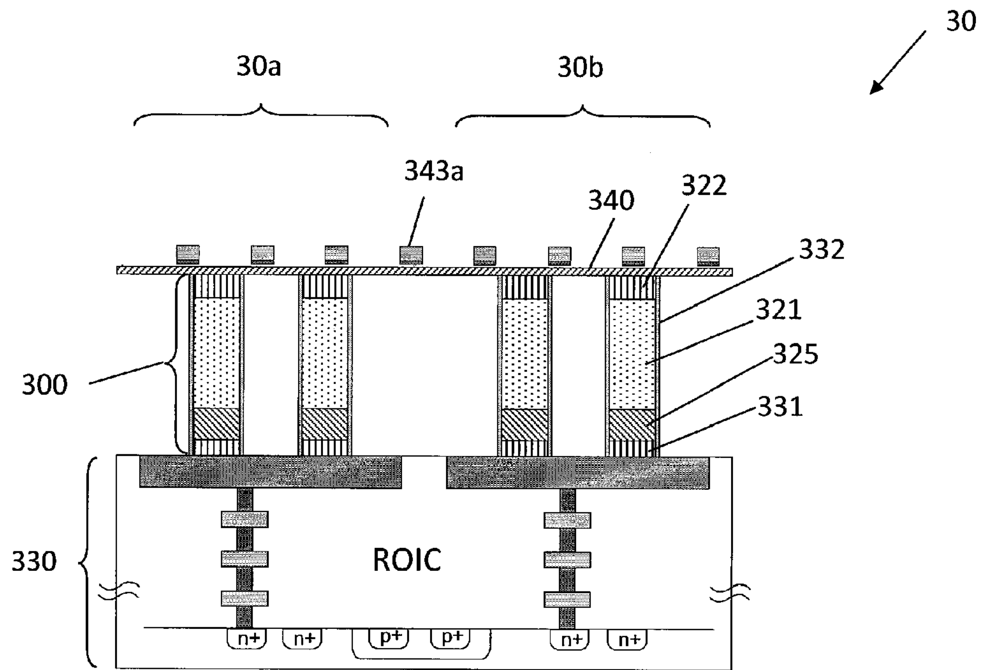
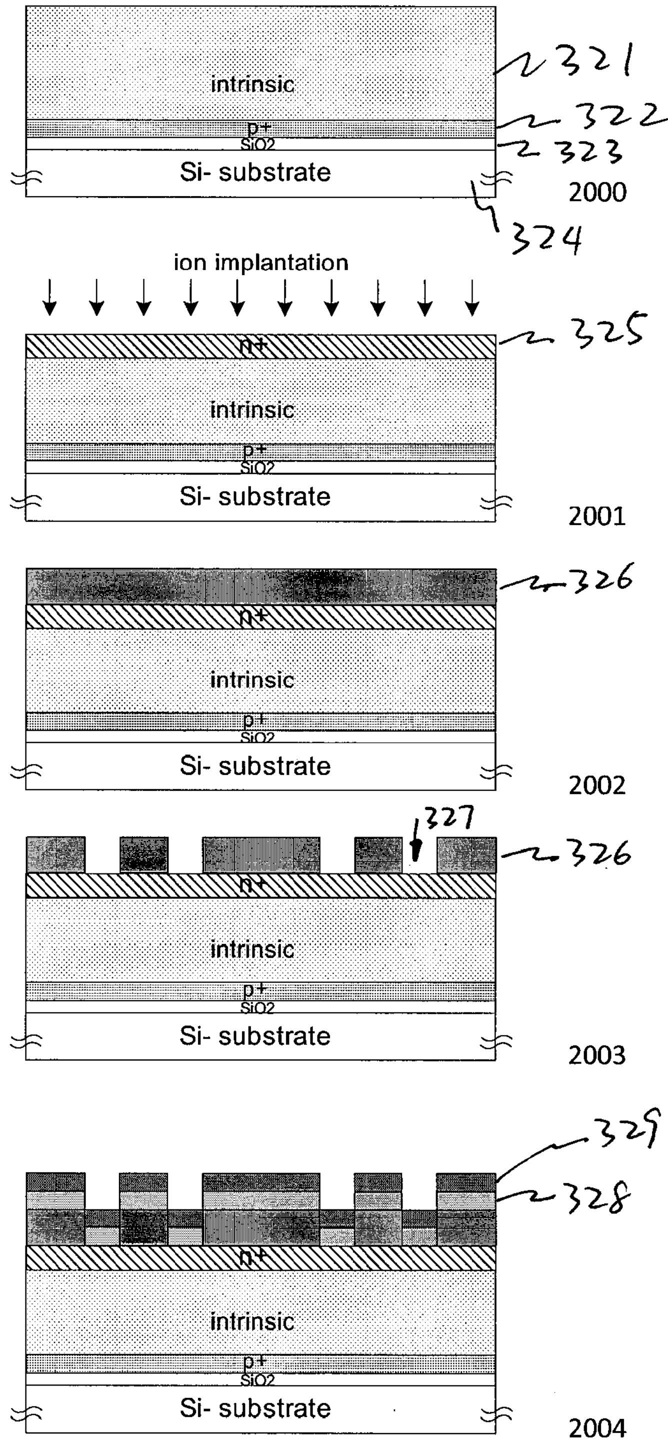


Fig. 5

Fig. 6



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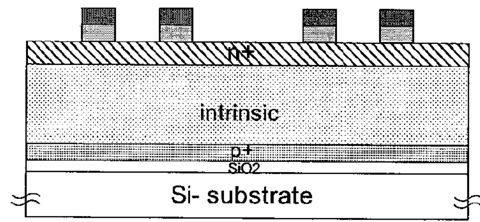

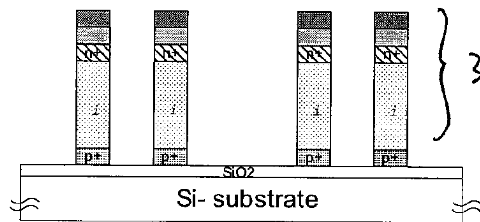

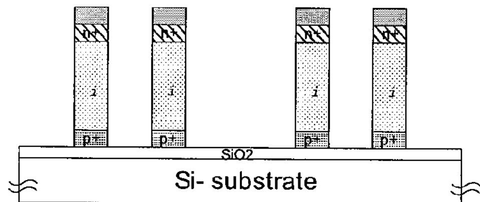

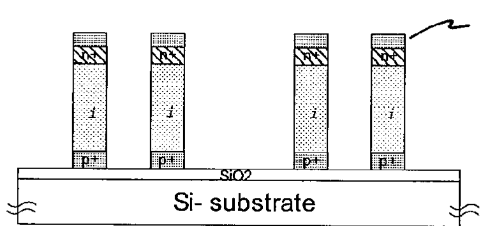

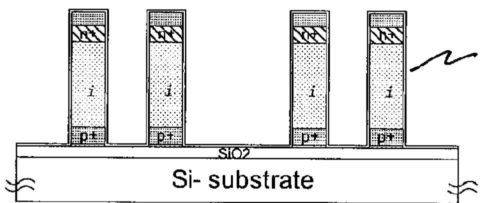

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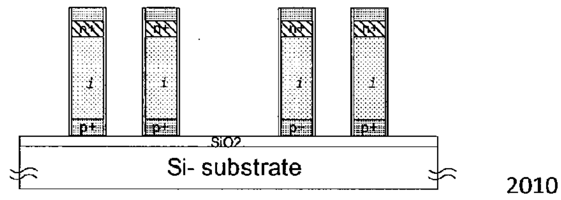

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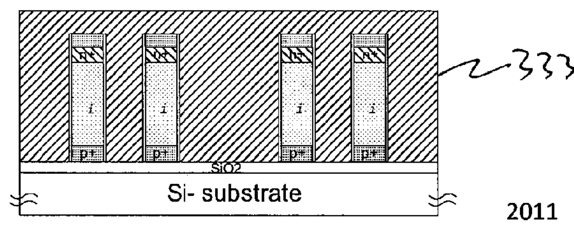
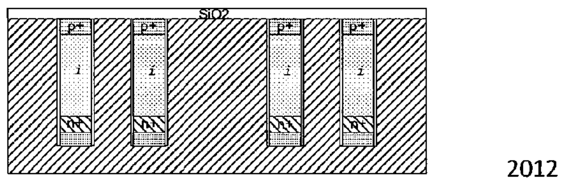


2011



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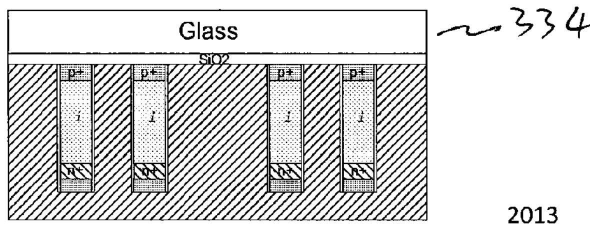

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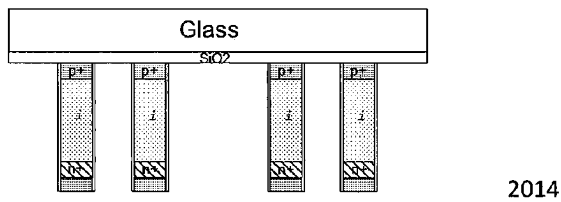

2014

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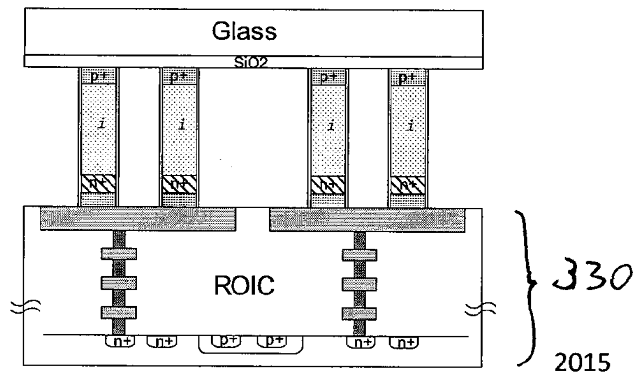

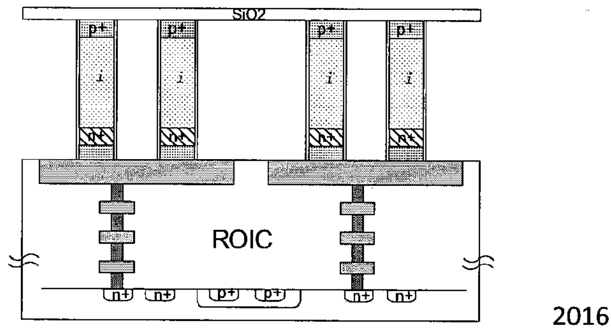

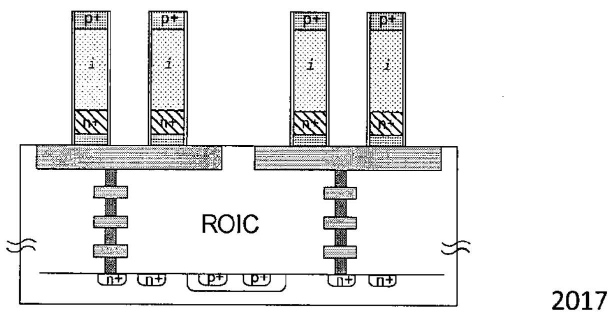

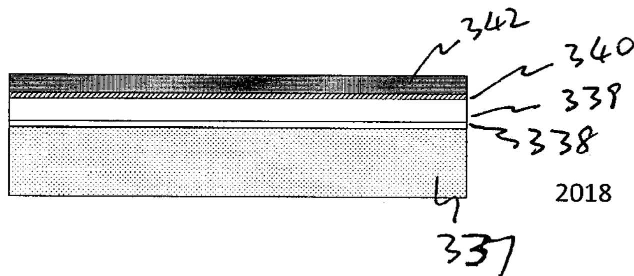

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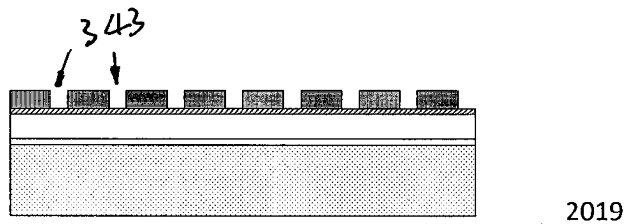

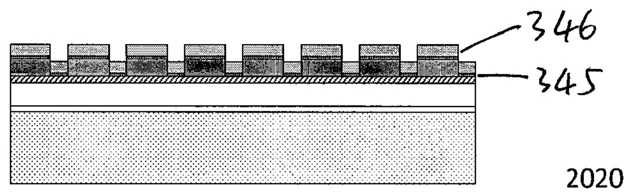

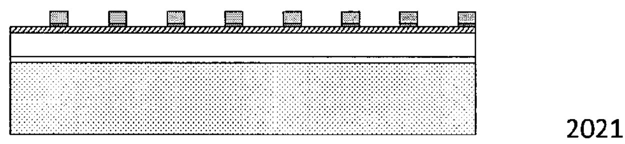

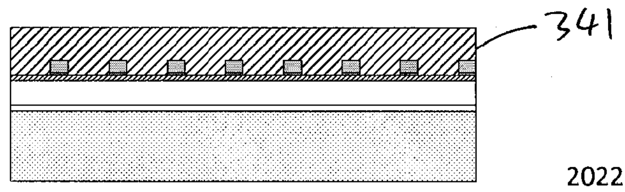

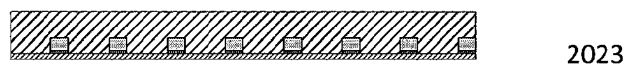

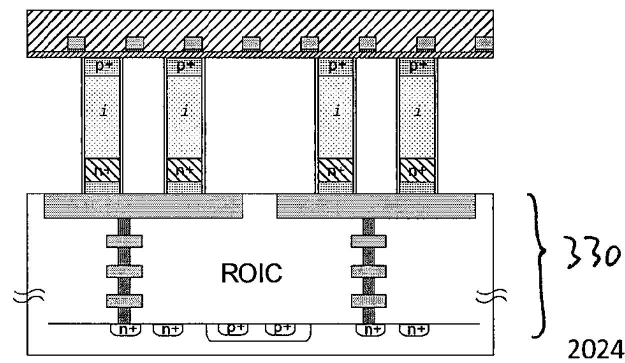

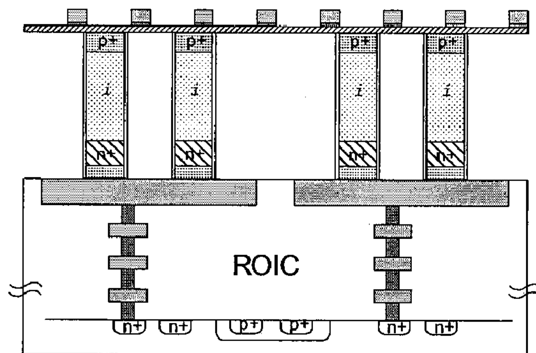

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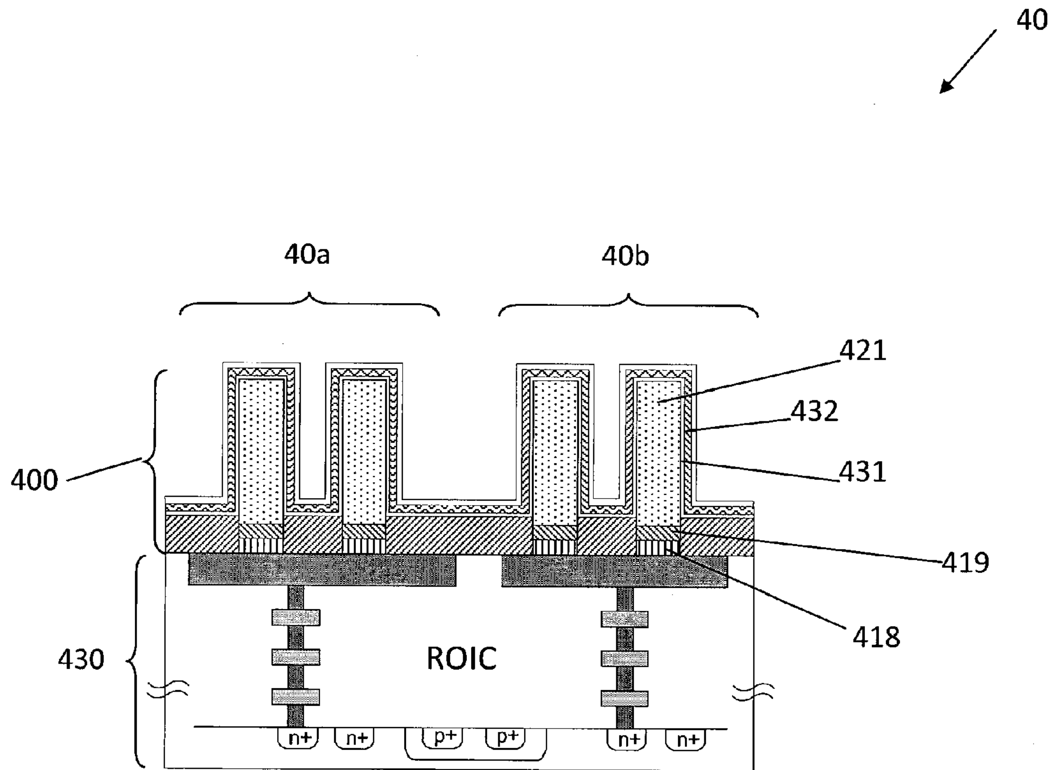
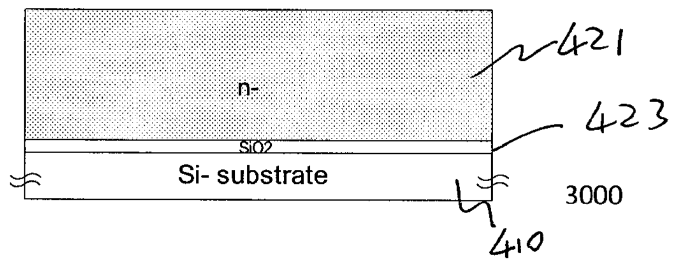
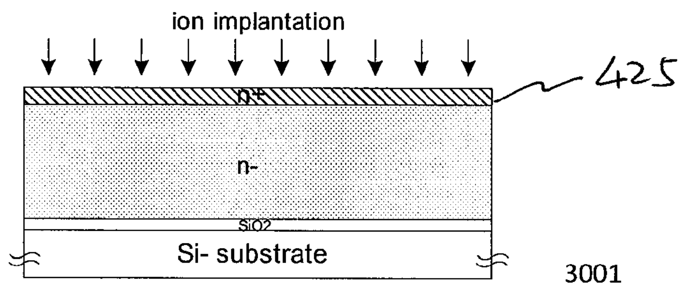
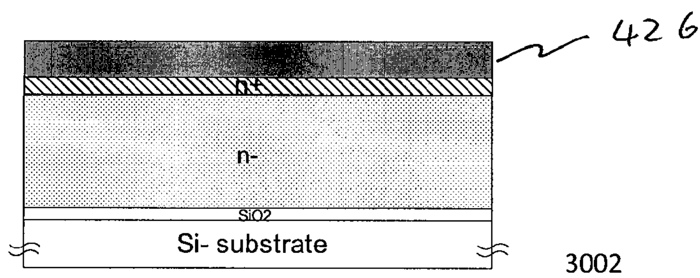


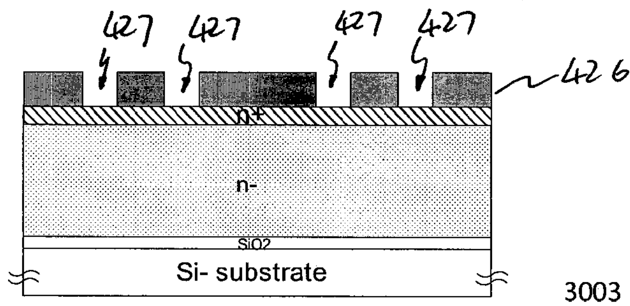
Fig. 7

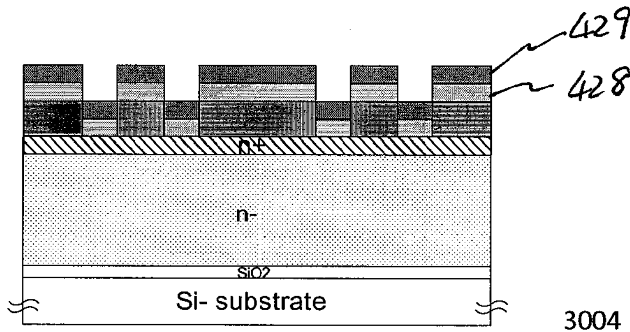
Fig. 8











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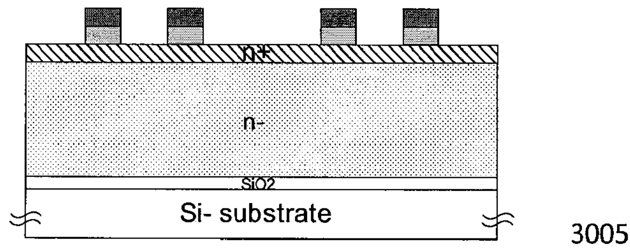

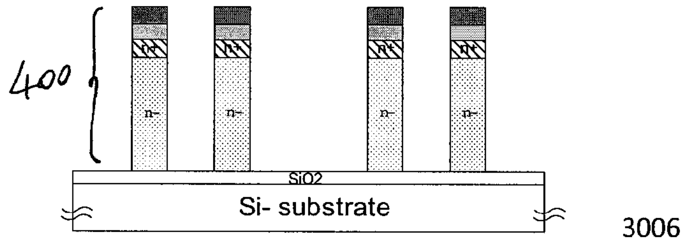

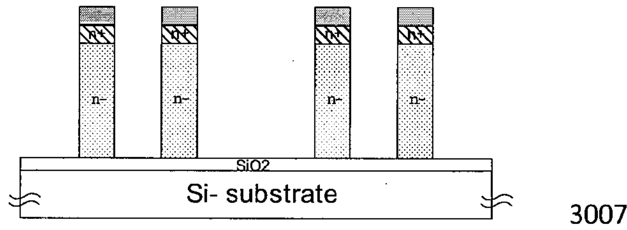

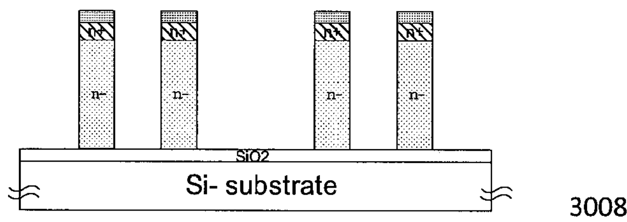

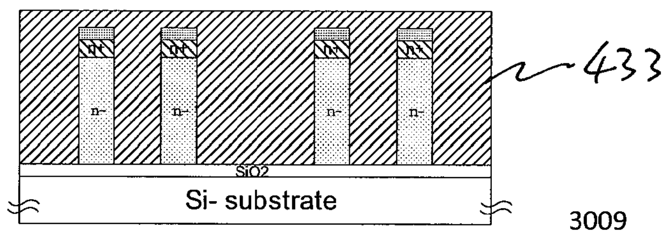

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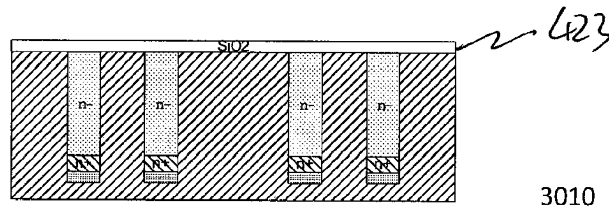

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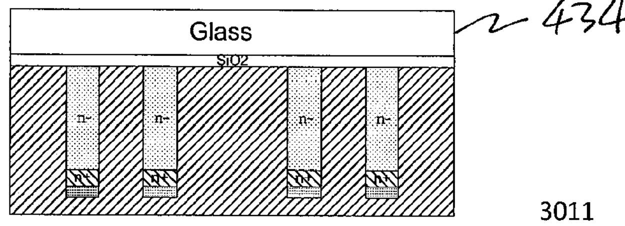

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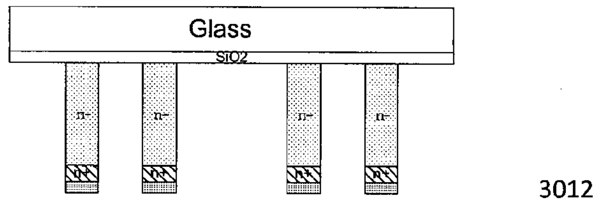

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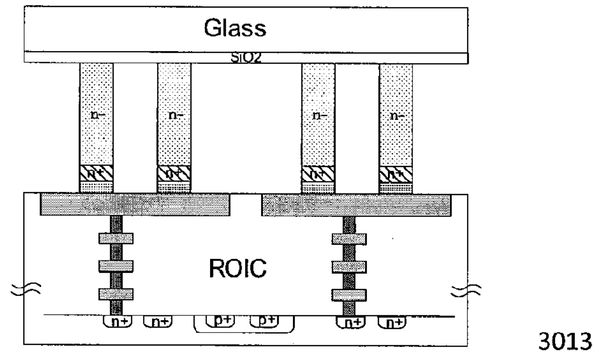

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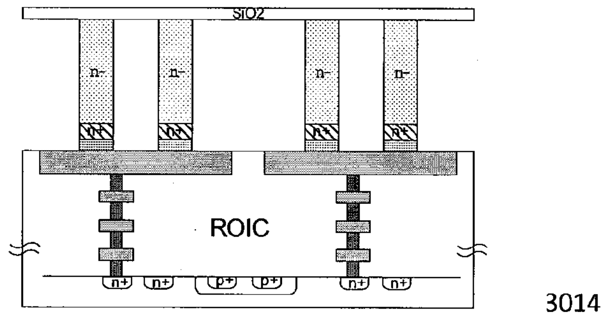

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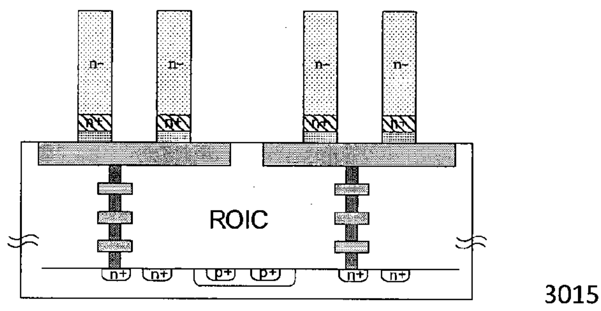

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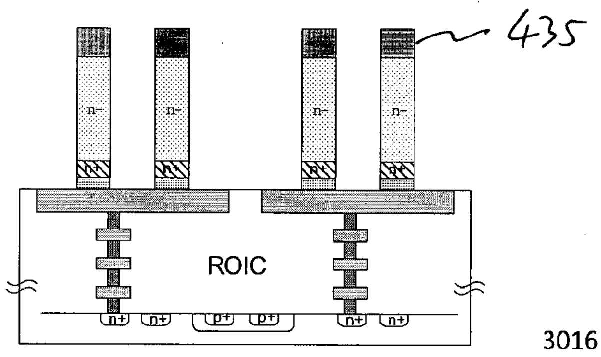

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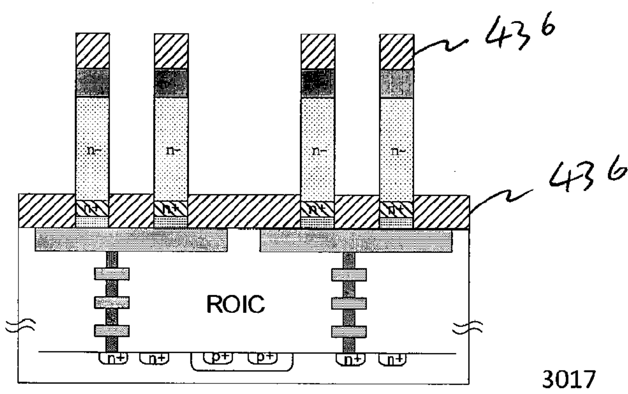

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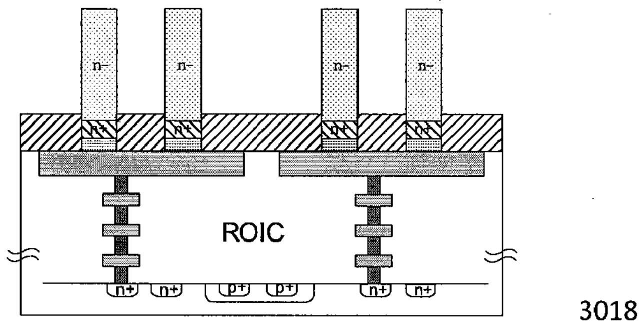

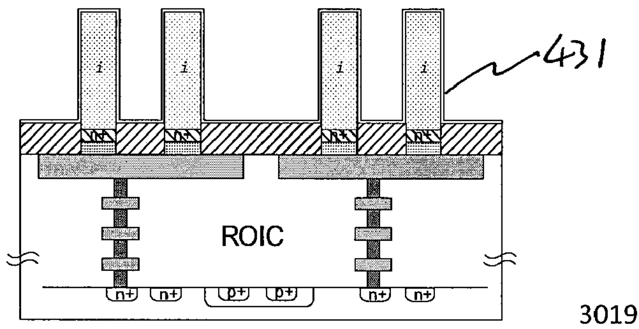

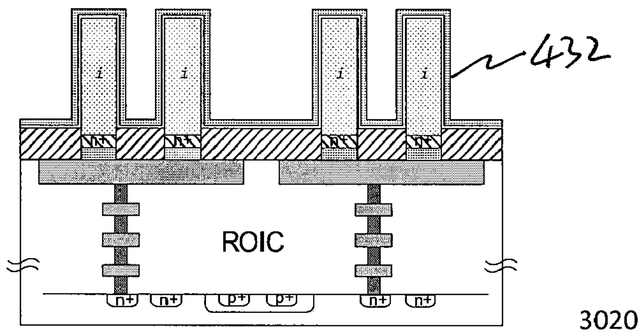

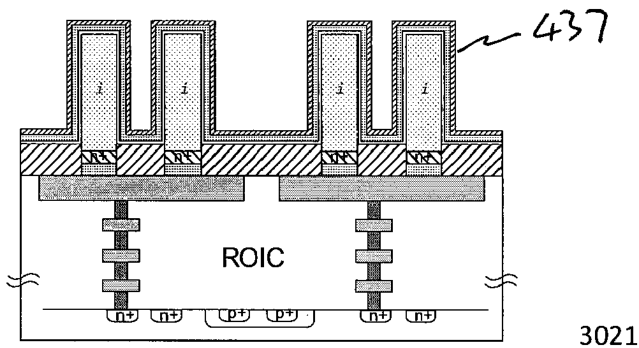

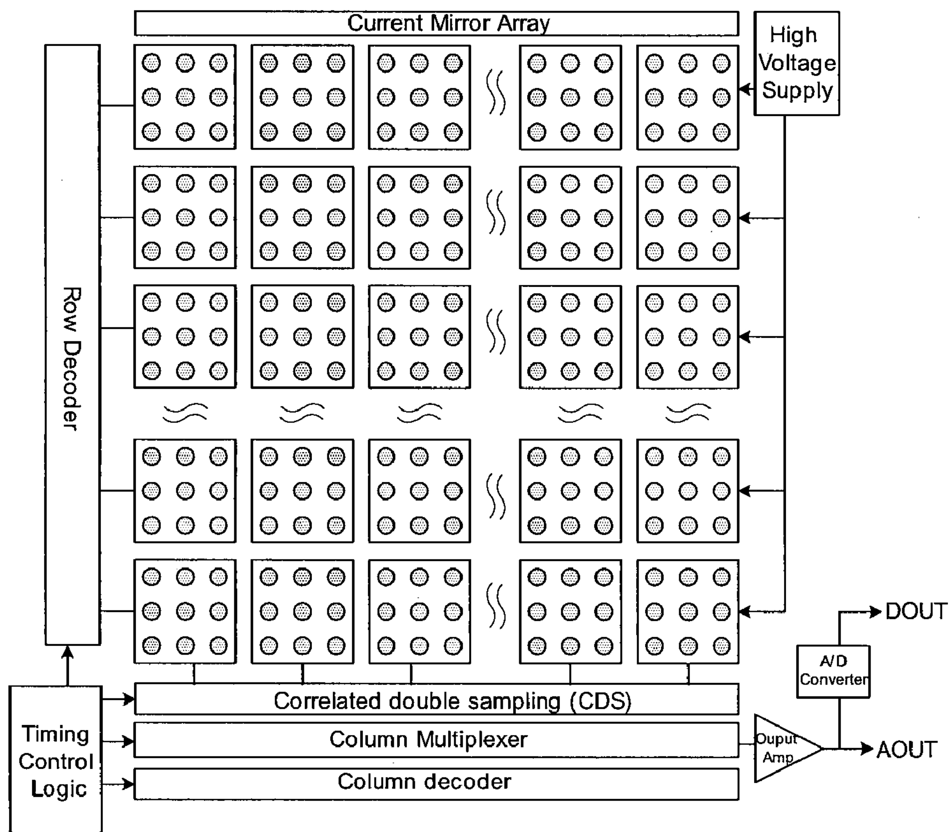

Fig. 9

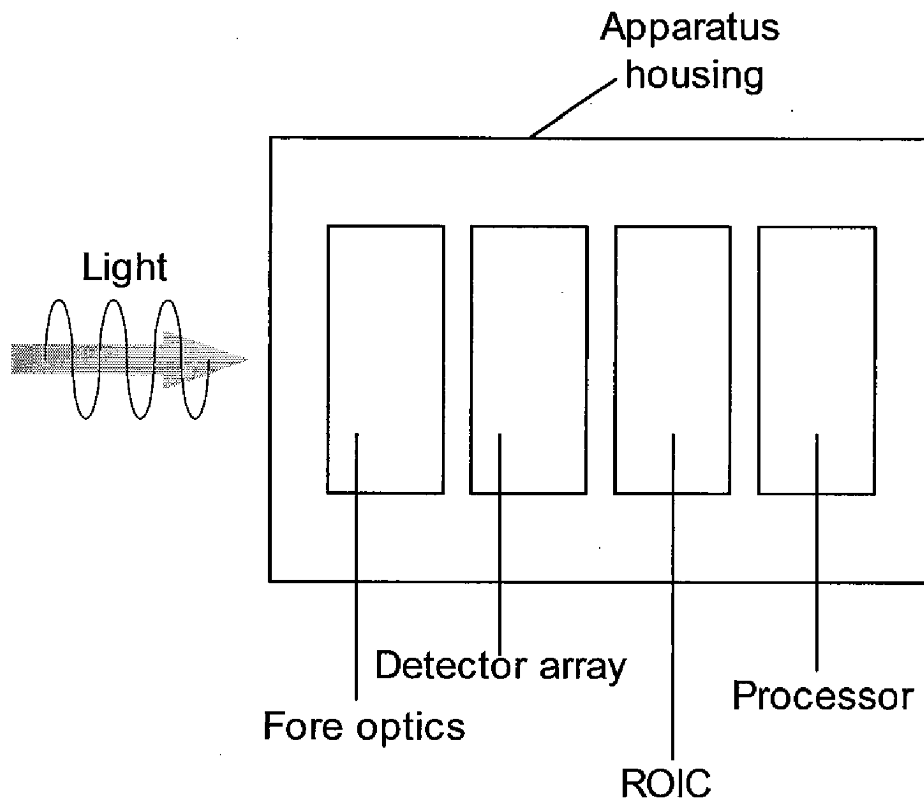

Fig. 10

SOLAR BLIND ULTRA VIOLET (UV) DETECTOR AND FABRICATION METHODS OF THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to U.S. patent application Ser. Nos. 61/266,064, 61/357,429, 61/360,421, 12/204,686 (granted as U.S. Pat. No. 7,646,943), 12/270,233, 12/472,264, 12/472,271, 12/478,598, 12/573,582, 12/575,221, 12/633,297, 12/633,305, 12/633,313, 12/633,318, 12/633,323, 12/621,497, 12/648,942, 12/910,664, 12/945,492, 12/966,514, 12/966,535, 12/966,573, 12/967,880, 12/974,499, 12/982,269 and 13/047,392, the disclosures of which are hereby incorporated by reference in their entirety.

BACKGROUND

[0002] The ozone layer of the Earth atmosphere strongly absorbs ultra violet (UV) radiations in the 300 nm to 200 nm wavelength region. Therefore, below the ozone layer, which is mainly located in the lower portion of the stratosphere from approximately 13 to 40 kilometres above Earth surface, UV radiations from the sun in the 300 nm to 200 nm wavelength region are essentially absent.

[0003] To be able to reject the visible wavelengths and to detect the solar blind UV (SBUV) light, wide band-gap materials such as AlGaN, SiC, ZnO have often been used in SBUV detectors. All of these materials are difficult to grow, not compatible with conventional semiconductor processing, and are difficult for integrate with silicon-based readout electronics.

[0004] On the other hand, to increase sensitivity of an SBUV detector, an avalanche multiplication is often implemented by using the avalanche photodiode (APD) structure. For most of direct band-gap compound materials, however, multiplication noise also increases at the same rate as the avalanche gain due to the almost unity ratio of the hole to electron impact ionization coefficients.

[0005] An APD is a highly sensitive semiconductor electronic device that exploits the photoelectric effect to convert light to electricity. APDs can be thought of as photodetectors that provide a built-in first stage of gain through avalanche breakdown. By applying a high reverse bias voltage (typically 100-200 V in silicon), APDs show an internal current gain (around 100). Avalanche breakdown is a phenomenon that can occur in both insulating and semiconducting materials. It is a form of electric current multiplication that can allow very large currents to flow within materials which are otherwise good insulators. It is a type of electron avalanche. The avalanche process occurs when the carriers in the transition region are accelerated by the electric field to energies sufficient to free electron-hole pairs via collisions with bond electrons.

SUMMARY

[0006] According to an embodiment, a device comprises a substrate; a plurality of pixels; a plurality of nanowires in each of the plurality of pixel, wherein the plurality of nanowires extend essentially perpendicularly from the substrate, wherein the plurality of nanowires extend essentially perpendicularly from the substrate, and the device is configured to be a solar-blind UV detector to detect UV radiation in the solar-blind UV region.

[0007] According to an embodiment, the plurality of nanowires are configured to react only to radiations in the solar-blind UV region.

[0008] According to an embodiment, each of the plurality of nanowires comprises a core and a cladding surrounding the core, wherein the core has a higher refractive index than the cladding.

[0009] According to an embodiment, each of the plurality of the nanowires comprises a coupler disposed on an end of each of the nanowire away from the substrate, the coupler being functional to guide radiation into the nanowires.

[0010] According to an embodiment, the nanowires have a diameter from about 5 nm to about 30 nm, a height from about 0.1 μm to about 5 μm; the cladding has a thickness of about 10 nm to about 200 nm. According to an embodiment, the nanowires have a diameter from about 5 nm to about 150 nm.

[0011] According to an embodiment, the nanowires have a pitch from about 0.2 μm to about 2 μm.

[0012] According to an embodiment, the nanowires detect UV radiation in the solar-blind UV region by converting UV radiation in the solar-blind UV region to an electrical signal.

[0013] According to an embodiment, the solar-blind UV detector further comprises electrical components configured to detect the electrical signal.

[0014] According to an embodiment, the solar-blind UV detector is functional to detect the electrical signal from the nanowires in different pixels separately.

[0015] According to an embodiment, each of the nanowires comprises a photodiode or forms a photodiode with the substrate, wherein the avalanche photodiode is functional to convert at least a portion of UV radiation in the solar-blind UV region impinged on the nanowires. According to an embodiment, the photodiode can be an avalanche photodiode.

[0016] According to an embodiment, each of the nanowires comprises a first heavily doped semiconductor layer, a lightly doped semiconductor layer or an intrinsic semiconductor layer, a second heavily doped semiconductor layer, and a metal silicide layer; wherein the first heavily doped semiconductor layer is disposed on the lightly doped semiconductor layer or the intrinsic semiconductor layer; the lightly doped semiconductor layer or the intrinsic semiconductor layer is disposed on the second heavily doped semiconductor layer; the second heavily doped semiconductor layer is disposed on the metal silicide layer; the metal silicide layer is disposed on the substrate; the first heavily doped semiconductor layer is of an opposite type from the second heavily doped semiconductor layer; and wherein the first heavily doped semiconductor layer, the lightly doped semiconductor layer or the intrinsic semiconductor layer, and the second heavily doped semiconductor layer form the photodiode. An intrinsic semiconductor, also called an undoped semiconductor or i-type semiconductor, is a substantially pure semiconductor without any significant dopant species present. A heavily doped semiconductor is a semiconductor with such a high doping level that the semiconductor starts to behave electrically more like a metal than as a semiconductor. A lightly doped semiconductor is a doped semiconductor but not have a doping level as high as a heavily doped semiconductor. In a lightly doped semiconductor, dopant atoms create individual doping levels that can often be considered as localized states that can donate electrons or holes by thermal promotion (or an optical transition) to the conduction or valence bands respectively. At high enough impurity concentrations (i.e. heavily doped) the individual impurity atoms may become close enough neighbors that their doping levels merge into an impurity band and the behavior of such a system ceases to show the typical traits of a semiconductor, e.g. its increase in conductivity with temperature.

[0017] According to an embodiment, the solar-blind UV detector further comprises a common electrode disposed on and electrically connected to ends of all the nanowires, wherein the common electrode is substantially transparent to UV radiation in the solar-blind UV region.

[0018] According to an embodiment, the common electrode is made of graphene.

[0019] According to an embodiment, space between the nanowires is filled with an oxide layer.

[0020] According to an embodiment, the solar-blind UV detector further comprises a metal grid on the common electrode, the metal grid configured to provide mechanical support for the common electrode.

[0021] According to an embodiment, each of the nanowires comprises a core of lightly doped semiconductor, an intermediate shell of intrinsic semiconductor and an outer shell of doped semiconductor; wherein the intermediate shell is conformally disposed over the core; the outer shell is conformally disposed over the intermediate shell; the outer shell is of an opposite type from the core; and the outer shell, the intermediate shell and the core form the photodiode.

[0022] According to an embodiment, each nanowire further comprises a heavily doped semiconductor layer of the same type as the core, and a metal silicide layer; wherein the heavily doped semiconductor layer and a metal silicide layer are sandwiched between the core and the substrate; the intermediate shell and the outer shell do not contact the heavily doped semiconductor layer and the metal silicide layer; and the metal silicide layer is in contact with the substrate and forms electrical contact to the substrate.

[0023] According to an embodiment, a solar-blind image sensor comprises the solar-blind UV detector above and electronic circuitry functional to detect electrical signals generated by the nanowires of the solar-blind UV detector.

[0024] According to an embodiment, the electronic circuitry comprises a high voltage supply.

[0025] According to an embodiment, a method of fabricating an image sensor comprising a substrate, a plurality of pixels, a plurality of nanowires in each of the plurality of pixel, wherein the plurality of nanowires extend essentially perpendicularly from the substrate; the method comprises bonding the plurality of nanowires onto the substrate. The term "image sensor" as used herein means a device that converts an optical image to an electric signal. An image sensor can be used in digital cameras and other imaging devices. Examples of image sensors include a charge-coupled device (CCD) or a complementary metal-oxide-semiconductor (CMOS) active pixel sensor.

[0026] According to an embodiment, the method further comprises conducting lithography, ion implantation, annealing, evaporation, atomic layer deposition, chemical vapor deposition, dry etch or a combination thereof.

[0027] According to an embodiment, the image sensor is a solar-blind UV detector or a color image sensor. The term "color image sensor" as used herein means an image sensor capable of converting an optical image in the visible spectrum (i.e. a color image) to an electric signal.

BRIEF DESCRIPTION OF FIGURES

[0028] FIG. **1**A shows one of the plurality of nanowires on a substrate.

[0029] FIG. **1**B shows simulated absorptance of the nanowire of FIG. **1**A.

[0030] FIG. **1**C shows optional couplers on the nanowires.

[0031] FIG. **2**A and **2**B show a perspective view and a top view of an image sensor according an embodiment.

[0032] FIG. **3** shows an SBUV detector according to one embodiment.

[0033] FIG. **4** shows an exemplary fabrication process of an image sensor such as the SBUV detector in FIG. **3**.

[0034] FIG. **5** shows an SBUV detector according to one embodiment.

[0035] FIG. **6** shows an exemplary fabrication process of an image sensor such as the SBUV detector in FIG. **5**.

[0036] FIG. **7** shows an SBUV detector according to one embodiment.

[0037] FIG. **8** shows an exemplary fabrication process of an image sensor such as the SBUV detector in FIG. **7**.

[0038] FIG. **9** shows a block diagram of a solar-blind image sensor.

[0039] FIG. **10** shows a schematic of the SBUV detector being used as fore optics.

DETAILED DESCRIPTION

[0040] In the following detailed description, reference is made to the accompanying drawings, which form a part thereof. In drawings, similar symbols typically identify similar components, unless the context dictates otherwise. The illustrate embodiments described in the detailed description, drawings, and claims are not meant to be limiting. Other embodiments may be utilized, and other changes may be made, without departing from the spirit or scope of the subject matter presented here.

[0041] This disclosure is drawn to, among other things, methods of use, methods of fabrication, apparatuses, systems, and devices related to an SBUV detector for detecting UV radiation in the solar-blind UV region. The SBUV region is the range of wavelengths in which the earth atmosphere absorbs essentially all UV radiation from the sun to the earth. For example, the wavelength region of 300 nm to 200 nm is within the SBUV region. A device that detects radiation only in the SBUV region and rejects visible and infrared radiation is called an SBUV detector or an SBUV sensor.

[0042] Sunlight does not interfere or blind a SBUV detector of the embodiments herein. Therefore, the SBUV detector of the embodiments herein is particularly useful for detecting manmade radiation sources that emit in the SBUV region and enjoys a very low false alarm rate. Such manmade radiation sources can include exhaust plumes of shoulder launched surface to air missiles (SLSAM), fire and flame, or any other UV emitting source including hydrogen flames. An SBUV detector of the embodiments herein can function at all lightning conditions including full daylight, without interference from the solar radiation and with very high signal to background ratio.

[0043] According to an embodiment, the SBUV detector comprises a substrate having a plurality of regions defined thereon (hereafter referred to as "pixels"). In each pixel, the SBUV detector comprises a plurality of nanowires extending essentially perpendicularly from the substrate. The term "nanowire" used herein means a structure whose dimension in a direction perpendicular to the substrate (hereafter referred to as the "normal direction") is substantially greater than dimensions of the structure in any direction perpendicular to the normal direction (hereafter referred to as a "transverse direction") and the dimensions in the transverse directions are less than 1000 nm. The plurality of nanowires can be equally or unequally spaced from each other, arranged in a

regular array or in random. The plurality of nanowires are configured to react only to radiations in the SBUV region and not to react to radiations outside the SBUV region. Here, the term "react" is meant to broadly encompass absorbing, reflecting, coupling to, detecting, interacting with, converting to electrical signals, etc.

[0044] FIG. **1**A shows one of the plurality of nanowires **100** on an SBUV **10**. For brevity, only one nanowires is shown but the SBUV **10** can comprise a plurality of nanowires **100**, such as more than 1000, or more than 1000000. The nanowires **100** extend essentially perpendicularly from a substrate **130**. Each of the nanowires **100** preferably comprises a core **110**, preferably made of silicon, and a cladding **120** surrounding the core **110**. The substrate **130** is preferably a metal. The core **110** preferably has high refractive index than the cladding **120**. The term "cladding" as used herein means a layer of substance surrounding the core **110**.

[0045] FIG. **1**B shows simulated absorptance of the SBUV detector **10** of UV light with wavelengths between **100** and **400** nm, incident in the normal direction. FIG. **1**B clearly shows that absorptance of the SBUV detector **10** of UV light with wavelengths between 140 and 290 nm is greater than 50% and absorptance of UV light drops quickly to almost zero outside wavelength region of 140-290 nm. FIG. **1**B indicate that the SBUV detector **10** indeed only reacts to radiations in the SBUV region. As shown in FIG. **1**C, each of the nanowires **100** can further comprise a coupler **140** disposed on an end of the nanowire **100** away from the substrate **130** (hereafter referred to as the "receiving end"). The term "coupler" as used herein means a layer effective to guide light into the nanowires.

[0046] According to an embodiment, the nanowires **100** have a diameter of from about 5 nm to about 30 nm, preferably about 20 nm. According to an embodiment, the nanowires **100** have a diameter of from about 5 nm to about 150 nm. The cladding **130** has a thickness of about 10 nm to about 200 nm, preferably about 30 nm. Pitch of the nanowires **100** (i.e. center-to-center distance of one of the plurality of nanowires to a nearest neighbor thereof) is from about 0.2 μm to about 2 μm. Height (i.e. dimension in the normal direction) of the nanowires **100** is from about 0.1 μm to about 5 μm. Each pixel can have one or more nanowires **100**.

[0047] FIG. **2**A and FIG. **2**B shows a perspective view and a top view, respectively, of the SBUV detector **10**. For brevity, only four pixels (regions enclosed by dotted rectangles) are shown. The nanowires **100** preferably detect UV radiation in the SBUV region by converting it to an electrical signal. For example, each nanowire **100** can comprise a photodiode (such as an avalanche photodiode) or form a photodiode (such as an avalanche photodiode) with the substrate **130**. The SBUV detector **10** can further comprise electrical components configured to detect the electrical signal from the nanowires **100**, for example, Readout Integrated Circuits (ROIC) in the substrate **130**, an electrode **150** disposed between and electrically connected to all the nanowires **110** on each pixel, a common electrode **160** disposed on and electrically connected to the receiving ends of all the nanowires **110** in the entire SBUV detector **10**. Preferably, the SBUV detector **10** can detect electrical signals from the nanowires **100** in different pixels separately.

[0048] FIG. **3** shows an SBUV detector **20** according to one embodiment. For brevity, two pixels **20**a and **20**b of a substrate **230** are illustrated. The SBUV detector **20**, however, can comprise a plurality of pixels such as more than 100, more than 1000, more than 1000000. The pixels preferably have a pitch of about 0.5 μm micron to 100 μm (more preferably 2 μm). In each of the pixels **20**a and **20**b, the SBUV detector **20** comprises a plurality of nanowires **200**, respectively. Each of the nanowires **200** comprises an APD, the APD being functional to convert at least a portion of UV radiation in the SBUV region impinged the nanowires **200** to an electrical signal. The nanowires **200** do not generate any electrical signal from any radiation outside the SBUV region. Each nanowire **200** comprises a first heavily doped semiconductor layer **222**, a lightly doped semiconductor layer or an intrinsic semiconductor layer **221**, a second heavily doped semiconductor layer **225**, and a metal silicide layer **231**. The first heavily doped semiconductor layer **222** is disposed on the lightly doped semiconductor layer or the intrinsic semiconductor layer **221**. The lightly doped semiconductor layer or the intrinsic semiconductor layer **221** is disposed on the second heavily doped semiconductor layer **225**. The second heavily doped semiconductor layer **225** is disposed on the metal silicide layer **231**. The metal silicide layer **231** is disposed on the substrate **230**. The first heavily doped semiconductor layer **222** is of an opposite type from the second heavily doped semiconductor layer **225**. As used herein, one semiconductor having an opposite type from another semiconductor means the former is n type if the latter is p type or, the former is p type if the latter is n type. The first heavily doped semiconductor layer **222**, the lightly doped semiconductor layer or the intrinsic semiconductor layer **221**, and the second heavily doped semiconductor layer **225** form an APD. The metal silicide layer **231** forms electrical contact to any electrical components of the substrate **230**. A common electrode **240** is disposed on the receiving ends of and electrically connected to all the nanowires **200**. The common electrode **240** is substantially transparent to UV radiation in the SBUV region. For example, the common electrode **240** can be made of graphene. Space between the nanowires **200** is preferably filled with an oxide layer **236**. The term "transparent" as used herein means a transmittance of at least 70%.

[0049] FIG. **4** shows an exemplary method of fabrication of the SBUV detector **10**.

[0050] In step **1000**, a silicon substrate **224** is provided, wherein the silicon substrate **224** comprises an silicon oxide layer **223** thereon and the first heavily doped semiconductor layer **222** (e.g. heavily doped p type silicon) on the silicon oxide layer **223**. A substrate of semiconductor material other than silicon (e.g. III-V or II-VI group compound semiconductor) can also be used.

[0051] In step **1001**, the second heavily doped semiconductor layer **225** (e.g. heavily doped n type silicon) is fabricated on the layer **221** by a method such as ion implantation and subsequent annealing. An exemplary n type dopant suitable for use in the ion implantation is phosphorous, arsenic, antimony, or a combination thereof.

[0052] In step **1002**, a resist layer **226** (e.g. a photoresist or an e-beam resist) is deposited on the second heavily doped semiconductor layer **225**, by a suitable method such as spin coating.

[0053] In step **1003**, a pattern is formed in the resist layer **226** using a lithography technique (e.g. photolithrograph or e-beam lithography) by removing portions **227** of the resist layer **226**. The second heavily doped semiconductor layer **225** is exposed under the removed portions **227**. The pattern corresponds to shapes and positions of the nanowires **200**.

[0054] In step **1004**, two metal layers **228** and **229** are deposited on the resist layer **226** and the exposed portions of the second heavily doped semiconductor layer **225**, using a suitable technique such as thermal evaporation, e-beam evaporation, and sputtering. Exemplary metal suitable for use in the metal layers **228** and **229** are aluminum, gold, chromium, silver, copper, titanium, nickel or a combination thereof.

[0055] In step **1005**, remainder of the resist layer **226** and portions of the metal layers **228** and **229** thereon are lift-off by a suitable technique such as plasma ashing and dissolution in a suitable solvent.

[0056] In step **1006**, the nanowires **200** are formed by etching into the layers **225**, **221** and **222**, the using a suitable technique, such as dry etching with remainder of the metal layer **229** as etch mask, until portions of the silicon oxide layer **223** not directly below the remainder of the metal layer **229** are exposed. The nanowires **200** now comprise remainder of the layers **225**, **221** and **222**.

[0057] In step **1007**, remainder of the metal layer **229** is removed by a suitable method such as etching with a suitable metal etchant. The metal layer **228** remains.

[0058] In step **1008**, a silicide layer **231** is formed from the second heavily doped semiconductor layer **225** and the metal layer **228** thereon by annealing (e.g. at about 850° C. for about 30 minutes). Any remainder of the metal layer **228** is removed by a suitable technique such as etching with a suitable metal etchant.

[0059] In step **1009**, an oxide layer **232** (e.g. HfO_2, SiO_2, Al_2O_3) is deposited isotropically over the nanowires **200** and the exposed portions of the silicon oxide layer **223**, using suitable technique such as atomic layer deposition (ALD) and chemical vapor deposition (CVD). The oxide layer **232** is functional to passivate surfaces of nanowires **200**. For example, the oxide layer **232** has a thickness of about 30 nm. The terms "passivation" and "passivate" as used herein means a process of eliminating dangling bonds (i.e., unsatisfied valence on immobilized atoms).

[0060] In step **1010**, portions of the oxide layer **232** above the silicide layer **231** and the exposed portions of the silicon oxide layer **223** are removed by a suitable technique such as anisotropic dry etch. Now the silicide layer **231** is exposed.

[0061] In step **1011**, a sacrificial layer **233** is deposited by pouring , spin coating or evaporation to fill space between the nanowires **200**. The sacrificial layer **233** can be a suitable material such as polydimethylsiloxane, polyimide or oxide.

[0062] In step **1012**, the substrate **224** is removed using a suitable technique such as etching with potassium hydroxide, until the silicon oxide layer **233** is exposed.

[0063] In step **1013**, a glass substrate **234** is bonded to the exposed silicon oxide layer **233**, using a suitable technique such as using a UV removable glue. The glass substrate **234** can provide mechanical support.

[0064] In step **1014**, the sacrificial layer **233** is removed by a suitable method such as wet etching. For example, polyimide can be removed by a suitable photoresist developer.

[0065] In step **1015**, the nanowires **200** are bonded to ROIC in the substrate **230** using a tin-silver alloy layer between the substrate **230** and the silicide layer **231** and annealing at about 220° C.

[0066] In step **1016**, the glass substrate **234** is released from the silicon oxide layer **233** by illumination with UV light.

[0067] In step **1017**, the silicon oxide layer **233** is removed by a suitable method such as etching with HF followed by rinsing.

[0068] In step **1018**, the oxide layer **236** is deposited by spin coating, evaporation or CVD to fill space between the nanowires **200**. The insulating material **236** preferably is transparent to UV radiation in the SBUV region. The insulating material **236** can be any suitable material such as silicon oxide, aluminum oxide, and grapheme oxide.

[0069] In step **1019**, the oxide layer **236** is planarized using a suitable technique such as chemical mechanical polishing (CMP) until the first heavily doped semiconductor **222** of the nanowires **200** is exposed.

[0070] In step **1020**, an oxide layer **238** and a metal layer **239** are sequentially deposited on a sacrificial silicon substrate **237** using a suitable method such as thermal evaporation, e-beam evaporation, and sputtering. The metal layer **239** can be of any suitable material, such as nickel and iron.

[0071] In step **1021**, a transparent conductive oxide (TCO) layer **240** is deposited on the metal layer **239** by a suitable method such as CVD using C_2H_4 or C_2H_2 gas. The TCO layer **240** can be any suitable material such as graphene. The TCO layer **240** is substantially transparent to UV radiation in the SBUV region.

[0072] In step **1022**, a plastic layer **241** is deposited on the TCO layer **240** by a suitable method such as spin coating. The plastic layer **241** can be any suitable material such as poly (methyl methacrylate) (PMMA).

[0073] In step **1023**, the sacrificial silicon substrate **237**, the oxide layer **238** and the metal layer **239** are removed by a suitable method such as wet etching with KOH, HF, metal etchant, respectively.

[0074] In step **1024**, the TCO layer **240** and the plastic layer **241** are transfer onto the receiving ends of the nanowires **200** under a wet condition, followed by annealing at about 220° C. for about 20 minutes to form electrical contact between the TCO layer **240** and the receiving ends of the nanowires **200**.

[0075] In step **1025**, the plastic layer **241** is removed by a suitable method such dry etch or wet etch.

[0076] In step **1026**, a resist layer **242** (e.g. a photoresist or an e-beam resist) is deposited on the TCO layer **240** (which functions as the common electrode **240**), by a suitable method such as spin coating. A pattern is formed in the resist layer **242** using a lithography technique (e.g. photolithrograph or e-beam lithography) by removing portions of the resist layer **425** above boundaries of pixels of the substrate **230**.

[0077] In step **1027**, a metal layer **243** is deposited, using a suitable method such as thermal evaporation, e-beam evaporation, and sputtering. Exemplary metal suitable for use in the metal layer **243** are aluminum, gold, chromium, silver, copper, titanium, nickel or a combination thereof.

[0078] In step **1028**, remainder of the resist layer **242** and portions of the metal layer **243** thereon are lift-off by a suitable technique such as plasma ashing and dissolution in a suitable solvent.

[0079] FIG. **5** shows an SBUV detector **30** according to one embodiment. For brevity, two pixels **30***a* and **30***b* of a substrate **330** are illustrated. The SBUV detector **30**, however, can comprise a plurality of pixels such as more than 100, more than 1000, more than 1000000. The pixels preferably have a pitch of about 0.5 μm micron to 100 μm (more preferably 2 μm). In each of the pixels **30***a* and **30***b*, the SBUV detector **30** comprises a plurality of nanowires **300**, respectively. Each of the nanowires **300** comprises an APD, the APD being func-

tional to convert at least a portion of UV radiation in the SBUV region impinged on the nanowires **300** to an electrical signal. The nanowires **300** do not generate any electrical signal from any radiation outside the SBUV region. Each nanowire **300** comprises a first heavily doped semiconductor layer **322**, a lightly doped semiconductor layer or an intrinsic semiconductor layer **321**, a second heavily doped semiconductor layer **325**, and a metal silicide layer **331**. The first heavily doped semiconductor layer **322** is disposed on the lightly doped semiconductor layer or the intrinsic semiconductor layer **321**. The lightly doped semiconductor layer or the intrinsic semiconductor layer **321** is disposed on the second heavily doped semiconductor layer **325**. The second heavily doped semiconductor layer **325** is disposed on the metal silicide layer **331**. The metal silicide layer **331** is disposed on the substrate **330**. The first heavily doped semiconductor layer **322** is of an opposite type from the second heavily doped semiconductor layer **325**. The first heavily doped semiconductor layer **322**, the lightly doped semiconductor layer or the intrinsic semiconductor layer **321**, and the second heavily doped semiconductor layer **325** form an APD. The metal silicide layer **331** forms electrical contact to any electrical components of the substrate **330**. A common electrode **340** is disposed on the receiving ends of and electrically connected to all the nanowires **300**. The common electrode **340** is substantially transparent to UV radiation in the SBUV region. For example, the common electrode **340** can be made of graphene. Space between the nanowires **300** is preferably not filled. A metal grid on the common electrode **340** can provide mechanical support for the common electrode.

[0080] FIG. **6** shows an exemplary method of fabrication of the SBUV detector **30**.

[0081] In step **2000**, a silicon substrate **324** is provided, wherein the silicon substrate **324** comprises an silicon oxide layer **323** thereon and the first heavily doped semiconductor layer **322** (e.g. heavily doped p type silicon) on the silicon oxide layer **323**. A substrate of semiconductor material other than silicon (e.g. III-V or II-VI group compound semiconductor) can also be used.

[0082] In step **2001**, the second heavily doped semiconductor layer **325** (e.g. heavily doped n type silicon) is fabricated on the layer **321** by a method such as ion implantation and subsequent annealing. An exemplary n type dopant suitable for use in the ion implantation is phosphorous, arsenic, antimony, or a combination thereof.

[0083] In step **2002**, a resist layer **326** (e.g. a photoresist or an e-beam resist) is deposited on the second heavily doped semiconductor layer **325**, by a suitable method such as spin coating.

[0084] In step **2003**, a pattern is formed in the resist layer **326** using a lithography technique (e.g. photolithrograph or e-beam lithography) by removing portions **327** of the resist layer **326**. The second heavily doped semiconductor layer **325** is exposed under the removed portions **327**. The pattern corresponds to shapes and positions of the nanowires **300**.

[0085] In step **2004**, two metal layers **328** and **329** are deposited on the resist layer **326** and the exposed portions of the second heavily doped semiconductor layer **325**, using a suitable technique such as thermal evaporation, e-beam evaporation, and sputtering. Exemplary metal suitable for use in the metal layers **328** and **329** are aluminum, gold, chromium, silver, copper, titanium, nickel or a combination thereof.

[0086] In step **2005**, remainder of the resist layer **326** and portions of the metal layers **328** and **329** thereon are lift-off by a suitable technique such as plasma ashing and dissolution in a suitable solvent.

[0087] In step **2006**, the nanowires **300** are formed by etching into the layers **325**, **321** and **322**, the using a suitable technique, such as dry etching with remainder of the metal layer **329** as etch mask, until portions of the silicon oxide layer **323** not directly below the remainder of the metal layer **329** are exposed. The nanowires **300** now comprise remainder of the layers **325**, **321** and **322**.

[0088] In step **2007**, remainder of the metal layer **329** is removed by a suitable method such as etching with a suitable metal etchant. The metal layer **328** remains.

[0089] In step **2008**, a silicide layer **331** is formed from the second heavily doped semiconductor layer **325** and the metal layer **328** thereon by annealing (e.g. at about 850° C. for about 30 minutes). Any remainder of the metal layer **328** is removed by a suitable technique such as etching with a suitable metal etchant.

[0090] In step **2009**, an oxide layer **332** (e.g. HfO_2, SiO_2, Al_2O_3) is deposited isotropically over the nanowires **300** and the exposed portions of the silicon oxide layer **323**, using suitable technique such as atomic layer deposition (ALD) and chemical vapor deposition (CVD). The oxide layer **332** is functional to passivate surfaces of nanowires **200**. For example, the oxide layer **332** has a thickness of about 30 nm.

[0091] In step **2010**, portions of the oxide layer **332** above the silicide layer **331** and the exposed portions of the silicon oxide layer **323** are removed by a suitable technique such as anisotropic dry etch. Now the silicide layer **331** is exposed.

[0092] In step **2011**, a sacrificial layer **333** is deposited by pouring , spin coating or evaporation to fill space between the nanowires **300**. The sacrificial layer **333** can be a suitable material such as polydimethylsiloxane, polyimide or oxide.

[0093] In step **2012**, the substrate is removed using a suitable technique such as etching with potassium hydroxide, until the silicon oxide layer **333** is exposed.

[0094] In step **2013**, a glass substrate **334** is bonded to the exposed silicon oxide layer **333**, using a suitable technique such as using a UV removable glue. The glass substrate **334** can provide mechanical support.

[0095] In step **2014**, the sacrificial layer **333** is removed by a suitable method such as wet etching. For example, polyimide can be removed by a suitable photoresist developer.

[0096] In step **2015**, the nanowires **300** are bonded to ROIC in the substrate **330** using a tin-silver alloy layer between the substrate **330** and the silicide layer **331** and annealing at about 220° C.

[0097] In step **2016**, the glass substrate **334** is released from the silicon oxide layer **333** by illumination with UV light.

[0098] In step **2017**, the silicon oxide layer **333** is removed by a suitable method such as etching with HF followed by rinsing.

[0099] In step **2018**, an oxide layer **338** and a metal layer **339** are sequentially deposited on a sacrificial silicon substrate **337** using a suitable method such as thermal evaporation, e-beam evaporation, and sputtering. The metal layer **339** can be of any suitable material, such as nickel and iron. The metal layer **339** preferably has a thickness at least **100** nm. A transparent conductive oxide (TCO) layer **340** (which functions as the common electrode **340**) is then deposited on the metal layer **339** by a suitable method such as CVD using C_2H_4 or C_2H_2 gas. The TCO layer **340** can be any suitable

material such as graphene. The TCO layer **340** is substantially transparent to UV radiation in the SBUV region. A resist layer **342** (e.g. a photoresist or an e-beam resist) is deposited on the TCO layer **340**, by a suitable method such as spin coating.

[0100] In step **2019**, a pattern is formed in the resist layer **342** using a lithography technique (e.g. photolithrograph or e-beam lithography) by removing portions **343** of the resist layer **342**. The TCO layer **340** is exposed under the removed portions **342**. The removed portions **343** preferable have a width about 30 nm. The pattern can be a grid pattern in which the removed portions **343** separate the resist layer **342** into discrete square regions, which preferably have a width of about 120 nm.

[0101] In step **2020**, two metal layers **345** and **346** are deposited on the resist layer **342** and the exposed portions of the TCO layer **340**, using a suitable technique such as thermal evaporation, e-beam evaporation, and sputtering. Exemplary metal suitable for use in the metal layers **345** and **346** are aluminum, gold, chromium, silver, copper, titanium, nickel or a combination thereof.

[0102] In step **2021**, remainder of the resist layer **342** and portions of the metal layers **345** and **346** thereon are lift-off by a suitable technique such as plasma ashing and dissolution in a suitable solvent.

[0103] In step **2022**, a plastic layer **341** is deposited on the TCO layer **340** by a suitable method such as spin coating. The plastic layer **341** can be any suitable material such as poly (methyl methacrylate) (PMMA) and polydimethylsiloxane.

[0104] In step **2023**, the sacrificial silicon substrate **337**, the oxide layer **338** and the metal layer **339** are removed by a suitable method such as wet etching with KOH, HF, metal etchant, respectively.

[0105] In step **2024**, the TCO layer **340**, and the metal layers **345** and **346** are transfer onto the receiving ends of the nanowires **300** under a wet condition, followed by annealing at about 220° C. for about 20 minutes to form electrical contact between the TCO layer **340** and the receiving ends of the nanowires **300**.

[0106] In step **2025**, the plastic layer **341** is removed by a suitable method such dry etch or wet etch.

[0107] FIG. **7** shows a device **40** according to one embodiment. For brevity, two pixels **40***a* and **40***b* of a substrate **430** are illustrated. The SBUV detector **40**, however, can comprise a plurality of pixels such as more than 100, more than 1000, more than 1000000. The pixels preferably have a pitch of about 0.5 μm micron to 100 μm (more preferably 2 μm). In each of the pixels **40***a* and **40***b*, the SBUV detector **40** comprises a plurality of nanowires **400**, respectively. Each of the nanowires **400** comprises an APD, the APD being functional to convert at least a portion of UV radiation in the SBUV region impinged on the nanowires **400** to an electrical signal. The nanowires **400** do not generate any electrical signal from any radiation outside the SBUV region. Each nanowire **400** comprises a core **421** of lightly doped semiconductor, an intermediate shell **431** of intrinsic semiconductor and an outer shell **432** of doped semiconductor. The intermediate shell **431** is conformally disposed over the core **421**. The outer shell **432** is conformally disposed over the intermediate shell **431**. The outer shell **432** is of an opposite type from the core **421**. The outer shell **432**, the intermediate shell **431** and the core **421** form the APD. Each nanowire **400** can further comprise a heavily doped semiconductor layer **419** of the same type as the core **421**, and a metal silicide layer **418** wherein the heavily doped semiconductor layer **419** and a metal silicide layer **418** are sandwiched between the core **421** and the substrate **430**. As used herein, one semiconductor having a same type as another semiconductor means the former is n type if the latter is n type or, the former is p type if the latter is p type. The intermediate shell **431** and the outer shell **432** do not contact the heavily doped semiconductor layer **419** and the metal silicide layer **418**. The metal silicide layer **418** is in contact with the substrate **430** and forms electrical contact to any electrical components of the substrate **430**.

[0108] FIG. **8** shows an exemplary method of fabrication of the SBUV detector **40**.

[0109] In step **3000**, a silicon substrate **410** is provided, wherein the silicon substrate **410** comprises a lightly doped semiconductor layer **421** (e.g. epitaxial n type silicon), and a silicon oxide layer **423** sandwiched between the silicon substrate **410** and the lightly doped semiconductor layer **421**. A substrate of semiconductor material other than silicon (e.g. III-V or II-VI group compound semiconductor) can also be used.

[0110] In step **3001**, the heavily doped semiconductor layer **419** (e.g. heavily doped n type silicon) is fabricated on the lightly doped semiconductor layer **421** by a method such as ion implantation and subsequent annealing. An exemplary n type dopant suitable for use in the ion implantation is phosphorous, arsenic, antimony, or a combination thereof.

[0111] In step **3002**, a resist layer **426** (e.g. a photoresist or an e-beam resist) is deposited on the heavily doped semiconductor layer **425**, by a suitable method such as spin coating.

[0112] In step **3003**, a pattern is formed in the resist layer **426** using a lithography technique (e.g. photolithrograph or e-beam lithography) by removing portions **427** of the resist layer **426**. The heavily doped semiconductor layer **425** is exposed under the removed portions **427**. The pattern corresponds to shapes and positions of the nanowires **400**.

[0113] In step **3004**, two metal layers **428** and **429** are deposited on the resist layer **426** and the exposed portions of the heavily doped semiconductor layer **425**, using a suitable technique such as thermal evaporation, e-beam evaporation, and sputtering. Exemplary metal suitable for use in the metal layers **428** and **429** are aluminum, gold, chromium, silver, copper, titanium, nickel or a combination thereof.

[0114] In step **3005**, remainder of the resist layer **426** and portions of the metal layers **428** and **429** thereon are lift-off by a suitable technique such as plasma ashing and dissolution in a suitable solvent.

[0115] In step **3006**, the nanowires **400** are formed by etching into the layers **425** and **421**, the using a suitable technique, such as dry etching with remainder of the metal layer **429** as etch mask, until portions of the silicon oxide layer **423** not directly below the remainder of the metal layer **429** are exposed. The nanowires **400** now comprise remainder of the layers **425** and **421**.

[0116] In step **3007**, remainder of the metal layer **429** is removed by a suitable method such as etching with a suitable metal etchant. The metal layer **428** remains.

[0117] In step **3008**, a silicide layer **418** is formed from the heavily doped semiconductor layer **425** and the metal layer **428** thereon by annealing (e.g. at about 850° C. for about 30 minutes). Any remainder of the metal layer **428** is removed by a suitable technique such as etching with a suitable metal etchant.

[0118] In step **3009**, a sacrificial layer **433** is deposited by pouring , spin coating or evaporation to fill space between the nanowires **400**. The sacrificial layer **433** can be a suitable material such as polydimethylsiloxane, polyimide or oxide.

[0119] In step **3010**, the substrate **410** is removed using a suitable technique such as etching with potassium hydroxide, until the silicon oxide layer **423** is exposed.

[0120] In step **3011**, a glass substrate **434** is bonded to the exposed silicon oxide layer **423**, using a suitable technique such as using a UV removable glue. The glass substrate **434** can provide mechanical support.

[0121] In step **3012**, the sacrificial layer **433** is removed by a suitable method such as wet etching. For example, polyimide can be removed by a suitable photoresist developer.

[0122] In step **3013**, the nanowires **400** are bonded to ROIC in the substrate **330** using a tin-silver alloy layer between the substrate **330** and the silicide layer **418** and annealing at about 220° C.

[0123] In step **3014**, the glass substrate **434** is released from the silicon oxide layer **423** by illumination with UV light.

[0124] In step **3015**, the silicon oxide layer **423** is removed by a suitable method such as etching with HF followed by rinsing.

[0125] In step **3016**, a resist layer **435** is deposited on the lightly doped semiconductor layer **421** by a suitable method such as imprinting.

[0126] In step **3017**, an oxide layer **436** is deposited on the substrate **430** and the resist layer **435** by a suitable method such as thermal evaporation, e-beam evaporation, and sputtering. The oxide layer **436** has a thickness greater than a total thickness of the heavily doped layer **419** and the silicide layer **418**.

[0127] In step **3018**, remainder of the resist layer **435** and portions of the oxide layer **436** thereon are lift-off by a suitable technique such as plasma ashing and dissolution in a suitable solvent.

[0128] In step **3019**, an intrinsic amorphous silicon (a-Si) layer (is deposited isotropically over the lightly doped semiconductor layer **421** and the oxide layer **436** to form the intermediate shell **431**, using a suitable technique such as ALD or CVD. ALD is preferred.

[0129] In step **3020**, a doped a-Si layer is deposited isotropically over the intermediate shell **431** to form the outer shell **432**, using a suitable technique such as ALD or CVD. The SBUV detector **40** is then annealed in a suitable atmosphere (e.g. forming gas) at about 450° C. for about 30 minutes.

[0130] In step **3021**, an oxide layer **437** (e.g. HfO_2, SiO_2, Al_2O_3) is deposited isotropically over the outer shell **432**, using suitable technique such as ALD or CVD. The oxide layer **437** is functional to passivate surfaces of the outer shell **432**.

[0131] According to one embodiment as shown in FIG. **9**, the SBUV detector **10**, **20**, **30** or **40** can be integrated with electronic circuitry into a solar-blind image sensor. The electronic circuitry can include address decoders, a correlated double sampling circuit (CDS), a signal processor, a multiplexor and a high voltage supply (e.g. a DC high voltage supply capable of supplying at least 50 V, 100 V, 200 V or higher) for driving the APDs in the nanowires **100**, **200**, **300** or **400**. The electronic circuitry is functional to detect the electrical signal generated by the nanowires **100**, **200**, **300** or **400**.

[0132] The SBUV detector **10**, **20**, **30** or **40** can also be used as fore optics in a light detector apparatus as shown in the schematic in FIG. **10**.

[0133] The foregoing detailed description has set forth various embodiments of the devices and/or processes by the use of diagrams, flowcharts, and/or examples. Insofar as such diagrams, flowcharts, and/or examples contain one or more functions and/or operations, it will be understood by those within the art that each function and/or operation within such diagrams, flowcharts, or examples can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or virtually any combination thereof.

[0134] Those skilled in the art will recognize that it is common within the art to describe devices and/or processes in the fashion set forth herein, and thereafter use engineering practices to integrate such described devices and/or processes into data processing systems. That is, at least a portion of the devices and/or processes described herein can be integrated into a data processing system via a reasonable amount of experimentation.

[0135] The subject matter described herein sometimes illustrates different components contained within, or connected with, other components. It is to be understood that such depicted architectures are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality. In a conceptual sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermediate components.

[0136] With respect to the use of substantially any plural and/or singular terms herein, those having skill in the art can translate from the plural to the singular and/or from the singular to the plural as is appropriate to the context and/or application. The various singular/plural permutations may be expressly set forth herein for sake of clarity.

[0137] All references, including but not limited to patents, patent applications, and non-patent literature are hereby incorporated by reference herein in their entirety.

[0138] While various aspects and embodiments have been disclosed herein, other aspects and embodiments will be apparent to those skilled in the art. The various aspects and embodiments disclosed herein are for purposes of illustration and are not intended to be limiting, with the true scope and spirit being indicated by the following claims.

What is claimed is:

1. A device comprising:

a substrate;

a plurality of pixels;

a plurality of nanowires in each of the plurality of pixel,

wherein the plurality of nanowires extend essentially perpendicularly from the substrate, and the device is configured to be a solar-blind UV detector to detect UV radiation in the solar-blind UV region.

2. The device of claim **1**, wherein the plurality of nanowires are configured to react only to radiations in the solar-blind UV region.

3. The device of claim **1**, wherein each of the plurality of nanowires comprises a core and a cladding surrounding the core, wherein the core has a higher refractive index than the cladding.

4. The device of claim **1**, wherein each of the plurality of the nanowires comprises a coupler disposed on an end of each of the nanowire away from the substrate, the coupler being functional to guide radiation into the nanowires.

5. The device of claim **1**, wherein the nanowires have a diameter from about 5 nm to about 30 nm, a height from about 0.1 μm to about 5 μm; the cladding has a thickness of about 10 nm to about 200 nm.

6. The device of claim **1**, wherein the nanowires have a pitch from about 0.2 μm to about 2 μm.

7. The device of claim **1**, wherein the nanowires detect UV radiation in the solar-blind UV region by converting UV radiation in the solar-blind UV region to an electrical signal.

8. The device of claim **7**, wherein the device further comprises electrical components configured to detect the electrical signal.

9. The device of claim **7**, wherein the device is functional to detect the electrical signal from the nanowires in different pixels separately.

10. The device of claim **1**, wherein each of the nanowires comprises a photodiode or forms a photodiode with the substrate, wherein the photodiode is functional to convert at least a portion of UV radiation in the solar-blind UV region impinged on the nanowires.

11. The device of claim **10**, wherein each of the nanowires comprises

a first heavily doped semiconductor layer,

a lightly doped semiconductor layer or an intrinsic semiconductor layer,

a second heavily doped semiconductor layer, and

a metal silicide layer;

wherein the first heavily doped semiconductor layer is disposed on the lightly doped semiconductor layer or the intrinsic semiconductor layer;

the lightly doped semiconductor layer or the intrinsic semiconductor layer is disposed on the second heavily doped semiconductor layer;

the second heavily doped semiconductor layer is disposed on the metal silicide layer;

the metal silicide layer is disposed on the substrate;

the first heavily doped semiconductor layer is of an opposite type from the second heavily doped semiconductor layer; and

wherein the first heavily doped semiconductor layer, the lightly doped semiconductor layer or the intrinsic semiconductor layer, and the second heavily doped semiconductor layer form the photodiode.

12. The device of claim **11**, wherein the device further comprises a common electrode disposed on and electrically connected to ends of all the nanowires, wherein the common electrode is substantially transparent to UV radiation in the solar-blind UV region.

13. The device of claim **12**, wherein the common electrode is made of graphene.

14. The device of claim **1**, wherein space between the nanowires is filled with an oxide layer.

15. The device of claim **12**, further comprising a metal grid on the common electrode, the metal grid configured to provide mechanical support for the common electrode.

16. The device of claim **10**, wherein each of the nanowires comprises

a core of lightly doped semiconductor,

an intermediate shell of intrinsic semiconductor and

an outer shell of doped semiconductor;

wherein the intermediate shell is conformally disposed over the core;

the outer shell is conformally disposed over the intermediate shell;

the outer shell is of an opposite type from the core; and

the outer shell, the intermediate shell and the core form the photodiode.

17. The device of claim **16**, wherein each nanowire further comprises

a heavily doped semiconductor layer of the same type as the core, and a metal silicide layer;

wherein the heavily doped semiconductor layer and a metal silicide layer are sandwiched between the core and the substrate;

the intermediate shell and the outer shell do not contact the heavily doped semiconductor layer and the metal silicide layer; and

the metal silicide layer is in contact with the substrate and forms electrical contact to the substrate.

18. A solar-blind image sensor, comprising the device of claim **1** and electronic circuitry functional to detect electrical signals generated by the nanowires of the device.

19. The solar-blind image sensor of claim **18**, wherein the electronic circuitry comprises a high voltage supply.

20. A method of fabricating an image sensor comprising a substrate, a plurality of pixels, a plurality of nanowires in each of the plurality of pixel, wherein the plurality of nanowires extend essentially perpendicularly from the substrate; the method comprising:

obtaining the plurality of nanowires and the substrate, and

bonding the plurality of nanowires onto the substrate.

21. The method of claim **20**, further comprising conducting lithography, ion implantation, annealing, evaporation, atomic layer deposition, chemical vapor deposition, dry etch or a combination thereof.

22. The method of claim **20**, wherein the image sensor is a device or a color image sensor.

23. The device of claim **10**, wherein the photodiode is an avalanche photodiode.

24. A method of detecting UV radiation, comprising obtaining the device of claim **1**, and detecting UV radiation with the device of claim **1**.

25. The method of claim **24**, wherein UV radiation in the solar-blind UV region.

26. The device of claim **1**, wherein the device is configured to detect UV radiation in only the solar-blind UV region.

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