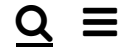


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Getting base stations ready for LTE

By Arun Iyengar, Altera Corp. 04.17.2007 0

Wireless cellular systems are moving from narrowband 2G Global Systems for Mobile **Communications** (GSM), IS-95 systems to Wideband Code Division Multiple Access (W-CDMA)-based **3G** and 3.5G systems.

As these standards progress, wireless base station OEMs must gear up with newer, better, more powerful, yet cost-effective technologies to handle the increasingly higher data rates these systems demand.

In the near future, third-generation partnership project long-term evolution (3GPP LTE) specifications will require complex signal **processing** techniques such as multiple-input, multiple-output (MIMO) along with new radio technologies like orthogonal frequency-division multiple access (OFDMA) and multi-carrier Code Division Multiple Access (MC-CDMA).

With technology demands like these looming in the near term, mobile and wireless service providers and operators want wireless base station OEMs to assure them the base stations they're placing in the field have the capability of supporting LTE.

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Operators are adamant about avoiding “rip and replace” situations. This means OEMs need to “future proof” their base stations with multi-protocol designs.

A multi-protocol base station is defined as one that can support W-CDMA to LTE standards. A base station family of this caliber will require the capability to move virtually seamlessly from one 3GPP release, for example, to a newer one in the same family without major costly re-designs.

Hybrid FPGA/digital signal processor-based platforms provide an effective design approach to comply with these ever-changing wireless standards. Intelligent partitioning between the FPGA and digital signal processor must be based on system throughput requirements and long-term cost considerations for product success. As standards stabilize, initial requirements for base station design flexibility should subside, while cost becomes a major success factor.

Selecting FPGAs with a risk-free migration path to low-cost structured **ASIC** technology translates into significant cost savings. For instance, Altera's HardCopy II technology provides a seamless, risk free **migration** from Stratix III FPGAs to significantly lower cost HardCopy II structured ASICs, while also increasing system performance and decreasing power consumption.

Evolving designs

Wireless operators worldwide are currently using High Speed Downlink **Packet** Access (HSDPA), which follows successful deployment of Universal Mobile Telecommunications Systems (UMTS) networks. The UMTS to HSPDA upgrade is similar to Enhanced Data Rates for GSM Evolution (EDGE), which has proven to be an effective upgrade to **GSM** networks.

HSDPA is targeted at mobile **multimedia** and can achieve reduced delays and peak data rates up to 14 megabits per second (Mbps) in the downlink from base station to mobile terminal. This is made possible by the addition of a new high-speed downlink shared channel along with three fundamental technologies relying on rapid adaptation of transmission parameters to the instantaneous channel conditions. Those are adaptive modulation and coding (AMC), fast hybrid automatic-repeat-request (ARQ) and fast scheduling.

High Speed Uplink Packet Access (HSUPA) will soon follow HSDPA, and the combination of the two technologies is called High Speed Packet Access (HSPA). HSPA is expected to be the dominant mobile data technology for the rest of the decade. To leverage operators' investments in HSPA, standards bodies are examining a series of enhancements to create “HSPA Evolution” also referred to as “HSPA+.”

HSPA Evolution, a logical development of W-CDMA, provides an effective transition to the completely new 3GPP LTE radio platform. LTE uses OFDM on the downlink and is targeted for deployment around 2009.

LTE taps the best-of-breed radio techniques to reach performance levels beyond what is practical with **CDMA** approaches. LTE systems will co-exist with 2G and 3G systems similarly to the way 3G co-exists with 2G systems in integrated networks.

Meanwhile, OFDM communications system designs continue making greater inroads. OFDM is a multi-carrier modulation scheme that encodes data onto a radio frequency (RF) signal. It is unlike conventional single-carrier modulation schemes, like amplitude or frequency modulation (AM/FM) that sends only one signal at a time using one radio frequency. Instead, OFDM sends multiple high-speed signals concurrently on specially-computed, orthogonal carrier frequencies. The result is much more efficient use of **bandwidth** as well as robust communications during noise and other interferences.

OFDMA on the downlink for LTE is well suited to achieve high peak data rates in high spectrum bandwidth. W-CDMA radio technology is about as efficient as OFDM for delivering peak data rates of about 10 Mbps in five **MHz** of bandwidth.

However, achieving peak rates in the 100 Mbps range with wider radio channels results in highly complex terminals and isn't practical with current technology. This is where OFDM provides a practical implementation advantage.

On the uplink, a pure OFDMA approach results in high signal Peak to Average Ratio (PAR), which compromises power efficiency and ultimately battery life. Hence, LTE uses an approach called single-carrier frequency division multiple access (SC-FDMA), which has some similarities with OFDMA but will have a two to six dB PAR advantage over the OFDMA method used by other technologies such as **IEEE** 802.16e.

LTE goals include:

- Downlink peak data rates up to 100 Mbps with 20 MHz bandwidth
- Uplink peak data rates up to 50 Mbps with 20 MHz bandwidth
- Operation in both TDD and FDD modes
- Scalable bandwidth up to 20 MHz, covering 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz, 15 MHz, and 20 MHz in the study phase. 1.6 MHz wide channels are under consideration for the unpaired frequency band, where a TDD approach will be used
- Increase spectral efficiency over Release 6 HSPA by a factor of two to four
- Reduce **latency** to 10 msec. round-trip time between user equipment and the base station and to less than 100 msec. transition time from inactive to active.

LTE is expected to address market needs of the next decade. After that, operators might deploy fourth generation (4G) networks using LTE technology as a foundation. There are no official standards efforts or formal definitions yet for 4G, but preliminary research focuses on technologies capable of delivering peak rates of one Gbps, being fully **IP** based, and supporting full network agility for handovers between different types of networks, e. g., 4G to 3G to WLAN.

Anticipating next designs

From a broad perspective, base station designers must anticipate some key design considerations. As they move into LTE, they should be aware there will be significant changes on the radio side.

W-CDMA signal modulation will move to OFDM as part of the migration to LTE, which features different characteristics. OFDM is more robust for delivering high throughput, but at the same time, stresses base station throughput capabilities.

OFDM also changes the peak to average characteristics of the modulated signal requiring new techniques to achieve crest factor reduction (CFR). Also, there are more stringent requirements on the error vector magnitude (EVM) requiring designers to pay particular attention to not just the type of algorithm used, but also the type of device to implement the algorithm.

On the baseband side, designers must consider different data rates moving from W-CDMA to OFDM since the required throughput is considerably higher. Also, WiMAX has so far been based on data and is not voice oriented. But when voice is introduced, designers must start provisioning similarly to that of wire line systems since the quality of service (QoS) for voice is different than for data.

As savvy base stations designers face off with LTE design challenges, they will continue to rely on the flexibility they have experienced with earlier FPGA-based designs and will exploit their newer advances to pull them through these daunting tasks.

The partitioning strategy between FPGAs and DSPs depends on processing requirements, system bandwidth as well as system configuration, and the number of transmit and receive antennas. Figure 1 shows a typical DSP/FPGA partitioning for baseband physical layer (PHY) functions in an OFDMA-based system such as WiMAX or LTE.

[Click here for Figure 1](#)

Figure 1: DSP/FPGA partitioning for OFDMA systems.

By incorporating advanced multiple antenna technologies, the throughput offered by such systems is expected to be between 75-100Mps. The baseband PHY functionality can be broadly categorized into bit-level processing and symbol-level processing functions.

The remainder of this article presents an overview of these functions and how FPGAs are used to complement DSPs for implementing both bit-level and symbol-level functions.

Bit-Level processing

The bit-level blocks include randomization, forward error correction (FEC), interleaving, and mapping to quadrature phase shift keying (QPSK) and quadrature amplitude modulation (QAM) functions on the transmit side.

The corresponding receive processing bit-level blocks are symbol de-mapping, de-interleaving, FEC decoding, and de-randomization. All bit-level functions except FEC decoding are relatively straightforward and not computationally intensive.

For example, randomization involves modulo-2 addition of the data bits with the output of a simple pseudo-random binary sequence generator. Although FPGAs offer more flexibility for bit-level manipulations than DSPs with fixed bus widths, the low computational complexity allows DSPs to manage these functions.

Conversely, FEC decoding including Viterbi decoding, Turbo convolutional decoding, Turbo product decoding, and LDPC decoding are computationally intensive and consume significant bandwidth when done with DSPs.

FPGAs are widely used to offload these functions and free DSP bandwidth for other functions. The same FPGA can also be used to interface to the MAC layer as well as implement certain lower MAC functions such as encryption/decryption and authentication. For example, Altera's low-cost Cyclone III FPGAs are suited to such DSP co-processing functions.

Symbol-Level Processing

Symbol-level functions in OFDMA systems include sub-channelization and de-sub-channelization, channel estimation, equalization and cyclic prefix insertion, and removal functions. The time-to-frequency domain conversion and vice-versa are implemented using FFT and IFFT, respectively.

Channel estimation and equalization can be performed offline and involve more control-oriented algorithms that are better suited for DSPs. Conversely, FFT and IFFT functions are regular data path functions involving complex multiplications at very high speeds and are better suited for implementation on FPGAs.

It is important for designers to know high system performance for DSP applications cannot be achieved by simply embedding dedicated multipliers. Rather, it is an aggregate result of high-performance multipliers and performance-matching logic structure and routing architecture implemented in an advanced FPGA.

Figure 2 shows the Stratix III DSP block is a high-performance silicon architecture with significant programmability that will deliver optimized processing across many applications.

Each DSP block provides eight 18 x 18 multipliers, as well as registers, adders, subtractors, accumulators, and summation unit-functions that are frequently required in typical DSP algorithms. The DSP block supports completely variable bit-widths and various rounding and saturation modes to efficiently meet the exact requirements of advanced wireless applications.

[Click here for Figure 2](#)

Figure 2: Embedded DSP blocks in FPGAs.

DSP processors typically have up to eight dedicated multipliers, whereas Stratix III devices will offer up to 768 18x18 dedicated multipliers providing throughputs of up to 500 GMACs, an order of magnitude higher than currently available DSPs.

Such a massive difference in signal processing capability between FPGAs and DSPs is further accentuated when dealing with base stations employing advanced, multiple antenna techniques such as space time coding (STC), beamforming, and MIMO schemes.

The combination of OFDM-MIMO is widely regarded as a key enabler of higher data rates in current and future WiMAX and LTE wireless systems. Figure 1, for example, shows multiple transmit and receive antennas employed at a base station.

In this station, symbol processing functions are implemented separately for each antenna stream before MIMO decoding is performed, producing a single bit-level data stream. The symbol-level complexity grows linearly when the antennas implemented on DSPs perform operations in a serial manner.

For example, when two transmit and two receive antennas are used; the FFT and IFFT functions consume approximately 40 percent of a 1GHz DSP when the transform size is assumed to be

2048 points.

In contrast, a multiple antenna-based implementation scales very efficiently when implemented with FPGAs. FPGAs provide parallel processing and time-multiplexing between the data from multiple antennas.

The same 2×2 antenna FFT/IFFT configuration can be implemented using less than five percent of an Altera Stratix III EP3SE260 FPGA.

Multiple antenna schemes provide higher data rates, array gain, diversity gain, and co-channel interference suppression. Beamforming and spatial multiplexing MIMO techniques are also computationally intensive, involving matrix decompositions and multiplications.

Specifically, Cholesky decomposition, QR decomposition, and singular value decomposition functions are useful in solving the linear set of equations common in these systems.

While these functions quickly exhaust DSP capabilities, they are well suited for FPGAs using well known systolic array architectures that provide a more cost-effective solution by exploiting FPGA parallelism. FPGAs can be used to perform these and other OFDM operations to offload digital signal processors (DSPs).

Doing so significantly reduces component count on an OFDM baseband board from a high number of DSP processors to two or three and about two FPGAs. In particular, high performance FPGAs, like Stratix III, can replace multiple DSPs. At the same time, they will provide more DSP performance at lower cost and less power, plus consume smaller board space and give designers more platform scalability.

About the author

***Arun Iyengar** is the senior director of Altera's Wireless Applications Business Group. He is responsible for leading Altera's activities in the wireless space, including identifying new trends, creating solutions and marketing these solutions to wireless infrastructure developers.*

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