13.3 A 65nm Single-Chip Application and Dual-Mode Baseband Processor with Partial Clock Activation and IP-MMU

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Presently, cellular phones are used not only for voice communications or SMS, but also for video telephony, 3D Java gaming and high-end business applications. Adoption of a High-Level-Operating System, such as SymbianOS or Linux in cellular phones is popular. A high-performance application processor serves as the host in such cellular phone systems and accompanies the baseband processor as a modem sub-system. Single-chip integration of an application processor and a baseband processor provides a good cost-performance balance. Our 1st generation of a one-chip integration of an application and a baseband processor, SH-MobileG1 (G1), had 20 power domains for very low leakage current [1], and a 2nd generation, SH-MobileG2 (G2), incorporated a dynamic clock-stop scheme to reduce idle time power consumption [2]. SH-MobileG3 (G3) is the third generation of a single-chip application and baseband processor, with both low power consumption and good performance.

The design highlights of G3 are as follows:

(1) Triple-V_t technology in a low-power 65nm CMOS process achieves 500MHz for two CPUs.
(2) Power domains are separated into 21 sub-blocks to reduce leakage power.
(3) A Partial clock activation method is introduced. Unnecessary clock systems are turned off following CPU core and other module activity.
(4) G3 introduceds a new IP-MMU, which translates virtual address to physical address or physical address to physical address, to 17 different kinds of media IPs.
(5) The interconnect buffer (ICB) [2] extends its function to involve the IP-MMU.

Figure 13.3.1 shows the G3 chip features and Fig. 13.3.7 presents a die micrograph. Supply voltages are 1.2V(internal) and 1.8/2.5/3.3V(I/O). G3 integrates a total of 307M transistors, 28.2M gates and 30.7Mb of memory. The die size is 9.3×9.3mm^2. To support applications, a large number of media engines are integrated. Powerful 2D/3D graphics engines, a video processing unit supports D1 size video decoding and encoding, and a camera-IF with image processing unit handles up to 12Mpixel cameras. The baseband portion has support for a dual-baseband system. The WCDMA block supports HSDPA service and a GSM block supports EDGE mode.

Figure 13.3.2 shows the CPU and bus architecture. The G3 system architecture has multiple OS on heterogeneous multi-CPU cores. In the application portion, an ARM1176 runs the OS and a SH-X2 runs realtime media applications. In the baseband, an ARM926 controls the baseband IPs including DSPs that handle modem protocols. 2D and 3D graphics IP cores and 15 other media IPs (for capturing, movie, displaying, blending, etc.) have IP-MMU or ICB between on-chip-buses. One of the architecture challenges of G3 is that in this super-heterogeneous system each MMU-enabled IP, ARM1176, SH-X, IP-MMU, and ICB, shares a single page table in a harmonized virtual address space.

The power domain view of G3 is shown in Fig. 13.3.3. A total of 21 hierarchical power domains are defined to provide useful power-down control for unused domains. The application part and baseband part are divided into 13 and 7 power domains, respectively, with one additional common power domain (C5). Clock buffers, clock dividers, repeater cells, hardware back-up FFs and a system controller are placed in the C5 domain whose power is always on. G3 introduces a partial clock activation method that separates the clock system, starting from the root PLL according to respective power domains and can terminate clock generation by shutting off separated power domains.

Figure 13.3.4 illustrates the partial clock activation method along with the reduction of current consumption expected. A dynamic clock-stop scheme [2] is used. For music playback, the CPU runs only 10% of the time for file handling, and the DSP works continuously for music decoding. Clock generation in the C5 domain is constantly working while clocks of most of the functional modules in the C5 domain are gated inside the modules. In this situation, the C5 domain consumes 17.4mA of 28mA total required current, due to a large number of FFs that could not be gated and clock sub-systems that include strong buffers. The dynamic-module-stop scheme stops the on-chip-bus router clock, and reduces current by an additional 3.8mA, but still the accumulation of power required by small circuitry, and continuously-running clock dividers and PLL consumes a large part of the power budget. Partial clock activation shuts-off the clock circuit, and stops the clock supply to a common area, reducing current from 13.6mA to 3.2mA, for a 33.5% reduction in total LSI power.

The OS maps the memory system, which is typically SDRAM, in the cellular phone system into page tables to maintain virtual address translation by the OS. Hardware media IPs typically use fixed allocated memories and memories cannot be re-configured even if the media IP finishes its operation. A Memory Management Unit (MMU) is widely employed in G3 for 17 different kinds of media IPs, which have different access patterns, and allows media IPs to access virtual address spaces. A IP-MMU is introduced for media IPs that are directly connected to the on-chip-bus and a ICB-MMU is introduced for media IPs that are connected to the on-chip-bus through an interconnect buffer (ICB) [2]. The SH-X CPU, which also has a MMU inside, takes care of control of the IP-MMU and ICB-MMU to minimize system performance impact.

The IP-MMU (Fig. 13.3.5) has a 16-entry, fully-associative Physical address space Mapping Buffer (PMB), and 64-entry, 2-way set-associative main virtual address space Table Lockup Buffer (main TLB). PMB holds addresses for physical-to-physical translation and the main TLB holds addresses for virtual-to-physical translation. The IP-MMU chooses one address from the PMB or main TLB according to the upper most bits of address issued by media IPs, and sends the address to the μTLB. The IP-MMU pre-fetches additional page table information for the main TLB when a main TLB miss occurs. This effectively decreases the TLB fill frequency as media IPs likely access contiguous memory, which is false for usual CPUs. In typical cellular phone systems, the IP-MMU allows the OS to free and re-use around 20 to 80MB of external memory and therefore reduces by the same size external memory.

The ICB is the bus bridge with buffering features supported by 512KB SRAM [2]. A newly introduced ICB-MMU (Fig. 13.3.6) is the MMU-enabled ICB that sits between 15 media IPs and the on-chip-bus (SHwy) router. The ICB-MMU translates the address like the IP-MMU does, but has a different structure to support a large number of connected IPs. The ICB-MMU has independent μTLBs for high-data-throughput media IPs (#0 to #2) and commonly used μTLBs for other media IPs (#3 to #15). In total four common μTLBs exist (for read, write, TLB and PMB). Buffered or cached data in MERAM will come or go through ICB0-15 and then uses a dedicated μTLB assuming that complicated accesses are buffered in the ICB and re-ordered into simple line directional (address incremental) access and that TLB misses will not be frequent. Of interest of this system is the data throughput when media IPs concentrate access at the same time. For example, it is important that the throughput of data doesn't decrease when the virtual memory translation is enabled at VGA 30fps in video camcorder applications.

References:

[1] T. Hattori, et al., "A Power Management Scheme Controlling 20 Power Domains for a Single-Chip Mobile Processor," *ISSCC Dig. Tech. Papers*, pp. 542-543, Feb. 2006.

[2] M. Ito, et al., "A 390MHz Single-Chip Application and Dual-Mode Baseband Processor in 90nm Triple-Vth CMOS," *ISSCC Dig. Tech. Papers*, pp. 274-275, Feb. 2006.

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Die size	9.3mm x 9.3mm
Process	65nm LP, CMOS triple V_{th}, 8M(7Cu+1Al)
CPU	AP-Realtime: SHX2, 500MHz AP-System: ARM1176JZF-S, 500MHz Baseband: ARM926EJ-S, 166MHz
Application Part	VPU(MPEG4/H.264/VC1), VIO(up to 12M pixel camera), 3D Graphics Accelerator, 512KB Media-RAM(MERAM), GPS SoundProcessingUnit
Baseband Part	Dual Baseband (WCDMA with HSDPA, GSM/GPRS/EDGE)
# of Power Domains	21 (1 for Common, 13 for Application, 7 for Baseband)
Supply voltage	1.2V(internal), 1.8/2.5/3.3V(I/O)
I/O	617 pins
# of TRs (logic cells, memory)	307M TRs (28.2M Gates, 30.7Mbit RAM, 6.4Mb ROM)

Figure 13.3.1: Chip features.

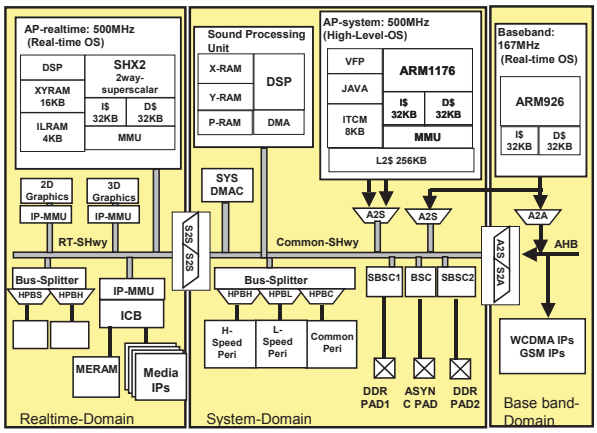


Figure 13.3.2: CPU and Bus architecture.

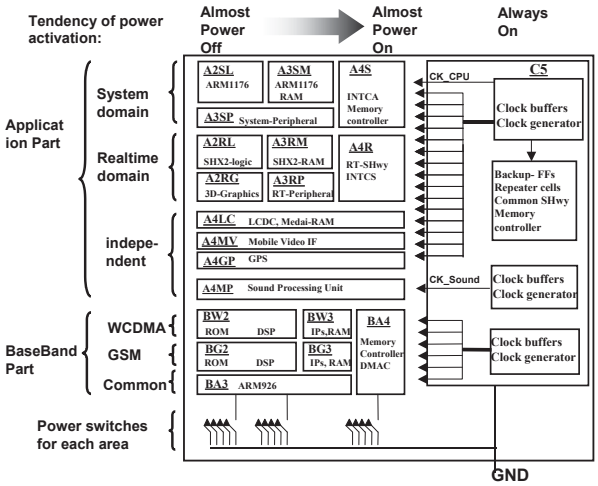
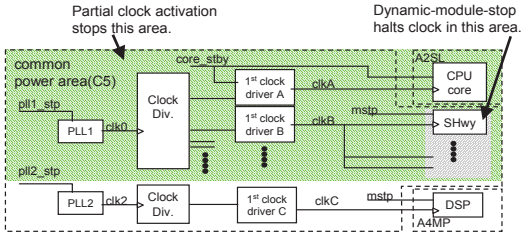


Figure 13.3.3: Power domains and partial clock activation method.



Measurement conditions	3DG game	ARM11 Drystone	Call waiting
SOC device current consumption(Total)	328mA	230mA	294uA

* 1.2V, normal condition

CPU Power-mode	Mode0	Mode1	Mode2
Dynamic module stop	Off	On	On
Partial clock activation	Off	Off	On
Common power area (C5) current (1.2V)	17.4mA *1	13.6mA *1*2	3.2mA *1*2

*1 module activity of SHwy is 1% (clk0=1GHz, clkA=500MHz, clkB=166MHz)
*2 clock active ratio is 10% (clk0=1GHz, clkA=500MHz, clkB=166MHz)

Figure 13.3.4: Implementation of dynamic clock activation scheme on SH-MobileG3 and measured power reduction results while playing music.

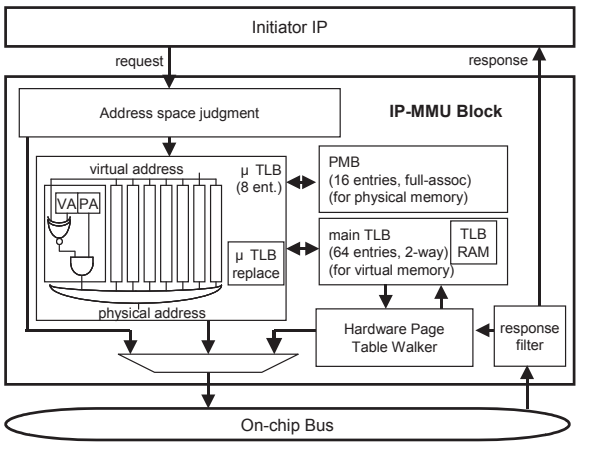


Figure 13.3.5: IP-MMU module block diagram.

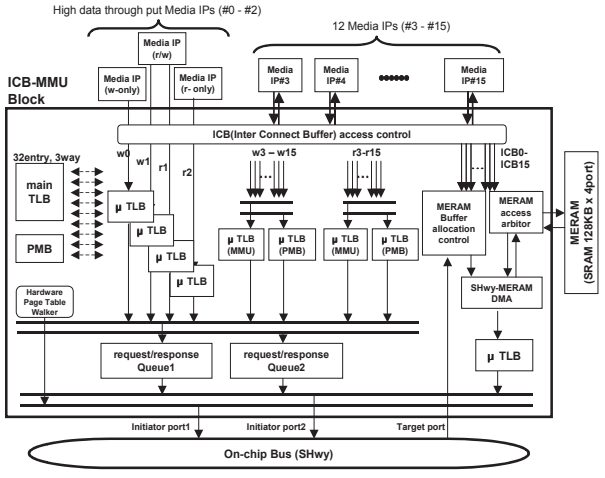


Figure 13.3.6: ICB-MMU module block diagram.

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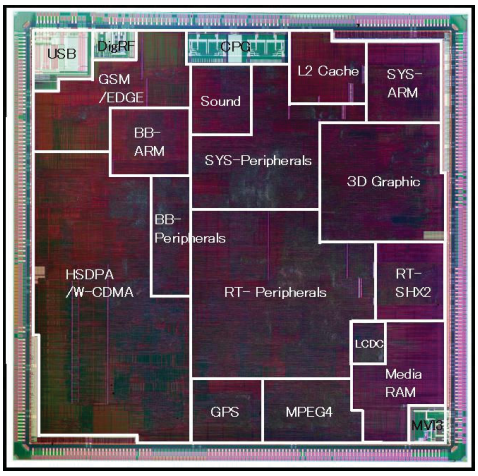

Figure 13.3.7: SH-Mobile G3 die micrograph.

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