**IN THE UNITED STATES PATENTS AND TRADEMARKS OFFICE**

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| In re Patent of: | Fwu-Iuan Hshieh |
| U.S. Patent No.: | 7,812,409 |
| Issue Date: | October 12, 2010 |
| Appl. Serial No.: | 11/633,366 |
| Filing Date: | December 4, 2006 |
| Title: | Trench MOSFET with cell layout, ruggedness, truncated corners |
| Attorney Docket No. | IPR02985-004 |

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 7,812,409**

**PURSUANT TO 35 U.S.C §§ 311–319, 37 C.F.R. § 42**

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# EXHIBITS

EX1001 U.S. Patent No. 7,812.409 to Hshieh (“the ‘409 Patent”)

EX1002 Prosecution History of the ‘409 Patent

EX1003 Declaration of Dr. Peter S. Gwozdz

EX1004 Curriculum Vitae of Dr. Peter S. Gwozdz

EX1005 U.S. Patent 5,072,266 (“Bulucea”)

EX1006 U.S. Patent Application Publication 2006/0273390 (“Hshieh”)

EX1007 U.S. Patent 6,984,864 (“Uno”)

EX1008 U.S. Patent 6,037,628 (“Huang”)

EX1009 U.S. Patent 7,285,822 (“Bhalla”)

**PETITION**

uPI Semiconductor Corp. ("Petitioner" or "uPI") petitions for *Inter Partes* Review ("IPR") of claims 1-5 (the "Challenged Claims") of U.S. Patent No. 7,812,409 ("'409 Patent"). Evidence presented herein shows a reasonable likelihood that uPI will prevail with respect to at least one of the Challenged Claims.

# I. OVERVIEW OF THE '409 PATENT

## 1. Brief Description

The '409 Patent was issued as U.S. patent 7,812,409 on October 12, 2010, based on U.S. patent application, serial no. 11/633,366, that was filed on December 4, 2006. The '409 Patent discloses a trenched power semiconductor device with truncated corners. EX1001. 1:9-13. Such devices include trench Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), also known as trench Metal-Insulator-Semiconductor Field-Effect Transistors (MISFETs). EX1003, ¶ 49. (In this Petition, for uniformity, the more popular term "MOSFET" will be used.) For purposes of this Petition, a trench MOSFET refers to a MOSFET with one or more trenched gates.

The preamble of Claim 1 of the '409 Patent recites "[a] trenched semiconductor power device comprising a plurality of trenched gates surrounding

a plurality of transistor cells formed in a semiconductor substrate." EX1001, 5:7-9. This preamble refers to a trench MOSFET in a "closed cell" configuration in which trenched gates surround "transistor cells.". EX1003, ¶ 55. The transistor cell refers to the structure bounded by the trenched gates. EX1003, ¶ 55. Indeed, the '409 Patent identifies its Figs. 1-3 as "closed cell units" or "close unit cells" of MOSFET devices with surrounding trenched gates. EX1001, 3:11-27. It is to be understood that the terms "closed cell unit" and "close unit cell" may be used herein interchangeably.

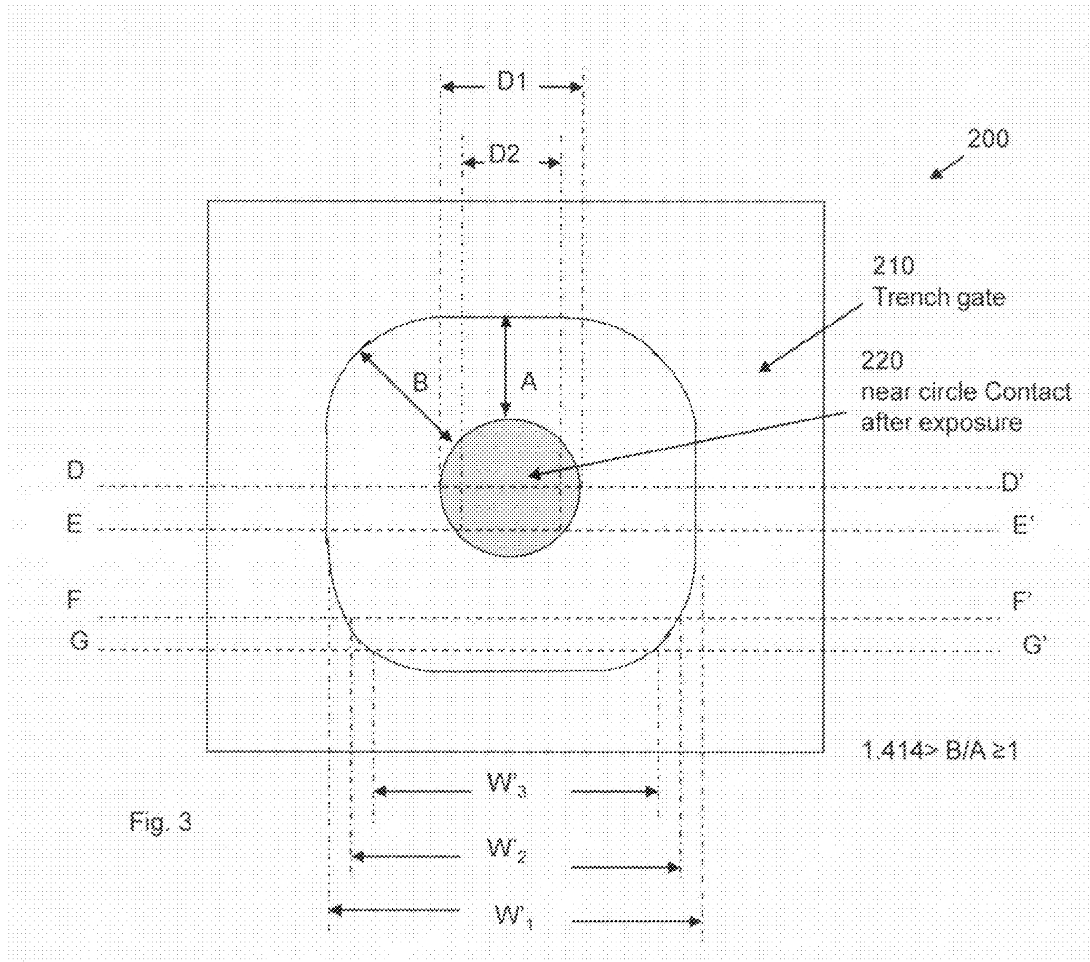
The '409 Patent concerns the "parasitic bipolar NPN latch up" problem in semiconductor power devices or trenched semiconductor power devices. EX1001, 1:15-18. (For brevity, Petitioner will refer to this latch-up phenomenon herein as the "Parasitic Bipolar Problem.") The '409 Patent notes that "[t]he parasitic bipolar NPN latch up difficulties are specially pronounced near the trench corners." EX1001, 1:18-20. The '409 Patent explains that "weak points of the MOSFET device due the non-uniform space between the square contact and the trench in the closed cell … occur at the four corners [resulting] in low avalanche current and reduced ruggedness due to the parasitic N+PN latches up near the trench corners …" EX1001, 1:50-57. (For brevity, Petitioner will refer herein this undesirable linkage between the Parasitic Bipolar Problem and weak points at the

corners of the gate trench as the "Surface Breakdown Link.") In other words, surface breakdown at the corners of the trenched gates can precipitate the Parasitic Bipolar problem. EX1003, ¶ 62.

To mitigate the Surface Breakdown Link, thereby enhancing ruggedness, the '409 Patent teaches forming trench gates that have rounded corners and forming dopant contact regions with a substantially circular shape:

> …[A] closed cell unit 200 of a MOSFET device includes trenched gate 210 surrounding a metal contact disposed above a doped contact region 220. The doped contact region 220 is formed with substantial circular shape and the trenched gate is formed with rounded corners 215.

EX1001, 4:5-9. See, also, Fig. 3. EX1003, ¶ 63.




The ‘409 Patent teaches that such a closed unit cell has a roughly uniform distance (i.e., 1.0 ≤ B/A ≤ 1.414) between the trenched gates (including the rounded corners) and a doped contact region under the circular metal contact. This roughly uniform distance mitigates the Surface Breakdown Link by eliminating the weak spots near the corners at the trenched gates:

> The distance from the edge of the circular doped contact region 220 to the trenched gate 200 including the distance B to the rounded corners 215 and to the distance A to the edges of the trenched gate are

> substantially the same, i.e., B=A. Therefore, the ratio of B/A is substantially kept near 1.0 and certainly smaller than 1.414. The weak spots near the corners of the trenched gate that caused reduced device ruggedness are therefore eliminated.

Ex1001, 4:9-17; EX1003, ¶ 64.

(For brevity, the roughly uniform distance closed unit cell of Fig. 3 will be referred herein as "Uniform Cell")

Note that the reference numeral 220 is used in the Specification to refer to both "doped contact region 220" (4:4-7) and "circular trench source-body trench contact 220" (4:25-30). Reference numeral 220 is associated in Fig. 3 with a feature labeled "near circle Contact after exposure" and in each of Figs. 3A-3D to the trench contact itself. EX1003, ¶ 65. The '409 Patent also teaches that, not only that the circular dopant region in the Uniform Cell of Fig. 3 has uniform space between it and the trenched gates, that uniform space is also seen between the contact metal and the trenched gates:

> In an exemplary embodiment, the closed cells further includes a contact metal to contact a source and a body region[] wherein the contact metal [and] the trenched gate surrounding the transistor cell have a uniform space between them.

EX1001, 2:39-43. EX1003, ¶ 66.

Claim 1 of the '409 Patent appears to be directed to this exemplary

embodiment:

> said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;
>
> each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, …
>
> (emphasis added) EX1001, 5:10-15; EX1003, ¶ 67.

The '409 Patent teaches that the Uniform Cell of Fig. 3 is formed by applying a photo-lithographical technique on a square closed unit cell with truncated corners:

> The process for manufacturing the semiconductor power device as disclosed above thus includes a step of "exposure through the mask," such that the square contact becomes approximately circular shaped contact and truncated corners become smoother. The truncated corners are formed by design layout not process. It is by nature that truncated corners in layout as that shown in FIG. 2 and becomes rounded as shown in FIG. 3. Such configuration is formed after exposure because of the photolithography resolution of 0.18-0.35 micrometers.

EX1001, 5:53-62. EX1003, ¶ 68.

The '409 Patent teaches that the truncated corners in the layout of the

trenched gates become rounded "by nature," meaning that the rounded corners are the necessary result when the lithographical technique is applied. EX1003, ¶ 69.

This photo-lithographical technique takes advantage of its resolution limits. EX1003, ¶ 70. Minimum line-width or "critical dimension" squares would necessarily become approximately circular after development. EX1003 ¶ 70. The truncated or beveled corners of the trenched gates are created by "design layout" and becomes "smoother" after lithographic development (i.e., "substantially square-shaped cells with rounded corners"). EX1003 ¶¶ 68-69.

(For brevity, this method of photo-lithographically creating an "after exposure" approximately circular image from a square feature of critical dimension will be referred herein as "Litho-rounding Technique.").

As quoted above, the truncated or beveled corners in the design layout of the trenched gates have internal angles of 135 degrees, thus presenting less acute angles than the 90-degree internal angles of a square. EX1003 ¶ 52. The '409 Patent teaches that, processing such a design layout using the Litho-rounding Technique would result in the "substantially square-shaped cells with rounded corners." EX1003 ¶¶ 68-69.

The '409 Patent describes, in conjunction with Fig. 3A, the location of the contact trench relative to source and body regions and the trenched gates:

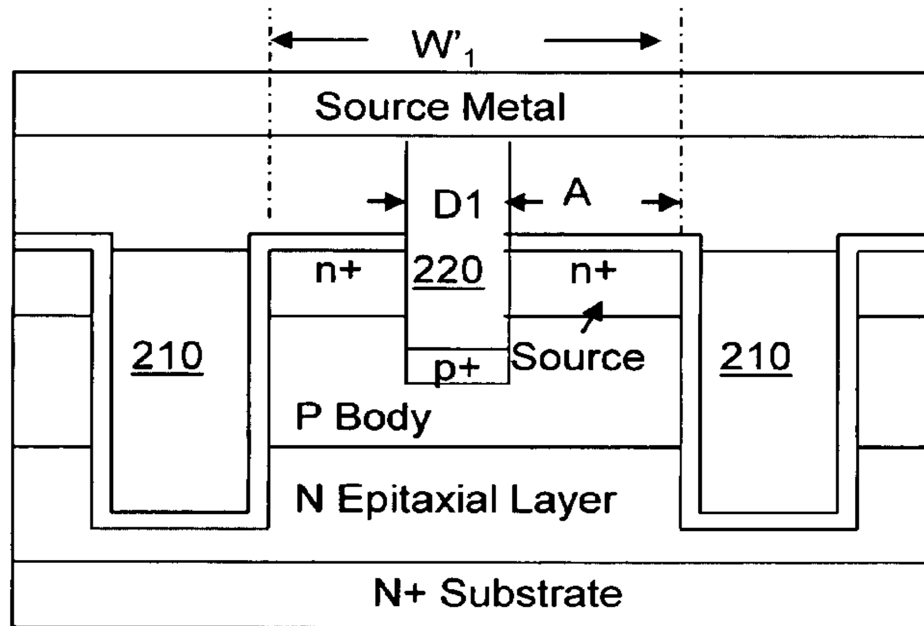



Fig. 3A (D-D' Cross Section)

> "The close semiconductor cell is surrounded by trench gates with a body region formed between the trench gates and encompassing a source region. … The closed semiconductor power cell further includes a circular trench source-body trench contact 220 extended into the body region through the source region of the closed semiconductor power cell in contact with a $p^+$ contact dopant region disposed immediately below the trench contact 120. The circular trench contact 220 is disposed at a distance away from a gate oxide lining of said trench gate from all circumferential points of the circular trench contact.

EX1001, 4:20-33. EX1003, ¶ 71.

This description supports Claim 1's circular trench contact limitations that recite:

> [the circular trench contact] … penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;
>
> said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact …"

EX1001, 5:15-26. EX1003, ¶ 72.

Providing a trench contact that reaches below the silicon surface into the body region to contact a contact dopant region that is immediately under the trench contact is known in the prior art. EX1003, ¶ 73. In fact, such a trench contact is shown in the admitted prior art in Figs. 1C and 1D. EX1003, ¶ 73. The only limitations trench contact 15 in admitted prior art Fig. 1C would not meet are "circular" and "circumferential." EX1003, ¶ 74. These remaining limitations are inherently met when the trench contact is formed approximately circular. (Figs. 3A-3D.) EX1003, ¶ 74.

(For brevity, a trench contact that reaches below the silicon surface to contact a contact dopant region that is immediately beneath the trench contact will be herein referred to as a "Deep Body Trench Contact").

Claim 1 recites:

> said contact metal plug connected to a source metal disposed on top of said circular trench contact.

EX1001, 5:27-28.

The claim term "source metal" above does not appear in the textual description of the '409 Patent, but appears in each of Figs. 3A-3D, and also in admitted prior art Fig. 1C. The above limitation is met by Fig.1C and is therefore part of prior art, EX1003, ¶ 76.

Limitations recited in Claims 2-4 of the '409 Patent do not appear in the textual description of the '409 Patent, appearing only as labels in the admitted prior art in Figs. 1B-1D. EX1003, ¶ 77. Claim 2 is met by the metal layer labeled "Ti or Ti/TiN" in Fig. 1B. Claim 3 is met by the metal layer labeled "Ti/TiN/W" in Fig. 1C. Claim 4 is met by the metal layer labeled "Al Alloys" in each of Figs. 1B and 1C.

Limitations recited in Claim 5 appear in neither the textual description nor the drawings, except as originally filed as a claim. The recited limitation of Claim

5 was introduced into then Claim 12 without justification on April 15, 2009.

EX1002, Amendment of April 15, 2009, at p.7. EX1002.345.

## II. Level of Ordinary Skill in The Art

A person of ordinary skill in the art pertaining to the subject matter of the ’409 Patent as of December 4, 2006 (“POSITA”) would have (i) attained an undergraduate degree in electrical engineering, physics, material science, chemistry, or a similar discipline, and (ii) two or more years of experience in the field working in the design or reliability of semiconductor devices. EX1003, ¶ 86. Attainment of a relevant advanced graduate degree, or relevant academic research experience, would be deemed equivalent to the work experience. EX1003, ¶ 86.

## III. LIST OF CHALLENGED CLAIMS

Petitioner challenges in this petition Claims 1-5. The following table sets forth their claim language and assigns references signals to their limitations.

| Reference Signals | Claim Language |
|---|---|
| [1pre] | 1.A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein |
| [1a] | said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners; |
| [1b] | each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, |
| [1c] | penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region; |
| [1d] | said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug |

| Reference Signals | Claim Language |
|---|---|
| [1e] | wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact; and |
| [1f] | said contact metal plug connected to a source metal disposed on top of said circular trench contact. |
| [2] | 2. The trenched semiconductor power device of claim 1 further comprising:<br>a contact resistance reduction metal layer composed of a titanium (Ti) layer disposed above a top surface said contact metal plug and below a bottom surface of said source metal for reducing a contact resistance between said contact metal plug and said source metal. |
| [3] | 3. The trenched semiconductor power device of claim 1 wherein:<br>said contact metal plug disposed in said hole of said circular trench contact further comprising a Ti/TiN/W metal plug. |

| Reference Signals | Claim Language |
|---|---|
| [4] | The trenched semiconductor power device of claim 1 wherein:<br>said source metal disposed on top of and in contact with a top surface of said metal plug further comprising a layer composed of aluminum alloys including alloys of AlCu or AlSiCu. |
| [5] | 5. The trenched semiconductor power device of claim 1 wherein:<br>a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer. |

# IV. REQUIREMENTS UNDER 37 C.F.R. § 42.104

## 1. Ground for standing

Petitioner certifies that the ’409 Patent is available for IPR. Petitioner is not barred or estopped from requesting this review.

## 2. Identification of challenge

Petitioner requests IPR of the ‘409 Patent based on the four grounds identified in the table below.

As set out in the table, Petitioner demonstrates for each ground that one or more of the Challenged Claims are obvious under 35 U.S.C. § 103. Accompanying explanations and support are provided in the Declaration of Dr. Peter S. Gwozdz Declaration. EX1003, ¶¶ 106-210.

| Ground | Claim(s) | §103 References |
|---|---|---|
| 1 | 1-5 | Bulucea, in view of Hshieh |
| 2 | 1 | Bulucea, in view of Uno |
| 3 | 1 | Bulucea, in view of Huang |
| 4 | 1, 3-5 | Bulucea, in view of Bhalla |

The ’409 Patent was issued on a U.S. patent application that was filed on December 4, 2006 and was published on June 5, 2008 as U.S. Patent Application Publication 2008/0128829. EX1001, cover sheet. December 4, 2006 is the ‘409 Patent’s “Effective Filing Date” or “Critical Date,” for purpose of priority.

Prior art references Bulucea, Uno and Huang are each available as either patent or printed publication, or both, under 35 U.S.C. § 102(b) as of its patent or publication date. All prior art references are available as patents or printed publications under 35 U.S.C. § 102(e) as of their respective patent or effective filing dates.

| **Prior Art Reference** | **Effective Filing Date or § 102(e) Date** | **Patent or Publication Date** |
|---|---|---|
| Bulucea (EX1005) | December 27, 1988 | December 10, 1991 |
| Hshieh (EX1006) | July 14, 2005 | December 7, 2006 |
| Uno (EX1007) | June 18, 2003 | January 22, 2004 |
| Huang (EX1008) | June 30, 1997 | March 14, 2000 |
| Bhalla (EX1009) | February 11, 2005 | August 17, 2006 |

All claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1311-1319 (Fed. Cir. 2005); 37 C.F.R. §

42.100. Additionally, "claim terms need only be construed to the extent necessary to resolve the controversy." *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011).

Petitioner, however, believes that the claim term "circular trench contact" should be construed broadly to include "approximately circular shaped trench contact" as taught in the '409 Patent. EX1001, 4:53-57. In this case, a narrower construction would omit the only disclosed embodiment. EX1003, ¶ 96. *Apple Inc. v. Corephotonics, Ltd.,* 81 F.4th 1353, 1358-60, 2023 USPQ2d 1056 (Fed. Cir. 2023).

The claim term "source metal" appears only in the claims and in figures. EX1003, ¶ 98. Petitioner believes that it should also be broadly construed to mean "a metal layer." EX1003, ¶ 100.

Petitioner sets forth the proposed claim construction in the following table"

| 1. Claim Term | 2. Proposed Construction |
|---|---|
| Circular trench contact | A trench contact that has a horizontal cross section that is circular or approximately circular |
| Source metal | A metal layer |

### 3. The Challenged Clams Are Unpatentable

#### (1) SUMMARY

The Parasitic Bipolar Problem and its causal Surface Breakdown Link that the claimed invention of the '409 Patent purports to have overcome have been known in the prior art, e.g., in Bulucea. In fact, Bulucea not only explains in detail both the Parasitic Bipolar problem and the causal Surface Breakdown Link, Bulucea provides specific solutions, and also general suggestions to other solutions. EX1003, ¶ 107.

Among the specific solutions proposed in Bulucea is rounding the corners at the trenched gates. Bulucea's methods for rounding include the Litho-rounding Technique, used in the '409 Patent, and a sacrificial oxidation of the silicon sidewalls of the gate trenches. EX1003, ¶ 108.

Bulucea also suggests providing a heavily doped $p^+$ deep body dopant region that is in contact with a source/body contact. This $p^+$ deep body dopant region reaches into the silicon substrate, at least as deep as the body region, so as to cause the currents related to the surface breakdown to move away from the high resistivity body region to the low resistive path through the $p^+$ deep body dopant region to the source/body contact. EX1003, ¶ 109.

The principles behind Bulucea's $p^+$ deep body dopant region are implemented in source/body trench contacts in trench MOSFETs. EX1003, ¶ 110. Examples of trench contacts are found in the prior art to the '409 Patent, including Hshieh, Uno, Huang and Bhalla. EX1003, ¶ 111.

All limitations of at least Claim 1 of the '409 Patent are met by combining the teachings of Bulucea with the teachings of any one of Hshieh, Uno, Huang and Bhalla. EX1003, ¶ 112.

### (2) GROUND 1: The Challenged Claims are obvious under 35 U.S.C. § 103 over Bulucea, in view of Hshieh

#### a) Relevant Teachings of Bulucea

Bulucea was issued as U.S. Patent 5,072,226 on December 10, 1991, from a U.S. patent application that was filed on December 27, 1988. Thus, Bulucea is available as prior art to the '409 Patent under as both patent and printed publication under pre-AIA 35 U.S.C. § 102(b).

Bulucea relates to a trench MOSFET that includes "a central deep $p^+$- (or $n^-$-) layer that is laterally adjacent to a p-body layer and that is vertically adjacent to an epitaxial layer of appropriate thickness and a gate dielectric of appropriate thickness in a trench." EX1005, 1:60-64. Bulucea's Fig. 21 discloses a trench MOSFET, with square transistor cells (i.e., square closed unit cells) and gate

trenches provided in a closed-cell configuration:

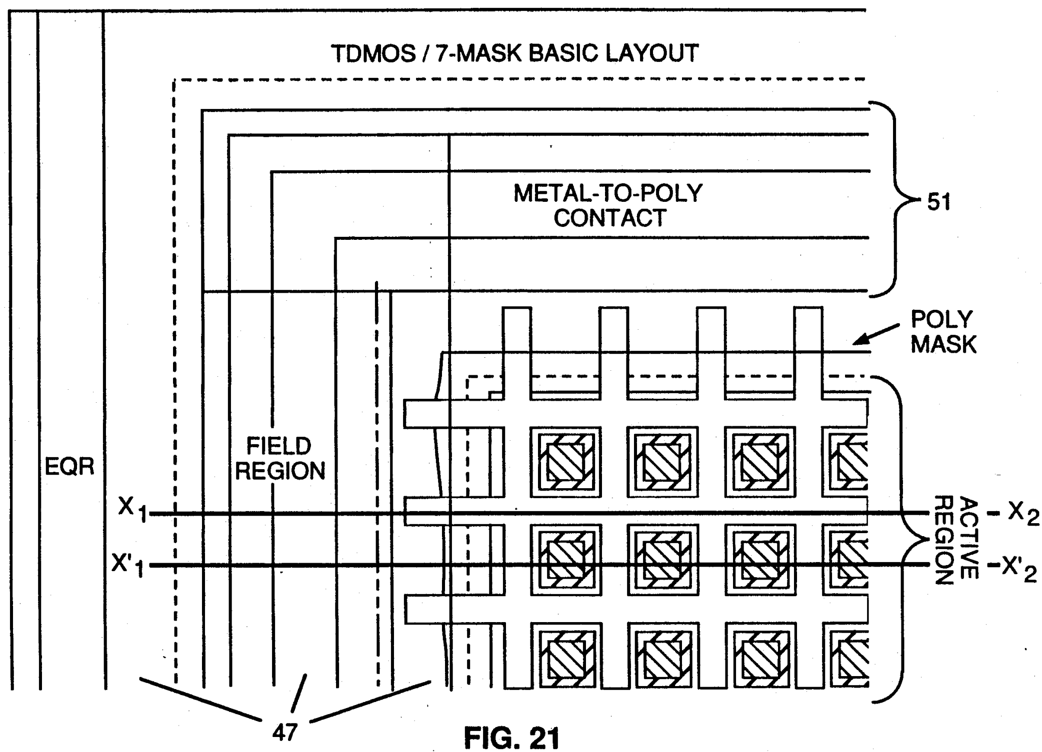


FIG. 21

EX1005, Fig. 21; EX1003, ¶ 114.

Bulucea's Fig. 21 is a schematic plan view of a group of transistor cells (square-cell geometry), EX1005, 3:14-15. EX1003, ¶ 115. Fig. 21 meets the [1pre] preamble of the '409 Patent, which recites:

> a trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate …

EX1001, 5:7-9. EX1003, ¶ 116.

To be discussed in further detail below:

(i) Bulucea -- like the '409 Patent -- is concerned about the Parasitic Bipolar Problem and its causal Surface Breakdown Link. EX1003, ¶ 117.

(ii) Bulucea also discloses that the rounded corners of the trenched gates and the circular profile in the source/body contact (plan view) of the Uniform Cell can be formed by the Litho-rounding Technique, in the same way as taught in the '409 Patent. EX1003, ¶ 118. Notably, the Uniform Cell meets limitations [1a] and [1b] of the '409 Patent. EX1003, ¶ 140.

(iii) Bulucea also discloses at least one additional method for creating "substantially square-shaped cells with rounded corners" (i.e., Claim 1's limitation [1a]). EX1003, ¶ 119.

(iv) While not expressly disclosing a Deep Body Trench Contact, Bulucea teaches a deep body dopant region, which encompasses principles for mitigating the Parasitic Bipolar Problem, as explained in further detail below. EX1003, ¶ 120. Bulucea's teachings would therefore motivate a POSITA to incorporate the Deep Body Trench Contact taught in each of

references Hshieh, Uno, Huang and Bhalla, as set forth in Grounds I-IV, respectively. EX1003, ¶ 121.

Thus, first, Bulucea explains the Parasitic Bipolar Problem:

> … "bipolar breakdown" [] is controlled in part by the resistance between the intrinsic body region below the gate region and the body contact. …
>
> … When the drain voltage exceeds a certain breakdown value, the bipolar breakdown phenomenon is manifest where the drain current increases prematurely for drain voltages below the drain-source junction breakdown voltage (BVDSS).

EX1005, 4:2-5, 11-16. EX1003, ¶ 122.

Using a computer simulation (Fig. 5), Bulucea demonstrates the Surface Breakdown Link:

> … surface breakdown is undesirable from the point of view of position of the source of avalanche-generated carriers relative to the body contact. If surface breakdown takes place adjacent to the trench, holes (electrons) flow laterally inside the $p^-$ ($n^-$) region, toward the body contact. This forward biases the source-to-body junction and brings the transistor into a bipolar breakdown mode, latch-back.

Ex1005, 5:26-33. EX1003, ¶ 123.

Based on the Surface Breakdown Link, Bulucea concludes that the Parasitic

Bipolar Problem can be mitigated by avoiding breakdown at the gate trenches. In conjunction with its Fig. 7, Bulucea explains that the sharp corners (e.g., 90 º angles) of the trenched gates can lead to a dielectric breakdown: EX1003, ¶¶ 124-125.

Bulucea states:

> … In a closed-cell geometry, the trench side wall oxide is grown under nonplanar, two-dimensional conditions at intersections of trench faces This causes nonplanar, viscous deformation and stress in the adjacent gate oxide material. … When these distortions are combined with conformal covering of the surface of gate material, the oxide profile may develop near-atomically sharp field concentration sites and may manifest premature dielectric breakdown.

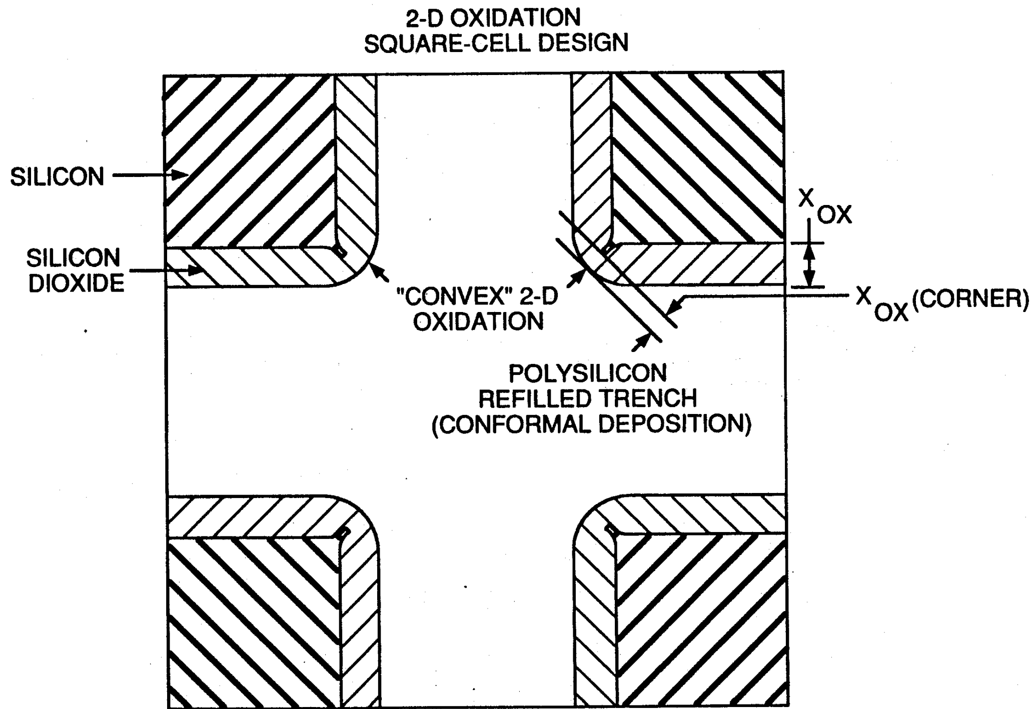



FIG. 7

EX1005, 5:55-68, Fig. 7. EX1003, ¶ 124. Dielectric breakdown, which occurs at the gate oxide layer next to the trenched gates, is one form of surface breakdown. EX1003, ¶ 126.

Accordingly, Bulucea discloses mitigating dielectric breakdown by rounding the corners at the trenched gates:

> This problem can be managed and eliminated to some extent by growing and etching away a 'sacrificial oxide layer' before the gate oxide is grown on the trench walls … This sacrificial oxidization

rounds off the sharp corners of the initial trench profile.

EX1005, 6:1-10. EX1003, ¶ 127.

Bulucea discloses in detail a process for using this sacrificial oxide layer approach in its Figs.25(a) and 25(b), in conjunction with the discussion at EX1005, 12:38-51. EX1003, ¶ 128. The process would result in "said trenched gates [of the square transistor cells of Fig. 21] surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners," thereby meeting limitation [1a] of Claim 1 in the '409 Patent. EX1003, ¶ 128.

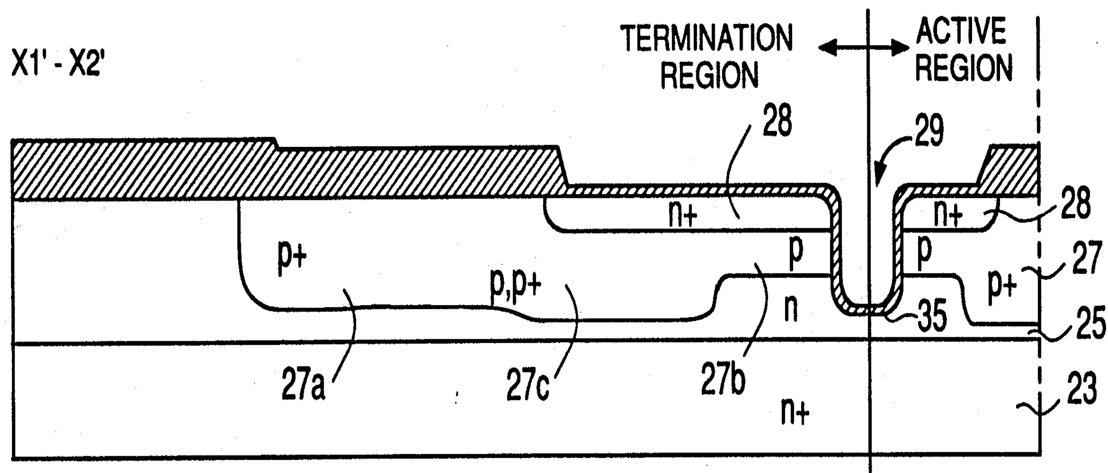



FIG. 25A

Bulucea's Fig. 25A shows teaches forming a uniform thickness gate oxide using the sacrificial oxidation approach. EX1005, 12:38-51. The resulting

trenched gate profile meets limitation [1a] of the '409 Patent: trenched gates 29 surround the transistor cells as closed cells constituting substantially square-shaped cells with rounded corners. EX1003, ¶ 129.

Bulucea discloses a further method of rounding the corners at the trenched gates. EX1003, ¶ 130. Bulucea discloses in conjunction with Fig. 8, a hexagonal cell. EX1003, ¶ 130. Bulucea teaches that the hexagonal cell, which has 120-degree internal angles, would become rounded when process under the Litho-rounding Technique:

> Further, the hexagon corners may become rounded off during the trench mask lithography and etching processes that precede trench formation so that the DMOS cells approach the cylindrical shape of a natural, field-controlled current valve.

EX1005:7:53-57. EX1003, ¶ 130.

Bulucea explains that, in a horizontal cross-section, the trench side walls intersect at angles of approximately 120°, as compared to an intersection angle of 90° in a rectangular cell design. Thus, Bulucea exchanges sharp 90° for the less acute 120° internal angles. Bulucea thus teaches in principle the same approach that is used in the '409 Patent, i.e., exchanging sharp 90° for less acute 120° internal angles. EX1003. ¶ 131.

Although Bulucea's Fig. 8 shows a hexagonal cell, Bulucea emphasizes that

the principle of rounding the corners using the lithography at the trenched gates is applicable to any polygonal cell, as eliminating the angles of the polygonal cell – towards the preferred shape of a circle -- is the goal for reducing dielectric breakdown at the trenched gates:

> For transistor operation the trench shape, in horizontal cross section (plan view), may be a polygon (not necessarily regular) or a circle or an oval; but the regular hexagon and polygonal shapes approaching a circle are the preferred shapes from the point of view of maximizing the gate oxide rupture voltage.

EX1005, 7:60-66. EX1003 ¶ 136. Maximizing gate oxide rupture volage means reducing the possibility of surface breakdown at a given gate voltage. EX1003 ¶ 137.

Because Bulucea teaches that the preferred horizontal cross section of a trench MOSFET cell is a circle or oval, a POSITA would be motivated to apply the Litho-rounding Technique to a square closed unit cell, e.g., the square cells of Bulucea' Fig. 21. EX1003, ¶ 138. As the source-body contact of the square closed unit cell is inside the surrounding trenches, with sides of critical dimensions, the Litho-rounding Technique would necessarily provide approximately circular source/body contacts. EX1003, ¶ 139. Thus, after development, that closed cell would further include a circular contact disposed

substantially in a central portion of the closed cell. In this regard, that resulting transistor cell in the plan view would be substantially identical to the Uniform Cell of Fig. 3 of the '409 Patent (EX1003, ¶ 140), meeting limitations [1a] and [1b] of Claim 1 of the '409 Patent. EX1003, ¶ 140.

In fact, applying both the Litho-rounding Technique on the source/body and the sacrificial oxidation on the trenched gates (as shown in Bulucea's Fig. 25A), the rounded corners of the trenched gate would also meet both limitations [1a] and [1b] of Claim 1 of the '409 Patent. EX1003, ¶ 141. Bulucea's Fig. 31A shows the circular trench contact – the horizontal portion of metal 43b in contact with both source region 28 and $p^+$ body region 27 -- disposed substantially in a central portion of the closed cell:

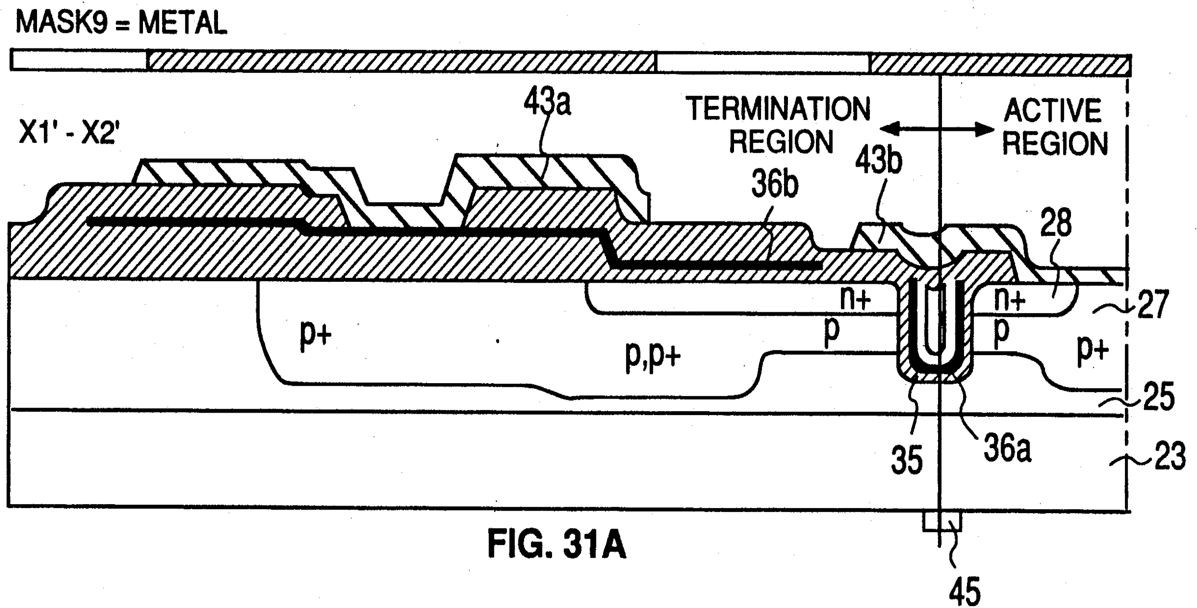


FIG. 31A

In addition to rounding the corners at the trenched gates, Bulucea discloses mitigating the Surface Breakdown Link by forcing surface breakdowns away from the body region next to the trenched gates – where the resistivity is high -- but towards the source/body contact at the center:

> Hence, for a latch-back-free design, the drain breakdown must be controlled such that breakdown occurs on the contact side of the $p^-$ ($n^-$) region, thus avoiding lateral current flow in the high resistivity body region.

EX1005, 5:33-37; EX1003, ¶ 143.

To achieve this result, Bulucea discloses, also in conjunction with its Fig. 8, providing a deep body dopant region underneath and in contact with the

source/body contact, such that a low conductivity path is provided away from the trench edge for the avalanche current, thus avoiding the Parasitic Bipolar Problem:

> As noted, a deep body dopant region is included in the center of the transistor cell 21 where the body contact is to be made. This diffusion is … so that the semiconductor breakdown is forced away from any trench surface or corner and into the bulk of the semiconductor material … Moreover, avalanche breakdown occurs below the body contact, not laterally along the contact, and lateral voltage drop through the body region, which would lead to bipolar breakdown, is avoided.

EX1005, 7:11-28. EX1003, ¶ 144.

Bulucea's deep body diffusion approach providing a low resistivity path between the source/body contact and the body region is a principle used in the Deep Body Trench Contact of admitted prior art Figs, 1C and 1D – i.e., the Deep Body Trench Contact electrically contacts a deep body diffusion at the center of the transistor cell, in the same manner Bulucea's source/body contact contacts its $p^+$ dopant diffusion region. Thus, a POSITA would be motivated to combine the teachings of Bulucea with the teachings of a reference that teaches a Deep Body Trench Contact, modifying Bulucea's source/body contact by the reference's Deep Body Trench Contact. EX1003, ¶ 146. Such a Deep Body Trench Contact may be found, for example, in each of Uno, Huang and Bhalla. EX1003, ¶ 146.

Also, in its mitigation of oxide breakdown at the trenched gates, Bulucea teaches to take on-resistance into consideration, as it is undesirable to have increased on-resistance:

> A third variable of importance here is the thickness of the oxide layer separating the gate material 29 (for example, doped polysilicon) from the surrounding n-type and p-type semiconductor materials. If the gate oxide thickness is increased, the gate oxide can take up a larger portion of the stress associated with the local electrical field, and initiation of avalanche breakdown adjacent to the trench becomes less likely. However, if the gate oxide thickness is increased, the on-state resistance is also increased (undesirable) …

EX1005, 10:27-37. EX1003, ¶ 147.

Thus, a POSITA would also be motivated to combine Bulucea's teaching with a reference that teaches reduction of on-resistance in a trench MOSFET, such as Hshieh. EX1003, ¶ 148.

**b) Relevant Teachings of Hshieh**

Hshieh is a U.S. Patent Application Publication based on a U.S. patent application that was filed on July 14, 2005, and that was published under 35 U.S.C. § 122(b) on December 7, 2006. In addition to inventor Fwu-Iuan Hshieh, Hshieh includes a second inventor, Brian Pratt. Thus, Hshieh is available as prior art to the '409 Patent as printed publication by another under pre-AIA 35 U.S.C. §

102(e)(1) as of its filing date. *Lynk Labs, Inc. v. Samsung Electronics Co. Ltd.*, 125 F.4th 1120, at 1132 (Fed. Cir. 2025) (precedential). *Ex parte DesOrmeaux*, 25 USPQ2d 2040, at 4 (Bd. Pat. App. & Inter. 1992),

Hshieh relates to a trenched semiconductor power device with improved source metal contacts. EX1006, ¶ [0003]. EX1003, ¶ 149. Hshieh teaches a trench MOSFET in closed-cell configuration, with trench gates surrounding source and body regions of a closed unit cell:

> [0013] … the present invention discloses a trenched metal oxide semiconductor field effect transistor (MOSFET) device that includes a trenched gate surrounded by a source region encompassed in a body region above a drain region disposed on a bottom surface of a substrate. …

EX1006, ¶ [0013]. EX1003, ¶ 150.

Hshieh concerns on-resistance in a trench MOSFET; specifically, Hshieh concerns high on-resistance due to gate and source resistances:

> [0011] Another aspect of the present invention is to reduce the source-body resistance and gate resistance by forming buried trench-poly gate runner with a source-body trench contact and gate-runner trench contact that are further covered by a thin low-resistance layer with greater contact area to a top thick metal. …
>
> [0012] Another aspect of the present invention is to further reduce the gate resistance; an opening is formed in the source metal layer on top

> of a trenched gate contact plug disposed on top of a trench-poly gate runner. …

EX1006, ¶¶ [0011]-[0012]. EX1003, ¶ 151.

Thus, as Bulucea and Hsieh both relate to trench MOSFETs of a closed-cell configuration, and both being concerned with on-resistance of trenches MOSFETs, a POSITA is motivated to combine the teachings of Bulucea and Hsieh. EX1003, ¶ 152.

In this MOSFET, Hshieh discloses a *cylindrical shaped* source-body trench contact (i.e., a circular source-body trench contact) that penetrates both the source region into the encompassing body region:

> [0013] … In a preferred embodiment the MOSFET device further includes a source-body contact trench opened through the insulation layer into the source and body regions and filled with a source-body contact metal plug. … In a preferred embodiment, the gate and the source-body contact metal plugs filled in the gate contact trench and the source-body contact trench includes a substantially cylindrical shaped plug. …

EX1006, ¶ [0013]. EX1003, ¶ 153.

Thus, a POSITA would modify Bulucea's source/body contact by incorporating the cylindrical source-body trench contact. EX1003, ¶ 146.

Such a preferred embodiment is shown in Hshieh's Figs. 3A-3E and

discussed in ¶¶ [0027]-[0028]:

> [0027] Referring to FIGS. 3A to **3**D for an alternate MOSFET **100′** device of this invention. … The MOSFET device 100' is supported on a substrate 105 formed with an epitaxial layer 110. The MOSFET device 100 includes a trenched gate 120 disposed in a trench with a gate insulation layer 115 formed over the walls of the trench. A body region 125 that is doped with a dopant of second conductivity type, e.g., P-type dopant, extends between the trenched gates 120. The P-body regions 125 encompassing a source region 130 doped with the dopant of first conductivity, e.g., N+ dopant. …
>
> [0028] … Furthermore, for the purpose of improving source metal layer 140 to contact the source regions 130, a plurality of trenched source contact filled with a tungsten plug 180 is formed in the protective insulation layer 135. These tungsten plugs 180 are surrounded by a barrier layer Ti/TiN (not specifically shown). The contact trenches are opened through the NSG-BPSG protective layers 135 to contact the source regions 130 and the P-body 125.

EX1006, ¶¶ [0027]-[0028], Figs. 3A-3D. EX1003, ¶ 154.

For example, Fig. 3C shows:

Fig. 3C

EX1006, Fig. 3C. EX1003, ¶ 155.

Thus, the above teachings of Hshieh meets limitations [1b]-[1f], including limitations “said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact,” which is clearly seen in Hshieh’s Fig. 3C, for example. EX1003, ¶ 156. There, circular trench contact 180 is separate from said trenched gates 120 with said source region 130 and body region 125 disposed between a gate oxide lining 115 of said trenched gates 120 and all circumferential points of the circular trench contact 180.

EX1003, ¶ 157. Fig. 3C also indicates that trench contact 180 comprises a Ti/TiN/W plug, which meets recited limitations [3] of Claim 3 of the ‘409 Patent. EX1003, ¶ 157.

At ¶ [0013], Hshieh also teaches a titanium (Ti) resistance-reduction conductive layer:

> [0013] … In a preferred embodiment, the MOSFET device further includes a thin resistance-reduction conductive layer disposed on a top surface covering the insulation layer and contacting the gate contact metal plug and source-body contact plug … In a preferred embodiment, the thin resistance-reduction conductive layer includes a titanium (Ti) layer. In a preferred embodiment, the thin resistance-reduction conductive layer includes a titanium nitride (TiN) layer.

EX1006, ¶ [0013]. EX1003, ¶ 158.

This resistance-reduction conductive layer meets the recited limitations [2] of Claim 2. EX1003, ¶ 159.

In Figs. 5E1 and in ¶ [0031], Hshieh teaches:

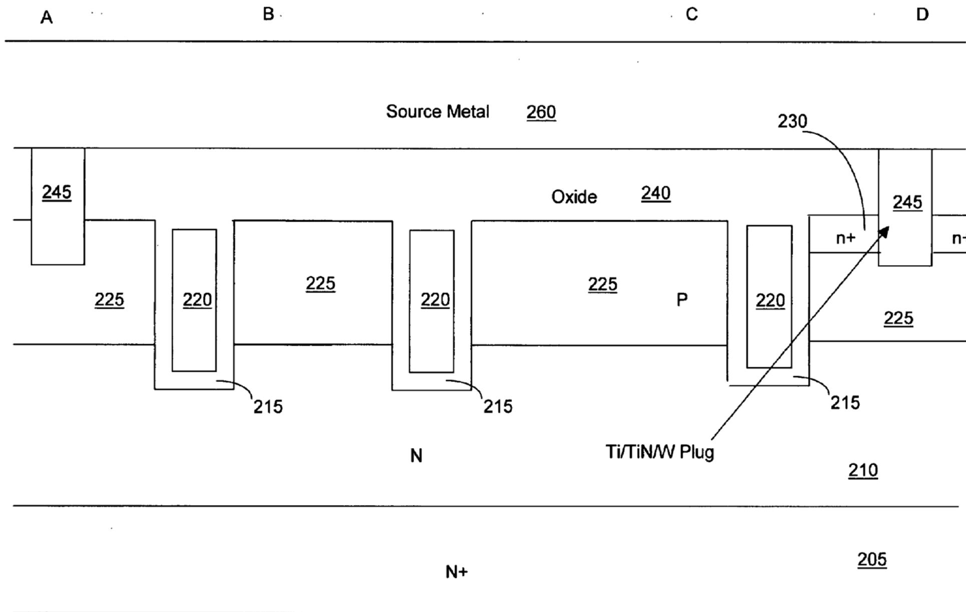


Fig. 5E-1

> [0031] … In FIGS. 5E-1 and **5**E-**2**, a low resistance metal layer **260** is deposited over the top surface. The low resistance metal layer may be composed of Ti/AlCu or Ti/TiN/AlCu to assure good electric contact is established followed by a metal etch to pattern the metal layer into a source metal pad **260** and a gate metal pads **270** in electrical contact with the source-body trench-plug **245** and the gate-runner trench plug **250** respectively.

EX1006, ¶ [0031]. EX1003, ¶ 160,

Hshieh's teachings in the above-quoted portion of ¶ [0031] meets recited limitations [4] of Claim 4. EX1003, ¶ 161.

In ¶ [0030], Hshieh teaches forming 0.4µm trench contact using chemical

vapor deposition (CVD):

> The tungsten plug is formed with the chemical vapor deposition (CVD) process and the chemical vapor has much better filling characteristics to fill the narrow and deep contact openings without development of void. The CVD process is suitable for process of circuits with critical dimension (CD) less than 0.4 micrometer (μms) in the semiconductor industries.

EX1006, ¶ [0030]. EX1003, ¶ 162.

Such a tungsten plug would meet recited limitations [5] of Claim 5 of the '409 Patent. EX1003, ¶ 163.

#### c) Combining the Relevant Teachings of Bulucea and Hshieh, Claims 1-5 are obvious under 35 U.S.C. ¶ 103

The following claim chart summarizes a combination of the relevant teachings of Bulucea and Hsieh, in which Bulucea's source/body contact is modified to incorporate Hsieh's source/body trench contact. EX1003, ¶ 197. The combination meets all limitations of and thus renders Claims 1-5 of the '409 Patent. Thus, each of these claims as a whole would have been obvious before the effective filing date of December 4, 2006 to a POSITA to which the claimed subject matter pertains. EX1003, ¶ 197.

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| [1pre] | 1.A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein | Bulucea teaches a trenched semiconductor power device formed by a group of transistor cells (square-cell geometry) in a semiconductor substrate.<br>See, EX1005, Fig. 21 and Fig. 31A, 3:14-18. |
| [1a] | said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners; | Bulucea teaches, in the semiconductor device of Fig. 21, trenched gates 29 surrounding the transistors cells as closed cells constituting substantially square-shaped cells with rounded corners. Fig.21, Fig. 31A. Bulucea teaches that the trenched gates surrounding the square closed unit cell becomes "substantially square-shaped cells with rounded corners" (i) by lithographical development (7:53-66), or (ii) by a sacrificial oxidation step (6:1-6. Fig. 25A, 12:38-51). |
| [1b] | each of said closed cells | Bulucea teaches that, using |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | further includes a circular trench contact disposed substantially in a central portion of said closed cells, | lithography development, a square feature can become circular (7:53-66); Bulucea shows a circular trench contact (Fig. 31A, portion of metallization layer 43B at the surface of the semiconductor surface, in contact with source region 28 and body region 27; 13:46-52).<br><br>Bulucea's teachings regarding latch-back free design (5:33-37) and the p+ deep body diffusion motivates a POSITA to modify Bulucea's circular contact to incorporate a circular trench contact, such as shown in Hshieh's cylindrical shaped source-body trench contact (i.e., a circular source-body trench contact) shown in Hshieh's Figs. 3A-3E, paragraphs [0027]-[0028]. |
| [1c] | penetrating through a source region surrounding said | Hshieh shows in Fig. 3C, for example, circular trench contact 180 |

| Reference Signals | Claim Limitations | Prior Art Teachings |
| --- | --- | --- |
| | trenched gates and extending into a body region encompassing said source region; | penetrating through source region 130 surrounding trenched gates 120 and extending into body region 125, which encompasses source region 130 (See, also, Hshieh's paragraph [0027]). |
| [1d] | said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug | Hshieh's Fig. 3C shows, for example, circular trench contact 180 comprises a hole opened from a top surface of the semiconductor substrate and is filled with a contact metal plug (Fig. 3C labels it as "Ti/TiN/W Plug"). See also, Hshieh's paragraphs [0027]-[0028]. |
| [1e] | wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a | Hshieh's Fig. 3C shows, for example, sidewalls of the hole (i.e., filled circular trench contact 180) are surrounded by and in contact source region 130 and body region 125 and circular trench contact 180 is separate from trenched gates 120 with source region 130 and body |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | gate oxide lining of said trenched gates and all circumferential points of the circular trench contact; and | region 125 disposed between gate oxide lining 115 of trenched gates 120 and all circumferential points (i.e., the circumference of a horizontal cross section) of circular trench contact 180; See also, Hshieh's paragraph [0027]. |
| [1f] | said contact metal plug connected to a source metal disposed on top of said circular trench contact. | Hshieh's Fig. 3C, for example, shows the contact metal plug in circular trench contact 180 connected to source metal 140 disposed on top of circular trench contact 180. See also, Hshieh's paragraph [0028]. |
| [2] | 2. The trenched semiconductor power device of claim 1 further comprising:<br>a contact resistance reduction metal layer composed of a titanium (Ti) layer disposed above a top surface said | In its paragraph [0013] Hshieh teaches,<br>"… In a preferred embodiment, the thin resistance-reduction conductive layer includes a titanium (Ti) layer. In a preferred embodiment, the thin resistance-reduction conductive layer includes a titanium nitride |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | contact metal plug and below a bottom surface of said source metal for reducing a contact resistance between said contact metal plug and said source metal. | (TiN) layer." Hshieh's Fig. 3C shows, for example, a contact resistance reduction metal layer 180 composed of a titanium (Ti) layer disposed above a top surface said contact metal plug and below a bottom surface of said source metal 140 for reducing a contact resistance between said contact metal plug and said source metal 140. |
| [3] | 3. The trenched semiconductor power device of claim 1 wherein:<br><br>said contact metal plug disposed in said hole of said circular trench contact further comprising a Ti/TiN/W metal plug. | Hshieh's Fig. 3C indicates that trench contact 180 comprises a Ti/TiN/W plug. See, also, Figs. 3F, 5D-1, 5E-1, 5D', and 5E'. |
| [4] | The trenched semiconductor power device of claim 1 wherein:<br><br>said source metal disposed | In paragraph [0031], Hshieh teaches:<br><br>"In FIGS. 5E-1 and 5E-2, a low resistance metal layer 260 is deposited over the top surface. The |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | on top of and in contact with a top surface of said metal plug further comprising a layer composed of aluminum alloys including alloys of AlCu or AlSiCu. | low resistance metal layer may be composed of Ti/AlCu or Ti/TiN/AlCu to assure good electric contact is established followed by a metal etch to pattern the metal layer into a source metal pad 260 and a gate metal pads 270 in electrical contact with the source-body trench-plug 245 and the gate-runner trench plug 250 respectively." |
| [5] | 5. The trenched semiconductor power device of claim 1 wherein:<br><br>a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer. | In ¶ [0030], Hshieh teaches forming 0.4μm trench contact using chemical vapor deposition (CVD):<br><br>"The tungsten plug is formed with the chemical vapor deposition (CVD) process and the chemical vapor has much better filling characteristics to fill the narrow and deep contact openings without development of void. The CVD process is suitable for process of circuits with critical dimension (CD) |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | | less than 0.4 micrometer (µms) in the semiconductor industries." |

EX1003, ¶ 197.

Accordingly, Claims 1-5 of the '409 Patent are obvious under 35 U.S.C. § 103 over Bulucea, in view of Hsieh. EX1003. ¶ 198.

### (3) GROUND 2: Claim 1 is obvious under 35 U.S.C. § 103 over Bulucea, in view of Uno

#### a) Relevant Teachings of Bulucea

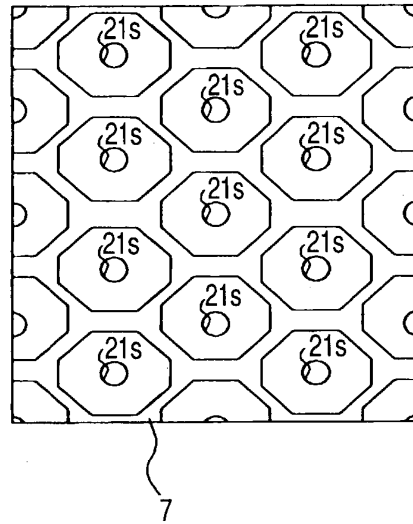
The relevant teachings of Bulucea is already provided in § IV.3(2)(a) above.

#### b) Relevant Teachings of Uno

Uno was issued on January 10, 2006 from a U.S. patent application, serial no. 10/463,771, that was filed on June 18, 2003 and that was published on January 22, 2004 as U.S. Patent Application Publication 2004/0012050 A1. Thus, Uno is available as prior art to the '409 patent as printed publication under both pre-AIA 35 U.S.C. ¶¶ 102(b) and 102(e)(1). EX1007, cover page.

Uno discloses a trench MOSFET and a method of manufacturing thereof in Figs. 1-11. EX1007, 4:51-62, Figs. 1-11. EX1003, ¶ 164. In particular, Uno discloses a circular trench contact in a MOSFET and a method of its formation. EX1007, 5:33-62, Figs. 6-9. EX1003, ¶ 164. Fig. 7 shows a plan-view for a portion of the trench MOSFET with numerous closed unit cells. EX1007, 3:4-6, Fig. 7. EX1003, ¶ 164.

Significantly, Fig. 7 shows circular trench contact 21s. EX1007, Fig. 7. EX1003, ¶ 164.




That contact trench 21s is circular is confirmed by the specification's reference to trench contact 21s' *diameter*:

> In FIG. 6 and FIG. 7, after forming a silicon oxide film 19 above the substrate 1, the substrate 1 ($p^-$-semiconductor region 15 and the $n^+$-semiconductor region 17) … is etched by using a not illustrated resist film as a mask to form contact trenches (Source contact) 21s. In this case, etching condition is controlled such that the *diameter* for the opening of the substrate 1 (17, 15) is smaller than the diameter for the opening of the Silicon oxide film.

EX1007, 5:33-42. EX1003, ¶ 165.

As to formation of circular trench contact 21s, Uno states:

> The $n^+$-semiconductor region **17** is exposed from the lateral

> wall of the contact trench **21** *s* and the $p^-$-semiconductor region **15** is exposed from the bottom thereof. In other words, the depth of the contact trench **21***s* exceeds the $n^+$-semiconductor region **17** and reaches as far as the $p^-$-semiconductor region **15**. …
>
> Then, as shown in FIG. 8, a p-impurity, for example, boron fluoride ($BF_2$) is implanted to the bottom of the contact trench **21***s* and diffused to form a $p^+$-semiconductor region (back gate contact region) **23**.

EX1007, 5:43-59. EX1003, ¶ 166.

As circular trench contact 21s reaches below silicon surface 31s to contact with $p^+$ contact dopant region 23 immediately underneath circular trench contact 21s, circular contact trench 21s is a Deep Body Trench Contact. EX1003, ¶ 167. Uno teaches that the Deep Body Trench Contact allows required mask alignment margins to be decreased:

> By forming the contact trench **21** *s* and disposing the $p^+$-semiconductor region **23** at the bottom thereof as described above, mask alignment margin can be decreased to refine the portion between the gates.

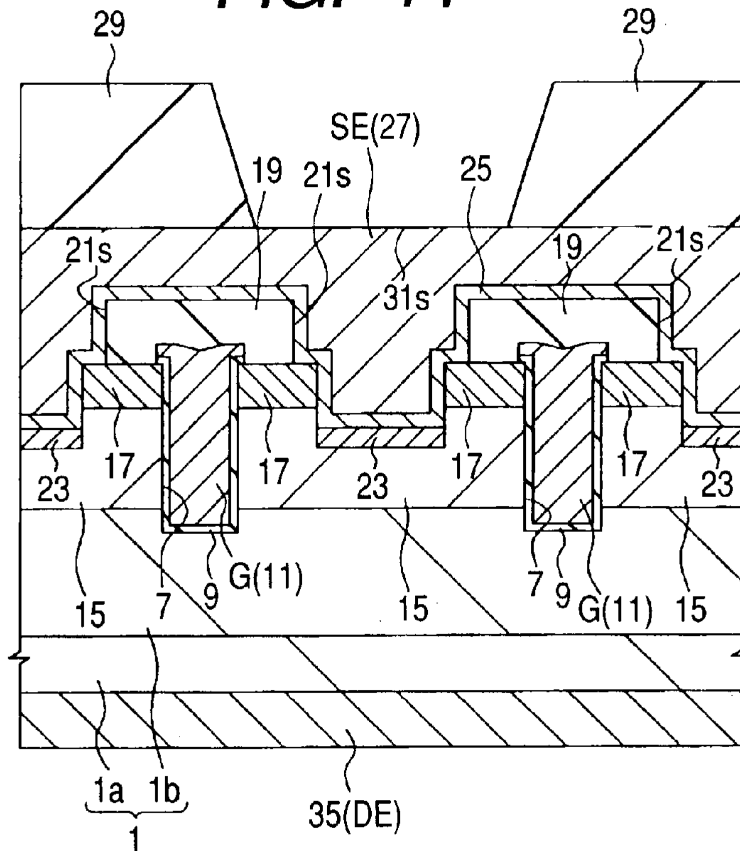
EX1007, 5:59-62. EX1003, ¶ 167.

Uno also discloses Bulucea's deep body diffusion approach in Fig. 12, showing that, when contact 21s contacts source region 17 and body region 15, $p^+$ dopant region 23 provides a low resistivity path between contact 21s and body

region 15. EX1003, ¶ 168.

Therefore, as Bulucea and Uno both relate to trench MOSFETs and, even more particularly, Uno discloses a Deep Body Trench Contact, a POSITA would be motivated to combine the teachings of Bulucea and Uno. EX1003, ¶ 169. The POSITA would modify Bulucea's source/body contact by incorporating Uno's circular source-body trench contact. EX1003, ¶ 146.

As shown in Uno's Fig. 11, circular trench contact 21s penetrates at a central portion of the cell through source region 17 surrounding trenched gates G(11) and extends into body region 15, which encompasses source region 17. EX1003, ¶ 170. Therefore, Uno meets limitations [1b] and [1c] in Claim 1 of the '409 Patent. EX1003, ¶ 170.




As shown also in Uno's Fig. 11, contact trench 21s is formed in a hole opened from a top surface 31s of the semiconductor substrate. EX1003, ¶ 171. Circular trench contact 21s is filled with a metal plug portion of source metal line SE (27). Sidewalls of circular trench contact 21s are surrounded by and in contact said source region 17 and body regions 15 and 23. EX1003, ¶ 171. Circular trench contact 21s is separate from trenched gates G(11) with source region 17 and body region 15 disposed between gate oxide lining 9 of trenched gates G(11) and all circumferential points of circular trench contact 21s (horizontal cross section).

EX1003, ¶ 171. The portion of source metal SE(27) that forms the contact metal plug in circular trench contact 21s is connected to source metal SE(27) disposed on top of circular trench contact 21s. EX1003, ¶ 171. Therefore, Uno's circular trench contact 21s meets limitations [1d], [1e] and [1f] in Claim 1 of the '409 Patent. EX1003, ¶ 171.

#### c) Combining the Relevant Teachings of Bulucea and Uno, Claim 1 is obvious under 35 U.S.C. ¶ 103

The following claim chart summarizes a combination of the relevant teachings of Bulucea and Uno, in which Bulucea's source/body contact is modified to incorporate Uno's source/body trench contact. EX1003, ¶ 199. The combination meets all limitations of and thus renders Claim 1 of the '409 Patent. Thus, Claim 1 as a whole would have been obvious before the effective filing date of December 4, 2006 to a POSITA to which the claimed subject matter pertains. EX1003, ¶ 199.

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| [1pre] | 1.A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of | Bulucea teaches a trenched semiconductor power device formed by a group of transistor cells (square-cell geometry) in a |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | transistor cells formed in a semiconductor substrate, wherein | semiconductor substrate.<br>See, EX1005, Fig. 21 and Fig. 31A, 3:14-18. |
| [1a] | said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners; | Bulucea teaches, in the semiconductor device of Fig. 21, trenched gates 29 surrounding the transistors cells as closed cells constituting substantially square-shaped cells with rounded corners. Fig.21, Fig. 31A. Bulucea teaches that the trenched gates surrounding the square closed unit cell becomes "substantially square-shaped cells with rounded corners" (i) by lithographical development (7:53-66), or (ii) by a sacrificial oxidation step (6:1-6. Fig. 25A, 12:38-51). |
| [1b] | each of said closed cells further includes a circular trench contact disposed substantially in a | Bulucea teaches that, using lithography development, a square feature can become |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | central portion of said closed cells, | circular (7:53-66); Bulucea shows a circular trench contact (Fig. 31A, portion of metallization layer 43B at the surface of the semiconductor surface, in contact with source region 28 and body region 27; 13:46-52).<br><br>Bulucea's teachings regarding latch-back free design (5:33-37) and the $p^+$ deep body diffusion motivates a POSITA to modify Bulucea's circular contact to incorporate a circular trench contact, such as that disclosed in Uno.<br><br>Uno also discloses Bulucea's deep body diffusion approach in Fig. 12, showing that, when contact 21s contacts source region 17 and body region 15, $p^+$ dopant region 23 provides a low |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | | resistivity path between contact 21s and body region 15. |
| [1c] | penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region; | As shown in Uno's Fig. 11, circular trench contact 21s penetrates at a central portion of the cell through source region 17 surrounding trenched gates G(11) and extends into body region 15, which encompasses source region 17. |
| [1d] | said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug | As shown in Uno's Fig. 11, circular contact trench 21s is formed in a hole opened from a top surface 31s of the semiconductor substrate.<br><br>Circular trench contact 21s is filled with a metal plug portion of source metal line SE (27). |
| [1e] | wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is | Sidewalls of the hole of circular contact trench 21s are surrounded by and in contact source region 17 and body |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact; and | regions 15 and 23.<br>Circular trench contact 21s is separate from trenched gates G(11) with source region 17 and body region 15 disposed between gate oxide lining 9 of trenched gates G(11) and all circumferential points of circular trench contact 21s (horizontal cross section). |
| [1f] | said contact metal plug connected to a source metal disposed on top of said circular trench contact. | In Uno's Fig. 11, the portion of source metal SE(27) that forms the contact metal plug in circular trench contact 21s is connected to source metal SE(27) disposed on top of circular trench contact 21s. |

EX1003, ¶ 199.

Accordingly, Claim 1 of the '409 Patent are obvious under 35 U.S.C. § 103 over Bulucea, in view of Uno. EX1003. ¶ 200.

### (4) GROUND 3: Claim 1 is obvious under 35 U.S.C. § 103 over Bulucea, in view of Huang

#### a) Relevant Teachings of Bulucea

The relevant teachings of Bulucea is already provided in section IV.3(2)(a) above.

#### b) Relevant Teachings of Huang

Huang was issued on March 14, 2000 from a U.S. patent application, serial no. 08/885,992, that was filed on June 30, 1997. Thus, Huang is available as prior art to the '409 patent as both patent and printed publication under pre-AIA 35 U.S.C. ¶ 102(b). EX1008, cover page.

Huang discloses a trench MOSFET and a method of manufacturing thereof in Figs. 1-9 and 11. EX1008, 1:44-45, 49-50, Figs. 1-9, 11. EX1003, ¶ 172. In particular, Huang discloses trench contact 34 in a MOSFET and a method of its formation. EX1008, 2:31-46, Figs. 8-9. EX1003, ¶ 172.

Huang's Figs. 8-9 show trench contact 34 being provided above where $p^+$ deep body diffusion 35 is implanted; $p^+$ deep body diffusion 35 is contacted by metal layer 36 in trench contact 34:

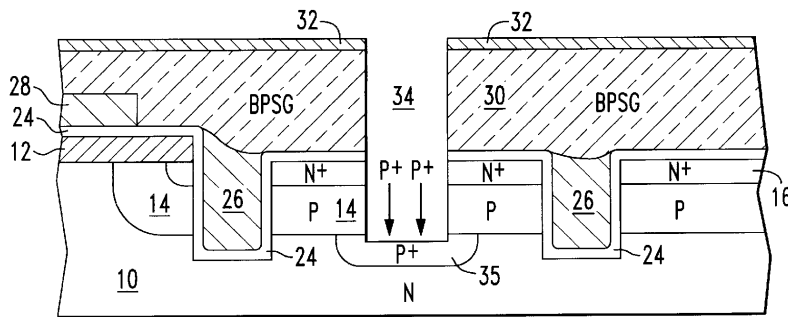



FIG. 8

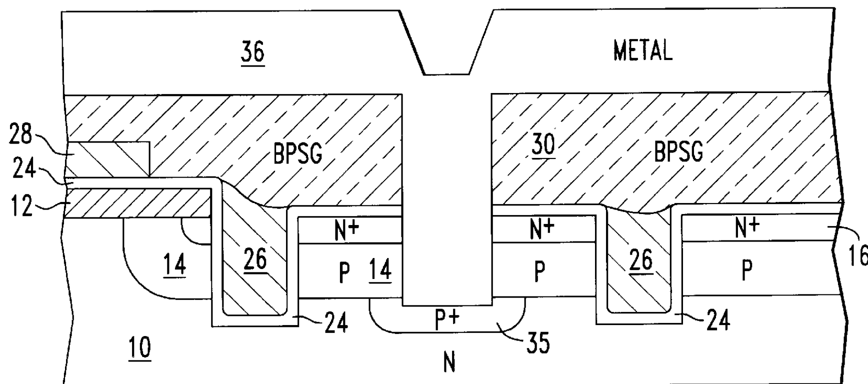



FIG. 9

EX1008, Figs. 8 and 9. EX1003, ¶ 173.

With respect to formation of trench contact 34, Huang states:

> … as shown in FIG. 8, a fourth mask 32 may be conventionally formed over the BPSG layer 30 to thereby define [an] area for a third trench 34 which may be etched through the BPSG layer 30, the gate oxide 24, the N+ source 16, and the P channel area 14 into the N semiconductor 10. Once the trench 34 has been etched, a P type impurity may be implanted and driven into the N wafer to thereby form a P+ area 35 of higher impurity concentration than the P channel

> region 14.
>
> As illustrated in FIG. 9, a metal layer 36 may then be formed over both the BPSG area 30 to thereby establish a contact with the N+ source region and the P+ high concentration region 35 at the bottom of the trench 34 of FIG. 8.

EX1008, 5:33-46. EX1003, ¶ 174.

Thus, as seen from Fig. 8, as trench contact 34 reaches below the silicon surface to contact with buried layer 35 (i.e., $p^+$ contact dopant region) immediately underneath trench contact 34, trench contact 34 is a Deep Body Trench Contact. EX1003, ¶ 175. Note that Huang states that its buried layer 35 makes "it possible for the MOSFET to break down at the PN junction 35 and protect the trench gate 26." EX1008, 3:4-7. This effect, which moves surface breakdowns from the trench gates to underneath the contact in the bulk silicon, is disclosed by Bulucea at EX1005, 7:11-28. EX1003, ¶ 176.

Therefore, as Bulucea and Huang both relate to trench MOSFETs and, even more particularly, Huang discloses a Deep Body Trench Contact, a POSITA would be motivated to combine the teachings of Bulucea and Huang. EX1003, ¶ 177. The POSITA would modify Bulucea's source/body contact by incorporating Huang's source-body trench contact. EX1003, ¶ 146.

As shown in Huang's Fig. 9, trench contact 34 penetrates at a central portion of the cell through source region 16 surrounding trenched gates 26 and extends into body region 14, which encompasses source region 16. EX1003, ¶ 178. Trench contact 34 is formed in a hole opened from the top surface of the semiconductor substrate. EX1003, ¶ 179. Trench contact 34 is filled with a metal plug portion of source metal line 36, wherein sidewalls of the hole are surrounded by and in contact said source region 16 and body regions 14. EX1003, ¶¶ 180-181. Trench contact 34 is separate from trenched gates 26 with source region 16 and body region 14 disposed between gate oxide lining 24 of trenched gates 26 and all points of trench contact 34 (horizontal cross section). EX1003, ¶ 180. Fig. 9 also shows trench contact 34 is provided contact metal plug as a portion of metal layer 36 and is thus connected to the portion of metal 36 that is disposed on top of trench contact 34. EX1003, ¶ 181.

While Huang does not disclose that its trench contact is circular, in view that Bulucea teaches that such a polygon feature in a horizontal cross section would become substantially a circle or an oval using the Litho-rounding Technique, the combined teachings would render trench contact 34 circular, and all the points in a horizontal cross section of trench contact 34 would become "circumferential." EX1003, ¶ 182. Accordingly, applying the Litho-rounding Technique to Huang's

trench contact, Huang meets all limitations [1c]-[1f] in Claim 1 in the ’409 Patent. EX1003, ¶ 182.

#### c) Combining the Relevant Teachings of Bulucea and Huang, Claim 1 is obvious under 35 U.S.C. ¶ 103

The following claim chart summarizes a combination of the relevant teachings of Bulucea and Huang, in which Bulucea’s source/body contact is modified to incorporate Huang’s source/body trench contact. EX1003, ¶ 201. The combination meets all limitations of and thus renders Claim 1 of the ‘409 Patent. Thus, Claim 1 as a whole would have been obvious before the effective filing date of December 4, 2006 to a POSITA to which the claimed subject matter pertains. EX1003, ¶ 201.

| Reference Signals | Claim Limitations | Prior Art Teachings |
| --- | --- | --- |
| [1pre] | 1.A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein | Bulucea teaches a trenched semiconductor power device formed by a group of transistor cells (square-cell geometry) in a semiconductor substrate.<br>See, EX1005, Fig. 21 and Fig. 31A, 3:14-18. |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| [1a] | said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners; | Bulucea teaches, in the semiconductor device of Fig. 21, trenched gates 29 surrounding the transistors cells as closed cells constituting substantially square-shaped cells with rounded corners. Fig.21, Fig. 31A. Bulucea teaches that the trenched gates surrounding the square closed unit cell becomes "substantially square-shaped cells with rounded corners" (i) by lithographical development (7:53-66), or (ii) by a sacrificial oxidation step (6:1-6. Fig. 25A, 12:38-51). |
| [1b] | each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, | Bulucea teaches that, using lithography development, a square feature can become circular (7:53-66); Bulucea shows a circular trench contact (Fig. 31A, portion of metallization layer 43B at the surface of the semiconductor |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | | surface, in contact with source region 28 and body region 27; 13:46-52).<br><br>Bulucea's teachings regarding latch-back free design (5:33-37) and the $p^+$ deep body diffusion motivates a POSITA to modify Bulucea's circular contact to incorporate a trench contact, such as shown in Huang's Figs. 8-9. Figs. 8-9 show trench contact 34 being provided above where p+ deep body diffusion 35 is implanted; $p^+$ deep body diffusion 35 is contacted by metal layer 36 in trench contact 34. |
| [1c] | penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region; | As shown in Huang's Fig. 9, trench contact 34 penetrates at a central portion of the cell through source region 16 surrounding trenched gates 26 and extends into body region 14, which |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | | encompasses source region 16. |
| [1d] | said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug | Trench contact 34 is formed in a hole opened from the top surface of the semiconductor substrate.<br><br>Trench contact 34 is filled with a metal plug portion of source metal line 36. |
| [1e] | wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact; and | The sidewalls of the hole filled by the contact metal plug of trench contact 34 are surrounded by and in contact source region 16 and body region 14. Trench contact 34 is separate from trenched gates 26 with source region 16 and body region 14 disposed between gate oxide lining 24 of trenched gates 26 and all points of trench contact 34 (horizontal cross section).<br><br>(While Huang does not disclose that its trench contact is circular, in view that Bulucea teaches that such a polygon feature in a |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | | horizontal cross section would become substantially a circle or an oval using lithographical development, the combined teachings would render trench contact 34 circular, and all the points in a horizontal cross section of trench contact 34 would become "circumferential." |
| [1f] | said contact metal plug connected to a source metal disposed on top of said circular trench contact. | Fig. 9 also shows trench contact 34 is provided contact metal plug as a portion of metal layer 36 and is thus connected to the portion of metal 36 that is disposed on top of trench contact 34. |

EX1003, ¶ 201.

Accordingly, Claim 1 of the '409 Patent is obvious under 35 U.S.C. § 103 over Bulucea, in view of Huang. EX1003. ¶ 202.

### (5) GROUND 4: The Challenged Claims are obvious under 35 U.S.C. § 103 over Bulucea, in view of Bhalla

#### a) Relevant Teachings of Bulucea

The relevant teachings of Bulucea is already provided in section IV.3(2)(a) above.

#### b) Relevant Teachings of Bhalla

Bhalla was issued on October 23, 2007 from a U.S. patent application, serial no. 11/056,346, that was filed on February 11, 2005 and published as U.S. Patent Application Publication 2006/0180855 A1 on August 17, 2006. Thus, Bhalla is available as prior art to the '409 patent as printed publication under pre-AIA 35 U.S.C. ¶ 102(e)(1). EX1007, cover page.

Bhalla discloses a double-diffuse MOSFET (DMOS device) and a method of manufacturing thereof. EX1009, 4:42-6:19 and 6:57-67, Figs. 3A-3P and Fig.7. EX1003, ¶ 183. In particular, Bhalla discloses etching trench contacts 624 and 626 (Fig. 3N) and trench contact 625 (Fig. 7) in a trench MOSFET and a method of its formation. EX1009, 5:64-6:19, 57-67, Figs. 3N, 7, 3N-3P. EX1003, ¶ 183.

As shown in Fig. 3N, trench contact 624 reaches from the surface of the silicon substrate, through source region 612 ($N^+$) and body region 460 (P). EX1009, Fig. 3N. EX1003, ¶ 184.

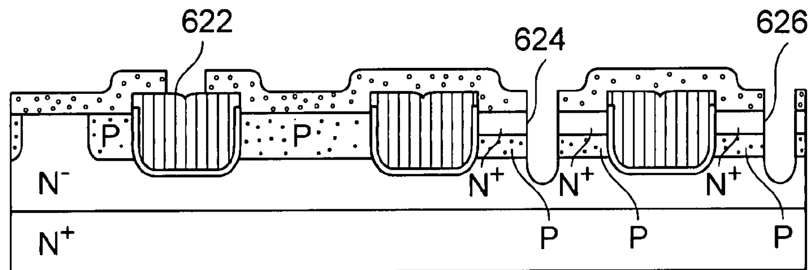



**FIG. 3N**

Alternatively, as Bhalla describes at 6:58-62, in conjunction with Fig. 7, trench contact etch can be followed by forming p+ deep body diffusion region 607 at the bottom of contact trench 625:

> … contact trench etch process is performed on a structure similar to **340** of FIG. 3M to form device **700**. After etch mask **614** is formed on the structure, contact trench etch is performed to form trench **625**. The depth of the trench may vary for different implementations. In the example shown, the bottom of trench **625** is controlled to be substantially coplanar to the source bottom. $P^+$-type material is implanted to the bottom of the trench and then activated to form $P^+$ region **607**.

EX1009, 6:58-62. EX1003, ¶ 185.

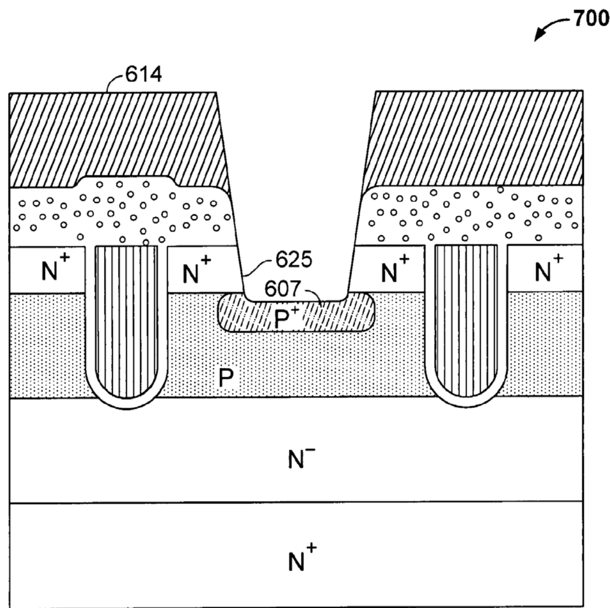



FIG. 7

EX1009, Fig. 7. EX1003, ¶ 185.

Thus, as seen from Bhalla's Figs. 3N and 7, as trench contact 625 reaches below the silicon surface to contact with $p^+$ contact dopant region 607 immediately underneath trench contact 625, trench contact 625 is a Deep Body Trench Contact. EX1003, ¶ 186.

Therefore, as Bulucea and Bhalla both relate to trench MOSFETs and, even more particularly, Bhalla discloses a Deep Body Trench Contact, a POSITA would be motivated to combine the teachings of Bulucea and Bhalla. EX1003, ¶ 187. The POSITA would modify Bulucea's source/body contact by incorporating Bhalla's source-body trench contact. EX1003, ¶ 146.

Bhalla teaches a circular trench contact to avoid breakdown due to high electric field, in conjunction with its description of the trench contact 624 in Fig. 3N:

> Since the trench such as **624** serve as contact openings where the metal and the semiconductor meet, sharp curvature in corner regions may lead to high electric fields and degrade device breakdown. In device **350** shown, *the trenches have round and smooth shapes without sharp corners,* thus avoiding low breakdowns due to high electric fields.

EX1009, 6:13-19. EX1003, ¶ 188.

Bhalla's Fig. 3P teaches providing a metal stack above, as well as filling, circular trench contact 624. EX1003, ¶ 189.

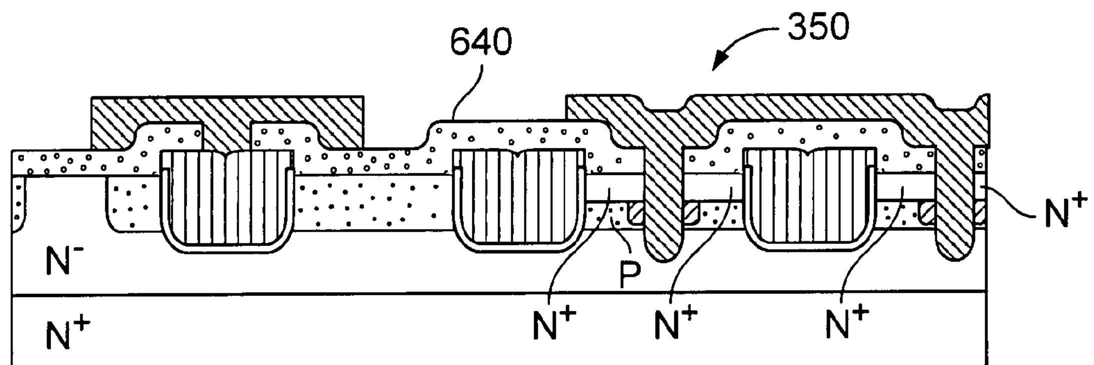



**FIG. 3P**

As seen in Bhalla's Fig. 3P, contact trench 624 penetrates at a central position in between gate trenches 442 through source region 612 surrounding said trenched gates 442 and extending into a body region (460,630) encompassing said source region 612. EX1003, ¶ 190. Thus, Bhalla meets limitations [1b], [1c] and [1d] of the '409 Patent. EX1003, ¶ 190.

As shown in Figs. 3N-3P and described in Bhalla's 6:1-19, contact trench 624 comprises a hole opened from a top surface of the semiconductor substrate substantially in a central position between gate trenches 442. EX1003, ¶ 191. Fig. 3P shows contact trench 624 is filled with a contact metal plug, being the portion of a metal stack filling the entire circular trench contact, consisting of Ti, TiN and Al-Si-Cu, wherein the sidewalls of the hole are surrounded by and in contact with source region 612 and body regions 460 and 630. EX1003, ¶ 192. Circular trench contact 624 separates from trenched gates 442 with source region 612 and body region 460 and 630 disposed between a gate oxide lining 432 of trenched gates 442 and all circumferential points of circular trench contact 624. EX1003, ¶ 192. The contact metal plug in trench 624 is connected by the same metal stack disposed on top of the circular trench contact. Thus, Bhalla's circular trench contact 624 meets limitations [1e] and [1f] in Claim 1 of the '409 Patent. EX1003, ¶ 193.

In addition to teaching Ti, TiN, and Al-Si-Cu in a metal stack for the metal

plug and the metal layer on top (EX1009, 6:10-12), Bhalla also teaches using palladium, platinum, titanium and tungsten in trench contacts:

> A layer of metal suitable for making Schottky contact with the lightly doped drain (such as titanium (Ti), platinum (Pt), palladium (Pd), tungsten (W) or any other appropriate material) is deposited on the bottom of source body contact trenches 112, 114 and 116, to form contact electrodes 122, 124 and 126, respectively.

EX1009, 3:58-63. EX1003, ¶ 194.

Thus, Bhalla's trench MOSFET also meets recited limitations [3]-[4] in Claims 3-4 of the '409 Patent. EX1003, ¶ 195.

Also, Bhalla teaches that its circular trench contact can be "approximately between 0.5-2.5 μm deep and approximately between 0.2-1.5 μm wide in some embodiments." EX1009, 5:5-7. Thus, Bhalla also meets the recited limitations [5] of the '409 Patent. EX1003, ¶ 196.

#### c) Combining the Relevant Teachings of Bulucea and Bhalla, Claims 1, 3-5 are obvious under 35 U.S.C. ¶ 103

The following claim chart summarizes a combination of the relevant teachings of Bulucea and Bhalla, in which Bulucea's source/body contact is modified to incorporate Bhalla's source/body trench contact. EX1003, ¶ 203. The combination meets all limitations of and thus renders Claims 1 and 3-5 of the '409

Patent. Thus, each of these claims as a whole would have been obvious before the effective filing date of December 4, 2006 to a POSITA to which the claimed subject matter pertains. EX1003, ¶ 203.

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| [1pre] | 1.A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein | Bulucea teaches a trenched semiconductor power device formed by a group of transistor cells (square-cell geometry) in a semiconductor substrate.<br>See, EX1005, Fig. 21 and Fig. 31A, 3:14-18. |
| [1a] | said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners; | Bulucea teaches, in the semiconductor device of Fig. 21, trenched gates 29 surrounding the transistors cells as closed cells constituting substantially square-shaped cells with rounded corners. Fig.21, Fig. 31A. Bulucea teaches that the trenched gates surrounding the square |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | | closed unit cell becomes "substantially square-shaped cells with rounded corners" (i) by lithographical development (7:53-66), or (ii) by a sacrificial oxidation step (6:1-6. Fig. 25A, 12:38-51).<br><br>. |
| [1b] | each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, | Bulucea teaches that, using lithography development, a square feature can become circular (7:53-66); Bulucea shows a circular trench contact (Fig. 31A, portion of metallization layer 43B at the surface of the semiconductor surface, in contact with source region 28 and body region 27; 13:46-52).<br><br>Bulucea's teachings regarding latch-back free design (5:33-37) and the $p^+$ deep body diffusion |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | | motivates a POSITA to modify Bulucea's circular contact to incorporate a circular trench contact, such as shown in Bhalla, which describes at 6:58-62, in conjunction with Fig. 7, trench contact etch can be followed by forming p+ deep body diffusion region 607 at the bottom of contact trench 625. |
| [1c] | penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region; | Bhalla teaches a circular trench contact to avoid breakdown due to high electric field, in conjunction with its description of the trench contact 624 in Figs. 3N-3P. Specifically, Bhalla teaches device **350** in Fig, 3P, which shows *the trenches have round and smooth shapes without sharp corners,* thus avoiding low breakdowns due to high electric fields." EX1009, |

| Reference Signals | Claim Limitations | Prior Art Teachings |
| --- | --- | --- |
| | | 6:13-19.<br><br>As seen in Bhalla's Fig. 3P, contact trench 624 penetrates at a central position in between gate trenches 442 through source region 612 surrounding said trenched gates 442 and extending into a body region (460,630) encompassing said source region 612. |
| [1d] | said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug | As shown in Figs. 3N-3P and described in Bhalla's 6:1-19, circular trench contact 624 comprises a hole opened from a top surface of the semiconductor substrate substantially in a central position between gate trenches 442.<br><br>Fig. 3P shows circular trench contact 624 is filled with a contact metal plug, being the portion of a metal stack filling |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | | the entire circular trench contact, consisting of Ti, TiN and Al-Si-Cu. |
| [1e] | wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact; and | The sidewalls of the hole that is filled by the contact metal plug of circular trench contact 624 are surrounded by and in contact with source region 612 and body regions 460 and 630.<br><br>Circular trench contact 624 separates from trenched gates 442 with source region 612 and body region 460 and 630 disposed between a gate oxide lining 432 of trenched gates 442 and all circumferential points of circular trench contact 624. |
| [1f] | said contact metal plug connected to a source metal disposed on top of said circular trench contact. | The contact metal plug in trench 624 is connected by the same metal stack disposed on top of the circular trench contact. |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| [3] | 3. The trenched semiconductor power device of claim 1 wherein:<br>said contact metal plug disposed in said hole of said circular trench contact further comprising a Ti/TiN/W metal plug. | Bhalla teaches having Ti, TiN, and Al-Si-Cu in a metal stack for the contact metal plug and the metal layer on top (EX1009, 6:10-12). Bhalla also teaches using palladium, platinum, titanium and tungsten in trench contacts. EX1009, 3:58-63. Thus, Bhalla teaches having Ti, TiN and W in a contact metal plug. |
| [4] | The trenched semiconductor power device of claim 1 wherein:<br>said source metal disposed on top of and in contact with a top surface of said metal plug further comprising a layer composed of aluminum alloys including alloys of AlCu or AlSiCu. | Bhalla teaches Ti, TiN, and Al-Si-Cu in a metal stack for the contact metal plug and the metal layer on top (EX1009, 6:10-12). |
| [5] | 5. The trenched semiconductor power device of claim | Bhalla teaches that its circular trench contact can be |

| Reference Signals | Claim Limitations | Prior Art Teachings |
|---|---|---|
| | 1 wherein:<br>a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer. | "approximately between 0.5-2.5 µm deep and approximately between 0.2-1.5 µm wide in some embodiments." EX1009, 5:5-7. |

EX1003, ¶ 203.

Accordingly, Claims 1 and 3-5 of the '409 Patent are obvious under 35 U.S.C. § 103 over Bulucea, in view of Bhalla. EX1003. ¶ 204.

# V. PTAB DISCRETION SHOULD NOT PRECLUDE INSTITUTION

### 1. 35 U.S.C. § 325(d)—*Advanced Bionics*

None of the prior references presented herein were considered by the Examiner during the prosecution of the '409 Patent. None of the prior art references presented herein is presented in the existing *Inter Partes Review* (IPR) No. IPR2024-00094. As the Petitioner participated in neither prosecution of the '409 Patent, nor the existing IPR, the arguments presented herein have been made during neither the prosecution of the '409 Patent nor the existing IPR. Thus, *Advanced Bionics* and the *Becton* factors strongly favor institution. *Advanced Bionics LLC v. MED-EL Elektromedizinische Gerate GmbH*, IPR2019- 01469, Paper 6, at 7-10 (PTAB Feb. 13, 2020) ("*Advanced Bionics*") (precedential); *Becton, Dickinson and Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8, at 17–18 (§ III.C.5, first paragraph). (PTAB Dec. 15, 2017) ("*Becton*") (precedential).

### 2. 35 U.S.C. § 314(a)—*Fintiv*

The '409 Patent is involved in co-pending IPR, IPR2024-00094, and in co-pending civil action, *Force Mos Technology Co., Ltd. v. ASUSTeK Computer, Inc.,* 2:22-cv-00460, (E.D. Tex.). A Written Opinion is expected in the co-pending IPR ahead of the target institution date of Petitioner's petition. The co-pending civil

action is currently in the post-trial stage. Petitioner is a party to neither co-pending proceeding. Petitioner sees no overlap between issues raised herein and either of the co-pending proceedings. Thus, none of *Fintiv* factors 1-5 favor exercise of discretion to deny institution of this requested IPR. As the merits in this Petition is believed to heavily favor Petitioner's prevailing, *Fintiv* factor 6 strongly supports institution. *Apple Inc. v, Fintiv, Inc.*, IPR2020-00019, Paper 11, at 5-16 (PTAB Mar. 20, 2020) ("*Fintiv*") (precedential).

#### 3. *General Plastic* Factors Favor Institution—35 U.S.C. § 314(a)

This Petition is Petitioner's first petition directed to the '409 Patent. Thus, Petitioner believes that the *General Plastic* factors are not applicable to this petition. *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, Case IPR2016-01357, Paper 19, at 15-19 (PTAB September 6, 2017) ("*General Plastic*") (presidential).

## 4. CONCLUSION

The instant Petition compellingly demonstrates the obviousness of the Challenged Claims. Accordingly, uPI respectfully requests institution.

Dated: April 24, 2025

Respectfully submitted,

/Edward C. Kwok/

*Lead Counsel for Petitioner*

IPR2025-00920

## VI. PAYMENT OF FEES – 37 C.F.R. § 42.103

uPI authorizes the Patent and Trademark Office to charge Deposit Account No. 606886 for the fee set in 37 C.F.R. § 42.15(a) for this Petition and further authorizes payment for any additional fees to be charged to this Deposit Account.

Dated: April 24, 2025

Respectfully submitted,

/Edward C. Kwok/

*Lead Counsel for Petitioner*

IPR2025-00920

# VII. MANDATORY NOTICES—37 C.F.R § 42.8(a)(1)

## 1. Real Party-In-Interest—37 C.F.R. § 42.8(b)(1)

Petitioner, uPI Semiconductor Corporation, is the real party-in-interest.

## 2. Related Matters—37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers or reexamination certificates for the '409 Patent. The '409 Patent is the subject of ongoing *inter partes* review petition IPR2024-00094 filed by Inergy on October 17, 2023.

The '409 Patent is also the subject of litigation in the following district court proceedings:

1. Force Mos Technology Co., Ltd. v. ASUSTeK Computer, Inc., 2:22-cv-00460, (E.D. Tex.)

### 3. Lead And Back-Up Counsel—37 C.F.R. § 42.8(b)(3)

Petitioner designates the following counsels:

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### 4. Service Information

Please address all correspondence and service to the following Lead Counsel's address:

Edward C, Kwok, Reg. No. 33,938
VLP Law Group LLP
19900 Price Ave
Cupertino, CA 95014

Petitioner consents to electronic service by email at the email address IPR02985-004@vlplawgroup.com of Lead Counsel, copying Backup Counsel at steven.chen@wbd-us.com.

Dated: April 24, 2025

Respectfully submitted,

/Edward C. Kwok/

*Lead Counsel for Petitioner*

IPR2025-00920

## VIII. CERTIFICATION UNDER 37 C.F.R. § 42.24

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 12,308 words, which is less than the 14,000 allowed under 37 C.F.R. § 42.24.

Dated: April 24, 2025

Respectfully submitted,

___/Edward C. Kwok/________

*Lead Counsel for Petitioner*

IPR2025-00920

## IX. CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on April 24, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express to the Patent Owner by serving the correspondence address of record as follows:

**35161 - Dickinson Wright PLLC - Washington DC**
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Respectfully submitted,

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