



Peter S. Gwozdz

Home Page

Engineering Professor, retired, and

Semiconductor Industry Consultant, self employed, semi - retired

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**uPI Semiconductor
Corp. Exhibit 1004**

Biography

Dr. Peter S. Gwozdz is a technologist in the field of semiconductor wafer fabrication. He has been continuously active in "Silicon Valley" since 1973. Gwozdz has been a part time industry consultant since 1988.

In the [College of Engineering](#) at [San Jose State University](#) (SJSU), 1988 - 2003, Professor Gwozdz taught courses part time in the field of Integrated Circuit (IC) Processing, in the departments of General Engineering, Materials Engineering, and Electrical Engineering.

Also at SJSU, Gwozdz was the Director of the Center for Electronic Materials and Devices. Peter developed and managed the IC Labs through the Center.

In addition, Dr. Gwozdz held more than 100 sessions of a three day [laboratory short course](#) on microfabrication in the IC Labs at SJSU. The short course was attended by industry professionals from all over the world. SEMI also sponsored a version of this [short course](#), taught by Gwozdz, at the SEMICON conventions held in San Francisco, San Jose, Austin, Boston, Munich, and Singapore. Gwozdz also did this course in-house for industry companies. Participants received Gwozdz's course materials, "Semiconductor Processing Technology", both in notebook format and in CD Power Point format. The course was also available from SemiZone.com, 2002 - 2009, in streaming web format.

Before joining SJSU in September, 1988, Gwozdz spent fifteen years in the local "Silicon Valley" semiconductor industry, including eight years at [Advanced Micro Devices](#), where he was a Director of technology development.

Peter's Ph.D. in Physics, from the University of Illinois, was on defects in Silicon, 1973.

Pete's hobby is [Polish genealogy](#).

Brief Resume. Dr. Peter S. Gwozdz

8/88 to Present; Independent Industry Consultant

Expert Witness, Technical Consultation. Semiconductor Processing for IC.

8/88 to 9/08; Short Course Instructor

Semiconductor Processing Technology. At SJSU, at SEMI Conventions, at companies, on the web.

8/88 to 1/03; San Jose State University. San Jose, CA 95192

Director, Center for Electronic Materials and Devices.
Developed and managed the Integrated Circuits Laboratories.
Professor. Materials Engineering.

1/80 to 7/88; Advanced Micro Devices (AMD). 915 DeGuigne, Sunnyvale, CA 94086

Directed Fab 9, a pilot line wafer fab for next generation high speed logic technology.

5/76 to 12/79; Wafer Fab Start Up Projects.

2/73 to 4/76; National Semiconductor. Santa Clara CA

9/66 to 1/73; University of Illinois. Urbana IL

MS & PhD in Physics, thesis topic - defects in silicon.

Publications. Dr. Peter S. Gwozdz

The Y-DNA of the alleged Copernicus remains is haplogroup R1b1b2a1
pages 127-157 of “The Nicolaus Copernicus grave mystery”, Polish Academy of Arts and Sciences, Edited by Michał Kokowski, Krakow, 22-23 February 2010. [Online Link](#)

Y-STR Mountains in Haplopace
Journal of Genetic Genealogy 5(2), [127-185 \(2009\)](#)

Semiconductor Processing Technology
Book for use in a 3 day short course. 416 pages. Available in electronic and notebook format. Continuously updated 1994 - 2008.

NSF Microfabrication Laboratory Workshops
Peter S. Gwozdz. IEEE Transactions on Education 39, 211 (1996)

Semiconductor Manufacturing Education at San Jose State University
Peter S. Gwozdz. IEEE Transactions on Semiconductor Manufacturing 5, 153 (1992)

Semiconductor Manufacturing Education at San Jose State University
Peter S. Gwozdz. ISMSS 91 Proceedings, IEEE Service Center, Piscataway, N.J. This is an invited paper that was presented at the Third International Semiconductor Manufacturing Science Symposium (ISMSS), which was held in conjunction with SEMICON WEST, the semiconductor annual trade show. The paper was also published in the IEEE Transactions on Semiconductor Manufacturing, above.

Yield Modeling on Your Personal Computer
Peter S. Gwozdz. Semiconductor International, p. 98, August, 1990

Denser Process Gets the Most out of Bipolar VLSI
Phil Downing, Pete Gwozdz, Bernie New. Electronics, June 28, 1984, p. 131
Also translated into the following journals:
Elettronica Domani 6/85, p. 93. Italian
Der Elektroniker Nr 1/1985, p. 75. German
New Electronics, 19 February 1985. British

Aluminum Intrusions or "Rat Bites"

Peter S. Gwozdz and H.M. Bath

1983 Electrochem Soc Meeting, San Francisco, CA. Extended Abstracts, p.682.

Positive vs Negative: a Photoresist Analysis

Peter S. Gwozdz. 1981 SPIE Meeting, San Jose, Develop. in Semic. Microlith. 275, 156 (1981)

Empirical Statistics for Yield Map Analysis

P.S. Gwozdz, 1978 SPIE Meeting, San Jose, Develop. in Semicond. Microlith. 135, 160 (1978)

An Analysis of Diffusion Process Control

P.S. Gwozdz, Solid State Technology, p. 71 (November 1977)

Electron Irradiation of Gold Below 2 K

P.S. Gwozdz & J.S. Koehler, Phys Rev B8, 3616 (1973)

Electron Irradiation and Annealing of Gold

P.S. Gwozdz & J.S. Koehler, Bull Amer Phys Soc 18, 479 (1973)

Changes in A-C Conductivity of Silicon with Electron Irradiation at 0.5 K.

P.S. Gwozdz & J.S. Koehler, Phys Rev B6, 4571, (1972)

Changes in A-C Conductivity of Silicon with Electron Irradiation at 0.5 K.

P.S. Gwozdz & J.S. Koehler, Bull Amer Phys Soc 17, 307 (1972)

A Simple Ion Source for Implantation Doping of Semiconductors

P.S. Gwozdz & J.S. Koehler Rev Sci Instr 41, 1677 (1970)

The Effect of Surface Treatment on Resonant Raman Scattering in CdS

P.J. Colwell, P.S. Gwozdz, & M.V. Klein. Tenth International Conf. on the Physics of Semiconductors, Cambridge, Mass. Aug 1970

High Conductivity Cu-Implanted CdS

P.S. Gwozdz & J.S. Koehler, Bull Amer Phys Soc 15, 397 (1970)

Hot Electron Effect in GaAs

R. Crandall & P.S. Gwozdz, Bull Amer Phys Soc 13, 407 (1968)

Patents. Dr. Peter S. Gwozdz

Method for Interconnecting Metallic Layers

Peter S. Gwozdz

US Patent # 4,451,326. Issued May 29, 1984

Process for dual and 3-layer aluminum interconnect. I developed this process for the 29116 microcontroller. I later extended this process for the 29300 family. This process has since been extended to all AMD IMOX Bipolar multilayer interconnect, manufactured in San Antonio, Texas.

Method of Making Integrated Bipolar Semiconductor Device By First Forming Junction Isolation Regions and Recessed Oxide Isolation Regions Without Birds Beak

Peter S. Gwozdz, Christopher Schmidt, Bill Price

US Patent # 4,622,738. Issued November 18, 1986

This is the patent on the device structure for the transistor used in the 29300 series of chips. 1.5 micron recessed isolation bipolar ECL.

Method for Interconnecting Conducting Layers of an Integrated Circuit

Peter S. Gwozdz and Hubert Bath

US Patent # 4,605,470. Issued August 12, 1986

Process for interlayer dielectric up to 5 microns thick.

Method for Filling a Trench in an Integrated Circuit Structure Without Producing Voids

Peter S. Gwozdz

US Patent # 4,714,520. Issued December 22, 1987

Process for filling isolation trenches, or slots.

Passivation For Integrated Circuit Structures

Bert L. Allen, Peter S. Gwozdz and Thomas R. Bowers

US Patent # 5,010,024. Issued April 23, 1991

Passivation for One Time Programmable ROMS, providing a low stress, ultraviolet transparent film.

Detailed University Experience. Dr. Peter S. Gwozdz

San Jose State University. San Jose, CA 95192

8/88 - 1/03: Director of the Center for Electronic Materials and Devices. Developed the Integrated Circuits Laboratories (IC Labs) and managed the IC Labs for 14 years. Developed, produced and instructed a [laboratory short course](#) for industry professionals. Provided the [NSF Microfabrication Laboratory Workshop](#), a series of one week workshops for undergraduate faculty, sponsored by the National Science Foundation, on IC laboratory education. Directed and coordinated more than 100 research and development projects with industry and government agencies. Professor, teaching courses in the field of Integrated Circuit (IC) Processing, in the departments of General Engineering, Materials Engineering, and Electrical Engineering. Advisor for Masters Thesis's.

Detailed Industry Experience. Dr. Peter S. Gwozdz

1/80 to 7/88; Advanced Micro Devices (AMD). 915 DeGuigne, Sunnyvale, CA 94086

12/87 - 8/88: Operations Manager for Wafer Foundry.

4/86 - 11/87: Member of the Technical Staff.
11/83 - 3/86: Director of Bipolar Logic Technology. Directed Fab 9.
1/80 - 10/83: Process Engineering & Technology Development Manager for Fab 9.

5/76 to 12/79; Wafer Fab Start Up Projects.

Worked for three different companies. In all 3 cases, successfully started up a new technology in production.

2/79 - 12/79: AMI, Santa Clara, CA. VMOS subfab for Epi & CVD.

11/77 - 2/79: Fairchild Semiconductor, Mt. View, CA. IIII for the 9440. High speed microprocessor.

5/76 - 11/77: Raytheon Semiconductor, Mt. View, CA. 2901 high speed microprocessor family.

2/73 to 4/76; National Semiconductor. Santa Clara CA

Sustaining Process Engineer, manufacturing, Linear.
Manager of Yield Improvement, Bipolar Memory.

1966 to 1968; Summer Semiconductor Research during graduate school

RCA Labs; 1967 and 1968 summers; GaAs.
Sprague Labs; 1966 summer; Tungsten CVD on Silicon.

Public Consulting Activity. Dr. Peter S. Gwozdz

2018: TSMC, Haynes and Boone

2014: Spansion, Ropes & Gray

2013: LSI Logic, Thompson & Knight

2012: uPI, Haynes & Boone, LSI Logic, Thompson & Knight

2011: Crane, Brooks, Intellectual Ventures, Weil Gotshal & Manges

2010: AMD, O'Melveny & Meyers, uPI, Covington & Burling, Freescale, Jones Day

2009: LSI Logic, Thompson & Knight, Sidley Austin

2008: Infineon, Baker Botts, BIAX, Williams Morgan & Amerson, Monitor, On Semiconductor, Jones Day, SMIC, Paul Hastings Janofsky & Walker

1993 to 2008: [SEMI](#): Provide short course "Semiconductor Processing Technology", an introduction for professionals in the semiconductor industry. More than 60 sessions were provided, at the SEMICON conventions held in San Francisco, San Jose, Austin, Boston, Munich, Singapore, Geneva, and other cities.

1993 to 2007: Provided short course “Semiconductor Processing Technology” in-house at companies world-wide. More than 40 sessions were provided, at more than 35 companies.

2007: Spiricon, Matsushita, McDermott Will Emery, Applied Materials, Weil Gotshal Manges, Goodwin Procter, Powerchip, Venable

2006: Spiricon, Matsushita, McDermott Will Emery, Applied Materials, Weil Gotshal Manges, Goodwin Procter, Monitor

2005: Helix, SMIC, Paul Hastings Janofsky & Walker, Micrel, O’Melveny & Meyers, Sidley Austin

2004: ZF Micro Solutions, BOC Edwards, RHEM (Rodel), ST Microelectronics, Thompson & Knight, California Micro, Tinicum, Royal Insurance, Helms Mulliss Wicker, Agere, Kirkland & Ellis

2003: GE Betz; Northrup Grumman, ST Microelectronics; Jenkins & Gilchrist, Shape Products

2002: Silicon Integrated Systems Corporation (SiS); Thelen Reid & Priest LLP; Wilson Sonsini Goodrich & Rosati; Andrews & Kurth; Munger, Tolles & Olson

2001: IXYS; Townsend, Townsend & Crew LLP; Microelectronics and Computer Technology Corporation (MCC)

2000: PRI Automation; Lam Research; Mitsubishi Texas Ultra Pure Air; Soros Fund Management; Gerson Lehrman Group

1999: Alexandria VA US District Court; Ericsson; MATEC Maricopa; Schlumberger

1998: Atmel; CTI Cryogenics; Hitachi; Hypervision; MPIi; PRI Automation; Rodel; Samsung; Senior Flexonics

Consultation Topics. Dr. Peter S. Gwozdz

Services:

- Expert Witness
- Technical Consultation
- Technical Training
- Technical Documentation
- Patent Review
- Research and Development
- Library research
- Wafer Foundry Management
- Wafer Foundry Search & Evaluation
- Technology Management

Consultation Fields:

- Semiconductor Processing

Multilevel Interconnect
Planarization
CMP - Chemical Mechanical Planarization
Chemical Vapor Deposition
Plasma Enhanced Chemical Vapor Deposition
Semiconductor Contamination Control
Defects in Oxide
Defects in Silicon
Microcontamination
Plasma Etching
Photolithography
Power Transistors
Semiconductor Devices
Transistors