

DECLARATION OF PETER S. GWOZDZ, Ph.D.

EXHIBITS

EX1001 U.S. Patent No. 7,812,409 to Hshieh (“the ‘409 Patent”)

EX1002 Prosecution History of the ‘409 Patent

EX1004 Curriculum Vitae of Dr. Peter S. Gwozdz

EX1005 U.S. Patent 5,072,266 (“Bulucea”)

EX1006 U.S. Patent Application Publication 2006/0273390 (“Hshieh”)

EX1007 U.S. Patent 6,984,864 (“Uno”)

EX1008 U.S. Patent 6,037,628 (“Huang”)

I. Introduction

I, Dr. Peter S. Gwozdz, declare *and* state as follows:

1. I am retained by uPI Semiconductor Corporation (“uPI” or “Petitioner”) as an independent expert in this *inter partes* review (“IPR”) before the Patent Trial and Appeal Board (“PTAB”) in the United State Patents and Trademarks Office (USPTO).

2. I am not an employee of uPI or any of its affiliates or subsidiaries.

3. I am tasked to provide my opinions as to whether certain references disclose, teach, or suggest the features recited in the claims of U.S. Patent No. 7,812,409 (the ’409 Patent) and as to whether the claims of the ’409 Patent are unpatentable as being anticipated or deemed obvious.

4. I am compensated at my usual rate of \$550.00 per hour for my time spent performing my assigned opinion tasks above, and for any time required of me to attend any meetings, to give testimony, or to attend depositions related to this IPR. I will be reimbursed for any reasonable, actual out-of-pocket expenses that I incur in conjunction with performing my assigned tasks.

5. My compensation is based solely on the time that I devote to performing my assigned tasks in connection with this IPR and is not contingent upon the substance of my work product or any outcome of this IPR.

6. My opinion and the bases for my opinions are set forth hereinbelow.

II. Education Background, Professional Experience, and other qualification

7. I hold a Ph.D. degree in Physics from the University of Illinois, awarded in 1973. My research topic was on defects in silicon.

8. I am a technologist in the field of semiconductor wafer fabrication. I have been continuously active in the “Silicon Valley” since 1973.

9. Between 1973-1988, I held various technical positions in the semiconductor industry, including eight years at Advanced Micro Devices, where I worked in development of next generation semiconductor technology and as a Director of Technology Development.

10. Between 1988-2023, I was professor in the College of Engineering at San Jose State University (SJSU), where I taught courses part-time in the field of Integrated Circuit (IC) Processing, in the departments of General Engineering, Materials Engineering, and Electrical Engineering. I retired from SJSU in 2003.

11. While at SJSU, I was Director of the Center for Electronic Materials and Devices, where I developed and managed the Integrated Circuits (IC) Labs.

12. At the IC Labs, I taught more than 100 sessions of a three-day laboratory course on microfabrication for industry professionals from all over the

world. This course was also taught at SEMICON conventions in San Francisco, San Jose, Austin, Boston, Munich, and Singapore, as well as in-house at many companies in the industry. The course materials, “Semiconductor Processing Technology”, are available in notebook format and in CD Power Point format. The course was also available from SemiZone.com, 2002-2009, in streaming web format.

13. Since 1988, I have also been a part-time industry consultant.
14. My curriculum vitae is attached hereto as EX1004.

III. DOCUMENTS AND REFERENCES CONSIDERED

15. I have reviewed U.S. Patent 7,812,409 and its prosecution history, listed herein as EX1001 and EX1002, respectively.

16. I have also reviewed U.S. Patents 5,072,266 (“Bulucea”), 6,984,864 (“Uno”), 6,037,628 (“Huang”), and 7,285,822 (“Bhalla”), and U.S. Patent Application Publication 2006/0273390 A1 (“Hshieh”), attached hereto as EX1005, EX1007, EX1008, EX1009, and EX1006 respectively.

IV. APPLICABLE LEGAL STANDARDS

17. I am not an attorney. However, in connection with this IPR and in my previous work, I have been informed of certain principles of patent law, which I have applied or used in arriving at my opinions.

18. In this section, I describe my understanding of these certain legal standards. In connection with this IPR, I have been informed of these legal standards by counsel for uPI and I have applied my understanding of these legal standards in my analysis as detailed below.

1) Claim Construction

19. I understand that a term in a claim (“claim term”) of a patented invention is used by the patentee to define what “the applicant regards as his invention.”

20. I understand that a claim term is to be given its ordinary and customary meaning. The process of ascertaining its meaning and its scope is referred to as “claim construction.”

21. The ordinary and customary meaning is the meaning that the term would have to a person of ordinary skill in the art (“POSITA”) in question at the

time of the patent filing, in the context of the entire patent, including its specification and its prosecution history (“intrinsic evidence”).

22. When the meaning of a claim term as understood by POSITAs is not immediately apparent, or when the term is used inconsistently in the intrinsic evidence, I may look to extrinsic evidence for claim construction; such extrinsic evidence preferably concerns relevant scientific principles, the meaning of technical terms, and the state of the art.

23. The extrinsic evidence that I may look into includes dictionaries, especially technical dictionaries, for accepted meanings of the claim term, as used in various fields of science and technology.

24. When construing a claim term in view of its specification, I first look for the meaning of that claim term as it is presented in the specification. In other words, in this effort, the claim term is to be understood in a manner that is consistent with the specification,

25. I understand, however, the interpretation to be given a claim term can only be determined and confirmed with a full understanding of what the inventors believe they have actually invented and what they intended to encompass with the claim.

26. When the patentee uses a claim term in a way that differs from the meaning it would otherwise possess, the inventor's lexicography governs. This is because the patentee is allowed to express his intentions with precision, for example, to effectuate an intentional disclaimer, or disavowal, of claim scope by the inventor.

27. I understand that the prosecution history is important to be consulted when construing a claim term because the claim term that emerged has been tested against the prior art during prosecution. I understand the term "prosecution history" to mean all the communications between the applicant for patent and the U.S. Patents and Trademarks Office during the time period between the filing of the application for patent and the issuance of the patent.

28. I look to the prosecution history to inform the meaning of the claim term for how the inventor understood the invention and whether the inventor limited the invention during prosecution to making the claim scope narrower than it would otherwise be.

29. In this case, I performed my claim construction using my understanding above.

2) Availability of a Reference Document as "prior art"

30. I understand that there is a body of law that governs whether a reference document is available as “prior art” for the purpose of a validity analysis. I have not been informed of that body of law, and I rely on uPI’s counsels’ determination for each prior art reference in the current IPR.

3) Anticipation

31. I understand that a patent claim is invalid as being “anticipated” under 35 U.S.C. § 102, if all the limitations of that patent claim are present in a single device or method that was previously known, used, or described in a single reference (i.e., a printed publication or a patent), such that a POSITA, looking at that single reference, could make and use the claimed invention without undue experimentation.

32. I understand that a claim can be anticipated even if all the limitations of that claim are not expressly found in a prior art reference, if the missing limitations are inherently present, i.e., if the prior art necessarily functions in accordance with, or includes, the claim limitations.

33. I understand that it is acceptable to examine evidence outside the prior art reference in determining whether a feature, while not expressly discussed in the reference, is necessarily or inherently present in it.

4) Obviousness

34. I understand that, when a prior art reference does not disclose all limitations of a claim, the claim can still be invalid under 35 U.S.C. § 103 as obvious, when the difference between what is disclosed in the prior art reference and the claimed invention, taken as a whole, is such that a POSITA would find obvious.

35. In determining obviousness, I understand that I am to determine if, at the time the claimed invention was made, it would have been obvious to a POSITA, considering the teachings of the relevant prior art.

36. In that regard, I understand that (i) I have to determine the scope and content of the prior art, (ii) the differences between the prior art and the claim, and (iii) the level of ordinary skill in the art at the time of the invention.

37. I understand that obviousness of a patent claim can be shown by combining the disclosures (“teachings”) of two or more prior art references, in a manner that would meet all the limitations of the patent claim, when a POSITA has reason, is prompted, or is motivated to combine the prior art references in such a manner.

38. I understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. In other words, when a claim simply arranges prior art elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, then such a combination is obvious.

39. I understand further that, when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another that is known in the field, the combination is likely to be obvious unless the combination yields an unpredictable result.

40. I understand that, when work is available in a field of endeavor, incentives and other market forces can motivate one of ordinary skill in the art to implement a predictable variation of that work based on knowledge derived from the prior art. Such a variation is likely unpatentable.

41. I understand that a finding of obviousness can also be supported by some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

42. In my analysis, I understand that a patent claim composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art. I understand that it can be important to identify a reason that would have prompted a POSITA to combine the elements in the way the claimed invention does.

43. In that regard, I understand that one of the ways in which subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims. I understand that any need or problem known in the field of endeavor at the time of alleged invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

5) Secondary Considerations

44. It is my understanding that obviousness determined in the manner of my understanding above may be rebutted by a showing of "secondary considerations" of non-obviousness. Such secondary considerations include, for example, evidence of commercial success of the invention, long-felt but unsolved needs, failure of others, unexpected results, and evidence of industry acquiescence.

45. I am further informed that, to support a finding of non-obviousness, the patentee must generally show a “nexus” between the secondary considerations and the features of the invention as claimed.

46. I understand that it is usually the patent owner who must demonstrate secondary considerations to rebut the obviousness findings in my analysis.

47. In my analysis, I have not sought out nor have I encountered any evidence that would support secondary considerations.

V. THE '409 PATENT

48. The '409 Patent discloses a trenched power semiconductor device with truncated corners. EX1001. 1:9-13.

49. Trench power semiconductor devices include trench Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), also often known in the literature as trench Metal-Insulator-Semiconductor Field-Effect Transistors (MISFETs). (In this Declaration, for uniformity, the more popular term "trench MOSFET" will be used.)

50. A trench MOSFET refers to a MOSFET in which the gate electrode or electrodes are formed embedded inside a vertical trench excavated in the silicon substrate. See, e.g., trenched gates 20 in Fig. 1C (prior art) of the '409 Patent. EX1001, Fig. 1C.

51. The '409 Patent discloses a trenched power semiconductor device in a "closed cell unit" configuration, where a trenched gate laid out with truncated corners -- or which, after lithographical development (see below) have rounded corners -- surround a transistor cell. EX1001, 1:66-2:3.

52. The truncated corners in the layout of the trenched gates exchange sharp internal 90° angles for less acute 135° angles.

53. The '409 Patent states that a conventional trenched power semiconductor device, such as a trenched MOSFET, has a square cell configuration. EX1001, 1:28-32.

54. A square cell configuration means that the MOSFET is formed by numerous closed-cell units, with the layout of each closed-cell unit having a square trenched gate that surrounds a square contact; the square contact electrically shorts a source region and a body region of the MOSFET. For example, the preamble of Claim 1 of the '409 Patent recites such a closed-cell unit: “[a] trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate.” EX1001, 5:7-9.

55. In the preamble of Claim 1, the trenched semiconductor power device is in a “closed cell” configuration, in which trenched gates surround “transistor cells.” Here, the term “transistor cell” refers to the structure bounded by the trenched gates. Thus, the '409 Patent identifies Figs. 1-3 as “closed cell units” or “close unit cells” of MOSFET devices with surrounding trenched gates. EX1001, 3:11-27.

56. The '409 Patent states that due to the square shapes of the trenched gate and the metal contact, the shortest distance between the peripheral sides of the

metal contact to the four corners of the trenched gate is longer than the shortest distance from the peripheral sides of the metal contact to the four sides of the trenched gate. EX1001, 1:28-39.

57. The '409 Patent states that the resistance between a channel and the metal contact of the trenched MOSFET is proportional to the shortest distance between the metal contact and the trenched gate. EX1001, 1:42-45.

58. The '409 Patent states that, due to the non-uniform distance between square contact and the square gate trench, there are weak points in the MOSFET device. EX1001, 1:48-50.

59. The '409 Patent concerns a “parasitic bipolar NPN latch up” problem in semiconductor power devices or trenched semiconductor power devices. EX1001, 1:15-18. (In the following, for brevity, I will refer herein to this phenomenon as the “Parasitic Bipolar Problem.”)

60. The '409 Patent states that “[t]he parasitic bipolar NPN latch up difficulties are specially pronounced near the trench corners.” EX1001, 1:18-20.

61. The '409 Patent traces a cause of the Parasitic Bipolar Problem to weak points at the corners of the trenched gate:

„, weak points of the MOSFET device due the non-uniform space between the square contact and the trench in the closed cell ... occur at the four corners [resulting] in low avalanche current and reduced ruggedness due to the parasitic N+PN latches up near the trench corners ...

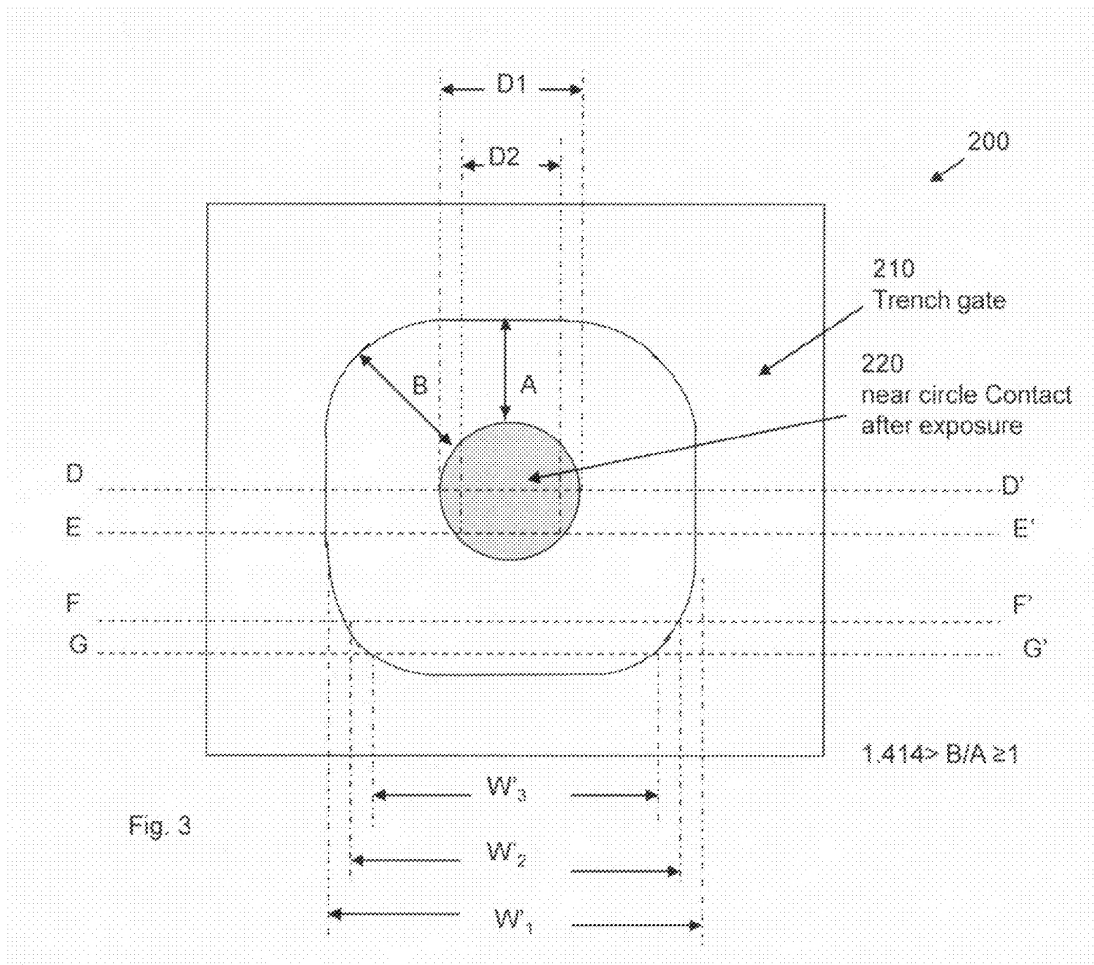
EX1001, 1:50-57.

62. In other words, the '409 Patent teaches that surface breakdown at the corners of the trenched gates can precipitate the Parasitic Bipolar problem. (For brevity, I will refer this undesirable causal link between the Parasitic Bipolar Problem and the weak points at the corners of the gate trench herein as “Surface Breakdown Link.”).

63. To mitigate the Surface Breakdown Link, so as to enhance ruggedness, the '409 Patent teaches forming trench gates with rounded corners and forming dopant contact regions with a substantially circular shape:

...[A] closed cell unit 200 of a MOSFET device includes trenched gate 210 surrounding a metal contact disposed above a doped contact region 220. The doped contact region 220 is formed with substantial circular shape and the trenched gate is formed with rounded corners 215.

EX1001, 4:5-9. See, also, Fig. 3.



64. The '409 Patent teaches that such a closed unit cell has a roughly uniform distance (i.e., $1.0 \leq B/A \leq 1.414$) between the trenched gates (including the rounded corners) and a doped contact region under the circular metal contact; this roughly uniform distance mitigates the Surface Breakdown Link by eliminating the weak spots near the corners at the trenched gates:

The distance from the edge of the circular doped contact region 220 to the trenched gate 200 including the distance B to the rounded corners

215 and to the distance A to the edges of the trenched gate are substantially the same, i.e., $B=A$. Therefore, the ratio of B/A is substantially kept near 1.0 and certainly smaller than 1.414. The weak spots near the corners of the trenched gate that caused reduced device ruggedness are therefore eliminated.

Ex1001, 4:9-15. (For brevity, I will refer herein the roughly uniform distance closed unit cell of Fig. 3 as the “Uniform Cell”)

65. I note that the reference numeral 220 is used in the specification of the 409 Patent to refer to both “doped contact region 220” (EX1001, 4:4-7) and “circular trench source-body trench contact 220” (EX1001, 4:25-30). Reference numeral 220 is associated in Fig. 3 with a feature labeled “near circle Contact after exposure” and in each of Figs. 3A-3D to the trench contact itself. EX1001, Figs. 3A-3D,

66. The ‘409 Patent also teaches that, not only that the circular dopant region in the Uniform Cell of Fig. 3 has a uniform space between it and the trenched gates, the uniform space can also be between the contact metal and the trenched gates:

In an exemplary embodiment, the closed cells further includes a contact metal to contact a source and a body regions [sic.] wherein the

contact metal the trenched gate surrounding the transistor cell have a uniform space between them.

EX1001, 2:39-43.

67. This embodiment described at 2:39-43 provides support for Claim 1 of the '409 Patent:

said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners; each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, ...
(emphasis added)

EX1001, 5:10-15

68. The '409 Patent teaches forming the Uniform Cell of Fig. 3 by applying a photo-lithographical technique on a square closed unit cell with truncated corners:

The process for manufacturing the semiconductor power device as disclosed above thus includes a step of “exposure through the mask,” such that the square contact becomes approximately circular shaped contact and truncated corners become smoother. The truncated corners

are formed by design layout not process. It is by nature that truncated corners in layout as that shown in FIG. 2 and becomes rounded as shown in FIG. 3. Such configuration is formed after exposure because of the photolithography resolution of 0.18-0.35 micrometers.

EX1001, 2: 16-20.

69. The '409 Patent teaches that the truncated corners in the layout of the trenched gates become rounded "by nature," meaning that the rounded corners are the necessary result when the lithographical technique is applied.

70. This photo-lithographical technique takes advantage of the lithography's resolution limits. Minimum line-width or "critical dimension" squares would necessarily become approximately circular after development. (For brevity, I will refer herein to this method of photo-lithographically creating an "after exposure" approximately circular image from a square feature as "Litho-rounding Technique.").

71. The '409 Patent describes, in conjunction with Fig. 3A, the contact trench relative to source and body regions and the trenched gates:

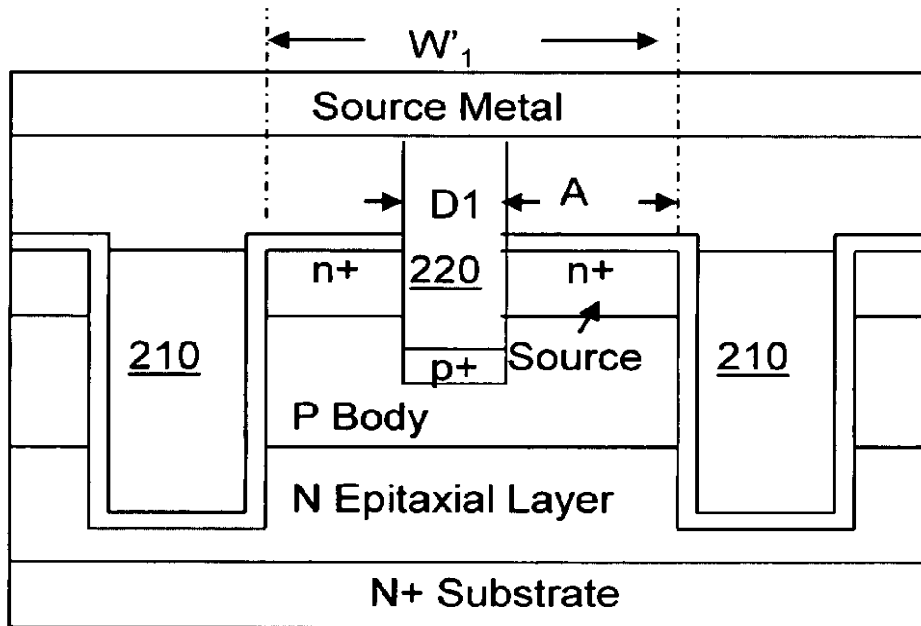


Fig. 3A (D-D' Cross Section)

“The close semiconductor cell is surrounded by trench gates with a body region formed between the trench gates and encompassing a source region. ... The closed semiconductor power cell further includes a circular trench source-body trench contact 220 extended into the body region through the source region of the closed semiconductor power cell in contact with a p⁺ contact dopant region disposed immediately below the trench contact 120. The circular trench contact 220 is disposed at a distance away from a gate oxide lining of said trench gate from all circumferential points of the circular trench contact.

EX1001, 4:20-33.

72. This description at 4:20-33 supports Claim 1's circular trench contact limitations that recite:

[the circular trench contact] ... penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;

said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact ...”

EX1001, 5:15-26.

73. Providing a trench contact that reaches below the silicon surface into the body region to be in contact with a contact dopant region immediately under the trench contact is known in the prior art. In fact, such a trench contact is shown in the admitted prior art Figs. 1C and 1D. EX1001, Figs. 1C and 1D.

74. The only limitations that trench contact 15 in admitted prior art Fig. 1D would not meet in Claim 1's limitations concerning the “circular trench contact” are “circular” and “circumferential.” These remaining limitations are

inherently met when the trench contact is formed circular. (Figs. 3A-3D.)
EX1001, Figs. 3A-3D. (For brevity, I will herein refer to a trench contact that reaches below the silicon surface to be in contact with a contact dopant region immediately under the trench contact will be referred to as a “Deep Body Trench Contact”).

75. Claim 1’s last sub-paragraph recites:

said contact metal plug connected to a source metal disposed on top of said circular trench contact.

EX1001, 5:27-28.

76. The claim term “source metal” above does not appear in the textual description of the ‘409 Patent, but appears in each of Figs. 3A-3D, and also in admitted prior art Fig. 1C. The above limitation “source metal” of Claim 1 is met by Fig.1C and is therefore part of prior art. EX1001, Figs, 1C, Figs. 3A-3D.

77. Limitations recited in Claims 2-4 of the ‘409 Patent do not appear in the textual description of the ‘409 Patent, appearing only as labels in the admitted prior art Figs. 1B-1D. EX1001, 5:29-6:7, Figs. 1B-1D.

78. Claim 2 is met by the metal layer labeled “Ti or Ti/TiN” in Fig. 1B.

79. Claim 3 is met by the metal layer labeled “Ti/TiN/W” in Fig. 1C.

EX1001, 5:36-40, Fig. 1.

80. Claim 4 is met by the metal layer labeled “Al Alloys” in each of Figs.

1B and 1C. EX1001, 6:1-6, Fig. 1B and 1C.

81. Limitations recited in Claim 5 appear in neither the textual description nor the drawings, except as originally filed as a claim. The recited limitation of Claim 5 was introduced into then Claim 12 on without justification on April 15, 2009. EX1002, Amendment of April 15, 2009, at p.7.

VI. STATE OF THE ART

82. Trench MOSFETs laid out in the closed-cell configuration have existed since the 1980's, as evidenced by the prior art reference Bulucea (EX1005).

83. Trench contacts, including circular trench contacts, have been known before the filing date of the '409 Patent. For example, "Hshieh" (EX1006), Uno (EX1007), Huang (EX1008) and Bhalla (EX1009) all disclose trench contacts.

84. In my own personal professional experience, I have multiple instances of working with trenches etched in silicon. In 1977 I worked with a MOSFET technology where the gate was in a V shaped trench. My 1987 patent (4,714,520) was a method for filling a trench. All the IC technologies I worked on had large (power) transistors built into the circuit, for example when a signal needs to be sent a long distance, or as input to numerous transistors, or off the chip. I have worked on patent cases that involve IC chips that are power transistors, and I understand the reasons why they must be designed as arrays of minimum transistors - strips or squares or hexagons; I have worked with power transistor technologies with and without trenches, bipolar and MOSFET.

85. For the reasons above, I consider trench MOSFETs to be a matured product type, where improvements are incremental and not pioneering.

VII. THE QUALIFICATIONS AND BACKGROUND OF THE PERSON OF ORDINARY SKILL IN THE ART

86. Based on my professional experience and observation, especially from work in the industry as Director of Technology Development, I estimate that a POSITA relating to the claimed subject matters of the '409 Patent as of December 4, 2006 would have (i) attained an undergraduate degree in electrical engineering, physics, material science, chemistry, or a similar discipline, and (ii) two or more years of experience in the field working in the processing, design or reliability of semiconductor devices. Attainment of a relevant advanced graduate degree, or relevant academic research experience, would deem equivalent to the work experience.

VIII. CLAIM CONSTRUCTION

87. Based on my understanding of the POSITA, as set forth above, I found that all words in Claims 1-5 of the '409 patent can be understood, in light of its specification, by their ordinary and customary meanings, except for the terms "circular trench contact" and "source metal" in Claim 1.

1) "Circular Trench Contact"

88. The '409 patent discloses "circular source-body trench contact 220" at 4:26-27. However, the '409 patent does not mean a trench contact that has a strictly circular cross section. This is because trench contact 220, also referred to as "doped contact region" (4:7), is disclosed in the '409 Patent as having been "formed with substantial circular shape." The '409 patent does not discuss nor illustrate contacts that are made to the trench gates, so "trench contact" refers only to the source-body trench contacts, and not to any gate trench contacts.

89. The '409 Patent discloses an "exposure through the mask" step in a method for manufacturing the source-body contact 220. The '409 Patent teaches that this step necessarily results in an "approximately circular shaped contact" (4:53-57).

90. As a semiconductor technologist, I am familiar with that lithographical technique. Depending on the processing conditions, of which there are numerous, the lithographical development would indeed transform a square feature into what could be described colloquially or imprecisely as an “approximately circular” feature, so long as the square feature in the layout is sized to be very close to the critical dimensions of a given manufacturing process.

91. Throughout my career, I have observed through microscopes various kinds of contacts. Contacts always have rounded corners because of the diffraction and scattering of light. As a result, minimum sized contacts are circular or approximately circular. A POSITA would know that, while some contacts (for example the pad openings for external connections) are drawn larger than minimum, almost all contacts in an integrated circuit are made as small as possible, which means using the minimum size (i.e. critical dimension) that can be reliably manufactured using the then current technology. Angular geometries that are drawn larger than minimum may not come out approximately circular, but each angle is necessarily rounded due to the diffraction and scattering of light.

92. While the ‘409 Patent does not discuss nor illustrate the overall layout of the claimed power transistor, a POSITA would know that power transistors are

designed as a large number of minimum transistors. In the case of the '409 Patent, the design is an array -- like a checkerboard -- of tessellated minimum "closed cell" transistors that are connected in parallel. In that design, a central contact is minimum-sized, but the overall closed cell is larger than minimum.

93. The '409 Patent shows the prior art drawn contact in Fig. 1A and the claimed drawn contact in Fig. 2; indeed, these contacts are drawn the same.

94. The '409 Patent shows the contact after development in Fig. 3 as a "near circle". This post-development contact in Fig. 3 represents both the prior art and the claimed contact in the '409 Patent. The '409 patent does not state that the contact in the claims is more nearly circular than the prior art under the same lithography process.

95. Fig. 3 is labeled "Contact after exposure". This is incorrect; a contact does not take shape until after development. Here, development means the removal of photoresist from the exposure, with the removal rate an increasing function of the amount of exposure (for positive photoresist), and the amount exposure referring to the spreading out at the edge of the contact, due to diffraction and scattering of light.

96. Therefore, to require the term “circular trench contact” to be understood as strictly circular would result in the term reading on no embodiment described in the specification. I have been informed that such a claim construction is disfavored.

97. I therefore propose that the term “circular trench contact” to be understood, in a very broad sense, as a “trench contact that has a horizontal cross section that is circular or approximately circular.”

2) “Source Metal”

98. The term “source metal” does not appear in the text of the specification in the ‘409 Patent, except in the drawings and in Claims 1-2, 4 and 6. EX1001, 5:7-6:38. In fact, the features that are labelled “source metal” which appear in Figs. 1C, 2A-2C, and 3A-3D are not even discussed in the Specification. EX1001, Figs. 1C, 2A-2C, and 3A-3D.

99. Claims 1, 4 and 6 provide the only substantive information regarding the “source metal,” which is that it is “disposed on top of said metal plug wherein said source metal layer composed of Ti/AlCu or Ti/AlSiCu alloys.” EX1001, 6:3-6, 35-38.

100. Therefore, I propose construing the term “source metal” to be a metal layer.”

3) “plug”, “Ti/TiN/W” and “Ti/TiN/Al Alloys”

101. The term “plug” appears in the claims but appears in neither the specification nor in the drawings.

102. The terms “Ti/TiN/W” or “Ti/TiN/Al Alloys” do not appear in the specification but appear in Fig. 1C (Prior Art); these terms are in the claims, in part.

103. I have extensive experience in the various metallization techniques for integrated circuits; my 1984 patent (U.S. Patent 4,451,326, entitled “Method for Interconnecting Metallic Layers”) was developed by an R&D wafer fab at AMD, where I started as Process Manager and was later promoted to Director of that R&D fab.

104. While at SJSU, I worked with a start-up company on a technique for tungsten (W) plugs, including obtaining grant money from a California program for university - start up joint projects for technology development.

105. In my opinion, the terms “plug”, “Ti/TiN/W” and “Ti/TiN/Al Alloys” are well known to a POSITA, and their meanings are understood by a POSITA.

These terms should be given meanings consistent with their use in the prior art to the '409 Patent.

IX. OVERVIEW OF THE PRIOR ART

1) Summary

106. All limitations of Claims 1-4 of the '409 patent are met by the admitted prior art in Figs. 1A, 1B, and 1C, except for the limitation of “with rounded corners,” with respect to the trench gates, and “circular,” with respect to the “trench contact.” However, in the manufacturing of the prior art trench MOSFET, the layout of the prior art closed-cell unit must necessarily be processed and developed by a lithographical process to be transferred to the silicon surface. As admitted in the '409 Patent, such a lithographical process *by nature* (i.e., necessarily) results in the rounding of angles at both the trenched gates and the trench contact. EX1001, 4:53-60. Thus, the limitations “with rounded corners” and “circular” are inherently met. (Recall that the claim limitation “circular trench contact” should be construed to include a “trench contact that has a horizontal cross section that is ... approximately circular”) is admitted as inherent (“by nature”) in the specification. EX1001, at 2:14-20 and 4:53-62.

107. I will provide in the following additional references from other references in the prior art. Specifically, I will show in the following that the Parasitic Bipolar Problem and its causal Surface Breakdown Link that the claims of the '409 Patent overcome have been known in the prior art, e.g., in Bulucea. In

fact, Bulucea not only explains both the Parasitic Bipolar problem and the causal Surface Breakdown Link, Bulucea provides specific solutions to overcome these difficulties and also general suggestions to other solutions.

108. Among the specific solutions proposed in Bulucea is rounding the corners at the trenched gates. Bulucea's methods for rounding include the Litho-rounding Technique, as used in the '409 Patent, and a sacrificial oxidation of the silicon sidewalls of the gate trenches.

109. Bulucea also suggests providing a heavily doped p^+ deep body diffusion region that is in contact with a source/body contact; this p^+ deep body diffusion region reaches into the silicon substrate, at least as deep as the body region, so as to move the currents related to the surface breakdown away from the high resistivity body region to the low resistive path through the p^+ deep body diffusion region to the source/body contact.

110. The principles behind Bulucea's deep body diffusion region are implemented in source/body trench contacts in trench MOSFETs,

111. I have reviewed examples of trench contacts found in the prior art to the '409 Patent; specifically I have reviewed such trench contacts in Hshieh, Uno, Haung and Bhalla.

112. All limitations of at least Claim 1 of the '409 Patent are met by combining the teachings of Bulucea with the teachings of any one of Hshieh, Uno, Huang and Bhalla.

2) Bulucea

113. Bulucea relates to a trench MOSFET that includes “a central deep p⁺- (or n⁻) layer that is laterally adjacent to a p-body layer and that is vertically adjacent to an epitaxial layer of appropriate thickness and a gate dielectric of appropriate thickness in a trench.” EX1005, 1:60-64.

114. Bulucea's Fig. 21 discloses a trench MOSFET, with square transistor cells and gate trenches provided in a closed-cell configuration:

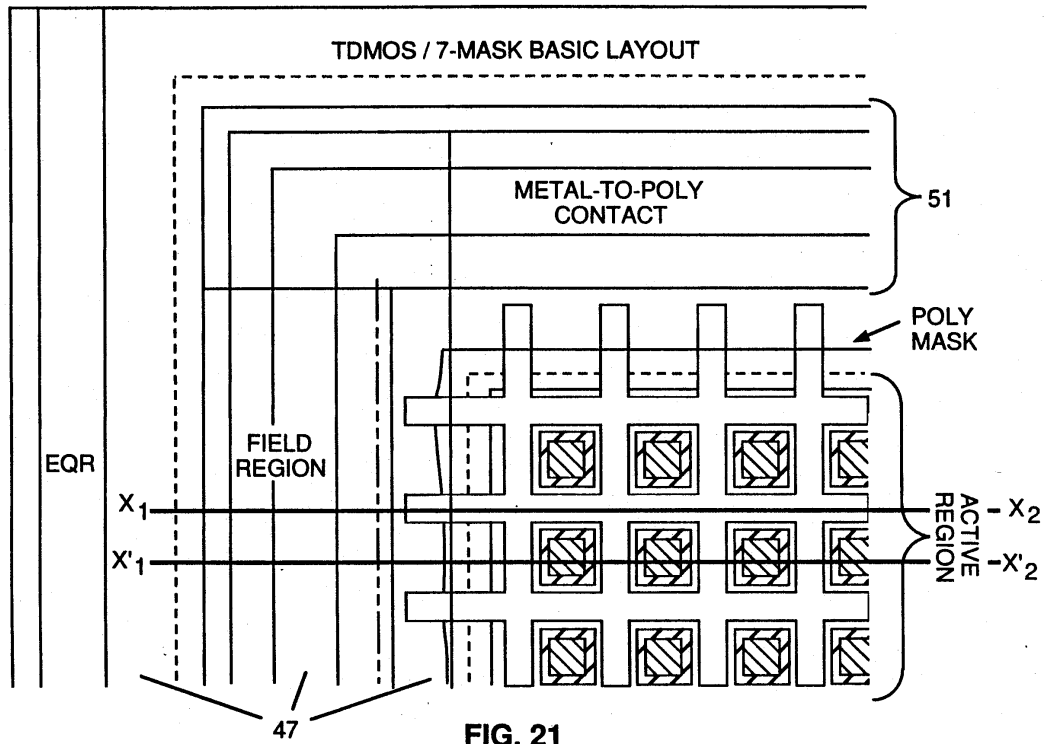


FIG. 21

EX1001, Fig. 21'

115. Bulucea's Fig. 21 is a schematic plan view of a group of transistor cells (square-cell geometry), EX1005, 3:14-15. In Figure 21, Bulucea shows a group of trench MOSFETs, also called trench vertical DMOSFET, in a closed-cell configuration, in which each trench MOSFET includes a square shaped trench gate surrounding a square shaped transistor cell area. EX1005, 3:14-18; EX1005, FIG. 21.

116. Fig. 21 meets the [1pre] preamble of the '409 Patent, which recites:

a trenched semiconductor power device comprising a plurality of trenched gates Surrounding a plurality of transistor cells formed in a semiconductor substrate ...

EX1001, 5:7-9.

117. To be discussed in further detail below, Bulucea -- like the '409 Patent -- is concerned about the Parasitic Bipolar Problem and its Surface Breakdown Link.

118. Bulucea also discloses that the rounded corners of the trenched gates and the circular profile in the source/body contact (plan view) of the Uniform Cell can be formed by the Litho-rounding Technique, in the same way as taught in the '409 Patent.

119. Bulucea also discloses at least one additional method for creating "substantially square-shaped cells with rounded corners" (i.e., Claim 1's limitation [1a]).

120. While not expressly disclosing the Deep Body Trench Contact, Bulucea teaches a deep body diffusion region, which encompasses principles for mitigating the Parasitic Bipolar Problem, explained in further detail below.

121. Buluce's teaching would therefore motivate a POSITA to incorporate the Deep Body Trench Contact taught in each of references Hshieh, Uno, Huang and Bhalla, as set forth in Grounds I-IV, respectively.

122. First, Bulucea explains the Parasitic Bipolar Problem:

... "bipolar breakdown" [] is controlled in part by the resistance between the intrinsic body region below the gate region and the body contact. ...

... When the drain voltage exceeds a certain breakdown value, the bipolar breakdown phenomenon is manifest where the drain current increases prematurely for drain voltages below the drain-source junction breakdown voltage (BVDSS).

EX1005, 4:2-5, 11-16.

123. Using a computer simulation (Fig. 5), Bulucea demonstrates the Surface Breakdown Link:

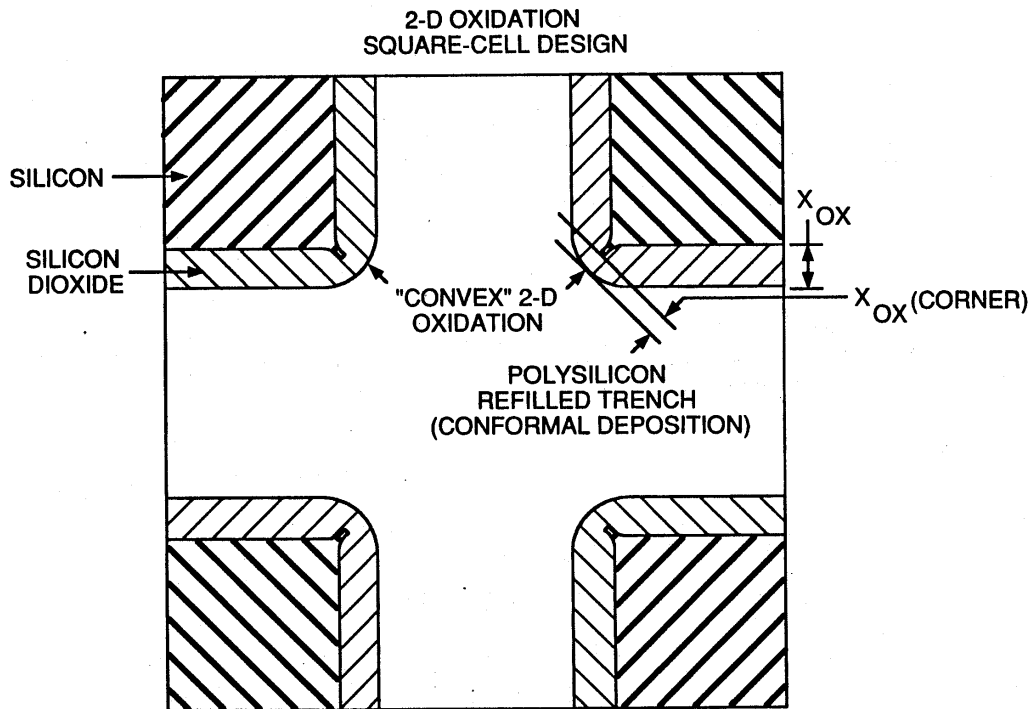
... surface breakdown is undesirable from the point of view of position of the source of avalanche-generated carriers relative to the body contact. If surface breakdown takes place adjacent to the trench, holes (electrons) flow laterally inside the p^- (n^-) region, toward the body contact. These forward biases the source-to-body junction and brings the transistor into a bipolar breakdown mode, latch-back.

Ex1005, 5:26-33.

124. Based on the Surface Breakdown Link, Bulucea concludes that the Parasitic Bipolar Problem can be mitigated by avoiding breakdown at the gate trenches.

125. In conjunction with its Fig. 7, Bulucea explains that the sharp corners (e.g., 90° angles) of the trenched gates can lead to a dielectric breakdown, Bulucea states:

... In a closed-cell geometry, the trench side wall oxide is grown under nonplanar, two-dimensional conditions at intersections of trench faces This causes nonplanar, viscous deformation and stress in the adjacent gate oxide material. ... When these distortions are combined with conformal covering of the surface of gate material, the oxide profile may develop near-atomically sharp field concentration sites and may manifest premature dielectric breakdown.



EX1005, 5:55-68, Fig. 7.

126. Dielectric breakdown, which occurs at the gate oxide layer next to the trenched gates, is one formed of surface breakdown.

127. Accordingly, Bulucea discloses mitigating dielectric breakdown by rounding the corners at the trenched gates:

This problem can be managed and eliminated to some extent by growing and etching away a 'sacrificial oxide layer' before the gate

oxide is grown on the trench walls ... This sacrificial oxidization rounds off the sharp corners of the initial trench profile.

EX1005, 6:1-10.

128. Bulucea discloses in detail a process using this sacrificial oxide layer approach in its Figs.25(a) and 25(b), in conjunction with the discussion at EX1005, 12:38-51. The process would result in "said trenched gates [of the square transistor cells of Fig. 21] surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners," thereby meeting limitation [1a] of Claim 1 in the '409 Patent.

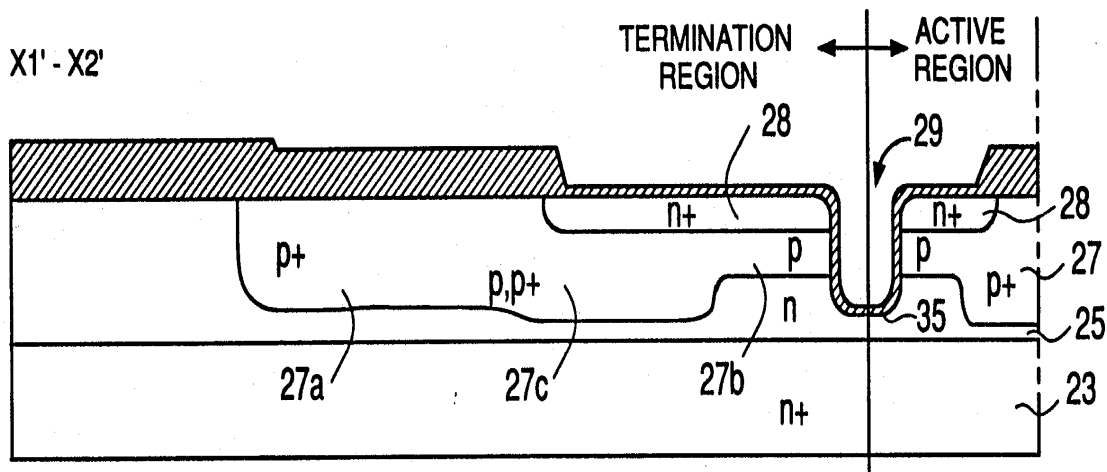


FIG. 25A

129. Bulucea's Fig. 25A shows teaches forming a uniform thickness gate oxide using the sacrificial oxidation approach. EX1005, 12:38-51. The resulting trenched gate profile meets limitation [1a] of the '409 Patent: trenched gates 29 surround the transistor cells as closed cells constituting substantially square-shaped cells with rounded corners.

130. Bulucea discloses a further method of rounding the corners at the trenched gates. Bulucea discloses in conjunction with Fig. 8, a hexagonal cell. Bulucea teaches that the hexagonal cell, which has 120-degree internal angles, would become rounded when process under the Litho-rounding Technique:

Further, the hexagon corners may become rounded off during the trench mask lithography and etching processes that precede trench formation so that the DMOS cells approach the cylindrical shape of a natural, field-controlled current valve.

EX1005:7:53-571.

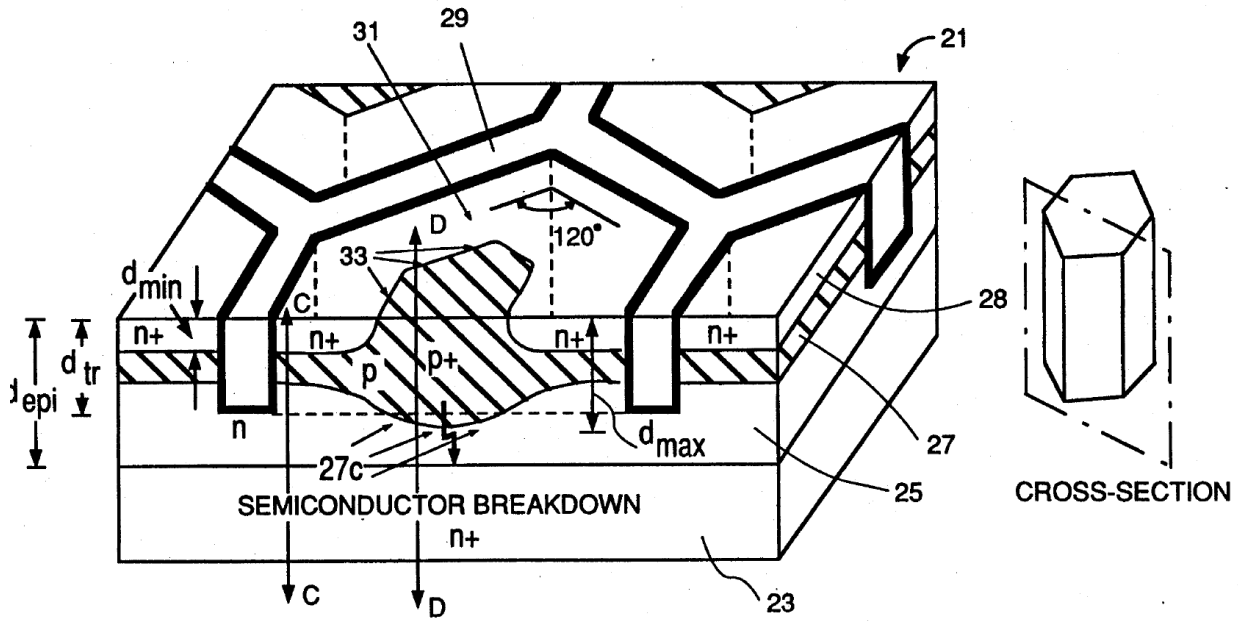


FIG. 8

131. Bulucea explains that, in a horizontal cross-section, the trench side walls intersect at angles of approximately 120° , as compared to an intersection angle of 90° in a rectangular cell design. Thus, Bulucea thus exchanges sharp 90° for less acute 120° internal angles. Bulucea thus teaches the same approach that is used in the '409 Patent, i.e., exchanging sharp 90° for less acute 120° internal angles.

132. The 120° internal angles also offer a substantial improvement for two-dimensional oxidation conditions as it reduces stress at the corners and promotes increased uniformity of oxide thickness. EX1005, 7:47-53.

133. The trenched corners may become rounded off during the trench mask lithography and etching processes that precede trench formation so that the transistor cells approach the cylindrical shape of a natural, field-controlled current valve. EX1005, 7:53-57.

134. Bulucea teaches:

... A hexagonal cell, trench DMOS is expected to have a higher gate rupture breakdown voltage than does its rectangular cell counterpart. For transistor operation the trench shape, in horizontal cross section (plan view), may be a polygon (not necessarily regular) or a circle or an oval; but the regular hexagon and polygonal shapes approaching a circle are the preferred shapes from the point of view of maximizing the gate oxide rupture voltage.

EX1005, 7:57-66

135. From a mitigation of Parasitic Bipolar Problem viewpoint, Bulucea teaches that the preferred transistor cell should have all angles rounded off (i.e., circle or oval).

136. Although Bulucea's Fig. 8 shows a hexagonal cell, Bulucea emphasizes that the principle of rounding the corners using the lithography at the trenched gates is applicable to any polygonal cell, as eliminating the angles of the polygonal cell – towards the preferred shape of a circle -- is the goal for reducing dielectric breakdown at the trenched gates:

For transistor operation the trench shape, in horizontal cross section (plan view), may be a polygon (not necessarily regular) or a circle or an oval; but the regular hexagon and polygonal shapes approaching a circle are the preferred shapes from the point of view of maximizing the gate oxide rupture voltage.

EX1005, 7:60-66.

137. Maximizing gate oxide rupture voltage means reducing the possibility of surface breakdown at a given gate voltage.

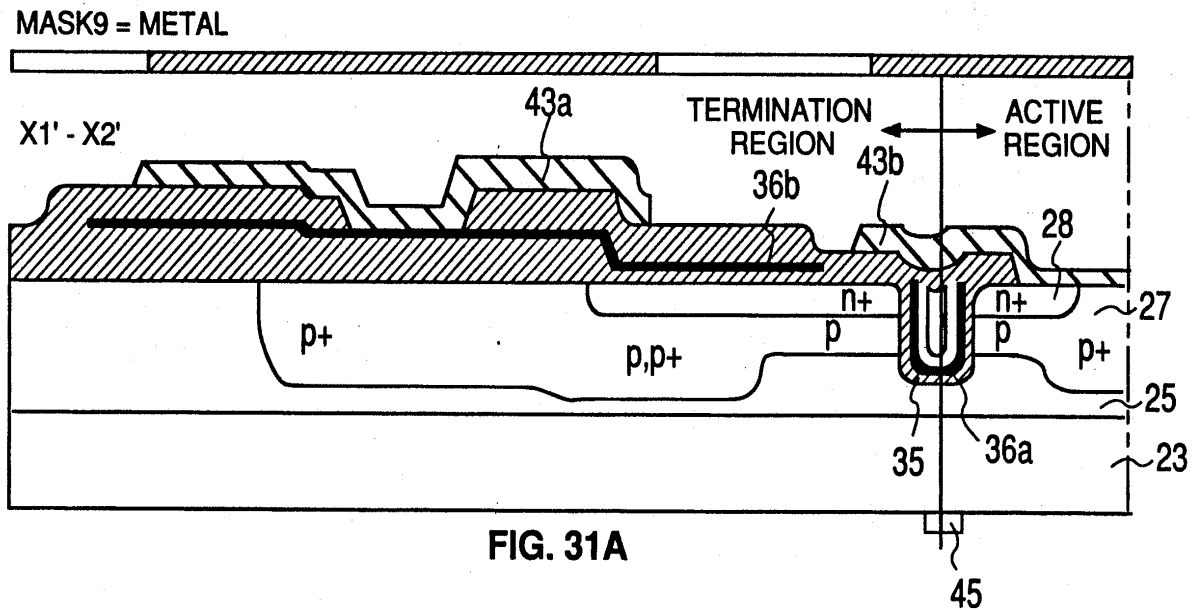
138. Because Bulucea teaches that the preferred horizontal cross section of a trench MOSFET cell is a circle or oval, a POSITA would be motivated to apply the Litho-rounding Technique to a square closed-cell unit, such as the square cells of Bulucea' Fig. 21.

139. As the source-body contact of the square closed-cell unit is inside the surrounding trenches, with sides of critical dimensions, the Litho-rounding Technique would provide approximately circular source/body contacts.

140. Thus, after development, that closed cell would further include an approximately circular contact disposed substantially in a central portion of the closed cell with rounded corners. In this regard, that resulting transistor cell in the plan view would be qualitatively identical to the Uniform Cell of Fig. 3 of the '409 Patent, meeting limitations [1a] and [1b] of Claim 1 of the '409 Patent.

141. In fact, applying both the Litho-rounding Technique on the source/body and the sacrificial oxidation on the trenched gates (as shown in Bulucea's Fig. 25A), the rounded corners of the trenched gate would also meet both limitations [1a] and [1b] of Claim 1 of the '409 Patent.

142. Bulucea's Fig. 31A shows an approximately circular source/body contact – the horizontal portion of metal 43b in contact with both source region 28 and p⁺ body region 27 -- disposed substantially in a central portion of the closed cell:



143. In addition to rounding the corners at the trenched gates, Bulucea discloses mitigating the Surface Breakdown Link by forcing surface breakdowns away from the body region next to the trenched gates – where the resistivity is high -- but towards the source/body contact at the center:

Hence, for a latch-back-free design, the drain breakdown must be controlled such that breakdown occurs on the contact side of the p^- (n^-) region, thus avoiding lateral current flow in the high resistivity body region.

EX1005, 5:33-37.

144. To achieve this result, Bulucea discloses, also in conjunction with its Fig. 8, providing a deep body diffusion region underneath and in contact with the source/body contact, so as to provide a low conductivity path for the avalanche current, away from the trench edge, thus avoiding the Parasitic Bipolar Problem:

As noted, a deep body diffusion is included in the center of the transistor cell 21 where the body contact is to be made. This diffusion is ... so that the semiconductor breakdown is forced away from any trench surface or corner and into the bulk of the semiconductor material ... Moreover, avalanche breakdown occurs below the body contact, not laterally along the contact, and lateral voltage drop through the body region, which would lead to bipolar breakdown, is avoided.

EX1005, 7:11-28.

145. Bulucea teaches a MOSFET with trenched gates, which along with forming a deep body diffusion region in the center of the transistor cell, suppresses semiconductor surface breakdown near the gate trench, thereby reducing the lateral flow of carriers in the body region from the gate trench toward the body contact, and avoiding the latch back of the N+PN bipolar. EX1005, 7:1-5; 7:24-28.

146. Bulucea's use of deep body diffusion approach to provide a low resistivity path between the contact and the body region is a principle used in the

Deep Body Trench Contact of admitted prior art Figs, 1C and 1D – i.e., the Deep Body Trench Contact includes a deep body diffusion region in the center of the transistor cell, where the source/body contact is to be made. Thus, a POSITA would be motivated to combine the teachings of Bulucea with a reference teaching a Deep Body Trench Contact. Such a Deep Body Trench Contact may be found, for example, in each of Uno, Huang and Bhalla.

147. Also, in its mitigation of oxide breakdown at the trenched gates, Bulucea teaches to take on-resistance into consideration, as it is undesirable to have increased on-resistance:

A third variable of importance here is the thickness of the oxide layer separating the gate material 29 (for example, doped polysilicon) from the surrounding n-type and p-type semiconductor materials. If the gate oxide thickness is increased, the gate oxide can take up a larger portion of the stress associated with the local electrical field, and initiation of avalanche breakdown adjacent to the trench becomes less likely. However, if the gate oxide thickness is increased, the on-state resistance is also increased (undesirable) ...

EX1005, 10:27-37

148. Thus, a POSITA would also be motivated to combine Bulucea's teaching with a reference teaching reduction of on-resistance in a trench MOSFET, such as Hshieh.

3) Hshieh

149. Hshieh relates to a trenched semiconductor power device with improved source metal contacts. EX1006, ¶ [0001].

150. Hshieh teaches a trench MOSFET in closed-cell configuration, with trench gates surrounding source and body regions of a closed unit cell:

[0013] ... the present invention discloses a trenched metal oxide semiconductor field effect transistor (MOSFET) device that includes a trenched gate surrounded by a source region encompassed in a body region above a drain region disposed on a bottom surface of a substrate. ...

EX1006, ¶ [0013].

151. Hshieh is concerned about on-resistance in a trench MOSFET; specifically, Hshieh is concerned about high on-resistance due to gate and source resistances:

[0011] Another aspect of the present invention is to reduce the source-body resistance and gate resistance by forming buried trench-poly gate runner with a source-body trench contact and gate-runner trench

contact that are further covered by a thin low-resistance layer with greater contact area to a top thick metal. ...

[0012] Another aspect of the present invention is to further reduce the gate resistance; an opening is formed in the source metal layer on top of a trenched gate contact plug disposed on top of a trench-poly gate runner. ...

EX1006, ¶¶ [0011]-[0012]

152. Thus, as Bulucea and Hsieh both relate to trench MOSFETs of a closed-cell configuration, and both being concerned with on-resistance of trenches MOSFETs, a POSITA is motivated to combine the teachings of Bulucea and Hsieh.

153. In this MOSFET, Hshieh discloses a cylindrical shaped source-body trench contact (i.e., a circular source-body trench contact) that penetrates both the source region into the encompassing body region:

[0013] ... In a preferred embodiment the MOSFET device further includes a source-body contact trench opened through the insulation layer into the source and body regions and filled with a source-body contact metal plug. ... In a preferred embodiment, the gate and the source-body contact metal plugs filled in the gate contact trench and the source-body contact trench includes a substantially cylindrical shaped plug. ...

EX1006, ¶ [0013].

154. Such a preferred embodiment is shown in Hshieh's Figs.3A-3E and discussed in ¶¶ [0027]-[0028]:

[0027] Referring to FIGS. 3A to 3D for an alternate MOSFET **100'** device of this invention. ... The MOSFET device 100' is supported on a substrate 105 formed with an epitaxial layer 110. The MOSFET device 100 includes a trenched gate 120 disposed in a trench with a gate insulation layer 115 formed over the walls of the trench. A body region 125 that is doped with a dopant of second conductivity type, e.g., P-type dopant, extends between the trenched gates 120. The P-body regions 125 encompassing a source region 130 doped with the dopant of first conductivity, e.g., N+ dopant. ...

[0028] ... Furthermore, for the purpose of improving source metal layer 140 to contact the source regions 130, a plurality of trenched source contact filled with a tungsten plug 180 is formed in the protective insulation layer 135. These tungsten plugs 180 are surrounded by a barrier layer Ti/TiN (not specifically shown). The contact trenches are opened through the NSG-BPSG protective layers 135 to contact the source regions 130 and the P-body 125.

EX1006, ¶¶ [0027]-[0028], Figs. 3A-3D.

155. For example, Fig. 3C shows:

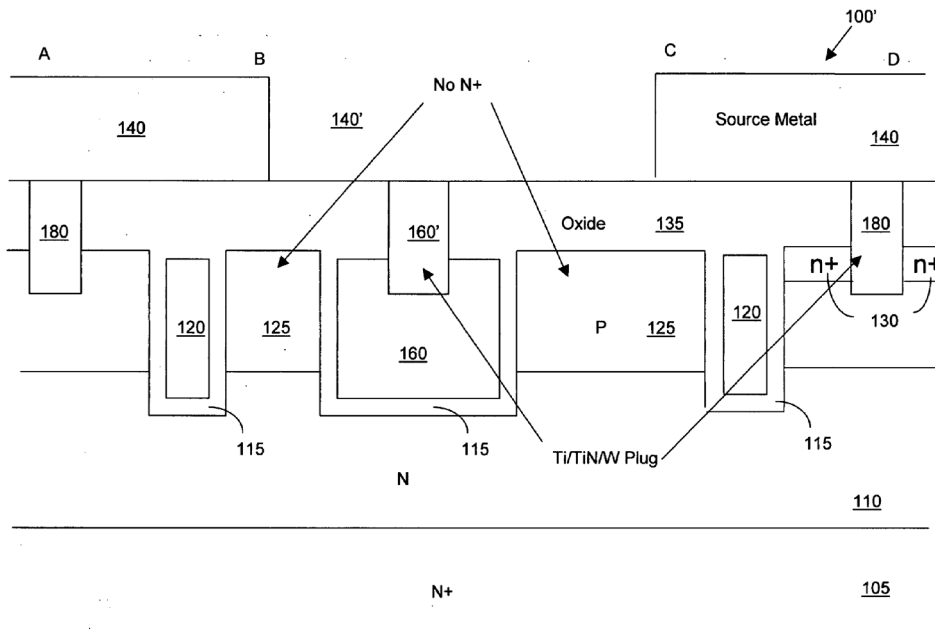


Fig. 3C

EX1006, Fig. 3C.

156. Thus, the above teachings of Hshieh meets limitations [1b]-[1f], including limitations “said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact,” which is clearly seen in Hshieh’s Fig. 3C, for example.

157. There, circular trench contact 180 is separate from said trenched gates 120 with said source region 130 and body region 125 disposed between a gate

oxide lining 115 of said trenched gates 120 and all circumferential points of the circular trench contact 180. Fig. 3C also indicates that trench contact 180 comprises a Ti/TiN/W plug, which meets recited limitations [3] of Claim 3 of the '409 Patent.

158. At ¶ [0013], Hshieh also teaches a titanium (Ti) resistance-reduction conductive layer:

[0013] ... In a preferred embodiment, the MOSFET device further includes a thin resistance-reduction conductive layer disposed on a top surface covering the insulation layer and contacting the gate contact metal plug and source-body contact plug ... In a preferred embodiment, the thin resistance-reduction conductive layer includes a titanium (Ti) layer. In a preferred embodiment, the thin resistance-reduction conductive layer includes a titanium nitride (TiN) layer.

EX1006, ¶ [0013].

159. This resistance-reduction conductive layer meets the recited limitations [2] of Claim 2.

160. In Figs. 5E1 and in ¶ [0031], Hshieh teaches:

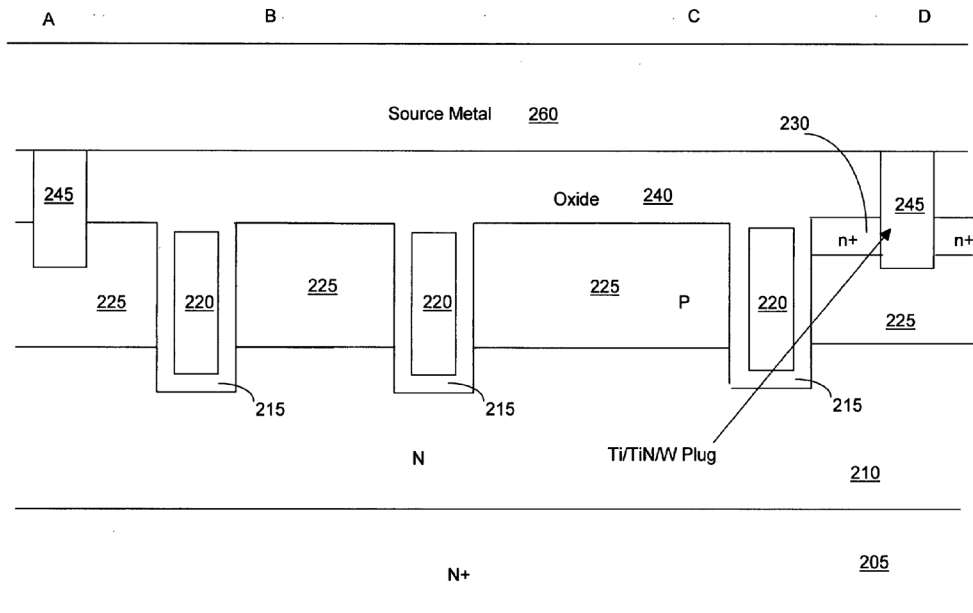


Fig. 5E-1

[0031] ... In FIGS. 5E-1 and 5E-2, a low resistance metal layer **260** is deposited over the top surface. The low resistance metal layer may be composed of Ti/AlCu or Ti/TiN/AlCu to assure good electric contact is established followed by a metal etch to pattern the metal layer into a source metal pad **260** and a gate metal pads **270** in electrical contact with the source-body trench-plug **245** and the gate-runner trench plug **250** respectively.

EX1006, ¶ [0031].

161. Hshieh's teachings in the above-quoted portion of ¶ [0031] meets recited limitations [4] of Claim 4,

162. In ¶ [0030], Hshieh teaches forming 0.4µm trench contact using chemical vapor deposition (CVD):

The tungsten plug is formed with the chemical vapor deposition (CVD) process and the chemical vapor has much better filling characteristics to fill the narrow and deep contact openings without development of void. The CVD process is suitable for process of circuits with critical dimension (CD) less than 0.4 micrometer (µms) in the semiconductor industries.

EX1006, ¶ [0031].

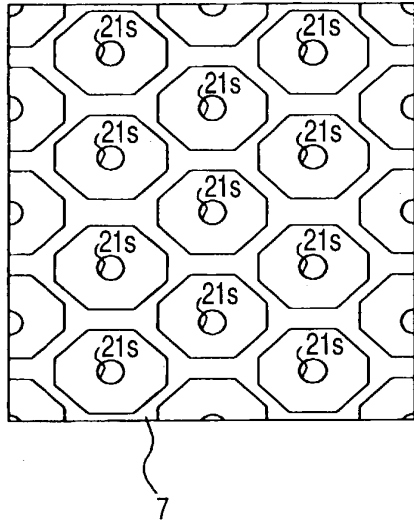
163. Such a tungsten plug would meet recited limitations [5] of Claim 5 of the '409 Patent.

4) Uno

164. Uno discloses a trench MOSFET and a method of manufacturing thereof in Figs. 1-11. EX1007, 4:51-62, Figs. 1-11. In particular, Uno discloses a circular trench contact in a MOSFET and a method of its formation. EX1007, 5:33-62, Figs. 6-9. Fig. 7 shows a plan view of a portion of the trench MOSFET with numerous closed-cell units. EX1007, 3:4-6, Fig. 7. Significantly, Fig. 7

shows circular trench contact 21s. EX1007, Fig. 7.

FIG. 7



165. That contact trench 21s is circular is confirmed by the specification's reference to trench contact 21s' *diameter*:

FIG. 7, after forming a silicon oxide film 19 above the substrate 1, the substrate 1 (p-Semiconductor region 15 and the n-semiconductor region 17) ... is etched by using a not illustrated resist film as a mask to form contact trenches (Source contact) 21s. In this case, etching condition is controlled such that the *diameter* for the opening of the substrate 1 (17, 15) is smaller than the diameter for the opening of the Silicon oxide film.

EX1007, 5:33-42.

166. As to formation of circular trench contact 21s, Uno states:

The n⁺-semiconductor region 17 is exposed from the lateral wall of the contact trench 21 s and the p⁻-semiconductor region 15 is exposed from the bottom thereof. In other words, the depth of the contact trench 21s exceeds the n⁺-semiconductor region 17 and reaches as far as the p⁻-semiconductor region 15. ...

Then, as shown in FIG. 8, a p-impurity, for example, boron fluoride (BF₂) is implanted to the bottom of the contact trench 21s and diffused to form a p⁺-semiconductor region (back gate contact region) **23**.

EX1007, 5:43-59.

167. As circular trench contact 21s reaches below silicon surface 31s to contact with p⁺ contact dopant region 23 immediately under circular trench contact 21s, circular contact trench 21s is a Deep Body Trench Contact. Uno teaches that the Deep Body Trench Contact allows a required mask alignment margins to be decreased:

By forming the contact trench **21** s and disposing the p⁺-semiconductor region **23** at the bottom thereof as described above, mask alignment margin can be decreased to refine the portion between the gates.

EX1007, 5:59-62.

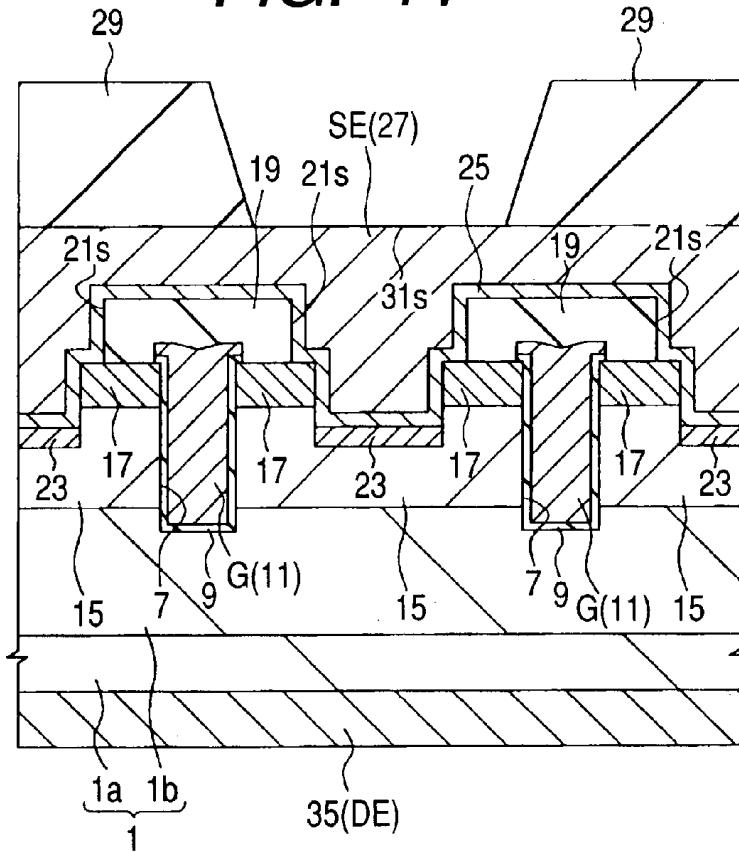
168. Uno also discloses Bulucea's deep body diffusion region approach in Fig. 12, showing that, when contact 21s contacts source region 17 and body region 15, p⁺ dopant region 23 provides to a low resistivity path between contact 21s and body region 15.

169. Therefore, as Bulucea and Uno both relate to trench MOSFETs and, even more particularly, Uno discloses a Deep Body Trench Contact, a POSITA would be motivated to combine the teachings of Bulucea and Uno.

170. As shown in Uno's Fig. 11, circular trench contact 21s penetrates at a central portion of the cell through source region 17 surrounding trenched gates G(11) and extends into body region 15, which encompasses source region 17.

Therefore, Uno meets limitations [1b] and [1c] in Claim 1 of the '409 Patent.

FIG. 11



171. As shown also in Uno's Fig. 11, contact trench 21s is formed in a hole opened from a top surface 31s of the semiconductor substrate. Circular trench contact 21s is filled with a metal plug portion of source metal line SE (27). wherein sidewalls of said hole are surrounded by and in contact said source region 17 and body regions 15 and 23. Circular trench contact 21s is separate from trenched gates G(11) with source region 17 and body region 15 disposed between

gate oxide lining 9 of trenched gates G(11) and all circumferential points of circular trench contact 21s (horizontal cross section). The portion of source metal SE(27) that forms the contact metal plug in circular trench contact 21s is connected to source metal SE(27) disposed on top of circular trench contact 21s. Therefore, Bhalla's circular trench contact 21s meets limitations [1d], [1e] and [1f] in Claim 1 of the '409 Patent.

5) Huang

172. Huang discloses a trench MOSFET and a method of manufacturing thereof in Figs. 1-9 and 11. EX1008, 1:44-45, 49-50, Figs. 1-8, 11. In particular, Huang discloses trench contact 34 in a MOSFET and a method of its formation. EX1008, 5:31-46, Figs. 8-9.

173. Huang's Figs. 8-9 show trench contact 34 provided a p+ deep body diffusion 35 is implanted and metal layer 36 in contact with and above trench contact 34, respectively:

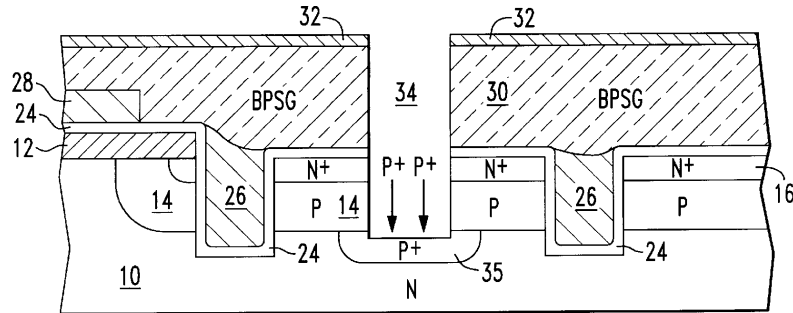


FIG. 8

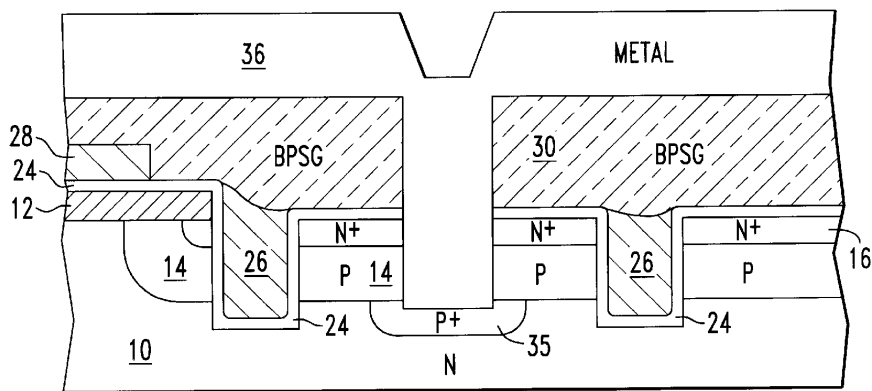


FIG. 9

EX1008, Figs. 8 and 9.

174. With respect to formation of trench contact 34, Huang states:

... as shown in FIG. 8, a fourth mask 32 may be conventionally formed over the BPSG layer 30 to thereby define [an] area for a third trench 34 which may be etched through the BPSG layer 30, the gate oxide 24, the N+ source 16, and the P channel area 14 into the N semiconductor 10. Once the trench 34 has been etched, a P type impurity may be implanted and driven into the N wafer to thereby

form a P+ area 35 of higher impurity concentration than the P channel region 14.

As illustrated in FIG. 9, a metal layer 36 may then be formed over both the BPSG area 30 to thereby establish a contact with the N+ source region and the P+ high concentration region 35 at the bottom of the trench 34 of FIG. 8.

EX1007, 5:43-59.

175. Thus, as seen from Fig. 8, as trench contact 34 reaches below the silicon surface to contact with buried layer 35 (i.e., p⁺ contact dopant region) immediately under trench contact 34, trench contact 34 is a Deep Body Trench Contact.

176. Note that Huang states that its buried layer 35 makes “it possible for the MOSFET to break down at the PN junction 35 and protect the trench gate 26.” EX1008, 3:48. This effect, which moves surface breakdowns from the trench gates to under the contact in the bulk silicon, is disclosed by Bulucea at EX1005, 7:11-28.

177. Therefore, as Bulucea and Huang both relate to trench MOSFETs and, even more particularly, Huang discloses a Deep Body Trench Contact, a POSITA would be motivated to combine the teachings of Bulucea and Huang.

178. As shown in Huang's Fig. 9, trench contact 34 penetrates at a central portion of the cell through source region 16 surrounding trenched gates 26 and extends into body region 14, which encompasses source region 16.

179. Trench contact 34 is formed in a hole opened from the top surface of the semiconductor substrate. Trench contact 34 is filled with a metal plug portion of source metal line 36.

180. The sidewalls of the hole are surrounded by and in contact said source region 16 and body regions 14. Trench contact 34 is separate from trenched gates 26 with source region 16 and body region 14 disposed between gate oxide lining 24 of trenched gates 26 and all points of trench contact 34 (horizontal cross section).

181. Fig. 9 also shows trench contact 34 is provided contact metal plug as a portion of metal layer 36 and is thus connected to the portion of metal 36 that is disposed on top of trench contact 34.

182. While Huang does not disclose that its trench contact is circular, in view that Bulucea teaches that such a polygon feature in a horizontal cross section would become substantially a circle or an oval using the Litho-rounding Technique, the combined teachings would render trench contact 34 circular, and all

the points in a horizontal cross section of trench contact 34 would become “circumferential.” Accordingly, applying the Litho-rounding Technique to Huang’s trench contact, Huang meets all limitations [1c]-[1f] in Claim 1 in the ’409 Patent.

6) Bhalla

183. Bhalla discloses a double-diffuse MOSFET (DMOS device) and a method of manufacturing thereof. EX1009, 4:42-6:29 and 6:57-67, Figs. 3A-3P and Fig.7. In particular, Bhalla discloses etching trench contacts 624 and 626 (Fig. 3N) and trench contact 625 (Fig. 7) in a trench MOSFET and a method of its formation. EX1009, 5:64-6:19, 57-67, Figs. 3N, 7, 3O-3P.

184. As shown in Fig. 3N, trench contact 624 reaches from the surface of the silicon substrate, through source region 612 (N^+) and body region 460 (P). EX1009, Fig. 3N.

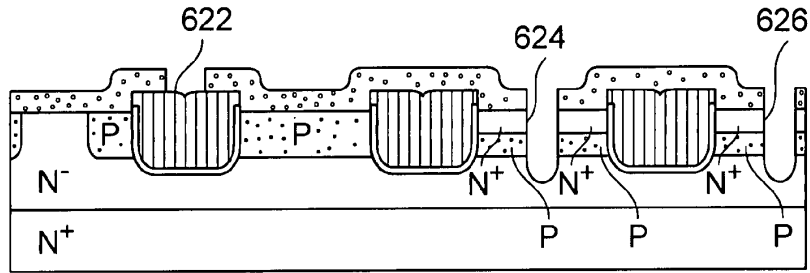


FIG. 3N

185. Alternatively, as Bhalla described at 6:58-62, in conjunction with Fig. 7, trench contact etch can be followed by forming p+ deep body diffusion region 607 at the bottom of contact trench 625:

... contact trench etch process is performed on a structure similar to **340** of FIG. 3M to form device **700**. After etch mask **614** is formed on the structure, contact trench etch is performed to form trench **625**. The depth of the trench may vary for different implementations. In the example shown, the bottom of trench **625** is controlled to be substantially coplanar to the source bottom. P⁺-type material is implanted to the bottom of the trench and then activated to form P⁺ region **607**.

EX1009, 6:58-62.

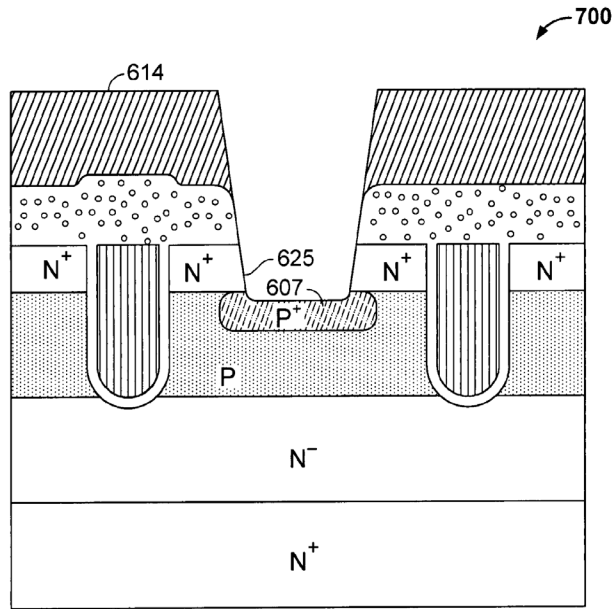


FIG. 7

EX1009, Fig. 7.

186. Thus, as seen from Bhalla's Figs. 3N and 7, as trench contact 625 reaches below the silicon surface to contact with p^+ contact dopant region 607 immediately under trench contact 625, trench contact 625 is a Deep Body Trench Contact.

187. Therefore, as Bulucea and Bhalla both relate to trench MOSFETs and, even more particularly, Bhalla discloses a Deep Body Trench Contact, a POSITA would be motivated to combine the teachings of Bulucea and Bhalla.

188. Bhalla teaches a circular trench contact to avoid breakdown due to high electric field, in conjunction with its description of the trench contact 624 in

Fig. 3N:

Since the trench such as **624** serve as contact openings where the metal and the semiconductor meet, sharp curvature in corner regions may lead to high electric fields and degrade device breakdown. In device **350** shown, *the trenches have round and smooth shapes without sharp corners*, thus avoiding low breakdowns due to high electric fields.

EX1009, 6:12-17.

189. Bhalla's Fig. 3P teaches providing a metal stack above, as well as filling, circular trench contact 624.

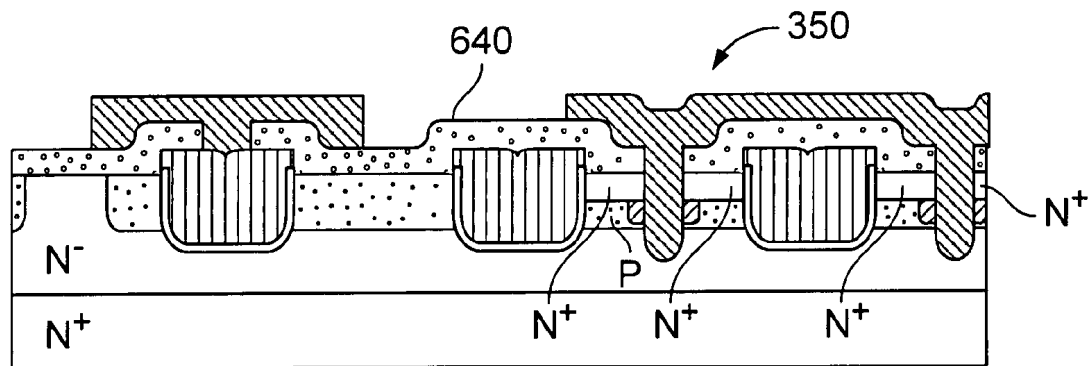


FIG. 3P

190. As seen in Bhalla's Fig. 3P, contact trench 624 penetrates at a central position in between gate trenches 44 through source region 612 surrounding said trenched gates and extending into a body region (460,630) encompassing said source region 612. Thus, Bhalla meets limitations [1b], [1c] and [1d] of the '409 Patent.

191. As shown in Figs. 3N-3P and described in Bhalla's 6:1-19, contact trench 624 comprises a hole opened from a top surface of the semiconductor substrate substantially in a central position between gate trenches 442.

192. Fig. 3P shows contact trench 624 is filled with a contact metal plug, being the portion of a metal stack filling the entire circular trench contact, consisting of Ti, TiN and Al-Si-Cu, wherein the sidewalls of the hole are surrounded by and in contact with source region 612 and body regions 460 and 630. Circular trench contact 624 separates from trenched gates 442 with source region 612 and body region 460 and 630 disposed between a gate oxide lining 430 of trenched gates 442 and all circumferential points of circular trench contact 624.

193. The contact metal plug in trench 624 is connected by the same metal stack disposed on top of the circular trench contact. Thus, Bhalla's circular trench contact 628 meets limitations [1e] and [1f] in Claim 1 of the '409 Patent.

194. In addition to teaching Ti, TiN, Al, Si and Cu in a metal stack for the metal plug and the metal layer on top (EX1009, 6:10-12), Bhalla also teaches using palladium, platinum, titanium and tungsten in trench contacts:

A layer of metal suitable for making Schottky contact with the lightly doped drain (such as titanium (Ti), platinum (Pt), palladium (Pd), tungsten (W) or any other appropriate material) is deposited on the bottom of source body contact trenches 112, 114 and 116, to form contact electrodes 122, 124 and 126, respectively.

EX1009, 3:58-63.

195. Thus, Bhalla's trench MOSFET also meets recited limitations [3]-[4] in Claims 3-4 of the '409 Patent.

196. Also, Bhalla teaches that its circular trench contact can be "approximately between 0.5-2.5 μm deep and approximately between 0.2-1.5 μm wide in some embodiments." Thus, Bhalla also meets the recited limitations [5] of the '409 Patent.

X. OPINIONS AS TO INVALIDITY OF THE ‘409 PATENT

1) Ground I – Claims 1-5 are obvious under 35 U.S.C. § 103 over Bulucea, in view of Hsieh

197. The following claim chart summarizes a combination of the relevant teachings of Bulucea and Hsieh, in which Bulucea’s source/body contact is modified to incorporate Hsieh’s source/body trench contact. The combination meets all limitations of and thus renders Claims 1-5 of the ‘409 Patent. Thus, each of these claims as a whole would have been obvious before the effective filing date of December 4, 2006 to a POSITA to which the claimed subject matter pertains.

Reference Signals	Claim Limitations	Prior Art Teachings
[1pre]	1.A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein	Bulucea teaches a trenched semiconductor power device formed by a group of transistor cells (square-cell geometry) in a semiconductor substrate. See, Bulucea’s Fig. 21 and Fig. 31A, 3:14-18.
[1a]	said trenched gates surrounding said transistor cells as closed cells	Bulucea teaches, in the semiconductor device of Fig. 21, trenched gates 35 surrounding the

Reference Signals	Claim Limitations	Prior Art Teachings
	constituting substantially square-shaped cells with rounded corners;	transistors cells as closed cells constituting substantially square-shaped cells with rounded corners. Fig.21, Fig. 31A. Bulucea teaches that the trenched gates surrounding the square closed-cell unit becomes “substantially square-shaped cells with rounded corners” (i) by lithographical development (7:53-66), or (ii) by a sacrificial oxidation step (6:1-6. Fig. 25A, 12:38-51).
[1b]	each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells,	Bulucea teaches that, using lithography development, a square feature can become circular (7:53-66); Bulucea shows a circular trench contact (Fig. 31A, portion of metallization layer 43B at the surface of the semiconductor surface, in contact with source region 28 and body region 27; 13:46-52). Bulucea’s teachings regarding latch-

Reference Signals	Claim Limitations	Prior Art Teachings
		back free design (5:33-37) and the p ⁺ deep body diffusion motivates a POSITA to modify Bulucea's circular contact to incorporate a circular trench contact, such as shown in Hshieh's cylindrical shaped source-body trench contact (i.e., a circular source-body trench contact) shown in Hshieh's Figs. 3A-3E, paragraphs [0027]-[0028].
[1c]	penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;	Hshieh shows in Fig. 3C, for example, circular trench contact 180 penetrating through source region 130 surrounding trenched gates 120 and extending into body region 125, which encompasses source region 130 (See, also, Hshieh's paragraph [0027]).
[1d]	said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and	Hshieh's Fig. 3C shows, for example, circular trench contact 180 comprises a hole opened from a top surface of the semiconductor

Reference Signals	Claim Limitations	Prior Art Teachings
	is filled with a contact metal plug	substrate and is filled with a contact metal plug (Fig. 3C labels it as “Ti/TiN/W Plug”). See also, Hshieh’s paragraphs [0027]-[0028].
[1e]	wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact; and	Hshieh’s Fig. 3C shows, for example, sidewalls of the hole (i.e., filled circular trench contact 180) are surrounded by and in contact source region 130 and body region 125 and circular trench contact 180 is separate from trenched gates 120 with source region 130 and body region 125 disposed between gate oxide lining 115 of trenched gates 120 and all circumferential points (i.e., the circumference of a horizontal cross section) of circular trench contact 180; See also, Hshieh’s paragraph [0027].
[1f]	said contact metal plug connected to a source metal disposed on top of said	Hshieh’s Fig. 3C, for example, shows the contact metal plug in circular trench contact 180

Reference Signals	Claim Limitations	Prior Art Teachings
	circular trench contact.	connected to source metal 140 disposed on top of circular trench contact 180. See also, Hshieh's paragraph [0028].
[2]	2. The trenched semiconductor power device of claim 1 further comprising: a contact resistance reduction metal layer composed of a titanium (Ti) layer disposed above a top surface said contact metal plug and below a bottom surface of said source metal for reducing a contact resistance between said contact metal plug and said source metal.	In its paragraph [0013] Hshieh teaches, "... In a preferred embodiment, the thin resistance-reduction conductive layer includes a titanium (Ti) layer. In a preferred embodiment, the thin resistance-reduction conductive layer includes a titanium nitride (TiN) layer a contact resistance reduction metal layer composed of a titanium (Ti) layer disposed above a top surface said contact metal plug and below a bottom surface of said source metal for reducing a contact resistance between said contact metal plug and said source metal."
[3]	3. The trenched semiconductor power device	Hshieh's Fig. 3C indicates that trench contact 180 comprises a

Reference Signals	Claim Limitations	Prior Art Teachings
	of claim 1 wherein: said contact metal plug disposed in said hole of said circular trench contact further comprising a Ti/TiN/W metal plug.	Ti/TiN/W plug. See, also, Figs. 3F, 5D-1, 5E-1, 5D', and 5E'.
[4]	The trenched semiconductor power device of claim 1 wherein: said source metal disposed on top of and in contact with a top surface of said metal plug further comprising a layer composed of aluminum alloys including alloys of AlCu or AlSiCu.	In paragraph [0031], Hshieh teaches: “In FIGS. 5E-1 and 5E-2, a low resistance metal layer 260 is deposited over the top surface. The low resistance metal layer may be composed of Ti/AlCu or Ti/TiN/AlCu to assure good electric contact is established followed by a metal etch to pattern the metal layer into a source metal pad 260 and a gate metal pads 270 in electrical contact with the source-body trench- plug 245 and the gate-runner trench plug 250 respectively.”
[5]	5. The trenched semiconductor power device	In ¶ [0030], Hshieh teaches forming 0.4µm trench contact using chemical

Reference Signals	Claim Limitations	Prior Art Teachings
	of claim 1 wherein: a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer.	vapor deposition (CVD): “The tungsten plug is formed with the chemical vapor deposition (CVD) process and the chemical vapor has much better filling characteristics to fill the narrow and deep contact openings without development of void. The CVD process is suitable for process of circuits with critical dimension (CD) less than 0.4 micrometer (μms) in the semiconductor industries.”

198. Based on the above, I conclude Claims 1-5 are obvious under 35 U.S.C. § 103 over Bulucea, in view of Hsieh.

2) Ground II – Claim 1 is obvious under 35 U.S.C. § 103 over Bulucea, in view of Uno

199. The following claim chart summarizes a combination of the relevant teachings of Bulucea and Uno, in which Bulucea’s source/body contact is modified to incorporate Uno’s source/body trench contact. The combination meets all

limitations of and thus renders Claim 1 of the '409 Patent. Thus, Claim 1 as a whole would have been obvious before the effective filing date of December 4, 2006 to a POSITA to which the claimed subject matter pertains.

Reference Signals	Claim Limitations	Prior Art Teachings
[1pre]	1.A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein	Bulucea teaches a trenched semiconductor power device formed by a group of transistor cells (square-cell geometry) in a semiconductor substrate. See, Bulucea's Fig. 21 and Fig. 31A, 3:14-18.
[1a]	said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;	Bulucea teaches, in the semiconductor device of Fig. 21, trenched gates 35 surrounding the transistors cells as closed cells constituting substantially square-shaped cells with rounded corners. Fig.21, Fig. 31A. Bulucea teaches that the trenched gates surrounding the square closed-cell unit becomes

Reference Signals	Claim Limitations	Prior Art Teachings
		<p>“substantially square-shaped cells with rounded corners” (i) by lithographical development (7:53-66), or (ii) by a sacrificial oxidation step (6:1-6. Fig. 25A, 12:38-51).</p>
[1b]	<p>each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells,</p>	<p>Bulucea teaches that, using lithography development, a square feature can become circular (7:53-66); Bulucea shows a circular trench contact (Fig. 31A, portion of metallization layer 43B at the surface of the semiconductor surface, in contact with source region 28 and body region 27; 13:46-52).</p> <p>Bulucea’s teachings regarding latch-back free design (5:33-37) and the p⁺ deep body diffusion motivates a POSITA to modify Bulucea’s circular contact to</p>

Reference Signals	Claim Limitations	Prior Art Teachings
		<p>incorporate a circular trench contact, such as that disclosed in Uno.</p> <p>Uno also discloses Bulucea's deep body diffusion approach in Fig. 12, showing that, when contact 21s contacts source region 17 and body region 15, p⁺ dopant region 23 provides to a low resistivity path between contact 21s and body region 15.</p>
[1c]	penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;	As shown in Uno's Fig. 11, circular trench contact 21s penetrates at a central portion of the cell through source region 17 surrounding trenched gates G(11) and extends into body region 15, which encompasses source region 17.
[1d]	said circular trench contact comprises a hole opened from a top surface of said	As shown in Uno's Fig. 11, circular contact trench 21s is formed in a hole opened from a

Reference Signals	Claim Limitations	Prior Art Teachings
	semiconductor substrate and is filled with a contact metal plug	top surface 31s of the semiconductor substrate. Circular trench contact 21s is filled with a metal plug portion of source metal line SE (27).
[1e]	wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact; and	Sidewalls of the hole of circular contact trench 21s are surrounded by and in contact source region 17 and body regions 15 and 23. Circular trench contact 21s is separate from trenched gates G(11) with source region 17 and body region 15 disposed between gate oxide lining 9 of trenched gates G(11) and all circumferential points of circular trench contact 21s (horizontal cross section).
[1f]	said contact metal plug connected to a source metal disposed on top of said circular trench contact.	In Uno's Fig. 11, the portion of source metal SE(27) that forms the contact metal plug in circular trench contact 21s is connected

Reference Signals	Claim Limitations	Prior Art Teachings
		to source metal SE(27) disposed on top of circular trench contact 21s.

200. Based on the above, I conclude Claim 1 is obvious under 35 U.S.C. § 103 over Bulucea, in view of Uno.

3) Ground III– Claim 1 is obvious under 35 U.S.C. § 103 over Bulucea, in view of Huang

201. The following claim chart summarizes a combination of the relevant teachings of Bulucea and Huang, in which Bulucea’s source/body contact is modified to incorporate Huang’s source/body trench contact. The combination meets all limitations of and thus renders Claim 1 of the ‘409 Patent. Thus, Claim 1 as a whole would have been obvious before the effective filing date of December 4, 2006 to a POSITA to which the claimed subject matter pertains.

Reference Signals	Claim Limitations	Prior Art Teachings
[1pre]	1.A trenched semiconductor	Bulucea teaches a trenched

Reference Signals	Claim Limitations	Prior Art Teachings
	power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein	semiconductor power device formed by a group of transistor cells (square-cell geometry) in a semiconductor substrate. See, Bulucea's Fig. 21 and Fig. 31A, 3:14-18.
[1a]	said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;	Bulucea teaches, in the semiconductor device of Fig. 21, trenched gates 35 surrounding the transistors cells as closed cells constituting substantially square-shaped cells with rounded corners. Fig.21, Fig. 31A. Bulucea teaches that the trenched gates surrounding the square closed-cell unit becomes "substantially square-shaped cells with rounded corners" (i) by lithographical development (7:53-66), or (ii) by a sacrificial oxidation step (6:1-6. Fig. 25A, 12:38-51).
[1b]	each of said closed cells further	Bulucea teaches that, using

Reference Signals	Claim Limitations	Prior Art Teachings
	<p>includes a circular trench contact disposed substantially in a central portion of said closed cells,</p>	<p>lithography development, a square feature can become circular (7:53-66); Bulucea shows a circular trench contact (Fig. 31A, portion of metallization layer 43B at the surface of the semiconductor surface, in contact with source region 28 and body region 27; 13:46-52).</p> <p>Bulucea's teachings regarding latch-back free design (5:33-37) and the p⁺ deep body diffusion motivates a POSITA to modify Bulucea's circular contact to incorporate a trench contact, such as shown in Huang's Figs. 8-9. Figs. 8-9 show trench contact 34 being provided above where p⁺ deep body diffusion 35 is implanted; p⁺ deep body diffusion 35 is contacted by metal layer 36 in trench contact 34.</p>

Reference Signals	Claim Limitations	Prior Art Teachings
[1c]	penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;	As shown in Huang's Fig. 9, trench contact 34 penetrates at a central portion of the cell through source region 16 surrounding trenched gates 26 and extends into body region 14, which encompasses source region 16.
[1d]	said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug	Trench contact 34 is formed in a hole opened from the top surface of the semiconductor substrate. Trench contact 34 is filled with a metal plug portion of source metal line 36.
[1e]	wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates	The sidewalls of the hole filled by the contact metal plug of trench contact 34 are surrounded by and in contact source region 16 and body region 14. Trench contact 34 is separate from trenched gates 26 with source region 16 and body region 14 disposed between gate oxide lining 24 of trenched gates

Reference Signals	Claim Limitations	Prior Art Teachings
	and all circumferential points of the circular trench contact; and	26 and all points of trench contact 34 (horizontal cross section). (While Huang does not disclose that its trench contact is circular, in view that Bulucea teaches that such a polygon feature in a horizontal cross section would become substantially a circle or an oval using lithographical development, the combined teachings would render trench contact 34 circular, and all the points in a horizontal cross section of trench contact 34 would become “circumferential.”
[1f]	said contact metal plug connected to a source metal disposed on top of said circular trench contact.	Fig. 9 also shows trench contact 34 is provided contact metal plug as a portion of metal layer 36 and is thus connected to the portion of metal 36 that is disposed on top of trench contact 34.

202. Based on the above, I conclude Claim 1 is obvious under 35 U.S.C. § 103 over Bulucea, in view of Huang.

4) Ground IV– Claims 1 and 3-5 are obvious under 35 U.S.C. § 103 over Bulucea, in view of Bhalla

203. The following claim chart summarizes a combination of the relevant teachings of Bulucea and Bhalla, in which Bulucea’s source/body contact is modified to incorporate Bhalla’s source/body trench contact. The combination meets all limitations of and thus renders Claims 1 and 3-5 of the ‘409 Patent. Thus, each of these claims as a whole would have been obvious before the effective filing date of December 4, 2006 to a POSITA to which the claimed subject matter pertains.

Reference Signals	Claim Limitations	Prior Art Teachings
[1pre]	1.A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a	Bulucea teaches a trenched semiconductor power device formed by a group of transistor cells (square-cell geometry) in a semiconductor substrate.

Reference Signals	Claim Limitations	Prior Art Teachings
	semiconductor substrate, wherein	See, EX1005, Fig. 21 and Fig. 31A, 3:14-18.
[1a]	said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;	Bulucea teaches, in the semiconductor device of Fig. 21, trenched gates 35 surrounding the transistors cells as closed cells constituting substantially square-shaped cells with rounded corners. Fig.21, Fig. 31A. Bulucea teaches that the trenched gates surrounding the square closed-cell unit becomes “substantially square-shaped cells with rounded corners” (i) by lithographical development (7:53-66), or (ii) by a sacrificial oxidation step (6:1-6. Fig. 25A, 12:38-51). .
[1b]	each of said closed cells further includes a circular trench contact disposed substantially in a	Bulucea teaches that, using lithography development, a square feature can become

Reference Signals	Claim Limitations	Prior Art Teachings
	central portion of said closed cells,	<p>circular (7:53-66); Bulucea shows a circular trench contact (Fig. 31A, portion of metallization layer 43B at the surface of the semiconductor surface, in contact with source region 28 and body region 27; 13:46-52).</p> <p>Bulucea's teachings regarding latch-back free design (5:33-37) and the p⁺ deep body diffusion motivates a POSITA to modify Bulucea's circular contact to incorporate a circular trench contact, such as shown in Bhalla, which describes at 6:58-62, in conjunction with Fig. 7, trench contact etch can be followed by forming p⁺ deep body diffusion region 607 at the bottom of contact trench 625.</p>
[1c]	penetrating through a source	Bhalla teaches a circular trench

Reference Signals	Claim Limitations	Prior Art Teachings
	<p>region surrounding said trenched gates and extending into a body region encompassing said source region;</p>	<p>contact to avoid breakdown due to high electric field, in conjunction with its description of the trench contact 624 in Figs. 3N-3P. Specifically, Bhalla teaches device 350 in Fig, 3P, which shows <i>the trenches have round and smooth shapes without sharp corners</i>, thus avoiding low breakdowns due to high electric fields.” EX1009, 6:12-17.</p> <p>As seen in Bhalla’s Fig. 3P, contact trench 624 penetrates at a central position in between gate trenches 442 through source region 612 surrounding said trenched gates 442 and extending into a body region (460,630) encompassing said source region 612.</p>
[1d]	said circular trench contact	As shown in Figs. 3N-3P and

Reference Signals	Claim Limitations	Prior Art Teachings
	<p>comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug</p>	<p>described in Bhalla's 6:1-19, circular trench contact 624 comprises a hole opened from a top surface of the semiconductor substrate substantially in a central position between gate trenches 442.</p> <p>Fig. 3P shows circular trench contact 624 is filled with a contact metal plug, being the portion of a metal stack filling the entire circular trench contact, consisting of Ti, TiN and Al-Si-Cu.</p>
[1e]	<p>wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched</p>	<p>The sidewalls of the hole that is filled by the contact metal plug of circular trench contact 624 are surrounded by and in contact with source region 612 and body regions 460 and 630.</p> <p>Circular trench contact 624 separates from trenched gates</p>

Reference Signals	Claim Limitations	Prior Art Teachings
	gates and all circumferential points of the circular trench contact; and	442 with source region 612 and body region 460 and 630 disposed between a gate oxide lining 430 of trenched gates 442 and all circumferential points of circular trench contact 624.
[1f]	said contact metal plug connected to a source metal disposed on top of said circular trench contact.	The contact metal plug in trench 624 is connected by the same metal stack disposed on top of the circular trench contact.
[3]	3. The trenched semiconductor power device of claim 1 wherein: said contact metal plug disposed in said hole of said circular trench contact further comprising a Ti/TiN/W metal plug.	Bhalla teaches having Ti, TiN, and Al-Si-Cu in a metal stack for the contact metal plug and the metal layer on top (EX1009, 6:10-12). Bhalla also teaches using palladium, platinum, titanium and tungsten in trench contacts. EX1009, 3:58-63. Thus, Bhalla teaches having Ti, TiN and W in a contact metal plug.
[4]	The trenched semiconductor	Bhalla teaches Ti, TiN, and Al-

Reference Signals	Claim Limitations	Prior Art Teachings
	<p>power device of claim 1 wherein: said source metal disposed on top of and in contact with a top surface of said metal plug further comprising a layer composed of aluminum alloys including alloys of AlCu or AlSiCu.</p>	<p>Si-Cu in a metal stack for the contact metal plug and the metal layer on top (EX1009, 6:10-12).</p>
[5]	<p>5. The trenched semiconductor power device of claim 1 wherein: a diameter of a top surface of said circular trench contact is smaller than 1.0 micrometer.</p>	<p>Bhalla teaches that its circular trench contact can be “approximately between 0.5-2.5 μm deep and approximately between 0.2-1.5 μm wide in some embodiments.” EX1009, 5:5-7.</p>

204. Based on the above, I conclude Claims 1 and 3-5 are obvious under 35 U.S.C. § 103 over Bulucea, in view of Bhalla.

5) GROUND V – Anticipation by Admitted Prior Art

205. The following claim chart summarizes the anticipation of Claims 1 and 3-4 of the '409 Patent.

Reference Signals	Claim Limitations	Prior Art Teachings
[1pre]	1. A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein	Admitted prior art at Fig. 1C shows a trenched semiconductor power device formed by a group of transistor cells (square-cell geometry) in a semiconductor substrate. See, EX1001, 1:28-33, Figs. 1A, 1B and 1C.
[1a]	said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;	Admitted prior art at Fig. 1C shows trenched gates 20 surrounding transistor cells as closed cells constituting substantially square-shaped cells with rounded corners (the “rounded corners” are inherent, as a result of the lithographical process).;

Reference Signals	Claim Limitations	Prior Art Teachings
[1b]	each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells,	Admitted prior art at Fig. 1C shows the closed cell further includes circular trench contact 15 disposed substantially in a central portion of the closed cell (i.e., equidistance between trenched gates 20.). The “circular trench contact” is inherent, as a result of the lithographical process,
[1c]	penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;	Circular trench contact 15 in the admitted prior art of Fig. 1C penetrates through source region n ⁺ surrounding trenched gates 20 and extends into body region P encompassing source region n ⁺ ;
[1d]	said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug	The circular trench contact at admitted prior art at Fig. 1C of the ‘408 Patent includes a hole opened from a top surface of the semiconductor substrate (i.e., the top surface of source region n ⁺)

Reference Signals	Claim Limitations	Prior Art Teachings
		and is filled with a contact metal plug indicated by the label “Ti/TiN/W” for titanium, titanium nitride and tungsten.
[1e]	wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact; and	The admitted prior art in Fig. 1C of the ‘409 Patent shows the sidewalls of circular trench contact 15 is surrounded by and in contact with source n+ and body region P and circular trench contact 15 is separate from trenched gates 20 with source region n+ and body region P disposed between the gate oxide lining adjacent trenched gates 20 and all circumferential points of circular trench contact 15; and
[1f]	said contact metal plug connected to a source metal disposed on top of said circular trench contact.	Admitted prior art in Fig. 1 of the ‘409 Patent shows the contact metal plug (labeled “Ti/TiN/W”) connected to a source metal

Reference Signals	Claim Limitations	Prior Art Teachings
		(labeled “source metal”) disposed on top of circular trench contact.15.
[3]	3. The trenched semiconductor power device of claim 1 wherein: said contact metal plug disposed in said hole of said circular trench contact further comprising a Ti/TiN/W metal plug.	Admitted prior art at Fig. 1C of the ‘409 Patent indicates that circular trench contact 15 comprises a Ti/TiN/W plug.
[4]	The trenched semiconductor power device of claim 1 wherein: said source metal disposed on top of and in contact with a top surface of said metal plug further comprising a layer composed of aluminum alloys including alloys of AlCu or AlSiCu.	Admitted prior art in Fig. 1C of the ‘409 Patent shows the source metal disposed on top of and in contact with a top surface of the metal plug (labeled “Ti/TiN/W”) further comprises a layer composed of aluminum alloys (labeled “Al alloys”).

206. Based on the above, I conclude Claims 1 and 3-4 as anticipated by admitted prior art in Figs. 1A, 1B and 1C under 35 U.S.C. § 102(a), 102(b) or 102(c).

6) Enablement

207. Based on my experience working with hexagonal cells, Bulucea's hexagonal cell is the best closed-cell unit for a trench MOSFET. As Bulucea points out above, "circles are the preferred shapes from the point of view of maximizing the gate oxide rupture voltage" and also for reducing occurrences of bipolar latch-up at the rounded angles. EX1005, 7:57-66. However, circles waste space, as the resulting MOSFET is less operating area. Likewise, octagons are also wasteful in space, as they cannot tessellate a plane.

208. in its Fig. 7, Uno discloses octagonal closed-cell units. EX1007, Fig. 7/ These octagonal closed-cell units show wasted space, for both minimum cell spacing and larger than minimum cell spacing. Such "wasted space" shows up in the trenched gate, causing a difficulty in filling the trench during conformal deposition of polysilicon, as the deposited silicon fills the trench from the sidewalls to the center. The wasted space also prolongs both the time required to fill the wider trenches, and the time required for etching back the excess deposition from the surface. Unfilled space in a trench cause problems.

209. A square closed-unit cell with truncated corners is essentially an octagon with two alternating sizes of sides. Thus, when one modifies a square closed-cell unit in a trench MOSFET to one with truncated corners, as taught in Fig. 2 of the '409 Patent, the resulting closed-cell unit would waste more space than the closed-unit cells of Uno's Fig 7, because of their large wasted space at each corner.

210. Hence, I believe the '409 Patent does not enable a POSITA to make and use its claimed invention. The trench MOSFET of the '409 Patent, with its trench gates with truncated corners, cannot be manufactured using the same trench-fill process optimized for the gate trench of the conventional square closed-cell unit, with its uniform size, usually at design minimum width, even with allowance for the slightly larger space where the trenches meet. A new trench process must be developed for the closed-cell unit in Fig. 2 of the '409 Patent. The lesser space available for carrying current in modified power transistor of the '409 Patent is also highly undesirable. A POSITA would prefer adopting the closed-cell unit of Bulucea's Fig. 8. EX1005, Fig. 8.

XI. DECLARATION

211. I understand this declaration will be used as evidence in a contested case before the PTAB.

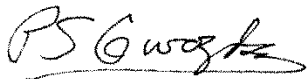
212. I am aware that willfully false statements in connection with this declaration are punishable by fine or imprisonment, or both under 18 U.S.C. § 1001 and may jeopardize the validity of the Petition.

213. All statements herein are made of my own knowledge true and all statements made on information and belief are believed to be true.

214. I declare under penalty of perjury that the foregoing is true and correct.

Executed on April 22, 2025 in Cupertino, Santa Clara County, CA.

Respectfully Submitted,

A handwritten signature in black ink, appearing to read "P S Gwozdz", with a horizontal line underneath.

Peter S. Gwozdz, Ph.D.