

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner

v.

ADVANCED CLUSTER SYSTEMS, INC.,
Patent Owner

IPR2025-00862
IPR2025-00863
U.S. Patent No. 10,333,768

**DECLARATION OF MELISSA SMITH, Ph.D.,
UNDER 37 C.F.R. § 1.68 IN SUPPORT OF PATENT OWNER'S
DISCRETIONARY DENIAL BRIEF**

I. INTRODUCTION

1. I, Melissa Smith, Ph.D., am making this declaration at the request of Patent Owner, Advanced Cluster Systems, Inc., (“ACS”) in the matter of the *Inter Partes* Review Nos. IPR2025-00862 and IPR2025-00863 of U.S. Patent No. 10,333,768 (“the ’768 Patent”). I understand that this declaration is being submitted in each of the IPRs as Exhibit 2010.

2. I am being compensated for my work in this matter at my standard hourly rate for consulting services. My compensation in no way depends on the outcome of this proceeding.

3. In conducting the analysis and forming the opinions set forth in this Declaration, I considered, in addition to my knowledge and expertise in the relevant field, at least the following written materials:

- ’768 Patent, Ex. 1001¹;
- Prosecution history of the ’768 Patent, Ex. 1002;
- AMD Petitions in IPR2025-00862 (Paper 1) and IPR2025-00863 (Paper 1);
- Declaration of Dr. Chandrajit L. Bajaj (“Bajaj Decl.”), Ex. 1003;
- *Curriculum Vitae* – Dr. Chandrajit L. Bajaj, Ex. 1004;

¹ Petitioner’s Exhibit Nos. identified herein are the same between IPR2025-00862 and IPR2025-00863.

- “MultiMATLAB: Integrating MATLAB with High-Performance Parallel Computing,” Menon et al., SC '97: Proceedings of the 1997 ACM/IEEE Conference on Supercomputing 1997 (“Menon”), Ex. 1005;
- “MultiMATLAB: MATLAB on Multiple Processors,” Trefethen et al., Cornell University 1996 (“Trefethen”), Ex. 1006;
- “RS/6000 SP: Planning Vol. 1, Hardware and Physical Environment,” IBM 2001 (“RS/6000”), Ex. 1007; and
- “The RS/6000 SP Inside Out”, Ex. 1010.

II. PROFESSIONAL BACKGROUND AND QUALIFICATIONS

4. I am a Professor in the Holcombe Department of Electrical and Computer Engineering at Clemson University. I received my Ph.D. in Computer Engineering from the University of Tennessee in 2003, and my M.S. and B.S. degrees in electrical engineering from Florida State University in 1994 and 1993, respectively.

5. My expertise includes high-performance computing (“HPC”), parallel processing, computer architecture, and reconfigurable computing systems. I worked for over a decade at Oak Ridge National Laboratory and have taught and conducted funded research in cluster computing, FPGAs, and scalable hardware/software systems for nearly 20 years.

6. I currently teach courses on digital systems design, FPGA and GPU accelerator systems, and high-performance architectures. I have advised numerous graduate students on HPC-related topics and served as Co-Chair of the Frederick National Laboratory Advisory Committee from 2018–2021, advising NCI/DOE collaborations on supercomputing in cancer research.

7. I have authored or co-authored many peer-reviewed papers in these fields. A current copy of my *curriculum vitae* is attached as Exhibit 2011.

III. SCOPE OF TESTIMONY

8. I understand that these IPRs involve a number of subjects related to the patentability of certain claims of the '768 Patent. For example, I understand that the ultimate question of whether the claims of the '768 Patent would have been obvious in view of the prior art at the relevant time is at issue in these IPRs. However, I understand that my testimony in these IPRs is limited in scope and that I have been asked to testify regarding a limited set of subjects relevant to these IPRs. The specific topics that I have been asked to address are listed in the lettered, bold headings of the section of this declaration labeled “SUBSTANTIVE TESTIMONY.” I have spent a significant amount of time, over multiple days, to analyze and express opinions about the specific topics addressed in this declaration.

9. With respect to these IPRs, I have not analyzed nor expressed any opinion, nor endeavored to analyze or express an opinion, about any subject that is

not expressly included in the section labeled “SUBSTANTIVE TESTIMONY.” While I could, if given sufficient time, analyze and express an opinion concerning additional subjects related to the field of the invention that are not expressly included in this declaration, doing so would require a significant investment of time, over multiple days, similar to the significant amount of time I devoted to the issues addressed in this declaration.

IV. RELEVANT LEGAL STANDARDS

10. I am an electrical and computer engineer by training and profession. The opinions I am expressing in this declaration involve the application of my knowledge and experience to the evaluation of the '768 Patent and certain prior art with respect to the '768 Patent. My knowledge of patent law is that of a lay person, albeit one who has had some experience relevant to patent law. Therefore, the attorneys who represent ACS have provided me with guidance as to the applicable patent law in this matter. The paragraphs below express my understanding of how I must apply current principles related to patentability to my analysis.

11. I understand that, in assessing the patentability of a patent claim, the Patent Office generally construes claim terms by giving them their ordinary and customary meaning as they would have been understood by a person of ordinary skill in the art (“POSITA”) at the time of the invention in view of the intrinsic record (*e.g.*, patent specification and file history). However, I understand that the inventors

may, in the patent specification, expressly define a claim term to have a meaning that differs from the term's ordinary and customary meaning. I also understand that the inventors may disavow or disclaim certain claim scope, thereby departing from the ordinary and customary meaning, when the intrinsic record demonstrates that a clear and unambiguous disavowal or disclaimer has occurred. I understand that extrinsic evidence, such as relevant technical literature and dictionaries, may be useful in ascertaining how a POSITA would have understood a claim term, but the intrinsic record is the primary source for determining the meaning of claim terms. For the purposes of this review and to the extent necessary, I have interpreted each claim term in accordance with the principles set forth in this paragraph.

12. It is my understanding that a claim is unpatentable as "anticipated" under 35 U.S.C. § 102 only if a single prior art reference discloses, expressly or inherently, every limitation of the claim, arranged as in the claim. I understand that a prior art reference does not anticipate a claim, however, when it discloses multiple, distinct teachings that a person of ordinary skill in the art might somehow combine to achieve the claimed invention. I understand that anticipation has not been alleged and, thus, is not at issue in these IPRs.

13. I understand that a claim is unpatentable under 35 U.S.C. § 103 only if the claimed subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the alleged invention. I also understand that an

obviousness analysis takes into account the following factors, which are sometimes referred to as the *Graham* factors: (1) the scope and content of the prior art, (2) the differences between the claimed subject matter and the prior art, (3) the level of ordinary skill in the art at the time of the invention, and (4) “objective indicia of nonobviousness,” also referred to as secondary considerations of non-obviousness. Those objective indicia include considerations such as whether a product covered by the claims is commercially successful due to the merits of the claimed invention, whether there was a long-felt need for the solution provided by the claimed invention, whether others failed to find the solution provided by the claimed invention, whether others copied the claimed invention, and whether there was acceptance by others of the claimed invention as shown by praise from others in the field.

14. In determining the scope and content of the prior art, it is my understanding that a reference is considered appropriate prior art if it falls within the field of the inventor’s endeavor. In addition, a reference is appropriate prior art if it is reasonably pertinent to the particular problem with which the inventor was involved. A reference is reasonably pertinent if it logically would have commended itself to an inventor’s attention in considering his problem. If a reference relates to the same problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

15. To assess the differences between prior art and the claimed subject matter, it is my understanding that 35 U.S.C. § 103 requires the claimed invention to be considered as a whole. This “as a whole” assessment requires showing that one of ordinary skill in the art at the time of invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would have selected the elements from the prior art and combined them in the claimed manner.

16. It is my further understanding that the courts have recognized several rationales for combining references or modifying a reference to show obviousness of claimed subject matter. Some of these rationales include combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to obtain predictable results; a predictable use of prior art elements according to their established functions; applying a known technique to a known device (method or product) ready for improvement to yield predictable results; choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and some teaching, suggestion, or motivation that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

17. I understand that an assessment of what a reference discloses or teaches – for purposes of an anticipation analysis or an obviousness analysis – must

be conducted from the perspective of a POSITA at the time of the invention. In other words, a reference discloses or teaches a claim limitation if a POSITA would, at the relevant time, interpret the reference as expressly, implicitly, or inherently disclosing the claim limitation. I further understand that a reference does not need to use the exact language of the claim to disclose a claim limitation.

18. I further understand that expert testimony in IPR proceedings must be supported by objective evidence and that conclusory opinions lacking factual substantiation are entitled to little or no weight.

19. I understand that a patent owner may attempt to establish a date of invention that is earlier than the effective filing date of the patent. However, I understand that ACS is not attempting to establish an earlier invention date for the purpose of these IPRs, and, thus, for the purpose of these IPRs, the time of the invention (also called the “relevant time” herein) is the effective filing date of the ’768 Patent. I understand that the earliest possible effective filing date of the ’768 Patent is June 13, 2006, and that Petitioner has not alleged that the ’768 Patent is not entitled to the June 13, 2006, filing date. Accordingly, I have assumed that June 13, 2006, is the time of invention or relevant time for purposes of these IPRs.

V. SUBSTANTIVE TESTIMONY

A. The field of the invention and the level of ordinary skill in the art.

20. I was asked to assess the field of the invention of the '768 Patent and the level of ordinary skill in the art. In making this assessment, I have considered the '768 Patent, my experience, and the testimony of Petitioner's expert, Dr. Bajaj.

21. In my opinion, the field of the invention of the '768 Patent is "cluster computing." This is supported by the "Field of Disclosure" section of the patent, the specification generally, and the claims. The "Field of Disclosure" section states: "The present disclosure relates to the field of cluster computer generally" The specification of the '768 Patent consistently discloses aspects of a computer cluster or methods of operating a computer cluster. And every challenged claim expressly recites a "computer cluster."

22. In my opinion, a POSITA would have had a Bachelor's degree in computer science, electrical engineering, or an equivalent field, and two years of academic or industry experience in cluster computing and parallel computation techniques. Additional academic training could substitute for some practical experience. In conducting my analysis set forth in this Declaration, I applied this identification of the level of ordinary skill in the art. However, my conclusions would not change even assuming that Dr. Bajaj's identification of the level of ordinary skill in the art (*see*, Ex. 1003, ¶¶ 18-21) were correct.

23. At the time of the invention and presently, I did and do have more training, expertise, and knowledge than a POSITA. However, I understand what a POSITA would have known and understood at the relevant time, and my testimony herein is from the perspective of a POSITA at the relevant time.

B. The Petition does not show that the prior art discloses or suggests a “hardware processor with a plurality of processing cores” or a “hardware processor [that] comprises multiple processor cores.”

24. I have reviewed the Petitions (IPR2025-00862 (Paper 1) and IPR2025-00863 (Paper 1)), the declaration of Dr. Chandrajit L. Bajaj (Ex. 1003), the RS/6000 SP: Planning Vol. 1, Hardware and Physical Environment reference (Ex. 1007), The RS/6000 SP Inside Out reference (Ex. 1010) along with other prior art references cited by Petitioner.

25. I understand that all of the challenged claims of the '768 Patent require a “hardware processor with a plurality of processing cores” or similar language. *See*, Ex. 1001, at independent claims 1, 26, 29 (“hardware processor with a plurality of processing cores”) (col 30, lines 44-45, 51-52; col. 32, lines 54-55, 60-61; and col. 33, lines 62-62, col. 34, lines 1-2, respectively); *id.* at independent claim 35 (“wherein the hardware processor comprises multiple processor cores” and “hardware processor with a plurality of processing cores”) (col., 35, lines 18-19 and lines, 38-40, respectively). It is my understanding that, because every other claim depends from one of these independent claims, every claim of the '768 Patent

requires a hardware processor with a plurality of processing cores (claims 1, 26, 29, and their dependent claims) or that comprises multiple processor cores (claim 35 and its dependent claims, this claim also includes an element that requires a plurality of processing cores).

26. I understand that Dr. Bajaj did not assign any specific meaning to the terms, “hardware processor,” “plurality,” or “processing cores.” (Ex. 1003, ¶¶ 60-72). I agree that these are well-known terms and that they should receive, and I have applied, their plain and ordinary meaning as they would be understood by a POSITA at the time of the invention.

27. The Petitions allege that “RS6000 also teaches that each node has a ‘Symmetric MultiProcessor (SMP)’ (‘hardware processor’) and that each SMP includes ‘four, eight, twelve, or sixteen 375 MHz 630FP 64-bit processors’ (plurality of processing cores).” IPR2025-00862 Pet. at 48 (citing Ex. 1007, 2², 9); IPR2025-00863 Pet. at 50 (same). Dr. Bajaj also contends that the IBM RS/6000 SP system satisfies this limitation, asserting that its “Symmetric MultiProcessor (SMP)” includes a “hardware processor with a plurality of processing cores.” (Ex. 1003, ¶ 185).

² All page number citations to exhibits reference the unique numbering added for the IPR that is stamped in the right corner of the document.

28. The allegations of Dr. Bajaj and the Petitions in the preceding paragraph are incorrect. The RS/6000 reference (Ex. 1007) never states that any individual hardware processor has multiple processing cores. Rather, it describes SMP as a configuration of multiple discrete hardware processors.

29. To begin with, on page 2 of the RS/6000 reference, the system is described as offering “a Symmetric MultiProcessor (SMP) configuration or a uniprocessor configuration.” (Ex. 1007, 2). The term “configuration” indicates an architectural layout of a system of multiple hardware processors working together, not a description of a hardware processor comprising multiple processor cores.

30. In describing its POWER3 SMP High Node (F/C 2058), the RS/6000 reference states that each node “use[s] PCI bus architecture and ha[s] four, eight, twelve, or sixteen 375 MHz 630FP 64-bit processors per node.” (Ex. 1007, 9). This describes the number of hardware processors per node but says nothing about the number of processing cores per hardware processor.

31. The RS/6000 reference also states that the F/C 2058 card includes “[f]our processor slots allowing a maximum of sixteen processors per node.” (Ex. 1007, 10). According to the RS/6000 reference, the “375 MHz Power3 SMP High Nodes require a minimum of four 375 MHz, 630FP processors mounted on one card.” (Ex. 1007, 10). To expand the number of hardware processors, “up to three additional four-processor cards (F/C 4350)” can be ordered to configure the node

with eight, twelve or “a total of sixteen CPUs.” (Ex. 1007, 9-10). This confirms that the RS/6000 SMP configuration uses multiple hardware processors—but says nothing about each of the hardware processors having multiple processing cores.

32. Dr. Bajaj’s assertion that the RS/6000 reference discloses a “hardware processor with a plurality of processing cores” is therefore unfounded. (*See*, Ex. 1003, ¶185). It is based on a misreading and partial quotation of the RS/6000 reference, omitting the word “configuration,” and ignoring context. The POWER3 processor, which is what is described in RS/6000 (Ex. 1007), is a single core processor. “The RS/6000 SP Inside Out” (Ex. 1010, 57).

33. As I stated earlier, the ’768 Patent’s claims require hardware processors each having multiple processing cores. Claim 1 recites “a hardware processor with a plurality of processing cores,” as do claims 26 and 29. (Ex. 1001, col 30, lines 44-45, 51-52; col. 32, lines 54-55, 60-61; and col. 33, lines 62-62, col. 34, lines 1-2). Claim 35 also recites this language (col. 35, lines 38-40) and also recites slightly different language, “wherein the hardware processor comprises multiple processor cores” (Ex. 1001, col., 35, lines 18-19), but I still understand this later language to still require a hardware processor with a plurality of processing cores. All dependent claims flow from one of these independent claims. This is consistent with Dr. Bajaj’s testimony where he cites back to the same portion of the RS/6000 reference when addressing this language from claim 35. (*See*, Ex. 1003, ¶403). Thus, every

challenged claim requires a hardware processor with a plurality of (*i.e.*, multiple) processor cores. This is consistent with the disclosure of the '768 Patent explaining that a “Core 2 Duo® processor ha[s] two processing cores.” *See, e.g.*, Ex. 1001 at 12 (col. 7, lines 28-29).

34. A system configured with multiple hardware processors, like those in RS/6000, that does not specify that each hardware processor includes multiple processing cores does not satisfy these limitations. Moreover, neither Dr. Bajaj nor the Petitions have pointed to any disclosure in the RS/6000 reference or elsewhere showing a hardware processor with more than one processing core.

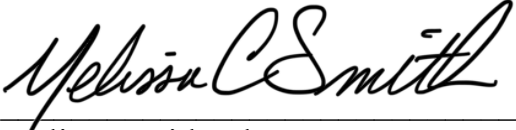
35. In summary, the RS/6000 SP system discloses a Symmetric MultiProcessor configuration with multiple discrete hardware processors or a uniprocessor configuration. It does not disclose or suggest a hardware processor with a plurality of processing cores or multiple processor cores. Petitioner’s interpretation is incorrect and unsupported by the technical record.

36. Thus, it is my opinion that the RS/6000 reference (Ex. 1007) does not disclose, suggest, or render obvious the claim limitations “a hardware processor with a plurality of processing cores” and “hardware processor comprises multiple processor cores” that are recited in the challenged claims. Petitioner’s expert testimony to the contrary is conclusory and factually unsupported.

VI. CONCLUSION

37. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: July 11, 2025



Melissa Smith, Ph.D.