Chapter 2
Image Sensor Technology

R. Daniel McGrath

Abstract Single photon imaging is an extension of solid state imaging, making use of devices that benefit from the outstanding electro-optical properties of silicon and which have the potential, like CCD and CIS devices before, to benefit from the integration made possible with silicon process technology. This chapter provides an introduction to the functionality of integrated image sensors. It presents the typical process flow and a discussion of where the technology used to build CMOS logic and mixed signal parts is useful to provide the special performance and unique features expected in imaging. As a conclusion, process enhancements including special process modules and design rules for high-performance image sensors are discussed.

This chapter also addresses the question to which degree single photon imaging devices can be an extension of the CIS model to achieve mass commercialization. The goal is to build valuable imaging products with an existing fabrication tool set, derived from a conventional CMOS process with some process enhancements using existing tools. This implies that the commercially interesting pixel array design can be achieved using special design rules, and that the process enhancements will support the operating voltages and clock rates required for single photon detection.

2.1 Program and a Brief History of Solid-State Image Sensors

Single-photon imaging is an extension of solid-state imaging where the sensitivity of the photodetection process is systematically increased until the arrival of individual photons can be detected.

There were attempts in the 1960s thru 1980s to realize solid-state image sensors with developing transistor technology and designs. Some foreshadowed the later metal-oxide-semiconductor (MOS) image sensors [1] and led to specialized sensors used for noncommercial imaging applications. Despite attempts at commercialization, the performance was not satisfactory due to process mismatch and defects. Attempts to overcome this with special transistors, for example, charge modulation

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devices (CMDs) and static induction transistors (SITs), did not overcome these limitations.

Charge-coupled devices (CCDs) emerged as the first widely commercialized imaging technology [2]. The CCD is a massively parallel device. As such it could be free to deviate from the design practices used for transistors. Instead of device geometries being defined by the active mask, that is openings in the field oxide, and a single gate pattern, the devices are defined by implant geometries and one or more gate patterns. It was necessary to develop processes providing specialized functionality, for example, buried channel potential profiles and vertical overflow drains. The process tools are the same used with mainstream silicon manufacture, but can have the goal change from achieving minimum geometry to achieving precise alignment. Operating voltages at multiple levels spanning a wider range from $-10\,\mathrm{V}$ (used to provide low dark current while holding charge) to $+20\,\mathrm{V}$ (used to provide a global clear of the array) are required. In addition, special care was needed for certain processes to control defects. The result was a specialized process using a combination of process modules used for logic and mixed-signal processes and of process modules optimized for imaging, for example, low defects. As in other process enhancements, the tool set lagged by generations behind the cutting edge logic process.

With the steady improvements in complementary metal-oxide-semiconductor (CMOS) technology since the 1970s, it was proposed in the 1990s [3] that CMOS image sensor (CIS) designs using the existing processes could meet image sensor performance requirements [4], not only achieving CCD performance within CMOS fabrication facilities, but also surpassing this in some aspects including data rate, integration with circuitry and cost. In reality, CIS was able to provide required performance only with process enhancements including the mixing of process tool sets between process technologies, that is adding more advanced interconnect technology. The result is that CIS products for mass markets can be built in CMOS process fabrication facilities where an investment has been made to develop and support process enhancements, though this requires implementation of special design rules to optimize the pixel array.

The expectation for single-photon imaging devices is that they will extend the CIS model. That is, that they can be built based on an existing fabrication tool set, derived from a conventional CMOS process with some process enhancements using existing tools. The pixel design will use special design rules. The enhanced process will support operating voltages that are obtainable from the process tools.

2.2 Anatomy of an Image Sensor

The function of an image sensor is to collect photons, convert them into electrical signal, and process this electrical signal (Fig. 2.1). The optical collection and the conversion are functions of the pixel. The processing is done using analog and digital CMOS circuitry downstream. The more sophisticated nuances of image sensors, those that provide the quality required for a photograph or a video, are not an issue in single-photon image sensors. Rather what is required is an

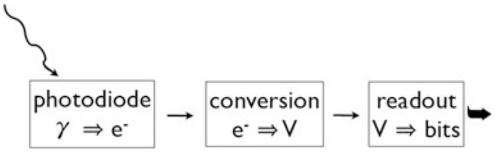


Fig. 2.1 Image sensor function

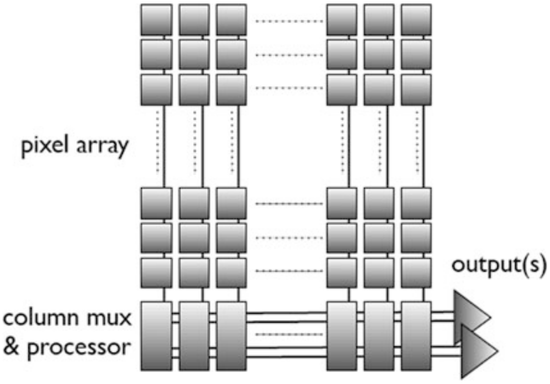


Fig. 2.2 Image sensor array architecture

understanding of the application-specific functionality for single-photon imaging, so there is only a need to understand the straightforward architecture. For instance, the single-photon imaging application does not require the number of pixels or the minimum-sized pixels of typical image sensors. But the basic functionality of light capture, conversion and readout is that of other image sensors.

The typical architecture of a commercial image sensor is a two-dimensional pixel array with a one-dimensional array of analog column readout circuitry, which is multiplexed onto one or more output channels (Fig. 2.2). The pixel array has local wiring plus drive, bus and signal lines, which form the optical aperture of the pixel.

For a CCD, the busing is done by extending the polysilicon gates, and the readout is done by shift registers so that interconnects can be fabricated with one layer of metal. While the number of metal layers is small, the gates must control the charge transfer regions leading to an issue of the gates absorbing visible light. The conversion from photons to charge is done either in the shift register, that is, a frame transfer pixel, where photons are absorbed in the silicon of the CCD register itself or in a photodiode from which charge can be transferred into the CCD register, that is, an interline pixel. Readout of the pixel array is through charge domain transfers with transport of charge packets realized under the influence of potential profiles. The photocharge is shifted from where it is generated into a local maximum where it is held and then through the manipulation of gate potentials through successive potential wells that are sequentially created (Fig. 2.3). The column circuit provides charge domain multiplexing into a horizontal shift register. At the end of each channel horizontal register, there is a diode capacitor, which converts charge to voltage. The only transistors, typically three to five, on the image sensor are involved in the buffering of this voltage, using a floating diffusion capacitor to convert charge

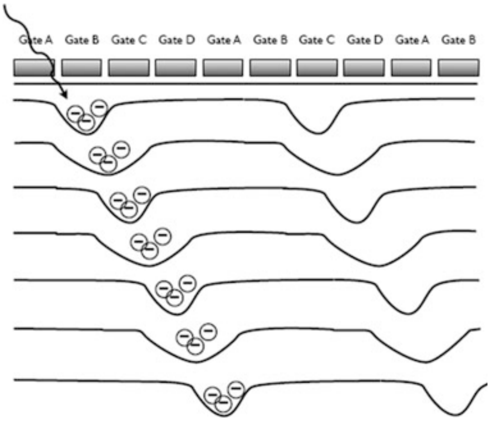


Fig. 2.3 CCD register operation

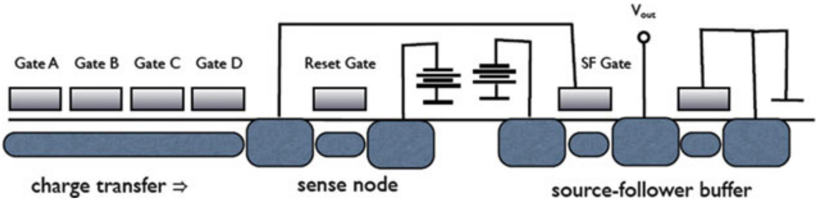


Fig. 2.4 CCD register operation

into voltage and providing low impedance drive for the signal output from the die (Fig. 2.4).

While a CCD is a MOS structure, it is more a device than a circuit. A series of process enhancements have been required to get excellent performance for imaging. To minimize light lost to the control gates, process enhancement (Figs. 2.5 and 2.6) include the following: (a) thinning the device to a silicon thickness of 10 µm to <3 µm so that photocharge can be generated and collected from photons illuminating the back surface; (b) creating photodiodes separate from the shift registers with control gates to transfer readout; and (c) opening subpixel-sized holes in the gate structures next to the shift registers with pinning layers to maintain the potential within the charge gathering and charge transfer depletion regions in the silicon. To increase charge readout efficiency and lower noise, doping has been developed to create buried channels in the shift registers and the readout transistors, so that the signal charge does not interact with the silicon–SiO_2 interface traps. To control regions created with no gate to increase optical response, shallow JFET-like pinning layers have been added, enabling the creation of interline transfer pixels (Fig. 2.7). The pixel-specific process enhancements lead to a process, which has little overlap with the process needed for building CMOS mixed-signal circuitry.

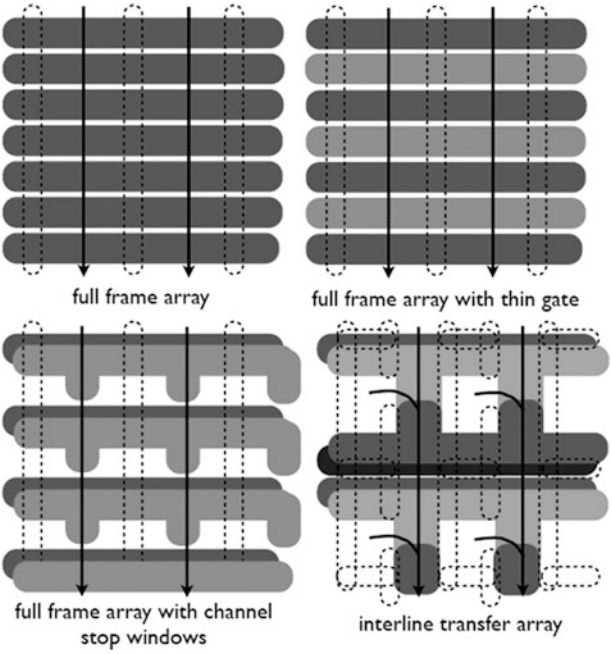


Fig. 2.5 CCD array options (*top view*)

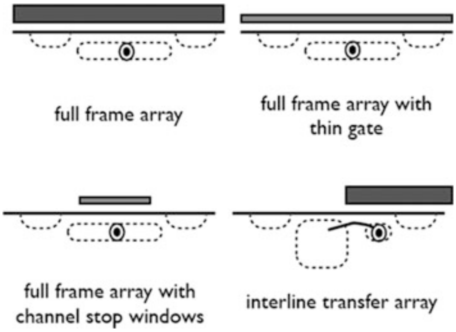


Fig. 2.6 CCD array options (*side view* across channel)

For a CIS, illumination is typically from the front side of the die, so that the optical aperture is formed by horizontal busing on one metal layer and vertical bussing on a second metal layer [5]. Depending on whether the local interconnect can be integrated with one of these bus layers, the pixel may require two or three metal layers. (The other circuitry integrated on the chip may require the use of more metal layers.) Photons are converted to charge in a photodiode and charge is converted on a diode capacitor, which may be the photodiode, "3T pixel," or a floating node onto which the charge is transferred by a gate, "4T pixel" (Fig. 2.8).

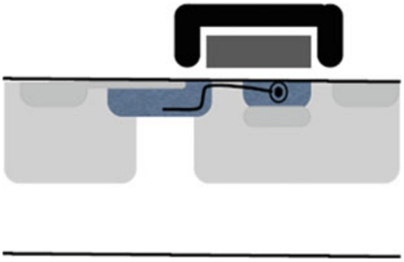


Fig. 2.7 CCD interline-transfer pinned-photodiode (*side view*)

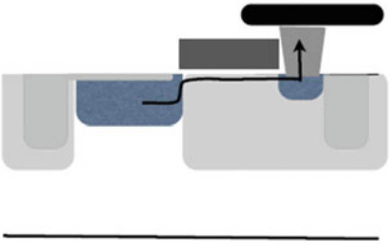


Fig. 2.8 CIS pinned-photodiode (*side-view*)

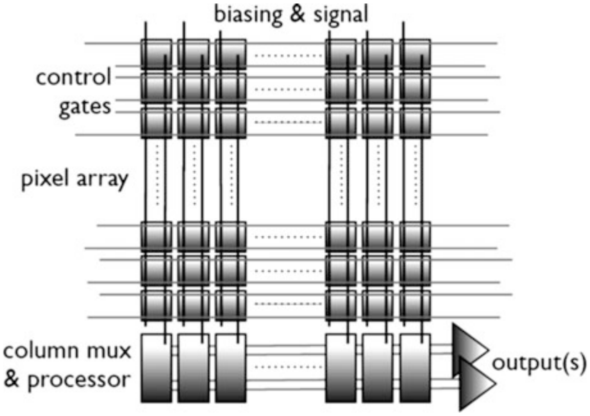
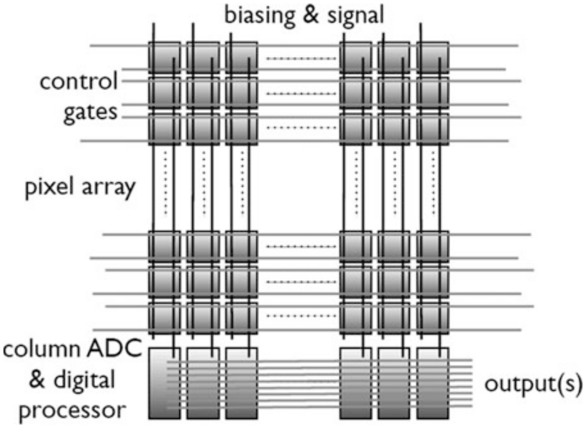


Fig. 2.9 *x–y* Nature of image sensor array with analog column processors

The one-dimensional column circuit array samples the readout from a row of pixels and places the signal onto channel buses, which feed into a gain stage followed by an analog-to-digital (A/D) conversion circuit for each channel (Fig. 2.9). An alternative architecture is to distribute the gain and A/D function into the column circuitry so that the channels are digital buses (Fig. 2.10) [6].

There are other possible architectures, for instance the CMD [7] or SIT [8] devices, where the photons are converted into charge, which is held on either a lateral or a vertical diffusion that modulates the current in a channel in the silicon. The motivation for this architecture is that it results in higher conversion gain due to the junction gate field-effect transistor JFET-like structure. These pixels have design challenges, linked with the implementation of reset function (e.g., memory effects due to incomplete reset), to the optical aperture (e.g., structures that limit a front-side aperture) and readout (e.g., lack of process control in readout threshold voltage).

Fig. 2.10 *x–y* Nature of image sensor array with digital column processors



2.3 Operation

The basic operation of an image sensor relies on a one-dimensional or two-dimensional array of pixels. The pixels in this array, typically laid out in a regular array of rows and columns, must provide a means to collect the light and convert it into electrons or holes. Then through some of elements in the pixels, in the array, in the column, and in a pipeline after the array, the signal is conveyed to the chip output.

In silicon image sensor arrays, the typical sensing element is a volume of the silicon itself. Photons are absorbed by creating electron–hole pairs across an indirect bandgap of 1.12 eV. This creation of photocarriers requires interaction with the lattice phonons to conserve momentum and energy. The bandgap is the right energy for photon absorption from the ultraviolet through the visible into the very near-infrared with one photon creating one pair of photocarriers. However, the absorption coefficient of silicon varies significantly between blue light absorbed very close to the silicon surface and red light where complete absorption requires several micron thickness.

There is also photoresponse due to more energetic photons, such as X-rays and gamma rays, which create multiple photocarriers per absorption in a single location and from charged particles such as beta rays, energetic electrons, high-energy particles, and cosmic rays, which create a trail of electron–hole pairs and often an end event consisting of a rather localized cloud of electron–hole pairs.

In a block of silicon that is not electrically biased, the photocarrier creation would be balanced by an increase in recombination, providing net current neutrality. For an image sensor pixel, it is necessary to take advantage of the semiconductor behavior of silicon to create a region out of equilibrium (e.g., a depletion region completely drained of mobile charge carriers), so that the photocarriers can be collected before they recombine. It is also necessary to have the low defect density present in semiconductor grade silicon with its associated long carrier lifetime, so that the probability of recombining is negligible during this transport phase.

Despite the high quality of single crystal silicon, there is background charge generation (i.e., dark current) independent of the illumination level. This is due to defects in the middle of the energy band from metal contamination, crystal defects and from the interface states between the surface of the silicon and insulators such as the gate oxide, the field oxide, or oxide-filled trenches. A key enabler for MOS devices is that the oxide–silicon interface is of very high quality, but natural mismatch between the amorphous oxide ring structure and the silicon lattice still contains a layer of defects. A dark-generated carrier and a photocarrier cannot be distinguished during image sensor operation, so dark current limits low light performance.

Dark current generation is a critical performance limitation for single-photon imaging because each defect-generated charge will trigger a false event in the imager. Covering the topic sufficiently is beyond the scope of this article, but it is worth providing a short overview. Image sensor pixels are built around regions in the silicon biased out of equilibrium in deep depletion so as to hold charge isolated in their band structure, for example, the photodiode or the floating diffusion used for charge conversion. These are subject to nonphotonic charge generation. Defects, such as metallic contaminates, located within a deep-depletion region can provide mid-bandgap energy states that act as isolated stepping stones, stepping stones isolated in both location and energy, for charge transfer from the valence band to the conduction band, forming dark current defects that are often isolated to a single pixel and very bright. Interface states at silicon–insulator interfaces within the depletion region provide a "U-shaped" continuum of such stepping stones with the minimum at mid-energy gap, but with the ones with energies near the center of the band gap being efficient producers with a distribution dark current sites with lower level generation rates. These generally are distributed with statistics across the pixels providing a noisy background in an image that can go from a near uniform distribution to a Milky-Way-like starry night. Defects located outside the deep-depletion region can also cause the neighboring silicon to be perturbed from equilibrium resulting in diffusion current thermalized to the bandgap energy. The current from these "bulk" defects provides a background distribution that contributes to all pixels. (Defects within the deep-depletion region and defects outside it can be distinguished by the activation energy of their generation rate: depletion traps are characterized as having energy near one half of the bandgap energy, while diffusion defects are characterized by having energy near the bandgap).

Dark current generation can be enhanced by compressive-stress-induced bandgap narrowing, by perturbations of the defect potential profile due to high fields, and by increased defect sites due to a combination of increase in crystalline defects, for example, dislocation planes and implant end-of-range damage. Dark current can be decreased by inducing defect sites, such as crystal defects or oxygen-precipitates away from the critical nonequilibrium depletion region, where metallic defects can diffuse and become trapped without generating defect charge. Dark current can also be decreased by minimizing damage within the depletion region or within the photocharge region within the diffusion paths of the depletion region. Thermal processes can anneal damage. Final thermal anneals with hydrogen or deuterium provided by the ambient or from hydrogen-rich dielectric layers can decrease electrically active interface states, decreasing dark current from these. Device design can minimize the contact in space and over operation for the depletion region with interfaces and enhancements due to electric fields and stress.

This current of photocarriers can be sensed and read out in various ways as follows:

(a) The photocurrent can be integrated in a potential well. The charge can then be transferred by using gate voltages to modify the potential of the well and of adjacent wells to transfer the signal charge through the array to an output node.
(b) The photocurrent can create a voltage drop across a resistor or a subthreshold MOSFET with the signal being sampled during readout rather than being integrated.
(c) The photocurrent can be integrated onto an isolated capacitive node created by space charge depletion regions, which are in a nonequilibrium state due to the biasing sequence of the operation.

CCD's use Option (a). CIS and other MOS sensors use Options (b) or (c) [9]. The result in all cases is to transform the photogenerated charge into a voltage, which is a function of the illumination level. Options (a) and (c) can provide a near-linear transfer function, while Option (b) can be used when a nonlinear performance (e.g., a logarithmic response) is desired.

The arrangement of the pixels as an array makes it natural to read out the pixels in a row-by-row order. A repeated pattern of horizontal bus lines connect single pixels or shared pixels (i.e., multiple photodiodes sharing a single readout) and provide clock signals to provide charge transfer, reset, and pixel select functions.

At the top and/or bottom of the columns of the array are output multiplexers built using charge domain or using MOS circuitry. Biasing and signal readout providing connections to the pixels within a column are provided by vertical bus lines.

The simplest readout is a nested pattern of row timing with the period of the row read and of column timing with the period of the output signal readout. In a typical sequence, a row of pixels is reset to clear the pixels in it of any initial charge by reading them out, by using a gate to force the charge to substrate or by using a gate to connect them to set voltage. The signal current or the integrated signal charge is read out, either buffered to give it sufficient drive impedance or directly digitized.

2.4 Image Sensor Devices

Silicon image sensors are made up of a combination of MOSFETs and diodes, but making an effective pixel requires extending it to new devices and to novel operation for existing devices.

The basic semiconductor device is a diode made by doping two adjoining areas in the semiconductor n-type and p-type [10]. Diodes can be reversed biased to provide isolation between the two regions of different doping to allow the separation of circuit elements and to create capacitors. Typically, the diode is formed with one of the regions having higher doping than the other to create an asymmetric region depleted of free charge to provide manufacturing control.

A second semiconductor device is the MOS capacitor, created between a heavily doped region in the silicon and a polysilicon gate separated by a thin silicon oxide. For example, a gate oxide capacitor designed to work at 3.3 V might have dielectric thickness of 7 nm, or a sandwich of silicon nitride between two layers of silicon oxide, for example, 100 nm for a 10 V process down to 7 nm for a 3.3 V process.

The MOSFET used in digital logic consists of a MOS capacitor placed between two diodes. The gate is patterned on top of a thin silicon oxide or oxide nitride layer so as to modulate a channel along the insulator silicon interface so as to act as a switch [11]. Heavily doped, very shallow diffusions are implanted at each end to provide the contacts for the carriers. Special processes such as implanting silicon or other species may be used to amorphize the silicon to keep the implant from becoming deeper through channeling, but these may cause a problem in an imaging device if it results in residual defects. An opposite type of doping in the form of a deep well and of a shallow threshold voltage adjust are formed under the channel to control the operating voltages. Engineering is done to lower the resistance and to set the work function of the gate through doping and the formation of a silicide layer. The potential profiles at the ends of the channel controlled by the gates are adjusted through the sidewall spacers formed with deposition and etching of silicon oxides and nitride layers. The potential under the spacer is engineered for speed and for reliability through lightly doped drain diffusions, LDD, as extensions of the diffusions and “halo” diffusions of the opposite polarity.

The MOSFETs in analog or mixed signal circuits has the same structure, but perform as transfer functions, either acting as switches to connect and isolate nodes or acting as analog components providing precise outputs depending on the voltage applied.

The CCD in its simplest form, a full-frame transfer array, is a single large integrated device built around registers of abutting MOS capacitors requiring at least one adjacent diode to provide a bias and a sink for its photocarriers and its dark current charge [2]. A single reverse-biased diode next to a MOS capacitor can create a nonequilibrium condition under the capacitor where the mobile charge near the surface is drained away to create a depleted region. The surface potential of silicon under the capacitor gate has a potential that depends on the diode and upon the gate voltage. In the same way, a series of capacitors can be held in nonequilibrium by a single diode with each capacitor being able to control the potential under its gate. By applying different voltages to the various gates, local potential maximums can be created where isolated packets of charge generated by light or by dark current can be collected. By a sequence of biases on the capacitor gates, the maximum of the potentials can be shifted from capacitor to capacitor until it reaches the diode. The capacitor gates can be arranged in more complicated arrays with the charge packets being moved synchronously in parallel arrays of shift registers and with parallel arrays being multiplexed into single serial arrays.

The CCD is commonly read out using a floating diffusion connected to the gate of a MOSFET. The floating diffusion is a diode inserted between two capacitor stages. On one side, there is a stage which acts as a switch to set a bias of the isolated diode, either by providing a barrier with its channel so that excess charge above this potential is drained off to a biased final diode or by acting as a switch to create a channel for charge to the biased final diode to force the floating node to this voltage. The gate of the MOSFET follows the bias on the floating node and modulates its channel potential to dynamically set the voltage of its source diffusion to create a classic source-follower circuit.

To address problems related to signal charge being corrupted by traps at the surface of the capacitors either capturing signal charge or creating dark current, a buried channel capacitor is formed where the surface is counter doped so that the potential maximum where charge is held is shifted from the interface with the gate to a potential channel deeper in the silicon. This keeps the signal charge away from interface traps to prevent signal charge from being trapped; it allows the potential well to be clocked so that for part of its duty cycle the surface is accumulated with free carriers to turn off the generation of dark current by defects there.

While logic and analog MOSFETs can be operated between a low voltage, typically ground, and a high voltage, Vdd, to get the benefit of a buried channel requires operating outside this range. This is because the buried channel has a threshold voltage that is shifted as in a depletion device with the channel being on at ground.

The need for control gates over all of the registers limits the responsivity of CCDs when used with front-side illumination. Photons need to enter through the gates or through the gaps between the gates. A solution to this used in interline transfer CCDs is the pinned photodiode, which consists of a diode doping located between a shallow, highly doped layer and a deep well doping with these two doping regions electrically connected. The result is a back-to-back diode controlled by the surface doping, so that it does not need to be covered by an obstructing gate. The pinned photodiode is read out by an adjoining gate providing a barrier to a shift register, which with a high gate bias provides a potential path. The pinned photodiode potential is a buried channel.

Barrier devices are created to provide means to control blooming in CCDs (i.e., the photocharge from one photodiode that has become full spilling into other photodiodes, creating image artifacts due to signal in the wrong location in an image) and to provide a means to flush unwanted charge. These are areas of lower potential along the shift register, where charge filling up a potential well will preferentially flow rather than spill into other pixels in a shift register. These can be static barriers to a laterally adjoining biased diffusion, gate-controlled stages with a lower potential to laterally adjoining biased diffusions or vertical barriers over the well to an oppositely doped substrate. The overflow will occur either because the stage is filling with charge or because the channel-to-barrier is collapsed by lowering the channel potential through gate control or, in the case of the vertical barrier, a combination of gate and substrate control.

The CIS pixel typically consists of photodiodes, diffusions used as floating nodes to hold charge and MOSFETs providing the three functions of switch, charge transfers device and analog buffer. While there are overlaps in the functions of the devices, the technology differences between CCDs and CISs make for differences in the device design.

The MOS vertical, parasitic, capacitor can be used for a photodiode and as a component of a floating diffusion capacitance. The top plate is a shallow heavy doping, the bottom is the well doping and the dielectric is the depleted silicon in between. Unlike in the peripheral circuitry, this diode's upper surface would not be silicided to let photons in for a photodiode and to avoid the extra dark current associated with silicide–silicon interfaces. This photodiode can be directly contacted by a contact so it can be wired to the gate of a buffer FET or a diffusion of a reset FET.

A pinned photodiode like the ones in an interline CCD is commonly used for CIS photodiodes due to its ability to be totally emptied of signal charge during reset and its low dark current [12]. It can be built adjacent to an FET to provide readout and reset and antiblooming. Unlike the CCD version, it cannot be reset to substrate and antiblooming is only possible laterally through FET structures. Its long wavelength response can be enhanced by chaining doping to create a deep diffusion volume.

The pixel has MOSFETs that are each customized for their function. In the same manner as FETs in the input–output circuits on the die, they are built with thicker gate oxide (e.g., $\sim$ 7 nm required for 3.3 V signals) because the voltages required for pixel operation does not scale as fast as logic. Beyond that, there are three functions required with their own requirements as follows [13]:

- Buffer FET such as that used in source-followers need to have a threshold shift doping to set the gate-to-source voltage drop to be a medium value, a value as low as possible without requiring increased gate length. They need to provide good transconductance with small current.
- Barrier devices as in CCDs are used to reset and maintain the voltage in floating diffusions. They are switches where having a zero or depletion threshold voltage allows operation within the normal voltage range.
- The transfer FET used to read out the pinned photodiode is unique in that it is a charge transfer device, which transfers charge from a buried channel device to a surface device. It provides a low potential channel from photodiode to floating diffusion to prevent lag, a high off-barrier for well capacity and a potential profile that minimizes dark current and directs what is generated away from the photodiode into the floating diffusion. The result of this is that it needs to be viewed as two FETs in series sharing a single gate, that is (1) a vertical FET at the photodiode end controlling a potential barrier away from the surface, which sets the photodiode charge handling capacity when "off" and allows complete

transfer when it is "on" and (2) a conventional surface channel FET controlling a horizontal channel connecting to the floating diffusion.

A typical CIS pixel only uses either n-MOSFET or p-MOSFET devices due to the need for tight packing of devices to enable small pixels [14, 15]. The full CMOS process is needed to enable low power, fast addressing and readout by allowing on-chip circuits.

The need for the development of new devices within the process enhancement can also extend beyond the pixel array to peripheral circuits required to provide the best performance for a pixel array. Examples include having both n-MOS and p-MOS devices with floating bases (achieved through the use of deep dopants to isolate the local well), having capacitors purposely made to achieve linear transfer functions to provide double sampling to shift time differences into voltage differential signals, and having dense memory to allow on-chip line stores for correlated signal correction.

2.5 Image Sensor Process Technology

The goal of mass market and high-performance image sensors is to build them in silicon integrated technology, so that they can benefit from the manufacturing infrastructure, expertise, and cost efficiencies existing because of the large global production for silicon integrated circuits. At the top level, this means building a planar technology on silicon wafers in a clean room environment [16, 17]. At the tool set level, it means wherever possible using the standard equipment set for manufacture and test. And at the process level, it means wherever possible using standard process modules and materials.

The top level flow is that wafers are sawed from single-crystal silicon ingots (boules) of semiconductor-grade purity pulled from a silicon seed crystal. While it is possible to use this wafer directly for building the integrated circuit, typically for image sensors, an additional thin epitaxial layer is grown in a reactor. The substrates and the epitaxial layers are doped as part of the growth process either n- or p-type. The doping type and the concentration of the epitaxial layer and the substrate can independently be varied. The wafers are introduced into a cleanroom environment and follow procedures to maintain cleanliness as handled by machines and people. Because the planar process is going to be used to create fine geometries precisely aligned, it is important that the wafers be flat and that the particle density is extremely small.

The basic tool sets silicon processing includes the following:

- Photolithography to create patterns to define structures in and on the silicon.
- Developing to remove organics patterned by photolithography.
- Thermal oxidation to create a high-quality oxide–silicon interface.
- Plasma deposition of insulating films used in building capacitors and MOSFETs, used to electrically isolate interconnect metal layers and used to provide device passivation.

- Spin-on coating to create insulating films used for creating optical elements such as color filters and microlenses.
- Chemical vapor deposition of polysilicon to create gates for MOSFET devices.
- Silicidation to chemically create a shunt layer on silicon diffusions and polysilicon.
- Plasma etching to create trenches or pattern overlayers.
- Metal deposition of aluminum, tungsten and copper and of boundary and antireflective layers for metals.
- Chemical mechanical polishing to planarize a surface (e.g., to achieve the flatness required by the depth of field of the photolithography optics) or to remove excess metal from a damascene process (i.e., a process where metal is defined by etching patterns in the underlying insulating layer and then polishing the metal back to the dielectric surface).
- Thermal treatments, either furnace or rapid thermal annealing using a pulsed heat source (e.g., for implant activation and reduction in crystalline defects).

A typical MOS process flow (Fig. 2.11) starts with a wafer with a lightly doped device layer (e.g., a doping that is low enough to result in a large depletion zone for charge collection but high enough to be controlled during the subsequent process), either substrate or epitaxial. Shallow trench isolations (STIs) are patterned, etched, and filled to provide isolation between devices and in the process of defining the dimensions of the devices in the circuit, in particular the channel width. A pair of photolithography steps divide the wafer into regions that are to get a chain of implants to create n-wells and regions that are to get a chain of implants to create p-wells. This establishes which devices are to be p-type and which are to be n-type. Photolithography and implants can be done at this point to set the threshold voltage of the MOSFETs. Gate oxides are thermally grown for each of the voltage ranges to be fabricated. Polysilicon gates are deposited, doped, patterned, and etched, providing the other critical dimension of a MOSFET, the channel length. The engineering of the MOSFET is then done through a combination of sidewall formation, halo and lightly doped drain implants and source–drain implants to control the channel ends and through silicidation to lower gate and drain resistances. Thermal processes are needed to activate the implanted doping that is to make sure the dopants substitute for silicon on the crystal lattice sites. After this there are

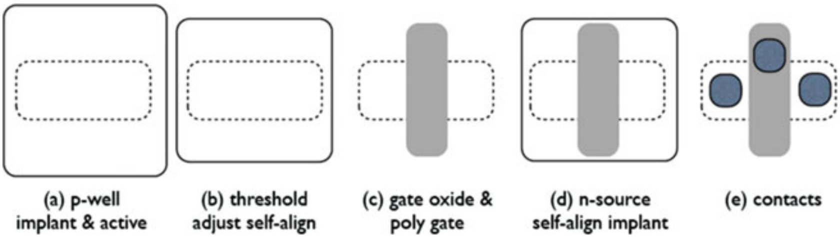


Fig. 2.11 Image sensor array architecture

a series of insulator depositions, contact and via patterning and filling and metal filling. At various critical points in the process, chemical–mechanical polishing is done to provide a flat surface to allow precision photolithography in following steps. At the end of the process, there is a final silicon nitride layer deposited for circuit reliability followed by a patterning and etching of this layer to create bond pads.

The basic device in a MOS process is the FET. It is formed in a well of the appropriate doping. Its critical dimensions are determined a geometry created by the STI pattern and by a geometry formed by the gate pattern. The issue that drives a MOSFET process is small size, consistent performance, device speed, and drive capability.

In going to "nanometer" processes (i.e., processes with feature sizes much less than 1 μm), there have been a couple of major refinements to the MOSFET process. One is a need for shallow doping distributions requiring precise control of thermal cycles, leading to the shift from furnace to rapid-thermal anneals. A second is a shift from aluminum to copper for metallization with the shift to a damascene process, where the metal pattern is established by etching trenches in the isolation and etching off metal not in the trench and where blanket protection layers are formed at each metal level.

CCD technology originated in the same time period when CMOS technology was being developed, before the semiconductor industry became dominated by it. CCD technology development was not constrained in either layout or the development of process modules. In contrast to the MOSFET device, the basic CCD device is made up of charge transfer channel created from gates from a series of layers of polysilicon, each one defining the length of a stage, running across a channel defined by channel-stop implants. There is only one well doping, which may be patterned at the pixel level to provide an antiblooming barrier to the substrate and which should be as high as feasible to improve the photodiode collection depth. And there is a counter-doping to relocate the channel from the surface to the substrate. There can be additional doping to direct charge flow within a single transfer stage and facilitate the transfer between phases. Getting good transfer in this buried channel means that electric fringing fields are important in setting the potentials for charge handling wells and channels created deeper in the silicon away from the gate insulator interface so there is benefit in continuing to use thicker oxide (e.g., there is a need to smooth the lateral potential profiles to avoid creating local potential wells that trap charge). Getting good optical response lead to the use of pinning implants to control buried channel potential in regions without gates. It also can lead to the development of a thinning process so that the final device can be illuminate from the back surface (albeit with the resulting loss of longer wavelengths from green into the near infrared). Silicides are not used on the gates. The massively parallel nature of a CCD pixel array means only one or two layers of metal are necessary.

A CCD process flow (Fig. 2.12) starts with a wafer with a lightly doped device layer, either substrate or epitaxial. It will have a specification for metal contamination levels and will have gone through some form of processing, such as oxygen precipitation to provide gettering of residual contaminants. Local oxidation isolation (LOCOS) or trench isolation may be used, but with doping in the trench

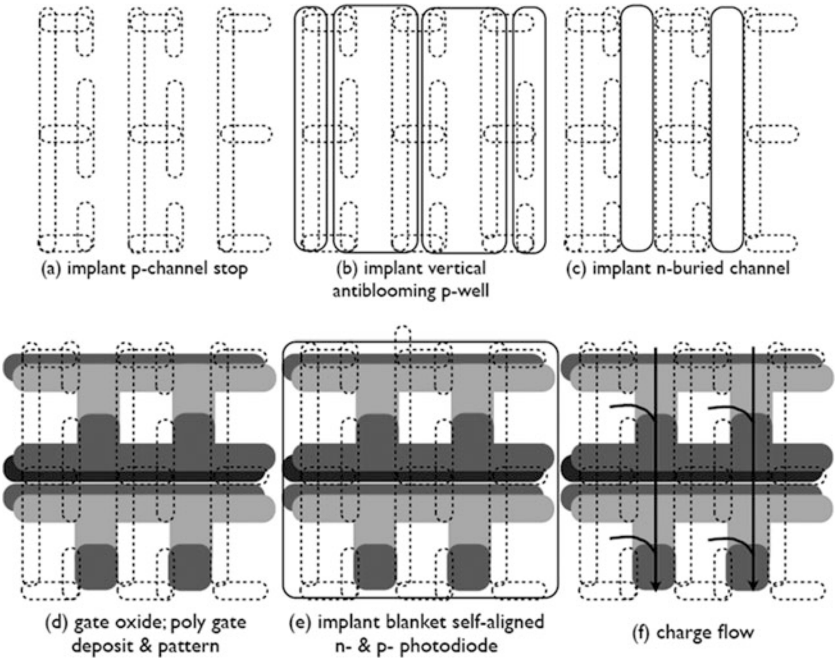


Fig. 2.12 CCD simplified process

walls providing passivation of the trench walls. Alternatively, there may be no trenches at all with the isolation being formed by just the doping between devices. Photolithography defines an in-pixel-patterned well that can be diffused into the wafer and laterally to contribute to the channel potential and provide isolation. Photolithography and implants can be done at this point to create the buried channel and to adjust the channel potentials in the transfer stages. Thick gate oxide is thermally grown for each of the voltage ranges to be fabricated. Multiple layers of polysilicon gates are deposited, doped, patterned, and etched, providing the other critical dimension of a transfer stage, the channel length. Thermal processes are needed to activate the implanted doping, that is to make sure the dopants substitute for silicon on the crystal lattice sites. After this, there is an insulator deposition, contact and via patterning and filling and metal filling. At the end of the process, there is a sequence of passivation deposition and post-metal anneal in a hydrogen environment to move hydrogen to reduce defect concentration by reacting with dark-current-generating dangling bonds at silicon–oxide interfaces. There is a patterning and etching of this layer to create bond pads. Following this is a sequence to form color filters and microlenses to provide color separation and increased responsivity.

To increase the responsivity, backside thinning to a few micrometers through the use of silicon-on-insulator or physical and chemical etching to allow backside illumination.

The issues that drive CCDs are optical response, near perfect charge transfer, and charge generation from defects. Defects can be due to defects at silicon–oxide interfaces and to metal contamination in the silicon.

While early on the claim for CIS devices was that they could be built using a standard CMOS process, the issues that drive the CIS technology today is to maintain CMOS functionality for peripheral circuitry while building a pixel array that meets the same challenges as CCDs, the optical response and the low defect levels. The approach for the CIS process then is to start with a CMOS process and add to it process enhancements that provide high-performance pixels, bearing in mind that the enhancements must leave the devices built in the base process unchanged in performance.

A CIS process flow (Figs. 2.13 and 2.14) starts with a wafer with a lightly doped device layer, either substrate or epitaxial. The wafer needs to have extremely low contamination and should go through gettering processes to reduce the contamination level further. Shallow trenches are patterned, etched, and filled to provide isolation between devices and in the process defining the dimensions of the devices in the circuit, in particular the channel width. The shallow trench process includes doping to passivate the upper corner, the sidewall and the bottom of the trench. A photolithography step divides the wafer into regions that are to get a chain of implants to create n-wells, regions that are to get a chain of implants to create p-wells, and the region in the pixel array, where the well doping is patterned at a

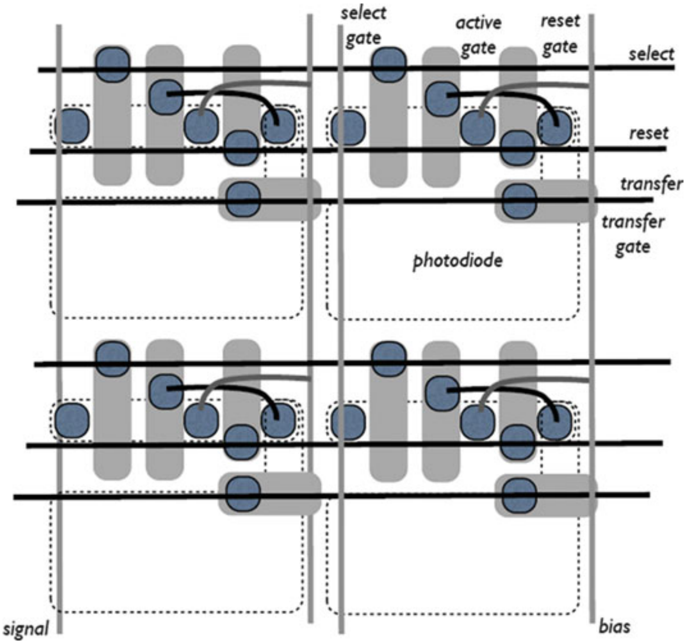


Fig. 2.13 CIS nonshared pinned-photodiode pixel

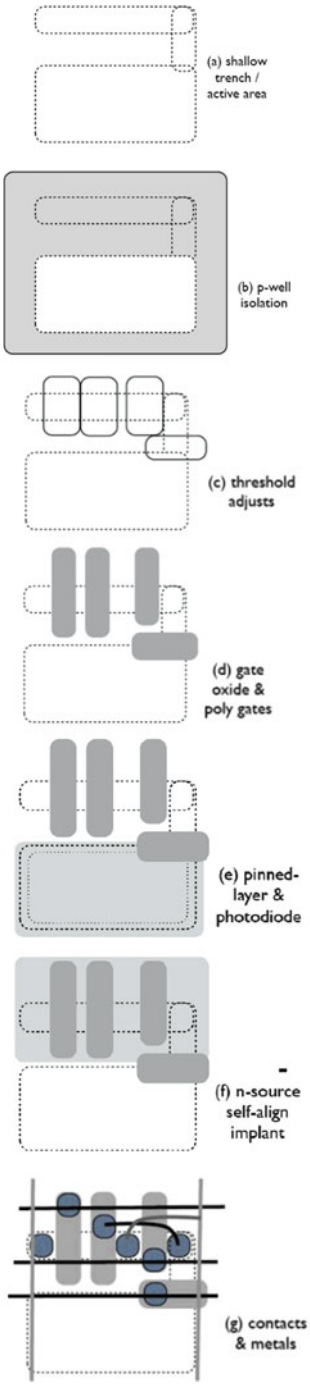


Fig. 2.14 Simplified CIS process

pixel scale with areas such as the photodiode left native. This establishes which devices are to be p-type, which are to be n-type, and which will be special devices for the pixel. Photolithography and implants can be done at this point to set the threshold voltage of the MOSFETs. Gate oxides are thermally grown for each of the voltage ranges to be fabricated with the higher voltage devices being used in the pixel array. While the base CMOS process for commercial image sensors has scaled to the 130 and 90 nm technology node, the operation of many pixels is based on devices and voltages from the 350 nm technology node. Polysilicon gates are deposited, doped, patterned, and etched, providing the other critical dimension of a MOSFET, the channel length. The engineering of the MOSFET is then done through a combination of sidewall formation, halo and lightly doped drain implants, and source–drain implants to control the channel ends. Additional depositions, photolithography and etches are used to engineer the charge transfer from the photodiode through the transfer gate and to the floating diffusion. Silicidation to lower gate and drain resistances are done selectively, excluded from the diffusions in the pixel array because they block light over the photodiode and because of its association with increased defect generation. Additional photolithography and implantation is used to create the pinned photodiode, forming a shallow doping for the pinning layer and providing a chain of implants to engineer the photodiode to extend the photodiode diffusion to extend deep into the silicon with a large aspect ratio. Thermal processes are needed to activate the implanted doping, that is to make sure the dopants substitute for silicon on the crystal lattice sites. After this, there are a series of insulator depositions, contact and via patterning and filling and metal filling. At various critical points in the process, chemical–mechanic polishing is done to provide a flat surface to allow precision photolithography in following steps. Additional process steps may be done to create a lightpipe (i.e., an optical means of guiding photons between the front-side interconnect structure) to enhance optical acceptance, particularly in processes with the copper metallization with its additional dielectric layers that would otherwise create a dielectric stack resulting in interference effects. At the end of the process, there is a sequence of passivation deposition and postmetallization anneal in a hydrogen environment to move hydrogen to reduce defect concentrations at interfaces. There is a patterning and etching of this layer to create bond pads. Following this is a sequence to form color filters and microlenses to provide color separation and increased responsivity.

To increase the responsivity, backside thinning through the use of silicon-on-insulator or physical and chemical etching to allow backside illumination [18]. This requires wafer bonding to a carrier wafer, a scheme to make electrical contact from the backside or the die edge and a process to allow alignment of backside processes such as metal light shield, color filters, and microlenses.

To work fully within the CMOS process technology flow, the process extension should not only include an enhanced process flow, but also the supporting physical design kit files that describe the enhanced process. These include updated design rules, device symbols, SPICE models, and layout-versus-schematic verification files.

2.6 Outlook for a Single Photon Process Technology

Image sensor process technology provides an approach to achieve commercial single photon image detectors: demonstrate that a pixel exists, understand what is critical and then look how these can be added as enhancements to a CMOS process flow.

Possible pixel device directions to achieve single photon counting through process enhancements include the following:

- Increased conversion gain by providing a floating diffusion with decreased capacitance.
- Refinement of the single photon avalanche detector to produce controlled multiplication with high yield.

These and other approaches will be discussed in the following chapters.

Process enhancements for a single photon detector will have similarities to those for an image sensor, but there are enough differences that the process flow should start from the basic logic process and not from the image sensor process. While there are similarities, for instance, both need high optical acceptance, good conversion gain, and low density of bright defects, there are critical performance parameters not required for the single photon pixel, including, for example:

- Linearity is essential for image sensors integrating tone scale, but is not needed when the pixel is detecting whether a single event happens. A single photon pixel may not require that the floating diffusion have linear capacitance or that the capacitance between pixels is well matched.
- Small size is essential for high-resolution photographic imaging, but not needed for applications with larger pixels providing higher responsivity.
- Well capacity need only be large enough to capture the photocarriers of a single photon event.

On the other hand, there are critical performance parameters required for a single photon pixel not required in an image sensor process flow as follows:

- Multiplication uniformity to make sure that pixels all have similar detection threshold.
- Almost 100% optical fill factor and quantum efficiency as every photon needs to be counted.
- High speed readout to allow image synthesis from multiple frames in a reasonable time.

In summary, the approach used for CIS process technology development can provide a model for single photon image sensors. Start with a standard process flow. Look to add as process enhancements the steps required to create the single photon pixel. In doing this, it is important to use the base process modules where possible and to add only process modules as are compatible with the base process flow so as to preserve their functionality consistent with their device models. The twin goals are to create an optimized pixel and to preserve the CMOS performance that allows the reuse of the CMOS design flow.

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