

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC., SONY GROUP CORPORATION

Petitioners

v.

SIONYX LLC,

Patent Owner

Inter Partes Review Case No. IPR2025-00845

U.S. Patent No. 10,224,359

DECLARATION OF DR. STANLEY SHANFIELD, PH. D.

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I, Dr. Stanley Shanfield, declare as follows:

I. INTRODUCTION

1. I have been retained by counsels for Petitioners as a technical expert in the above-captioned case. Specifically, I have been asked to render certain opinions regarding the IPR petition with respect to U.S. Patent No. 10,224,359 (“the ’359 Patent”). I understand that the Challenged Claims are 1-83, and my opinions are limited to those claims. A true and correct copy of my Curriculum Vitae, which provides further details about my background and experience, is appended to this Declaration.

A. Educational Background and Professional Experience

2. In 1977, I received a B.S. Degree in Physics cum laude from the University of California, Irvine. I received a Ph. D. in Physics from Massachusetts Institute of Technology in 1981.

3. After obtaining my Ph.D. in 1981, I was a Staff Scientist at Spire Corporation in Bedford, Massachusetts. Among other activities, I developed new equipment and a new method for performing low temperature silicon epitaxy using PECVD. From 1985-1999, I worked at Raytheon Corporation. As staff and later as section manager, among other projects, I designed and fabricated experimental Si optical sensor arrays intended for visible and near-IR government applications. This involved my efforts in numerous areas, including layout optimization, materials

growth, process development in trench RIE and doped oxide deposition and reflow, wafer-scale bonding, and scalable sensor integration with mixed signal ASICs.

4. In 1996, I became the Manager of Semiconductor Operations at Raytheon. As Manager, I built and led a 300-employee, \$60 million revenue-generating semiconductor development, commercial system design, and electronic module manufacturing operation. The research portion of Raytheon's Semiconductor Operations continued to develop optical sensing array components, including with materials other than Si. I was directly involved in design and critical processing choices, sensor fabrication management, and problem-solving, and I established the direction of research investment in sensor development over several years.

5. In 1999, I co-founded and became Vice President of Operations at AXSUN Technologies in Bedford/Billerica, Massachusetts, and later became Director of Manufacturing and Wafer Fab Technology. The company's product was based on a co-patented optical sensor, which was incorporated into a miniature spectrometer for fiber optic network monitoring. The company successfully released a commercial product and was eventually acquired.

6. In 2003, I joined the Draper Laboratory in Cambridge, Massachusetts. I have been the Division Leader of Advanced Hardware Development, with around 80 staff members; a Distinguished Member of Technical Staff; and Technical

Director. I led the Advanced Hardware Development division in relaunching a multi-chip integrated circuit module facility. Among other activities, we designed, fabricated and tested flat profile optical sensor arrays for a range of star-based space navigation systems. The arrays accommodated the space radiation environment using an innovative semiconductor layout and optical design.

7. I have received many awards at Draper, including the 2015 Distinguished Performance Award and the 2010 Best Patent Award.

B. Materials Considered

8. I have relied upon my education, knowledge, and experience with semiconductor devices and in particular optical semiconductor devices, as well as the other materials as discussed in this declaration in forming my opinions.

9. In developing my opinions, I have considered the following materials:

Exhibit	Description
1001	U.S. Patent No. 10,224,359 (“the ’359 Patent”)
1002	File History of the ’359 Patent (Application No. 15/216,244)
1003	Declaration of Dr. Stanley Shanfield (“Dec.”)
1004	U.S. Patent No. 7,675,099 to Hwang et al. (“Hwang-099”)
1005	U.S. Patent Publication No. 2010/0302432 to Komuro (“Komuro”)
1006	<i>Not submitted</i>
1007	U.S. Patent Publication No. 2011/0019050 to Yamashita (“Yamashita”)

1008	U.S. Patent No. 7,709,775 to Konno et al. (“Konno”)
1009	U.S. Patent Publication No. 2009/0160000 to Kim (“Kim”)
1010	U.S. Patent No. 7,492,027 to Mouli (“Mouli”)
1011	<i>Not submitted</i>
1012	U.S. Patent Publication No. 2007/0108476 to Hong (“Hong”)
1013	Certified English Translation of Korean Patent No. 10-0688584 to Hwang (“Hwang-584”)
1014	<i>Certain Sensors with Pixels and Products Containing the Same</i> , Inv. No. 337-TA-1403, USITC Pub. 841145, Order No. 36: Construing Certain Claim Terms (January 15, 2025)
1015	<i>SiOnyx, LLC vs. Samsung Electronics, CO., LTD. et al.</i> , Case No. 2:24-cv-00291-JRG (EDTX, Dkt. No. 4-9)
1016	<i>SiOnyx, LLC vs. Samsung Electronics, CO., LTD. et al.</i> , Case No. 2:24-cv-00291-JRG (EDTX, Dkt. No. 4-10)
1017	<i>SiOnyx, LLC v. Apple, Inc.</i> , Case No. 1:24-cv-12354 (D. Mass, Dkt. No. 22-4)
1018	<i>SiOnyx, LLC v. Apple, Inc.</i> , Case No. 1:24-cv-12354 (D. Mass, Dkt. No. 53)
1019	<i>SiOnyx, LLC v. Apple, Inc.</i> , Case No. 1:24-cv-12354 (D. Mass, Dkt. No. 51)
1020	D. Mass Local Patent Rules
1021	S. M. Sze & Kwok Ng, <u>Physics of Semiconductor Devices</u> (3 rd ed. 2007) (“Sze”)
1022	James R. Janesick, <u>Scientific Charge-Coupled Devices</u> (2001) (“Janesick”)
1023	Alistair Sproul, <u>Solar Cells: Resources for the Secondary Science Teacher</u> , University of New South Wales (2003) (“Sproul”)

1024	U.S. Patent Publication No. 2007/0190681 to Lee et al. (“Lee”)
1025	R. Daniel McGrath, <i>Image Sensor Technology, in Single-Photon Imaging 27</i> (Peter Seitz & Albert JP Theuwissen eds., 2011) (“McGrath”)
1026	Christopher Shea, <i>A Silicon p-i-n detector for a hybrid CMOS imaging system</i> , Rochester Institute of Technology, https://repository.rit.edu/theses/7116 (2012) (“Shea”)
1027	<i>Photodiode Characteristics and Applications</i> , OSI Optoelectronics (2005) (“OSI Whitepaper”)
1028	H. A. Macleod, <i>Thin-Film Optical Filters</i> (3rd ed. 2001) (“Macleod”)
1029	Misha Boroditsky, Regina Ragan & Eli Yablonovitch, <i>Absorption Enhancement in Ultra-Thin Textured AlGaAs Films</i> , 57 <i>Solar Energy Materials and Solar Cells</i> 1 (1999) (“Boroditsky”)
1030	Jan Provoost and Piet De Moor, <i>Backside-illuminated image sensors: Optimizing manufacturing for a sensitivity payoff</i> , https://www.vision-systems.com/print/content/16744520 (2011, retrieved February 24, 2025) (“Provoost”)
1031	A. Tournier et al., <i>R 5 Pixel-to-Pixel Isolation by Deep Trench Technology: Application to CMOS Image Sensor</i> (2011) (“Tournier”)
1032	Vyshnavi Suntharalingam, Dennis D. Rathman, Gregory Prigozhin, Steven Kissel, and Mark Bautz, <i>Back-illuminated three-dimensionally integrated CMOS image sensors for scientific applications</i> , Proc. SPIE 6690, Focal Plane Arrays for Space Telescopes III, 669009 (2007) (“Suntharalingam”)
1033	U.S. Patent No. 6,888,214 to Mouli et al. (“Mouli-214”)
1034	Kyriaki Minoglou et al., <i>Reduction of Electrical Crosstalk in Hybrid Backside Illuminated CMOS Imagers Using Deep Trench Isolation</i> , in IEEE 2008 International Interconnect Technology Conference 129 (2008) (“Minoglou”)

1035	U.S. Patent No. 6,710,370 to Street et al. (“Street”)
1036	U.S. Patent Publication No. 2004/0251513 to Su et al. (“Su”)
1037	Maximillian A. Perez et al., <i>Rubidium Vapor Cell with Integrated Bragg Reflectors for Compact Atomic MEMS</i> , 154 Sensors and Actuators A: Physical 295 (2009) (“Perez”)
1038	I. H. Malitson, Interspecimen Comparison of the Refractive Index of Fused Silica*, †, J. Opt. Soc. Am. 55 (1965) (“Malitson”)
1039 - 1047	<i>Not submitted</i>
1048	Yoshio Mita et al., <i>Deep-Trench Vertical Si Photodiodes for Improved Efficiency and Crosstalk</i> , 13 IEEE Journal of Selected Topics in Quantum Electronics 386 (2007) (“Mita”)
1049 - 1063	<i>Not submitted</i>
1064	U.S. Patent Publication No. 2008/0265349 to Kasano et al. (“Kasano”)
1065	Joint Statement Identifying Accused Products, <i>In the Matter of Certain Sensors with Pixels and Products Containing the Same</i> , USITC Inv., No. 337-TA-1403, Jan. 31, 2025 (Redacted)
1066	U.S. Patent Publication No. 2011/0241148 (“Hiyama”)
1067	Werner, et al., <i>Very low surface recombination velocities on p- and n-type c-Si by ultrafast spatial atomic layer deposition of aluminum oxide</i> , Appl. Phys. Lett. 97, 162103 (2010) (“Werner”)
1068	U.S. Patent Publication No. 2012/0033119 (“Shinohara”)
1069	PCT Pub. WO2011/160130 (“Carey”)
1070	Certified Translation of JPH06-244444 (“Uematsu”)
1071	U.S. Patent Publication No. 2006/0286766 (“Cole”)
1072	<i>Not submitted</i>

1073	Declaration of June Munford
1074	U.S. Patent No. 6,395,650 (“Callegari”)
1075	U.S. Patent Publication No. 2008/0121962 (“Forbes”)
1076	U.S. Patent No. 7,135,350 (“Smith”)
1077	M. Aguilar-Frutis, et al., <i>Optical and electrical properties of aluminum oxide films deposited by spray pyrolysis</i> , Appl. Phys. Lett., 72, 1700 (1998) (“Aguilar-Frutis”)
1078	U.S. Patent Publication No. 2011/0156186 A1 (“Iida”)
1079	Weiming He, et al., Atomic Layer Deposition of Lanthanum Oxide Films for High-k Gate Dielectrics, Electrochemical and Solid-State Letters, 7(7), G131 (2004) (“He”)
1080	Meza-Rocha, et al., Characterization of Lanthanum-Aluminum Oxide Thin Films Deposited by Spray Pyrolysis , ECS Journal of Solid State Science and Technology, 3 (2) N1-N6 (2014) (“Meza-Rocha”)
1081	U.S. Patent Publication No. 2011/002589 (“Hibbeler”)
1082	U.S. Patent No. 8,357,984 (“Mao”)

10. I have considered these materials from the viewpoint of a POSITA as of the priority date of the '359 Patent. For the purposes of this declaration, I have been asked to assume that the priority date of the '359 Patent is March 22, 2012. I note that my opinions provided in this Declaration are made from the perspective of a POSITA as of this priority date of the '359 Patent unless expressly stated otherwise. To the extent that I use any verb tense in this Declaration that is present tense (e.g., “a POSITA would understand” instead of “a POSITA would have

understood”), such verb tense should be understood to be my opinion as of the ’359 Patent’s priority date (again, unless expressly stated otherwise). I merely use the present verb tense for ease of reading.

II. OVERVIEW AND LEGAL STANDARDS

11. In formulating my opinions, I have been instructed to apply certain legal standards. I am not a lawyer. I do not offer any testimony regarding what the law is. Instead, the following sections summarize the law as I have been instructed to apply it in formulating and rendering my opinions found later in this declaration. I understand that, in an *inter partes* review (“IPR”) proceeding, patent claims may be deemed unpatentable if it is shown that they are anticipated or rendered obvious in view of the prior art. I understand that prior art in an IPR review is limited to patents or printed publications that predate the priority date of the patent at issue. I understand that questions of claim clarity (definiteness) and enablement cannot be considered as a ground for considering the patentability of a claim in these proceedings.

A. Person of Ordinary Skill in the Art

12. I understand that the ’359 Patent, the record of the proceedings at the Patent Office (which I understand is called the “File History” or “Prosecution History”), and the teachings of the prior art are evaluated from the perspective of a person of ordinary skill in the art (“POSITA”). I understand that the factors

considered in determining the ordinary level of skill in the art may include: (i) the levels of education of the inventor; (ii) the types of problems encountered in the art; (iii) prior art solutions to those problems; (iv) the rapidity with which innovations are made; (v) the sophistication of the technology; and (vi) the educational level of persons working in the field.

13. I understand that a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors above. The hypothetical person is presumed to have the same level of skill as the typical practitioner of the art and is presumed to have knowledge of all prior art in the relevant field. I understand that the inventor's actual knowledge or lack of knowledge of prior art reference is irrelevant to the obviousness determination.

B. Obviousness

14. I understand that a claim may be invalid under 35 U.S.C. § 103(a) if the subject matter described by the claim as a whole would have been "obvious" to a POSITA in view of a single or combination of prior art references at the time the claimed invention was made. I further understand that a POSITA is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent-in-suit and all analogous prior art. I understand that obviousness in an IPR review

proceeding is evaluated using a preponderance of the evidence standard, which means that the claims must be more likely obvious than nonobvious.

15. I also understand that an obviousness determination includes the consideration of various factors including: (1) the scope and content of the prior art, (2) the differences between the prior art and the claim at issue, and (3) the level of ordinary skill in the pertinent art. I understand that secondary considerations of non-obviousness such as commercial success, long-felt but unresolved needs, failure of others, and so forth may be assessed as well. I have been informed that an obviousness analysis must consider the full scope of the claims to avoid impermissibly using hindsight to invalidate a patent.

16. In considering whether certain prior art renders a particular patent claim obvious, I have been informed that I can consider the scope and content of the prior art, including the fact that a POSITA would regularly look to the disclosures in patents, trade publications, journal articles, conference papers, industry standards, product literature and documentation, texts describing competitive technologies, requests for comment published by standard setting organizations, and materials from industry conferences, as examples.

17. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. A reference is analogous art if: (1) the reference is from the same field of

endeavor as the claimed invention (even if it addresses a different problem); or (2) the reference is reasonably pertinent to the problem faced by the inventor (even if it is not in the same field of endeavor as the claimed invention). For a reference to be “reasonably pertinent” to the problem, it must logically have commended itself to an inventor’s attention in considering the problem. In determining whether a reference is reasonably pertinent, one should consider the problem faced by the inventor, as reflected either explicitly or implicitly, in the specification. I believe that the documents I considered in forming my opinions in this IPR are well within the range of documents a POSITA would have consulted to address the type of problems described in the Challenged Claims.

18. I have been informed that to establish that a claimed invention was obvious based on a combination of prior art elements, an articulation of the reason(s) why a claimed invention would have been obvious must be provided. Specifically, I have been informed that the prior art, either as a single reference or a combination of multiple items of prior art, renders a patent claim obvious when there was an apparent reason for a POSITA, at the time of the invention, to combine or modify the prior art. Rationales for combining or modifying the prior art include, but are not limited to, any of the following: (A) combining prior art methods according to known methods to yield predictable results; (B) substituting one known element for another to obtain predictable results; (C) using a known technique to improve a

similar device in the same way; (D) applying a known technique to a known device ready for improvement to yield predictable results; (E) trying a finite number of identified, predictable potential solutions, with a reasonable expectation of success; (F) identifying that known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art; or (G) identifying an explicit teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine the prior art references to arrive at the claimed invention.

19. I have also been informed that where there is a motivation to combine, claims may be rejected as obvious provided a POSITA would have had a reasonable expectation of success regarding the proposed combination. I have also been informed that common sense may be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes. I have been informed that if the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than non-obvious innovation.

20. I have been informed that the existence of an explicit teaching, suggestion, or motivation to combine known elements of the prior art is a sufficient, but not a necessary, condition to a finding of obviousness. In determining whether

the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose described in the patent-in-suit controls. I have been further informed that the obviousness analysis may consider the effects of demands known to the technological community or present in the marketplace and the background knowledge possessed by a POSITA. These issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent.

21. I have been informed that it is improper to combine references where the references teach away from their combination. A reference may be said to teach away when a POSITA, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the patent applicant. I have also been informed that a reference does not teach away if it merely expresses a general preference for an alternative invention but does not criticize, discredit, or otherwise discourage investigation into the invention claimed.

22. I am informed that even if a case of obviousness is established, the final determination of obviousness must also consider “secondary considerations” if presented. Secondary considerations include: (a) commercial success of a product due to the merits of the claimed invention; (b) a long-felt, but unsatisfied need for the invention; (c) failure of others to find the solution provided by the claimed

invention; (d) deliberate copying of the invention by others; (e) unexpected results achieved by the invention; (f) praise of the invention by others skilled in the art; (g) lack of independent simultaneous invention within a comparatively short space of time; and (h) teaching away from the invention in the prior art.

23. I have been further informed that secondary considerations evidence is only relevant if the offering party establishes a connection, or nexus, between the evidence and the claimed invention. The nexus cannot be based on prior art features. The establishment of a nexus is a question of fact. While I understand that Patent Owner here has not offered any secondary considerations at this time, I will supplement my opinions should Patent Owner raise secondary considerations during the course of this proceeding.

C. Claim Construction

24. I understand that the claim terms in an IPR proceeding are construed according to their plain and ordinary meaning as understood in light of the claim language, the patent's description, and the prosecution history viewed from the perspective of a POSITA. I further understand that where a patent defines claim language, the definition of the patent controls, even if there are other definitions that might be understood by those working in the art.

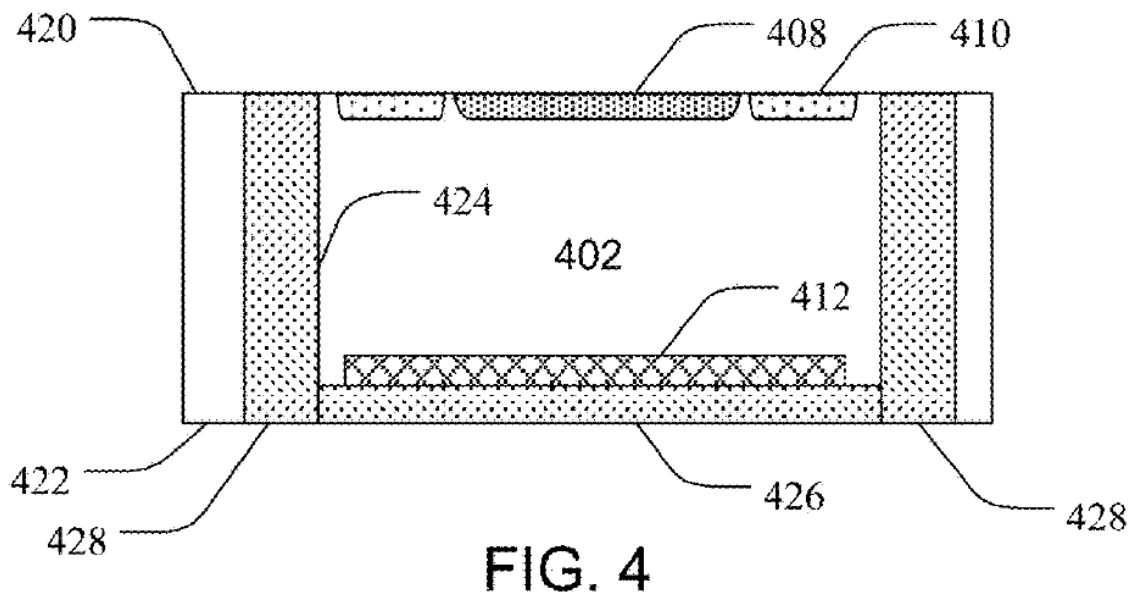
III. OVERVIEW OF THE '359 PATENT

A. Summary of the '359 Patent

25. The '359 Patent describes “[l]ight trapping pixels” and “devices incorporating such pixels...” *'359 Patent* at Abstract. The '359 Patent utilizes “[a] variety of light trapping materials ...to trap light in a pixel[.]” *'359 Patent* at 1:56-59. For example, “a backside light trapping material substantially covering the backside surface, and a peripheral light trapping material substantially covering the peripheral sidewall[.]” and “an internally reflective frontside light trapping material[.]” *'359 Patent* at Abstract, 2:46-47. Per the '359 Patent, “[a] variety of light trapping materials can be utilized and are contemplated, and any such material capable of being used to trap light in a pixel is considered to be within the present scope.” *'359 Patent* at 1:56-59.

26. FIG. 4 is an exemplary light trapping pixel device having “a light sensitive pixel or device 402 having a light incident surface 420, a backside surface 422 opposite the light incident surface 420, and a peripheral sidewall 424 disposed into at least a portion of the pixel 402 and extending at least 20 substantially around the pixel periphery.” *'359 Patent* at 11:15-21. “It is noted that the pixel sidewall is also known as a trench.” *'359 Patent* at 11:21-22. To trap light, the pixel includes “a backside light trapping material 426 substantially covering, partially covering, or completely covering the backside surface 422,” and “[a] peripheral light trapping

material 428 ... substantially covering, partially covering, or completely covering the peripheral sidewall 424.” ’359 Patent at 11:22-27. “As such, light contacting the backside light trapping material 426 or the peripheral light trapping material 428 is reflected back toward the pixel 402.” ’359 Patent at 11:27-30.



’359 Patent at FIG. 4.

27. To trap and reflect light within pixel 402, the aforementioned light trapping materials include “either single or multiple layer structures” (’359 Patent at 11:35-36), such as “a high refractive index material sandwiched between two low refractive index materials.” ’359 Patent at 1:61-62. Additionally, “the frontside light trapping material can be an antireflective layer coating” or “a reflective layer having an aperture to allow entry of light into the pixel” with “a lens functionally coupled to the aperture[.]” ’359 Patent at 2:34-36; see also, *id.* at FIG. 6.

B. Field of Endeavor

28. I have been informed that the field of endeavor of the claimed invention can be determined by reference to explanations of the invention's subject matter in the patent application, including the embodiments, function, and structure of the claimed invention.

29. The '359 Patent generally relates to "light trapping pixels, devices incorporating such pixels, photovoltaic solar cells, and other optoelectronic devices . . ." '359 Patent at 1:40-43. The '359 Patent describes "an image sensor [that] can be capable of detecting visible and infrared light[.]" '359 Patent at 6:30-33. For example, "[i]n one aspect, a variety of optoelectronic devices are provided such as, without limitation, . . . imagers capable of detecting visible and infrared light[.]" '359 Patent at 6:48-52. The described embodiments "provide[] semiconductor devices and associated methods that can exhibit various enhanced properties, such as, for example, enhanced light detection properties." '359 Patent at 6:13-18. FIGS. 1-6 depict embodiments of the '359 Patent that include structures for detecting light. '359 Patent at FIGS. 1-6, 3:31-48, 7:64-8:1. For these reasons, a POSITA would understand that the field of endeavor of the '359 Patent includes semiconductor devices for detecting light.

C. Problem Solved by the Inventors of the '359 Patent

30. I have been informed that a prior art reference is “reasonably pertinent” if a POSITA would have consulted it and applied its teachings when faced with the problem(s) that the inventor was trying to solve. As such, I have been asked to analyze the '359 Patent and determine the problem(s) that the inventors were trying to solve.

31. The '359 Patent recognizes problems caused by “electrical and optical cross-talk between adjacent sensor pixels....” *'359 Patent* at 1:27-40. The '359 Patent further describes that “[s]ignificant cross-talk can be generated due to reflection off the often planar back surface of the device.” *'359 Patent* at 1:34-36. The '359 Patent aims to prevent loss of light from pixels by proposing “image sensor pixels and elements for trapping light within such pixels.” *'359 Patent* at 6:16-20, 6:38-42. Thus, a POSITA would have understood the '359 Patent is directed to solving the problems of reducing electrical and/or optical cross-talk between adjacent pixels and/or reducing the loss of light from each pixel.

D. File History of the '359 Patent

32. I understand that the application leading to the '359 patent (Appl. No.: 15/216,244, “the '244 application”) was filed on July 21, 2016. *'359 patent* at (22). I understand that it ultimately claims priority to a provisional application filed on March 22, 2012. *'359 patent* at (60).

33. I understand that upon filing the '244 application, Applicant filed a Track One Request for Prioritized Examination which was granted. Ex. 1002, p. 287. Applicant also presented a preliminary amendment which cancelled claims 1-33 and added claims 34-59. Ex. 1002, p. 354. I understand that the Examiner issued a restriction requirement, identifying the then-pending claims as being directed to “patentably distinct species: embodiment or species 1 of fig. 1, embodiment or species 2 of fig. 2, embodiment or species 3 of fig. 3, embodiment or species 4 of fig. 4, embodiment or species 5 of fig. 5, embodiment or species 6 of fig. 6, embodiment or species 7 of fig. 7.” Ex. 1002, p. 281. In response, I understand that Applicant elected without traverse Species 4 (i.e., the Figure 4 embodiment) for continued prosecution and further added new claims 60-65. Ex. 1002, p. 261. I understand that this means that the Applicant considers the claims presented in this application to refer to the Figure 4 embodiment of the '359 patent.

34. I understand that the Examiner then issued a Non-Final Office Action in which the Examiner rejected certain of the pending claims as 1) anticipated over Velichko (U.S. Pat. App. Pub. 2013/0200251) and/or 2) obvious over Velichko, Yanagisawa (JP 403183037), Bour (U.S. Pat No. 8,470,619), and/or Gray (U.S. Pat. No. 8,906,670). The Examiner also indicated the subject matter of application claims 62 and 65 to be allowable. Ex. 1002, pp. 219-227.

35. In response, I understand that Applicant amended the independent claims to incorporate the limitations of the allowable claims and added an additional claim. Applicant did not present any arguments in view of the prior art. Ex. 1002, p. 199.

36. The Examiner then withdrew the indication of allowability as to claims 62 and 65 and issued a second Non-Final Office Action in which the Examiner rejected the pending claims as 1) anticipated by Haddad (WO 2011035188), and/or 2) obvious over Haddad, Yanagisawa (JP 403183037), Gray (U.S. Pat. No. 8,906,670), and/or Bour (U.S. Pat. No. 8,470,619). Ex. 1002, pp. 163-173.

37. In Response, Applicant amended, canceled, and added claims, and presented arguments purporting to distinguish the prior art. Applicants also contended that Yanagisawa was not analogous art. Ex. 1002, 11/13/2017, pp.133-137.

38. The Examiner then finally rejected certain of the claims as obvious over the art previously cited, with the exception that the Examiner did not rely further on the Yanagisawa art and instead relied on Ooka (JP 407074240). Ex. 1002, pp. 94-104.

39. The Examiner also identified the subject matter of application claims 35, 38, and 53 as being allowable. Ex. 1002, pp. 101-102. These application claims are reproduced below:

35. (Currently Amended) The device of claim 34, wherein said peripheral isolation element comprises a first, a second and a third layer, wherein said third layer is disposed between said first and second layers, and wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer ~~the backside light trapping material reflects the light incident thereon back into the pixel.~~

38. (Currently Amended) The device of claim ~~35~~ 34, wherein at least one of said first and second layers comprises silicon dioxide ~~the peripheral sidewall extends from the light incident surface to the backside surface.~~

53. (Currently Amended) The device of claim 52, wherein said peripheral isolation element comprises a first, a second and a third layer, wherein said third layer is disposed between said

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Application No.: 15/216,244
Examiner: Long Pham

Attorney Docket No.: 143705.05221
Art Unit: 2814

first and second layers, and wherein each of said first and second layers exhibits an index of refraction less than an index of refraction of said third layer ~~said backside light trapping material substantially covers the backside surface.~~

Ex. 1002, pp. 128-132.

40. In response, Applicant filed a Request for Continued Examination, amended certain claims to incorporate the subject matter deemed allowable, canceled other claims, and added new claims 68-121. Ex. 1002, pp. 55-70.

41. I understand that the Examiner then allowed the then-pending claims, but did not provide any specific reasons for allowance. Ex. 1002, pp. 16-20.

IV. LEVEL OF A PERSON OF ORDINARY SKILL

42. For purposes of this proceeding, I have been asked to apply the following level of ordinary skill as of March 22, 2012: “[A]t least a bachelor’s degree in electrical engineering, materials science, or physics (or an equivalent degree), at least two years of experience in optoelectronics, and at least three years of work experience in semiconductor manufacturing....[A] master’s degree or Ph.D. in a relevant field may substitute for some work experience or vice versa.” I meet this definition. When I refer to the understanding of a POSITA, I am referring to the understanding of such a person as of March 22, 2012.

V. OVERVIEW OF THE TECHNOLOGY

43. I was asked to briefly summarize the background of the prior art from the standpoint of a person having ordinary skill in the art prior to March 22, 2012. As explained below, the image sensor technologies described by the ’359 Patent were based on well-known principles of light-to-electrical signal conversion and semiconductor design. Thus, the techniques discussed in the ’359 Patent were well-known and conventional prior to the invention of the ’359 Patent.

A. Image Sensor Operation

44. Image sensors are built on semiconductor technology, which provides the foundation for converting light into electrical signals. Semiconductors serve as the medium for photon absorption and the generation of electron-hole pairs, a foundational process in optoelectronic devices. *Sze* at p. 53 (“When light passes through a semiconductor, absorption of light and generation of electron-hole pairs (G,) occur...”). An electron-hole pair is “a carrier pair produced when a photon or particle photoelectrically interacts with a silicon atom.” *Janesick* at p. 879. “Interacting photons with sufficient energy will excite an electron into the conduction band, creating an electron-hole pair.” *Janesick* at p. 26 The pair is free to “move and diffuse in the silicon lattice structure.” *Janesick* at p. 26.

45. The structure that converts light into electron-hole pairs is known as a PN junction. A PN junction is formed by joining regions of positively doped (P-type) and negatively doped (N-type) material. *Sproul* at p. 16 (“Doping one side of a piece of silicon with boron (a p-type dopant) and the other side with phosphorus (an n-type dopant) forms a p-n junction”).

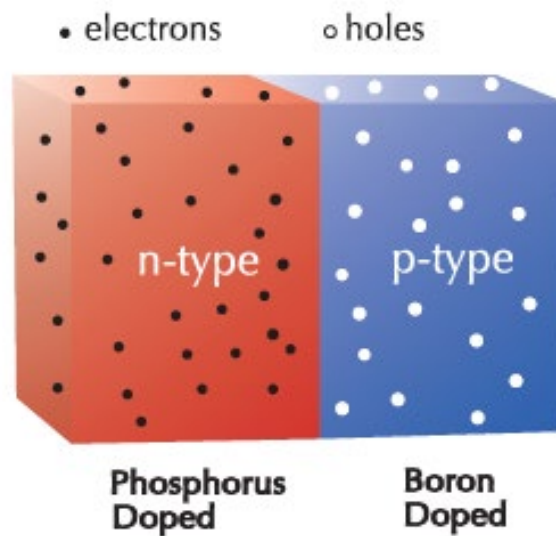
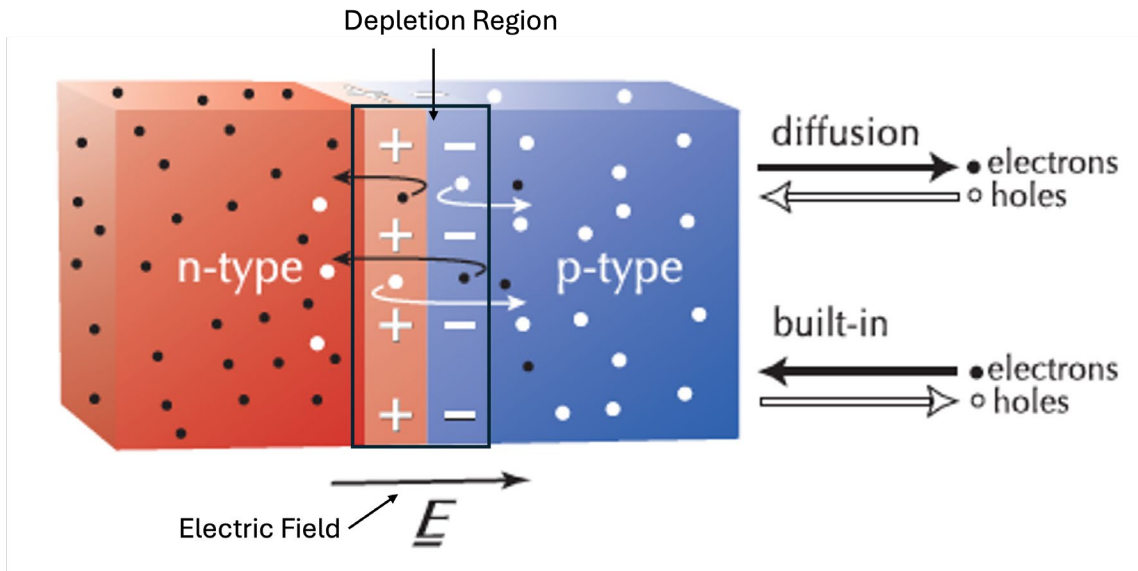


Figure 2 n-type and p-type materials brought together.

Sproul at p. 17.

46. A PN junction has a “depletion (or space charge region) at the junction interface [that] has a high electric field and readily separates photogenerated electron-hole pairs.” *Lee* at [0004]. As the electron-hole pairs diffuse, the electrons leave behind positively charged ions, and the holes leave behind negatively charged ions. *Sproul* at p. 18 (“As the electrons in the n-type material diffuse across towards the p-type side, they leave behind positively charged phosphorous ions. . . Similarly, the positive holes in the p-type region diffuse towards the n-type side and leave behind negatively charged boron ions...”). This process “set[s] up an electric field right at the junction between the n-type and p-type material.” *Sproul* at p. 18. The electric field “causes some of the electrons and holes to flow in the opposite direction

to the flow caused by diffusion...” *Sproul* at p. 18. “These opposing flows eventually reach a stable equilibrium” such that “the net flow of electrons across the junction is zero and the net flow of holes across the junction is also zero,” thereby forming a region depleted of mobile charges called the depletion region. *Sproul* at p. 19.



Sproul at p. 18.

47. The built-in electric field provided by the depletion region of the PN junction makes it such that “electrons are attracted towards the positive charge on the n-type material side” while “holes are attracted to the negative charge on the p-type material side.” *Sproul* at p. 22. It is “[t]his separation of charges [that] causes a current to flow across the junction,” thereby creating an electrical signal. *Sproul* at p. 22.

48. The electric field provided by the depletion region of a PN junction is essential for the generation of an electrical signal. Without it, “[e]lectrons and holes can remain excited only for a short period of time” and will undergo recombination where “excited electrons stray too close to holes and the two fall back into bonded positions.” *Sproul* at p. 22. In such an instance, “the [electron-hole] pair’s electrical energy is lost as heat.” *Sproul* at p. 22. Thus, the separation of electron-hole pairs generates an electrical signal in image sensors.

49. This means that both P-type and N-type regions are needed to convert light into an electrical signal. Indeed, “[i]n a block of silicon that is not electrically biased,” (i.e., not doped) “photocarrier generation” (i.e., electron-hole pair generation) “would be balanced by an increase in recombination, providing net current neutrality.” *McGrath* at p. 33. “For an image sensor pixel, it is necessary to take advantage of the semiconductor behavior of silicon to create a region out of equilibrium (e.g., a depletion region completely drained of mobile charge carriers), so that the photocarriers can be collected before they recombine.” *McGrath* at p. 33. That is, a PN junction’s depletion region is required for electron-hole pairs to be separated.

B. Quantum Efficiency (QE)

50. Quantum efficiency (QE) “is a measure of the effectiveness at converting photons into electrons.” Shea at p. 35. Specifically, QE “is a measure of

the fraction of electrons extracted from a device per incident photon as a function of wavelength.” *Shea* at p. 25.

51. QE “varies with the wavelength of the incident light ... as well as applied reverse bias and temperature.” *OSI Whitepaper* at p. 4. QE is “related to responsivity” of the semiconducting material. *OSI Whitepaper* at p. 5. “The responsivity of a silicon photodiode is a measure of the sensitivity to light, and it is defined as the ratio of the photocurrent to the incident light power at a given wavelength.” *OSI Whitepaper* at p. 5. The design of photodiodes directly influences QE because they affect the responsivity of the semiconductor. For example, “by controlling the thickness of the bulk substrate, the speed and responsivity of the photodiode can be controlled.” *OSI Whitepaper* at p. 2.

52. Often, anti-reflective coatings “are required for the reduction of surface reflection.” *Macleod* at p. 86. The reduction of surface reflections allows more incident light to enter the photodiode, thereby increasing the number of photons available for absorption. To further enhance the amount of light reaching the active region, optical coatings are applied in multiple layers. “Antireflection coatings can range from a simple single layer having virtually zero reflectance at just one wavelength, to a multilayer system of more than a dozen layers, having virtually zero reflectance over a range of several octave.” *Macleod* at p. 86.

53. Beyond coatings, surface texturing can be used to alter the interaction of light with the photodiode material. “A correlation between the degree of light randomization and trapping, with the scale length of the texturization geometry was found. The observed absorption enhancement corresponds to 90% of the best possible theoretical value, or 90% light randomization.” *Boroditsky* at p. 1. The increased path length of photons within the material improves the probability of absorption, leading to greater carrier generation. “In all the textured samples, an increase in absorption was measured in comparison with the untextured films.” *Boroditsky* at p. 3.

54. The choice of semiconductor material also affects quantum efficiency, as different materials exhibit varying absorption properties across the electromagnetic spectrum. silicon is commonly used in photodiodes due to its suitable bandgap energy. “Energy band, carrier concentration, and transport properties are briefly surveyed, with emphasis on the two most-important semiconductors: silicon (Si) and gallium arsenide (GaAs).” *Sze* at p. 1. Material properties influence absorption efficiency, particularly in thin-film applications. “Amorphous silicon (a-Si) is a well-studied material for thin-film... [where] the difference between crystalline and amorphous Si is dramatic; the former has an indirect bandgap of 1.1 eV, whereas hydrogenated a-Si has an optical absorption characteristic resembles that expected for a crystal with a direct bandgap of 1.6 eV.”

Sze at p. 88. These bandgap energies are well-suited for applications in the visible light spectral range.

55. By modifying materials and structures, photodiodes can achieve higher quantum efficiency. These methods collectively enhance the ability of the sensor to convert incident photons into charge carriers, improving overall performance in imaging, sensing, and optical communication applications.

C. Backside and Frontside Illuminated Sensors

56. The evolution of CMOS and CCD image sensors has driven the development of backside-illuminated (BSI) sensors, which outperform traditional frontside-illuminated (FSI) designs in many respects. “Backside-illuminated CMOS image sensors (BSI) capture light directly on the silicon light-sensitive layer. They have a higher sensitivity in a broader spectrum than the mainstream frontside-illuminated imagers (FSI).” *Provoost* at p. 1. The key innovation of BSI technology is its ability to optimize light absorption by repositioning the photodiode to the light-facing side of the sensor. Additionally, “in the fabrication process, after the CMOS circuitry and the interconnect layers have been created, the backside of the chip is ground and etched away until the photoactive layer is exposed. The resulting chip is very thin, sometimes below 5 μ m. When carefully engineered, such a sensor can improve the chance of capturing an input photon to over 90%. It will also be sensitive

over a wider spectrum than is possible with FSI sensors, having a good efficiency even into the ultraviolet bands.” *Provoost* at p. 1.

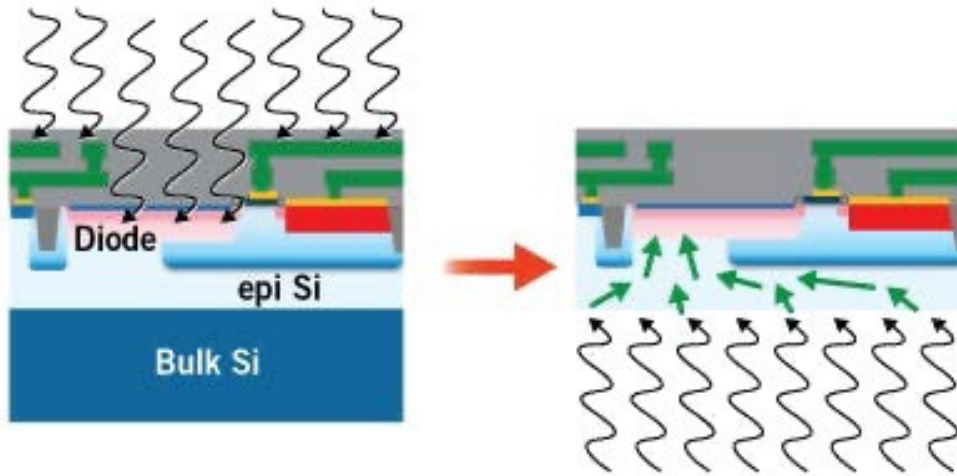


FIGURE 2. Schema of an FSI imager (left) and BSI imager (right).

Provoost at Fig. 2.

57. In FSI sensors, “incident photons must pass through the poly gates before they can interact with the epitaxial layer [and] gate absorption represents a significant QE loss mechanism, especially for photons with short absorption lengths. Reflection loss also degrades QE performance over a major portion of the working spectrum. Transmission loss is important for very long and very short wavelength photons that penetrate the epitaxial layer without interaction.” *Janesick* at p. 167. Crosstalk, both optical and electrical, poses further challenges in achieving high image fidelity. In FSI sensors, “the circuits share ground currents, which in turn causes cross-talk problems.” *Janesick* at 706. “[E]lectrical crosstalk consists in the

diffusion of electrical charge (electrons or holes depending the pixel type) between adjacent pixels. It occurs in silicon material due to electrical mechanisms (diffusion and drift).” *Tournier* at p. 1. Further, “optical crosstalk corresponds to a photon exchange between neighboring pixels before electron/holes pairs generation. It mainly appears in back-end stack due to optical mechanisms (reflexion, refraction or diffraction) but can also occur in silicon substrate.” *Tournier* at p. 1.

58. BSI sensors address the challenges of FSI architecture by reversing the structure: the photodiode is positioned on the light-facing side of the sensor, while the circuitry is moved to the rear. *Tournier* at p. 8. In a back-illuminated (BSI) sensor, the chip is turned upside down, with the light falling on the backside.” *Provoost* at p. 4. “When carefully engineered, such a sensor can improve the chance of capturing an input photon to over 90%. It will also be sensitive over a wider spectrum than is possible with FSI sensors, having a good efficiency even into the ultraviolet bands.” *Provoost* at p. 4. The backside architecture significantly improves fill factor; in some cases, “a wafer-scale back-illumination process is used to achieve 100% fill factor photodiodes.” *Suntharalingam* at p. 1.

59. The unimpeded light path in BSI sensors results in higher quantum efficiency, as more photons are absorbed and converted into electrical signals and allows “the image sensor to be operated with light directly incident on the photo detector without obscuration from pixel circuitry” *Suntharalingam* at p. 2.

Additionally, the BSI design is particularly advantageous in high-resolution sensors with small pixels and “permits aggressively small pixels which are 100% fill factor after back illumination. The use of high resistivity detector tier substrates, similar to those used for scientific-grade CCDs, provides much greater spectral sensitivity.” *Suntharalingam* at p. 7.

60. BSI sensors also tackle crosstalk issues more effectively than their FSI counterparts while also “preserv[ing] the functionality of the sensor operation.” *Suntharalingam* at p. 7. Deep trench isolation (DTI) further enhances pixel isolation by confining charge carriers to their respective regions. “Comparison with other pixel isolation architectures show that Deep Trench is the best approach to suppress electrical crosstalk.” *Tournier* at p. 1. “With ... DTI integration... [c]rosstalk is extremely low and permits a great color fidelity to be achieved.” *Tournier* at p. 3.

D. Isolation Techniques

61. “Deep Trench technology for CMOS image sensor was successfully developed and industrialized for best-in-class 1.4 μ m pixel Front-Side Illumination (FSI) technology. The performance achievements on QE both on and off-axis without any degradation of other pixel parameters show the need of a perfect pixel isolation for better color fidelity. Comparison with other pixel isolation architectures show that Deep Trench is the best approach to suppress electrical crosstalk.” *Tournier* at p. 1.

62. Shallow trench isolation (STI) is used in image sensor fabrication prior to the implementation of deep trench isolation (DTI). “DTI formation is performed after Shallow Trench Isolation (STI) formation.” *Tournier* at p. 2. STI provides physical and electrical separation between adjacent pixels. *See e.g., Mouli-214* at 2:1-3 (“Shallow trench isolation (STI) is one technique, which can be used to isolate pixels, deices or circuitry from one another.”).

63. Despite its use in preventing pixel-to-pixel interference, using STI alone has certain limitations. “One drawback associated with shallow trench isolation in the case of CMOS image sensors is cross-talk from a photon impinging on a particular pixel of a photosensitive device causing changes that may diffuse under the shallow trench isolation structure to an adjacent pixel.” *Mouli-214* at 2:15-19. “Another drawback is that a hole accumulation layer along the sidewall of the trench is relatively small since it is limited by the depth of the shallow trenches.” *Mouli-214* at 2:19-22.

64. To address these concerns, deep trench isolation (DTI) is implemented to improve pixel separation. “Comparison with other pixel isolation architectures show that Deep Trench is the best approach to suppress electrical crosstalk.” *Tournier* at p. 2. The use of “deep trench structure” contributes to the physical isolation of pixels. *Tournier* at p. 2. These methods are also applicable to sensors with smaller pixel sizes. “This technology also permits improvement in performance

of bigger pixels and will be key for 1.1 μ m or smaller pixels either in Front-Side or Back-side Illumination (FSI / BSI) technologies.” *Tournier* at p. 5.

65. Doped trenches enhance the functionality of isolation structures by introducing electric fields that repel charge carriers, complementing the physical isolation provided by the trench itself. For instance, “highly doped polysilicon filled high aspect ratio trenches” reduces crosstalk and enhances pixel isolation. *Minoglou* at p. 129. “By incorporating highly doped polysilicon filled high aspect ratio trenches in between pixels, a strong lateral drift field is generated. In theory, this blocks inter pixel diffusion and thus confines the collection volume to an individual pixel.” *Minoglou* at p. 129. Additionally, it is well-known that sloped sidewalls help to increase “light collection efficiency and, hence, the amount of light absorbed” by an image sensor. *Street* at 10:55-59. Further, a “sloped sidewall” provides an “advantage over vertical sidewalls” by “reducing the tendency for voids to form” in “dielectric layer deposition.” *Su* at [0035].

66. The materials used to fill isolation trenches have also evolved to improve their effectiveness in blocking both optical and electrical crosstalk. “Then standard gapfill, anneal and CMP are realized to finalize DTI formation.” *Tournier* at p. 2. “This waveguide-like structure at silicon level is due to differences in refractive index between SiO₂ (n=1.5 at 532nm) and Si (n=4 at 532nm).” *Tournier* at p. 3. Deep trench structures employing materials with different refractive indices

serve to isolate pixels and in some cases function as “the interface Si-SiO₂ which is used as a wall against electron diffusion.” *Tournier* at p. 1. These materials work alongside other light-management features, such as anti-reflective coatings, to maximize quantum efficiency.

E. Additional Efforts to Reduce Crosstalk

67. The incorporation of CMOS image sensors into consumer devices, such as mobile phones and digital cameras, “led to the development of technology with pixel sizes down to 2µm x 2µm, and even sub-1µm [1,2].” *Tournier* at p. 1. With smaller pixels, the major challenge was “the need to suppress all parasitic charge exchange between neighbouring pixels, also called crosstalk,” which “can cause a loss in image quality.” *Tournier* at p. 1. “Optical crosstalk corresponds to a photon exchange between neighbouring pixels before electron/holes pairs generation.” *Tournier* at p. 1. “[E]lectrical crosstalk consists in the diffusion of electrical charge (electrons or holes depending on the pixel type) between adjacent pixels.” *Tournier* at p. 1.

68. Another approach to mitigating optical crosstalk involves the use of Bragg reflectors. These structures have alternating layers of materials with different refractive indices, enabling control over the reflection and transmission of light through interference. “In the distributed Bragg reflector (DBR), light reflected at the interface between each layer is designed to constructively interfere to maximize the

total reflected optical power at a specific wavelength.” *Perez* at p. 297. “The reflectivity is maximized if the structure is composed of alternating layers of two materials of different indices of refractions.” *Perez* at p. 297. These structures provide control over the reflection and transmission of light, allowing for precise optical management. “A hybrid bulk micromachining and multilayer PECVD thin film process is used to form the Bragg reflectors on angled sidewalls, which redirect...light through the vapor cell and back toward the plane of the source with reduced optical power loss.” *Perez* at p. 295.

69. Strategies for reducing electrical crosstalk include modifications to doping profiles, which create potential wells that confine charge carriers within individual pixels. Doping strategies provide an additional method of controlling charge carrier movement. “Starting from a conventional structure, a first solution is to isolate neighbored pixels by using dedicated P+ implants with varying energies to create a wall.” *Tournier* at p. 1. “The purpose is to optimize differently the photon collection for each color and to isolate laterally the pixels.” *Tournier* at p. 1. “Another solution consists in the use of adapted pinned deep diode on n-substrates.” *Tournier* at p. 1. “In this case, the inter-pixel isolation is realized by p-implants at multiple energies and doses, in order to create a junction isolation wall,” which “are said to be 4-11 times more effective than the first solution.” *Tournier* at p. 1.

70. Doped trenches function as both optical and electrical isolation structures by creating physical barriers that confine carriers. “The use of pinned deep diode on n-substrates. In this case, the inter-pixel isolation is realized by p-implants at multiple energies and doses, to create a junction isolation wall.” *Tournier* at p. 1.

F. Related Fields

71. The principles underlying CMOS and CCD image sensors are closely connected to advancements in other optoelectronic technologies, such as solar cells and LEDs. “Solar cells which to some extent share some similarity with photodetectors in that they both convert light to electricity.” *Sze* at p. 667. These fields share fundamental processes involving the interaction of light with semiconductors to produce measurable electronic responses. “The purpose of the solar cells, however, is for power generation from the sunlight, as opposed to detection of faint light . . . [s]o one difference between them is the intensity of light involved. *Sze* at p. 667. “The second difference being that solar cells are power generators and as such no external bias is required, whereas photodetectors usually require some bias and the change of current is detected as signal.” *Sze* at p. 667. This similarity has fostered a transfer of knowledge and innovation between these technologies.

72. Solar cells have influenced the development of image sensors by advancing techniques for optimizing light absorption. One such advancement is the

use of textured surfaces to trap and redirect light. “To reduce light reflection, a textured surface, either on the front or on the back, has been used to trap the light.” *Sze* at p. 731. By enhancing light absorption, these innovations have helped ensure that more photons reach the active region of the sensor, improving efficiency and reducing losses.

73. Anti-reflective coatings and light-trapping techniques for semiconductors have significantly influenced sensor design. “The addition of an anti-reflection coating reduces the overall reflection to a few percent.” *Sze* at p. 731. Originally developed to enhance light emission in LEDs and photon capture in solar cells, these techniques have been adapted to minimize reflection losses in CMOS and CCD sensors. “For detectors with internal photoemission, it is more efficient to direct the incoming light through the substrate. ... It is possible to choose a proper metal and antireflection coating so that a large fraction of the incident radiation will be absorbed near the surface of the semiconductor.” *Sze* at 682.

74. Multilayer anti-reflective coatings are specifically engineered to reduce unwanted reflections and maximize light transmission. A three-layer coating on germanium, where “each layer is quarter-wave thick.” If properly designed, the reflectance vectors “will completely cancel at these wavelengths, giving zero reflectance.” *MacLeod* at p. 102.

75. The anti-reflective coatings ensure that incident light is effectively directed toward the photodiode, enhancing quantum efficiency and overall sensor performance. “In optical instruments with multiple reflecting components, overall transmission is determined by the product of the reflectances of each element.” *MacLeod* at 164. “Many spectrometers, for instance, contain ten or more reflections, causing a significant drop in transmission, but must still function over a wide spectral range.” *MacLeod* at 164.

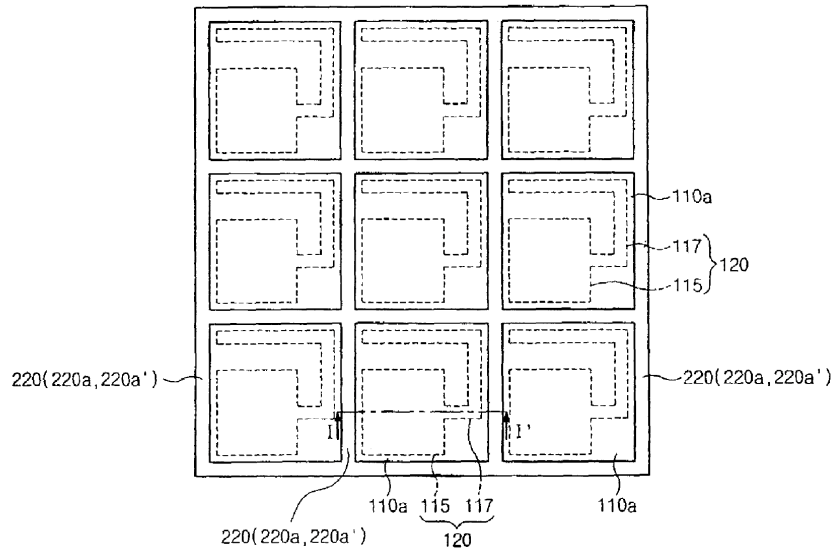
VI. SUMMARY OF THE PRIOR ART REFERENCES

A. Hwang-099

76. Hwang-099 teaches “an image sensor that converts incident light into electrical signals and methods of forming the image sensor.” *Hwang-099*, 1:14-19. Hwang-099 recognizes that “there are many factors that can reduce the spectral sensitivity” and describes one example where “the amount of light absorbed by the photodiode” within an image sensor may be “reduced according to the wavelength of the light.” *Hwang-099*, 1:30-42. As such, “regions of light with a long wavelength...are likely not to be absorbed completely by the photodiode, thus reducing the spectral sensitivity.” *Hwang-099*, 1:44-47.

77. To solve this problem, Hwang-099 proposes an “image sensor with an increased spectral sensitivity” that is “capable of minimizing interference between neighboring pixels[.]” *Hwang-099*, 1:52-58. Hwang-099’s image sensor includes an

array of pixels “arranged two-dimensionally in rows and columns on a substrate 300.” *Hwang-099*, 5:52-54.

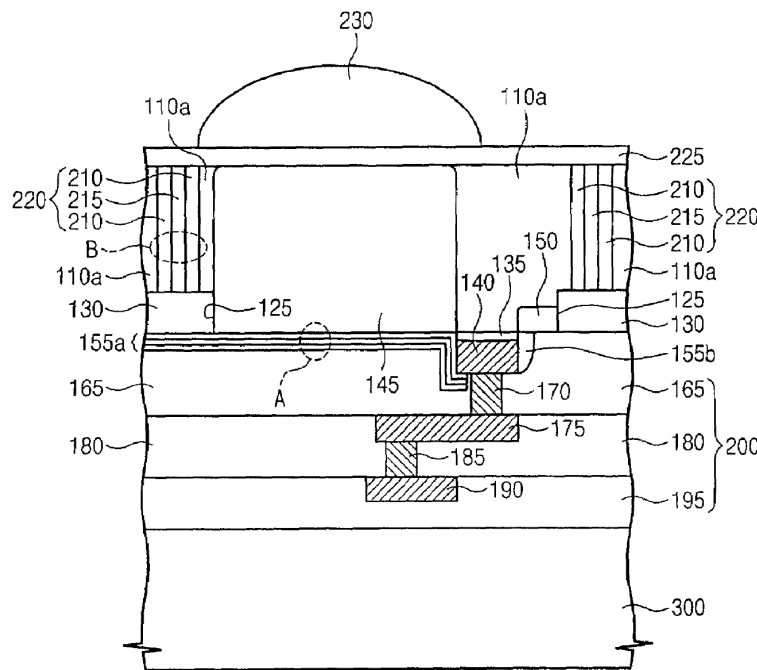


Hwang-099, FIG. 1.

78. Each pixel semiconductor pattern 110a in the array is enclosed by sidewall multi-layered reflection layer 220. *Hwang-099*, 6:15-19 (“The sidewall multi-layered reflection layer 220 encloses the side walls of the pixel semiconductor patterns 110a. As shown, the sidewall multi-layered reflection layer 220 can be disposed between all of the pixel semiconductor patterns 110a.”), FIG. 1. The sidewall multi-layered reflection layer 220 includes a “plurality of layers sequentially stacked at the walls of the pixel semiconductor patterns 110a” where the layers have “different respective refractive indexes.” *Hwang-099*, 6:9-13, FIGS. 1-2. Similarly, a base multi-layered reflection layer 155a that “includes at least two

tacked layers having different refractive indexes” contacts a surface of the “pixel semiconductor pattern 110a on which the photodiode 145 is formed.” *Hwang-099*, 8:32-37.

79. The base multi-layered reflection layer reflects incident light such that reflected light is “incident again on the photodiode 145,” which increases “the light sensitivity of the image sensor.” *Hwang-099*, 9:10-14. The sidewall multi-layered reflection layer 220 “minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels” and reflects light to be “incident again on the photodiode 145,” which minimizes “image distortion” and increases “absorption efficiency of incident light.” *Hwang-099*, 10:19-27, 10:31-35, 15:38-41.



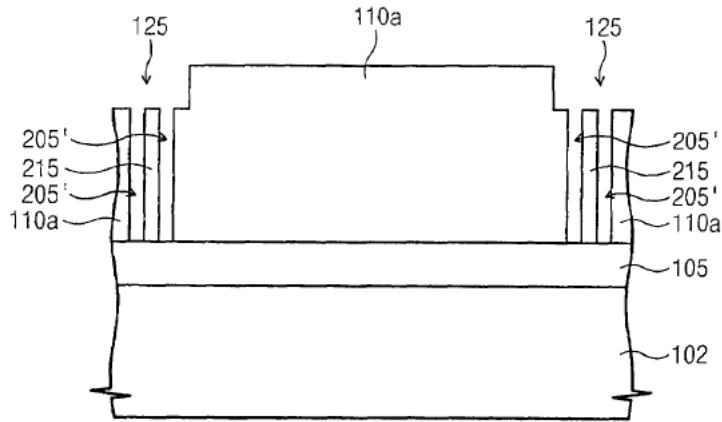
Hwang-099, FIG. 2.

80. Hwang-099 also teaches a micro lens 230 that “covers the photodiode 145 [and] is disposed on the color filter 225. External light passes through the micro lens 230 and the color filter 225, and is incident on the second surface of the photodiode 145.” *Hwang-099*, 8:18-22. The positioning of Hwang-099’s micro lens 230 is such that quantum efficiency of Hwang-099’s pixel is enhanced. That is, Hwang-099 expressly teaches that “photodiodes 145 form a PN junction with the pixel semiconductor pattern 110” and are “doped at a low concentration, so that most or the entirety the photodiodes 145 become depletion regions.” *Hwang-099*, 6:3-6. Hwang-099 also states that “[w]hen external light is incident on a depletion region in the photodiode, electron-hole pairs are generated, and the external light is converted to electrical signals.” *Hwang-099*, 1:25-29. As such, a POSITA would appreciate that Hwang-099’s micro lens is strategically placed above photodiode 145, such that incident light is directed to the depletion region of the PN junction formed by photodiode 145 and pixel semiconductor pattern 110a. It was known that “electron-hole pairs that are generally formed outside of the depletion region are not separated as effectively as they would have been within the depletion region, and thus have a higher chance to recombine (which lessens the sensitivity of pixels). *Mao* at 35-39. Thus, a POSITA would have appreciated that while pixel semiconductor pattern 110a and photodiode 145 together form a PN junction, having a micro lens to direct light specifically into photodiode 145 (depletion region) would

advantageously increase the number of electron-hole pairs that are separated, which generates current, rather than undergo recombination where “no current or charge accumulation results.” *Hibbeler* at [0035].

81. FIGS. 18 and 19 represent the intermediate steps of a method of manufacturing the image sensor. *Hwang-099*, 14:3-37. Regarding FIG. 18, “a first substrate 100 having a semiconductor layer 110 is prepared, after which the semiconductor layer is patterned to form a trench 125 that restricts an active region.” *Hwang-099*, 14:3-6. After trench 125 is formed, the “floor of trench 125 is selectively etched to form a plurality of grooves 205’ that “define[] a pixel semiconductor pattern 110a.” *Hwang-099*, 14:7-9. Grooves 205’ are shown below in FIG. 18, where they are “spaced apart from one another” and a “residual portion 215 of semiconductor layer 110 is left between the grooves 205’.” *Hwang-099*, 14:10-12.

Fig. 18



Hwang-099, FIG. 18.

82. The following manufacturing steps are disclosed with reference to FIG. 19, where “an oxide layer i[s] formed to fill the trench 125 and grooves 205’” such that “the portion of the oxide layer filling the trench 125 corresponds to a device isolation pattern 130, and the portion of the oxide layer filling groove 205’ corresponds to a first sidewall reflection layer 210.” *Hwang-099*, 14:13-18. “The residual portion 215 of the semiconductor layer 110 between the grooves 205’ is a second sidewall reflection layer 215.” *Hwang-099*, 14:18-20.

Fig. 2

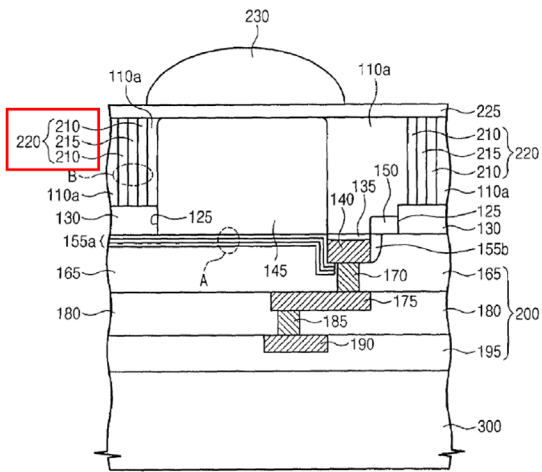
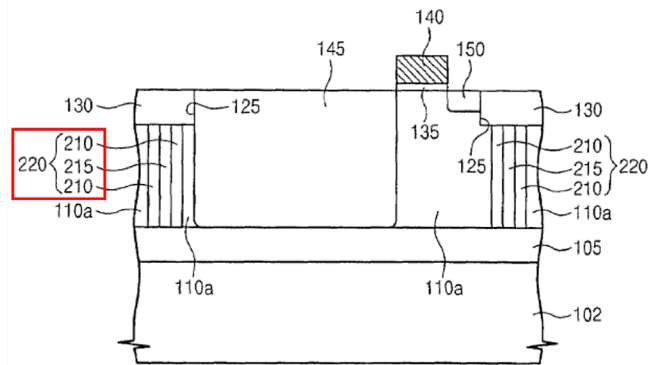


Fig. 19



Hwang-099, FIGS. 2 and 19.

84. Regarding FIG. 19, Hwang-099 expressly states that the portions of oxide filling trench 125 and grooves 205 correspond to device isolation pattern 130 and first sidewall reflection layer 210. See ¶ 82; Hwang-099, 14:13-18. Similarly, Hwang-099 expressly states that the residual portion 215 of semiconductor layer 110 in FIG. 19 corresponds to second sidewall reflection layer 215.” Hwang-099, 14:18-20. I note that reference numerals 210 and 215 are only used in the FIG. 2 embodiment of Hwang-099. Hwang-099, FIG. 2, FIG. 5, FIG. 6 (noting the different reference numerals used in sidewall multi-layered reflection layer 220 in FIGS. 5-6 compared to FIG. 2). Therefore, it is clear that the method of manufacturing disclosed with reference to FIGS. 18 and 19 corresponds to the embodiment of FIG. 2.

85. I note that Hwang-099 references the use of “silicon oxide” through the specification. *Hwang-099*, 1:20-22, 4:3-4, 9:25-29, 10:2-3, 10:50-52, 11:54-55, 13:11-13. Hwang-099 teaches silicon oxide has a refractive index of “approximately 1.46” and discloses embodiments that are applicable to “external light having a long red-colored wavelength.” *Hwang-099*, 9:25-32, 10:48-55. Because Hwang-099 teaches that silicon oxide has a refractive index of 1.46, a POSITA would have understood that Hwang-099 is specifically referring to silicon dioxide because silicon dioxide has a refractive index of approximately 1.46 at the wavelength of red light. *See e.g., Maltison* at p. 1205-1206 (showing the refractive index of silicon dioxide across many wavelengths, including that of red light); *Komuro* at [0137], Table 1.

86. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

87. As discussed above, the field of endeavor of the claimed invention of the '359 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, Hwang-099 is directed to “an image sensor that converts

incident light to electrical signals” and the embodiments described are directed to increasing the light sensitivity of an image sensor. Thus, Hwang-099 is directed to semiconductor devices for detecting light and accordingly is in the same field of endeavor as the claimed invention of the ’359 Patent.

88. Hwang-099 is also reasonably pertinent to the problems solved by the inventors of the ’359 Patent. As discussed above, the ’359 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels. *See* ¶¶ 30-31. As demonstrated above, Hwang-099 describes a sidewall multi-layered reflection layer 220 that “minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels” (i.e., cross-talk). Thus, a POSITA would have consulted Hwang-099 and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

B. Cole

89. Cole is directed to image sensors having an array of pixels. *Cole*, ¶0002. Cole states: “[a]n image sensor generally includes an array of pixel cells, which include photo-conversion devices for converting light incident on the array into electrical signals, and peripheral circuitry, which includes circuitry for controlling devices of the array and circuitry for converting the electrical signals into a digital image.” *Cole*, ¶0002.

90. Cole further teaches isolation structures for pixels in image sensors. *Cole*, Abstract, ¶0002. Some of Cole’s embodiments relate to structures to separate pixels from peripheral circuitry, but Cole also emphasizes the need to optically and electrically isolate individual pixels from one another. *Cole*, ¶0005. Cole states:

“A photon impinging on a particular pixel of a photosensitive device may diffuse to an adjacent pixel, resulting in detection of the photon by the wrong pixel, i.e. cross-talk. Therefore, **CMOS image sensor pixels must be isolated from one another to avoid pixel cross talk.** In the case of CMOS image sensors, which are intentionally fabricated to be sensitive to light, **it is advantageous to provide both electrical and optical isolation between pixels.**”

Cole, ¶0005 (Emphasis added).

91. An exemplary cross-section containing a pixel is illustrated in Fig. 7, reproduced below, which shows a pixel region with a photodiode, separated at the periphery by structures 340:

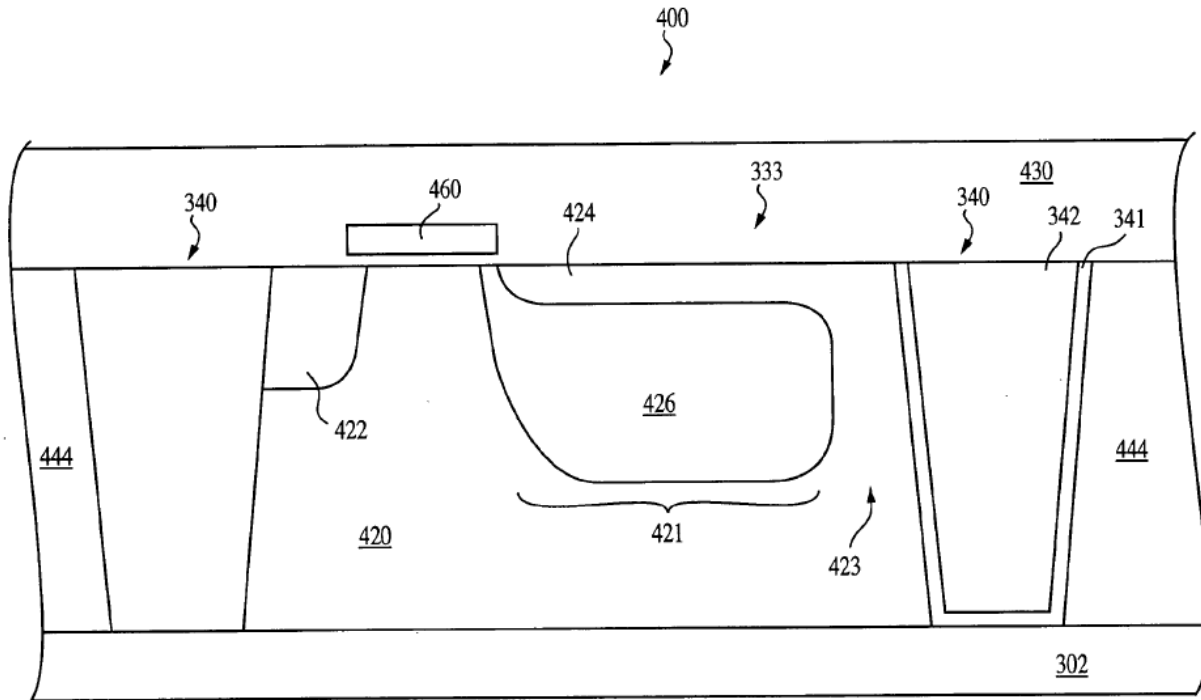


FIG. 7

Cole, Fig. 7, ¶0044.

92. The pixel region has a “p-type active layer 420”, having within it an “n-type photodiode region 426”. *Cole*, ¶0045. The pixel has, at its periphery, a trench isolation region 340, that can be formed according to the embodiments of Figs. 4-6.

93. *Cole* teaches an embodiment in Fig. 6, in which trench 340 is filled with materials 343, 344, and 345, thus forming a five-layer separation structure. *Cole*, ¶0042. Fig. 6 is shown here:

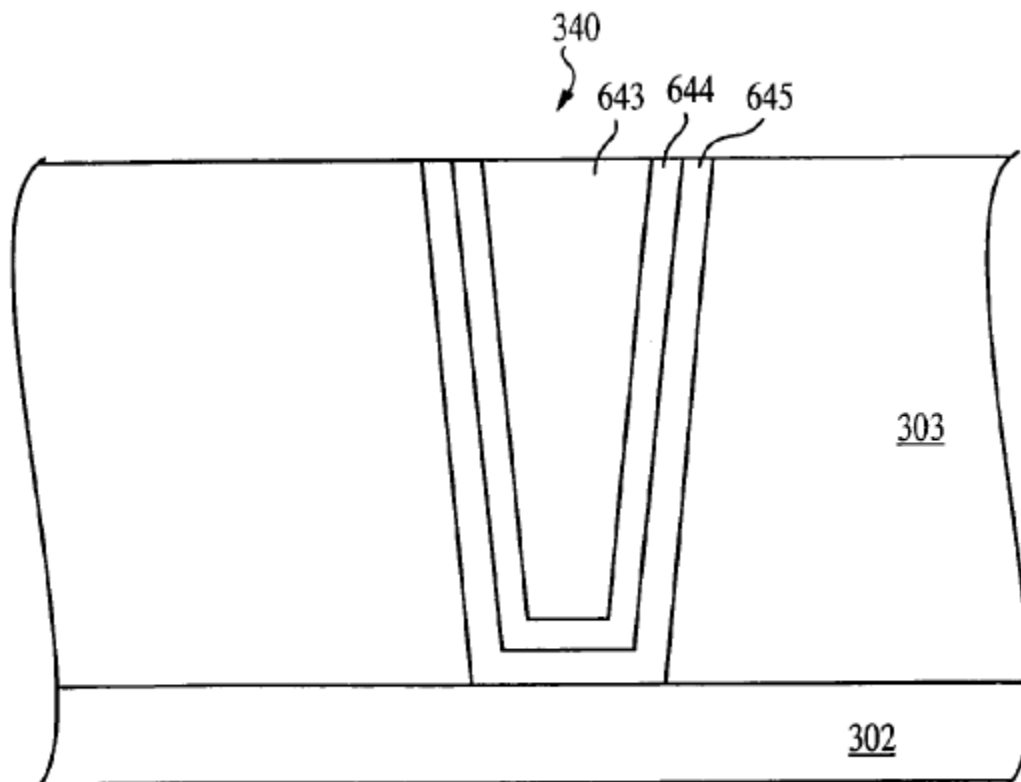


FIG. 6

94. About this structure, Cole states:

“Trench 340 can also be filled with more than two materials. For example, FIG. 6 depicts trench 340 containing three materials 643, 644, and 645. Materials 643, 644, and 645 have different refractive indices. Based on the refractive indices of materials 643, 644, and 645, the layering structure of materials 643, 644, and 645 is configured such that photons entering the trench from peripheral circuitry (FIG. 3) will be reflected away from array 333. Illustratively, material 643 has a greater refractive index than material 644, which in turn has a greater refractive index than material 645.”

Cole, ¶0042.

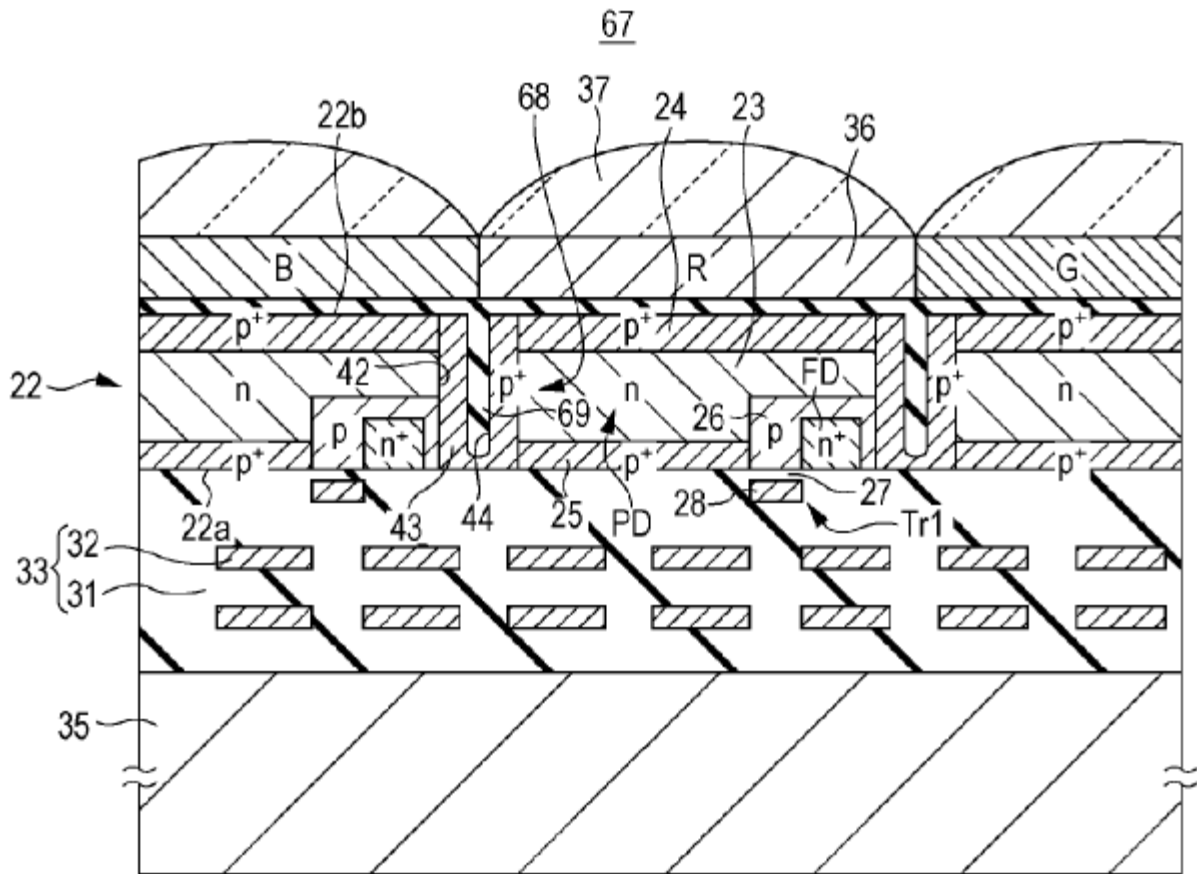
95. As discussed above, the field of endeavor of the claimed invention of the '359 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, Cole is directed to semiconductor image sensors. *Cole*, ¶0002, Title, Abstract. Thus, Cole is directed to semiconductor devices for detecting light and accordingly is in the same field of endeavor as the claimed invention of the '359 Patent.

96. Cole is also reasonably pertinent to the problems solved by the inventors of the '359 Patent. As discussed above, the '359 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels. *See* ¶¶ 30-31. As demonstrated above, Cole emphasizes the need to reduce electrical and optical crosstalk between devices, and describes a multi-layer isolation structure configured to reflect away incident light. *Cole*, ¶0042. Thus, a POSITA would have consulted Cole and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

C. Shinohara

97. Shinohara teaches a “solid-state imaging device” having pixels. *Shinohara*, Abstract. A cross-sectional view of a pixel (with neighboring pixels to the right and left) is provided in Fig. 9A, reproduced here:

FIG. 9A



Shinohara, Fig. 9A. In Fig. 9A, the central pixel occupies the region that is overlain by the hemispherical on-chip lens 37 at the top. *Shinohara*, ¶¶0059, 0092.

98. In these regions, *Shinohara* teaches having “an element isolation region 68 for isolating pixels...” *Shinohara*, ¶0090. The element isolation region is formed of alternating layers of silicon (43) and an oxide or nitride film (69). The purpose of the element isolation region is to prevent optical and electrical cross-talk between pixels, similar to the peripheral isolation element of the ’359 patent and the sidewall multi-layered reflection layer 220 of *Hwang-099*. *Shinohara* explains:

“According to the solid-state imaging device 67 of the second embodiment, the p-type semiconductor layer 43 having the void 44 is formed in the trench 42, and the insulating film 69 is further filled in the void 44, so that the element isolation region 68 is formed. Since the insulating film 69 is filled in the void 44, adjacent pixels are further electrically insulated from each other, thereby suppressing the leakage of photoelectrically converted charge into an adjacent pixel. In addition, since the filled **insulating film 69 has a refractive index different from that of the p-type semiconductor layer 43**, even if inclined incident light is incident thereon, the light is not photoelectrically converted in an adjacent pixel after passing through the element isolation region 68. That is, inclined incident **light is reflected at the interface between the silicon and the insulating film and does not leak outside from the pixel**, and hence no color mixture occurs.”

Shinohara, ¶0094.

99. Shinohara teaches that its layer 69 can be made from silicon oxide or nitride, or, if a negative fixed charge is desired, from any of “hafnium dioxide (HfO_2), dialuminum trioxide (Al_2O_3), ditantalum pentaoxide (Ta_2O_5), and dilanthanum trioxide (La_2O_3)....” *Shinohara*, ¶0092.

100. As discussed above, the field of endeavor of the claimed invention of the '359 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, Shinohara is directed to semiconductor image sensors. *Shinohara*, Title, Abstract. Thus, Shinohara is directed to semiconductor devices for

detecting light and accordingly is in the same field of endeavor as the claimed invention of the '359 Patent.

101. Shinohara is also reasonably pertinent to the problems solved by the inventors of the '359 Patent. As discussed above, the '359 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels. *See* ¶¶ 30-31. As demonstrated above, Shinohara teaches peripheral isolation structures configured such that “incident **light is reflected at the interface between the silicon and the insulating film and does not leak outside from the pixel**”. Shinohara, ¶0094. Thus, a POSITA would have consulted Shinohara and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

D. Carey

102. Carey teaches photosensitive devices including imaging devices having an array of pixels made from photodiodes. *Carey*, e.g. Figs. 13 and 14, 024:15-16, 022:15-16; 026:14-34, 011:14-19. Carey discloses the advantageous use of textured regions within image-sensor pixels, allowing them to be thinner. *Carey*, Abstract. Textured surfaces, according to Carey, “refer to a surface having a topology with nano- to micron-sized surface variations”—similar to the definition of the '359 patent. *Carey*, 006:33-007:9; '359 Patent, 4:40-43.

103. Carey teaches that textured surfaces have a variety of benefits. *Carey*, 009:13-19, 010:7-15, 011:11-22, 012:18-29, 014:15-20, 015:26-34, 017:18-19, 021:21-25, 025:9-17, 026:18-21, 026:25-27, 027:6-13, 022:2-14, 026:14-34. According to Carey, textured layers work by scattering long-wavelength light. *Carey*, 011:11-22. When scattered, the light will take on a different direction, potentially increasing its path-length through the silicon, and giving it a better chance of being absorbed. (*Id.*). According to Carey, this can increase the sensitivity of the device to longer wavelengths, allow the device to be thinner, and increase the operation speed of the device. (*Id.*). Textured regions on the light incident surface are in fact a well-known approach to increase the amount of light collected by semiconductor devices.

104. As discussed above, the field of endeavor of the claimed invention of the '359 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, Carey is directed to semiconductor image sensors. *Carey*, Title, Abstract. Thus, Carey is directed to semiconductor devices for detecting light and accordingly is in the same field of endeavor as the claimed invention of the '359 Patent.

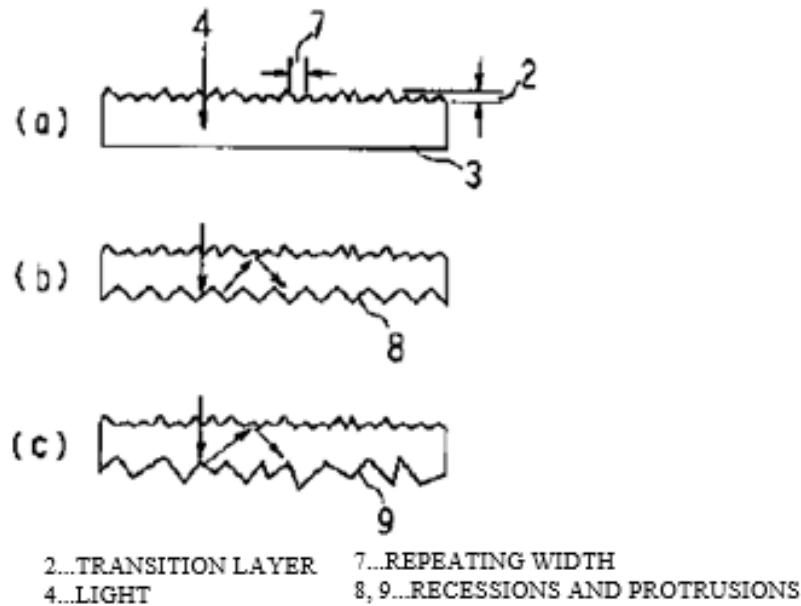
105. Carey is also reasonably pertinent to the problems solved by the inventors of the '359 Patent. As discussed above, the '359 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent

sensor pixels. *See* ¶¶ 30-31. As demonstrated above, Carey teaches textured layers which can increase the sensitivity of the device to longer wavelengths, allow the device to be thinner, and increase the operation speed of the device. Thus, a POSITA would have consulted Carey and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

E. Uematsu

106. Uematsu is directed to photodetectors for detecting incoming light. *Uematsu*, Abstract, Title, ¶0001. Uematsu teaches that the efficiency of the conversion of light to electric charges “can be increased by effectively introducing light into the substrate and confining the light inside the substrate without allowing it to escape to the outside of the substrate.” *Uematsu*, ¶0002. To confine light into the substrate, Uematsu teaches forming its textured regions (in Uematsu, “recesses and protrusions”) on the light-incident and backside surfaces, as shown, for example, in Figs. 7(b)-(c):

FIG. 7



Uematsu, Fig. 7, ¶¶0017-0018. As shown in Fig. 7, by forming layers in the specific manner *Uematsu* suggests, one can achieve an advantageous increase in the internal path length of the light, increasing efficiency. *Uematsu*, ¶¶0017-0018. Textured regions on the light incident surface are in fact a well-known approach to increase the amount of light collected by semiconductor devices.

107. As discussed above, the field of endeavor of the claimed invention of the '359 Patent includes semiconductor devices for detecting light. See ¶¶ 28-29. As demonstrated above, *Uematsu* is directed to semiconductor image sensors. *Uematsu*, Title, Abstract. Thus, *Uematsu* is directed to semiconductor devices for detecting light and accordingly is in the same field of endeavor as the claimed invention of the '359 Patent.

108. Uematsu is also reasonably pertinent to the problems solved by the inventors of the '359 Patent. As discussed above, the '359 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels. *See* ¶¶ 30-31. As demonstrated above, Uematsu teaches textured layers which can achieve an advantageous increase in the internal path length of the light, increasing efficiency. Thus, a POSITA would have consulted Uematsu and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

F. Callegari

109. Callegari teaches the use of tantalum oxide, lanthanum oxide, and lanthanum aluminum oxide in semiconductor fabrication. *Callegari*, 7:17-20, Title, Abstract. Callegari states that these materials were desirable as transistor gate oxides in semiconductors, a role that requires excellent electrical insulation properties. *Callegari*, 7:11-20, 1:58-2:17. Callegari specifically teaches the use of such materials in “sensor image array optoelectronic microelectronic fabrications”, which are image sensors. *Callegari*, 6:5-17, *see also* 7:11-13, 4:3-8. Tantalum oxide, lanthanum oxide, and lanthanum aluminum oxide were well-known materials in semiconductor fabrication, with established deposition techniques. *Callegari*, 4:66-5:8.

110. As discussed above, the field of endeavor of the claimed invention of the '359 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, Callegari is directed to semiconductor image sensors. *Callegari*, Title, Abstract. Thus, *Callegari* is directed to semiconductor devices for detecting light and accordingly is in the same field of endeavor as the claimed invention of the '359 Patent.

111. Callegari is also reasonably pertinent to the problems solved by the inventors of the '359 Patent. As discussed above, the '359 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels. *See* ¶¶ 30-31. As demonstrated above, Callegari teaches materials for use in semiconductor fabrication, and specifically in image sensor fabrication. Thus, a POSITA would have consulted Callegari and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

G. Forbes

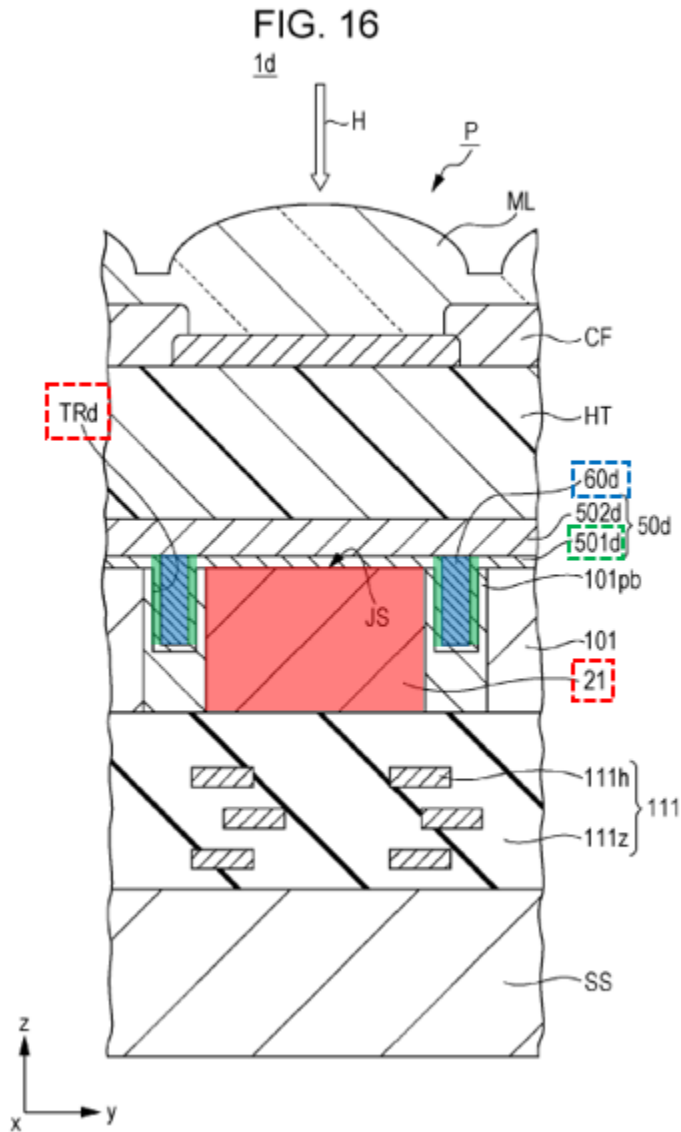
112. Forbes teaches that tantalum aluminum oxynitride films are “for use in a variety of electronic systems and devices.” *Forbes*, Title, Abstract, ¶¶0033, 0103. Tantalum aluminum oxynitride was a well-known oxide useful in the semiconductor arts. *Forbes*, Title, Abstract.

113. As discussed above, the field of endeavor of the claimed invention of the '359 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, Forbes is directed to semiconductor fabrication. *Forbes*, Title, Abstract, ¶¶0033, 0103. Thus, Forbes is directed to semiconductor devices for detecting light and accordingly is in the same field of endeavor as the claimed invention of the '359 Patent.

114. Forbes is also reasonably pertinent to the problems solved by the inventors of the '359 Patent. As discussed above, the '359 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels. *See* ¶¶ 30-31. As demonstrated above, Forbes teaches materials for use in semiconductor fabrication. Thus, a POSITA would have consulted Forbes and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

H. Hiyama

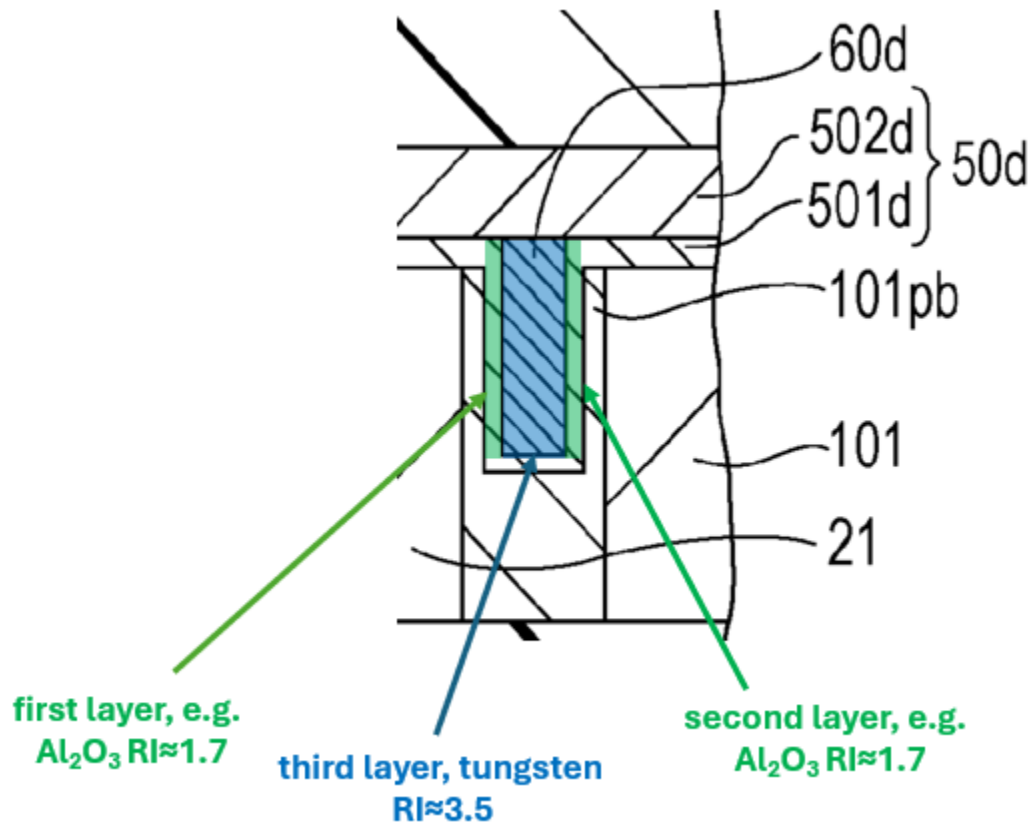
115. Hiyama teaches a solid-state imaging device. *Hiyama*, Abstract, ¶0273, ¶0002. Hiyama's Fig. 16 (below) shows a cross-section of an individual pixel (21) (red) and associated components, having peripheral isolation elements (TRd) containing lower-refractive-index layers 501d (green) and a higher-refractive-index layer 60d (blue) surrounding the pixel:



116. Hiyama’s device specifically contains photodiode 21, as shown with red annotations in Fig. 16. *Hiyama*, ¶¶0112-0114, 0294, 0081, 0182, 0213, Fig. 2, ¶¶0094, 0177, 0075. In Fig. 16, “incident light H” passes through a microlens (“ML”) and “is incident” on the “light sensing surface JS” of photodiode area 21, where it is converted to an electric signal. *Hiyama*, ¶¶0110, 0143, 0275, 0112-0114.

117. Hiyama teaches a groove TRd (Fig. 16, left side) that is filled with layers 501d and 60d. *Hiyama*, Fig. 16, ¶¶0286. The filled groove TRd is located at the sides of each pixel. The filled groove TRd prevents optical crosstalk between neighboring pixels (*Hiyama*, ¶0294), and contains a dielectric oxide such as Al₂O₃, HfO₂, or Ta₂O₅ (*Hiyama*, ¶¶0150-0152), each of which is *electrically* insulating. Hiyama teaches that the pixels have a doped region (separation regions 101pb “in which p type impurities are diffused”). *Hiyama*, ¶0117.

118. Hiyama’s groove TRd (and materials 501 and 60d) has three layers where the first and second layers are composed of the high-κ dielectric oxide of layer 501 (e.g. Al₂O₃, HfO₂, or Ta₂O₅) and the third, middle layer is composed of Tungsten, as shown in the annotated portion of Fig. 16:



Hiyama, Fig. 16.

119. As discussed above, the field of endeavor of the claimed invention of the '359 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, *Hiyama* is directed to semiconductor devices for detecting light and accordingly is in the same field of endeavor as the claimed invention of the '359 Patent.

120. *Hiyama* is also reasonably pertinent to the problems solved by the inventors of the '359 Patent. As discussed above, the '359 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent

sensor pixels. *See* ¶¶ 30-31. As demonstrated above, Hiyama describes a semiconductor device uses a peripheral isolation element to optically isolate adjacent pixels from one another. *Hiyama*, Fig. 16, ¶¶0293-0294. Thus, a POSITA would have consulted Hiyama and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

I. Werner

121. Werner is a technical journal article that teaches using Atomic Layer Deposition (ALD) to produce Al₂O₃ layers with a high negative fixed charge density of on single-crystal silicon (c-Si) to achieve surface recombination velocities of under 10 cm/s. *Werner*, Abstract, pp. 001-003, Fig. 4.

122. As discussed above, the field of endeavor of the claimed invention of the '359 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, Werner is directed to semiconductor fabrication. *Werner* Title, Abstract. Thus, Wener is directed to semiconductor devices for detecting light and accordingly is in the same field of endeavor as the clamed invention of the '359 Patent.

123. Werner is also reasonably pertinent to the problems solved by the inventors of the '359 Patent. As discussed above, the '359 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent

sensor pixels. See ¶¶ 30-31. As demonstrated above, Wener teaches methods for use in semiconductor fabrication. Thus, a POSITA would have consulted Werner and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

VII. SUMMARY OF UNPATENTABILITY

124. I have reproduced the Proposed Grounds of Unpatentability from the Petition for ease of reference:

Ground	Grounds of Unpatentability
1	Claims 1-4, 7, 10, 18, 38-40, 42-47, 49-52, 56-58, 62-63, 67-69, and 73-75 are anticipated by Hwang-099.
2	Claims 1-5, 7, 10, 18, 23, 38-40, 42-47, 49-64, 67-70, 73-75, and 80-83 were obvious over Hwang-099.
3	Claims 5, 23, 38-40, 43, 45-47, 50, 65-66, 68-69, 71-72, and 74-75 were obvious over Hwang-099 and Cole.
4	Claims 6, 8, 11, 24, 30, 32, 34, 36, 53-54, 59-60, 80 and 82 were obvious over Hwang-099 and Shinohara.
5	Claims 12-17, 19-22, 25-29, 65-66, 71-72, and 76-79 were obvious over Hwang-099 and Carey.
6	Claims 12-17, 19-22, 25, 27, and 29 were obvious over Hwang-099 and Uematsu.
7	Claims 30, 32-34, and 36-37 were obvious over Hwang-099 and Callegari.
8	Claims 30-31 and 34-35 were obvious over Hwang-099 and Forbes.
9	Claims 1-2, 6-8, 10-11, 18, 30, 34, 38-39, 42-46, 49-52, 58, 64, 67, 70 and 73 were obvious over Hiyama.

10	Claims 1, 5, 18, 23-24, 38-41, 43, 45-48, 50, 55, 61, 68-69, 74-75, and 80-83 were obvious over Hiyama and Cole.
11	Claim 9 was obvious over Hiyama and Werner.

VIII. OPINIONS REGARDING GROUND 1: CLAIMS 1-4, 7, 10, 18, 38-40, 42-47, 49-52, 56-58, 62-63, 67-69, AND 73-75 ARE ANTICIPATED BY HWANG-099.

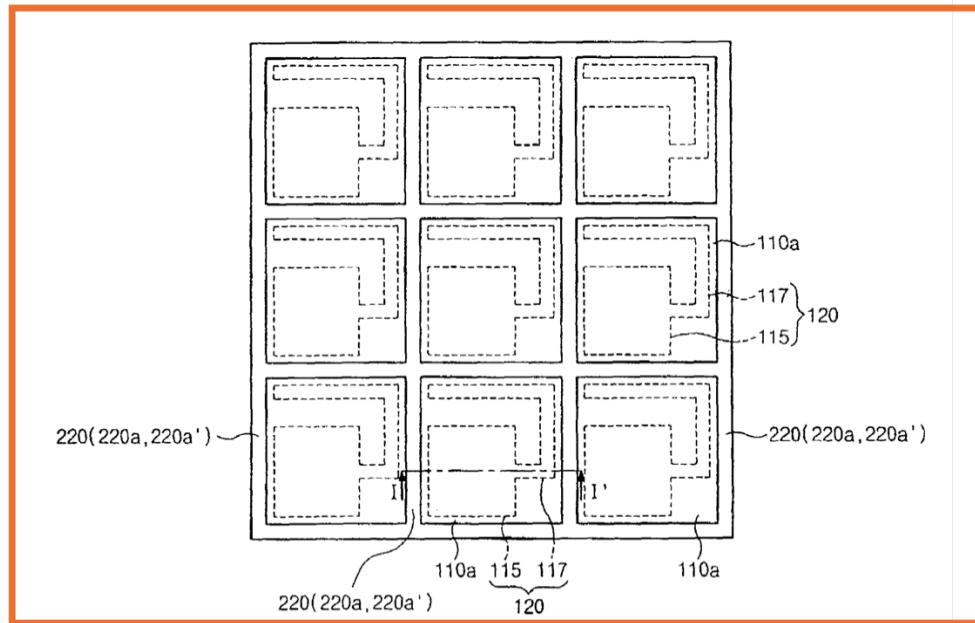
125. The above-referenced claims are anticipated by Hwang-099 (Ex. 1004).

A. “1[Pre] “An imager device, comprising:”

126. Hwang-099 teaches an *imager device*, namely the image sensor shown in Figure 1. *Hwang-099*, Figure 1; Specifically, Hwang-099 teaches “an image sensor capable of minimizing interference between neighboring pixels[.]” *Hwang-099*, 1:55-58. Because Hwang-099 teaches an image sensor, Hwang-099 teaches an *imager device*.

Imager Device

Fig. 1

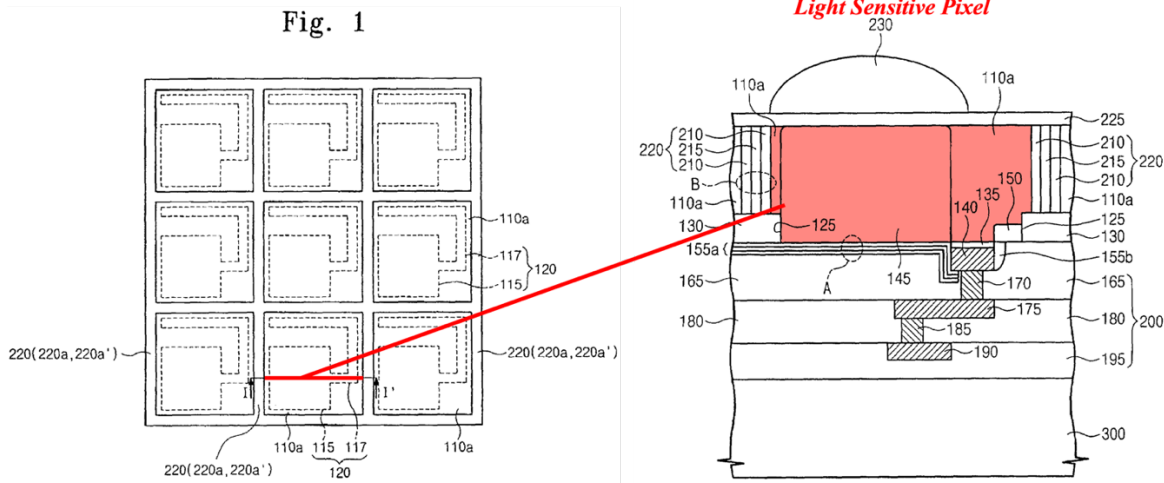


B. 1[a] “at least two adjacent light sensitive image sensor pixels”

127. As I discussed above, Hwang-099’s image sensor includes an array of “neighboring pixels” that are “arranged two-dimensionally in rows and columns on a substrate 300.” *Hwang-099* at 1:55-57¹, 5:52-58, FIG. 1; *see also*, Claim 1[Pre]. “FIG. 2 is a sectional view of FIG. 1 taken along line I-I’” and depicts *at least one light sensitive pixel*, which at least includes photodiode 145 and pixel semiconductor pattern 110a:

¹ All emphases are added unless noted otherwise.

Fig. 2



128. Each pixel semiconductor pattern 110a with photodiode 145 disposed therein are *light sensitive image sensor pixels* because they are part of the image sensor of Figure 1 and collectively allow efficient collection of electron-hole pairs generated by absorbed light, thus converting light into an electrical signal. *Hwang-099*, 5:52–6:4, 1:23-29, 10:36-40, 1:52-54, 1:14-29. There are *at least two adjacent light sensitive image sensor pixels* because at least 9 pixel semiconductor patterns 110a are arranged in rows/columns as shown in Figure 1, thus making at least two of the pixel semiconductor patterns 110a adjacent each other.

129. The silicon pixel semiconductor pattern 110a is “doped with a first conductive dopant” that is “a P-type dopant.” *Hwang-099* at 5:58-64. Photodiode 145 is a region in pattern 110a “doped with a second conductive dopant” that is “an

N-type dopant.” *Hwang-099* at 5:59-65.² “Therefore, the photodiodes 145 form a PN junction with the pixel semiconductor pattern 110a.” *Hwang-099* at 6:3-4.

130. As I discussed above, a PN junction facilitates converting light into an electrical signal by separating electron-hole pairs that causes generation of a charge, which is then stored in circuitry that will allow it to be accessed as a signal. *See* ¶¶44-49, above. A PN junction has a “depletion (or space charge region) at the junction interface [that] has a high electric field and readily separates photogenerated electron-hole pairs.” *See e.g., Lee* at [0004]. Due to the depletion region’s electric field, “electrons are attracted towards the positive charge on the n-type material side[,]” while “holes are attracted to the negative charge on the p-type material side.” *See e.g., Sproul* at p. 22. It is “[t]his separation of charges [that] causes a current to flow across the junction” (i.e., an electrical signal). *See e.g., Sproul* at p. 22.

131. *Hwang-099* confirms that photodiode 145 is “doped at a low concentration, so that most of the entirety of the photodiodes 145 become depletion regions.” *Hwang-099* at 6:4-6. “When external light is incident on a depletion region

² Because photodiode 145 is a “region doped...within a predetermined region of a pixel semiconductor pattern 110a,” photodiode 145 is not a separate structure from pattern 110a. *Hwang-099* at 5:60-63. Instead, the box surrounding photodiode 145 in FIG. 2 merely delineates the locations of the P-type and N-type dopants within the silicon substrate. In other words, photodiode 145 and pattern 110a are a single, contiguous layer of silicon having different doped regions.

in the photodiode, electron-hole pairs are generated, and the **external light is converted to electrical signals.**” *Hwang-099* at 1:23-29.

132. For these reasons, Hwang-099’s *light sensitive pixel* includes a PN junction formed by photodiode 145 and pixel semiconductor pattern 110a that converts light into an electrical signal.

133. Further, Hwang-099 teaches a “sidewall multi-layered reflection layer 220” that contacts a “pair of neighboring pixel semiconductor patterns 110a.” *Hwang-099* at 10:14-17. Sidewall multi-layered reflection layer 220 is expressly described as “enclos[ing]” pixel semiconductor patterns 110a. *Hwang-099*, 3:38-40, 6:33-36. Sidewall multi-layered reflection layer 220 comprises “boundary surfaces” that minimize incidence of light on a neighboring photodiode 145 (disposed in pixel semiconductor pattern 110a. *Hwang-099* at 10:19-27. “Thus, the occurrence of interference between neighboring pixels can be minimized.” *Hwang-099* at 10:18-19, 1:55-58. A POSITA would have understood that because 1) Hwang-099 describes sidewall multi-layered reflection layer 220 as enclosing pixel semiconductor patterns 110a, and 2) sidewall multi-layered reflection layer 220 minimizes interference between neighboring **pixels**, that Hwang-099’s pixel semiconductor pattern 110a is a *pixel*. In other words, because Hwang-099 teaches that interference between neighboring pixels is minimized, that sidewall-multi-layered reflection layer 220 is the structure that minimizes interference between

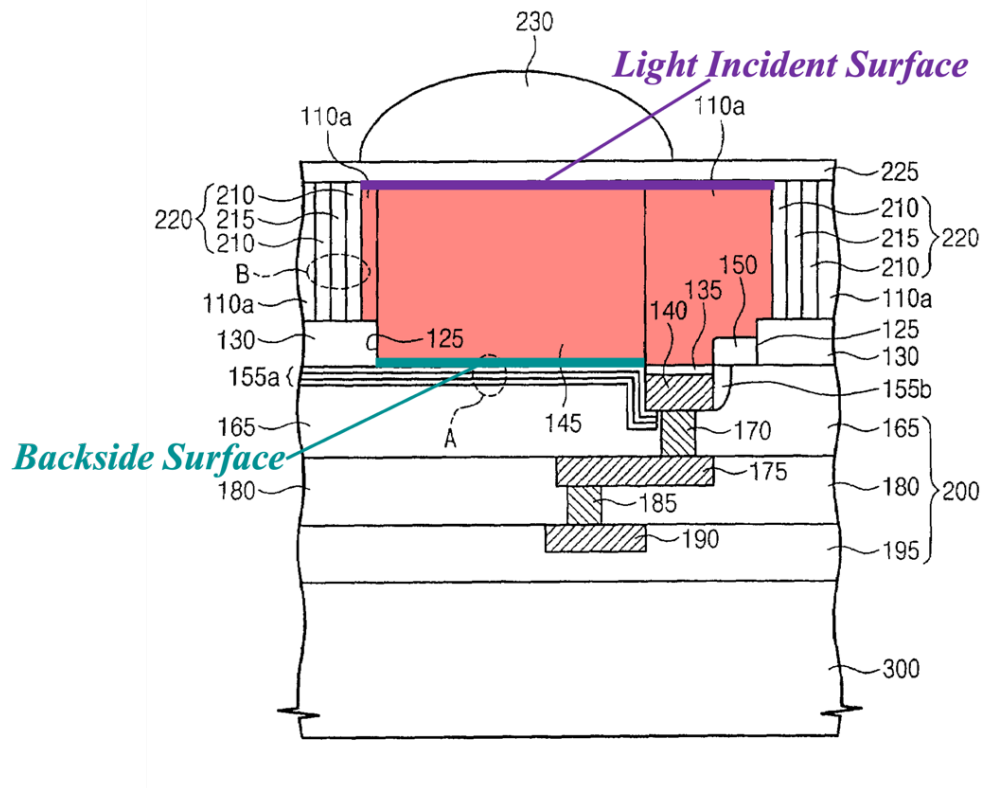
neighboring pixels, and that sidewall layer 220 encloses pixel semiconductor pattern 110a (with photodiode 145 disposed therein), that pixel semiconductor pattern 110a is a *pixel*. Hwang-099 also teaches a micro lens 230 that “covers the photodiode 145 [and] is disposed on the color filter 225. External light passes through the micro lens 230 and the color filter 225, and is incident on the second surface of the photodiode 145.” *Hwang-099* at 8:18-22. The positioning of Hwang-099’s micro lens 230 is such that quantum efficiency of Hwang-099’s pixel is enhanced. That is, Hwang-099 expressly teaches that “photodiodes 145 form a PN junction with the pixel semiconductor pattern 110” and are “doped at a low concentration, so that most or the entirety the photodiodes 145 become depletion regions.” *Hwang-099* at 6:3-6. Hwang-099 also states that “[w]hen external light is incident on a depletion region in the photodiode, electron-hole pairs are generated, and the external light is converted to electrical signals.” *Hwang-099* at 1:25-29. As such, a POSITA would appreciate that Hwang-099’s micro lens is strategically placed above photodiode 145, such that incident light is directed to the depletion region of the PN junction formed by photodiode 145 and pixel semiconductor pattern 110a. It was known that “electron-hole pairs that are generally formed outside of the depletion region are not separated as effectively as they would have been within the depletion region, and thus have a higher chance to recombine (which lessens the sensitivity of pixels).” *Mao* at 3:35-39. Thus, a POSITA would have appreciated that while pixel

semiconductor pattern 110a and photodiode 145 *together* form a PN junction, having a micro lens to direct light specifically into photodiode 145 (depletion region) would advantageously increase the number of electron-hole pairs that are separated, which generates current, rather than undergo recombination where “no current or charge accumulation results.” *Hibbeler* at [0035]. To separate an electron-hole pair, a PN junction needs to be created. To create a PN junction, an N-doped material and a P-doped material are needed. To optimize incidence of light, it is common to place a microlens over the area comprising a depletion region, which in *Hwang-099* is at least an area comprising photodiode 145. *Hwang-099* at 6:5-6. In *Hwang-099*, the semiconductor layer 110a is P-doped, and the photodiode formed in the layer 110a is formed by doping a portion of 110a with N⁺. Although the microlens could be placed over the entirety of the light incident surface of semiconductor layer 110a, the P-doped portion receiving incident light thereon is not going to be as effective in separating electron-hole pairs. Therefore, a POSITA would have understood there is no measurable advantage to extending the microlens across the entirety of layer 110a’s light incident surface. On the other hand, however, pixel semiconductor layer 110a that is P-doped is needed for creation of the PN junction that facilitates the separation of the electron-hole pair. Therefore, the P-doped portion of the pattern 110a is a pixel because it works with the N-doped, photodiode 145 portion to create the PN junction for electron-hole pair separation.

C. 1[b] “each having a **light incident surface**, and a **backside surface** opposite the **light incident surface** ;”

134. Per the '359 Patent, “a device can include at least a semiconductor substrate having a first side for receiving incident light and a second side opposite the first side.” *'359 Patent* at 6:63-65; *see also, id.* at 13:49-50 (describing “...the top surface (i.e. the light incident surface)...”). Hwang-099 similarly teaches that pixel semiconductor pattern 110a and photodiode 145, which is “disposed” within pattern 110a, have “first and second surfaces in parallel, i.e., that face one another” and where “the first surface of a pixel semiconductor pattern 110a is more proximate to the substrate 300 than is the second surface.” *Hwang-099* at 5:57-58, 6:37-40; *see also, id.* at 6:61-65 (“The photodiode 145 also has a first surface and a second surface that face each other. Here, the first surface of the photodiode 145 is coplanar with the first surface of the pixel substrate pattern 110a.”). As shown in the annotated figure, below, at least a portion of the first surface on the bottom of pattern 110a/photodiode 145 is a **backside surface** of the **pixel**, and at least a portion of the second surface on the top of pattern 110a/photodiode 145 is a **light incident surface** of the **pixel**:

Fig. 2



135. The pixel semiconductor pattern 110a and photodiode 145, which is “disposed” within pattern 110a, “have first and second surfaces in parallel, i.e., that face one another.” *Hwang-099*, 5:57-58, 6:37-38, 6:61-65. In annotated Figure 2, above, at least the portion of the first surface of 110a/145 as annotated is a bottom surface (*backside surface*) because it “is more proximate to the substrate 300[,]” and at least the portion of the second surface of 110a/145 as annotated is a top surface (*light incident surface*) because it receives incident light. *Hwang-099*, 6:38-40, 8:20-22, 9:6-7, 1:14-18. Because the top/second and bottom/first surfaces of pattern

110a “face one another” and are “parallel,” the surfaces are *opposite*. *Hwang-099*, 6:37-38. I note that Claim 1[b][i] does not include any limitations regarding a width of each surface, including widths relative to each other or other claimed elements.

136. Because Figure 2 is a cross-section of Figure 1, a POSITA would have understood that each of the *pixels* in Figure 1 similarly comprise a *light incident surface* and a *backside surface* opposite the *light incident surface*. Thus, *Hwang-099* teaches each of the *at least two adjacent light sensitive image sensor pixels each having a light incident surface*, and a *backside surface* opposite the *light incident surface*.

D. 1[c] “a peripheral isolation element at least partially separating said two adjacent light sensitive pixels;”

137. *Hwang-099* teaches a *peripheral isolation element at least partially separating said two adjacent light sensitive pixels*, namely “[s]idewall multi-layered reflection layer 220 that] encloses the side walls of the pixel semiconductor patterns 110a.” *Hwang-099*, 6:15-23 (further disclosing layer 220 separating patterns 110a and “disposed along the boundaries” of the patterns), 6:32-36, 3:63-67, Figure 1. Because layer 220 “encloses” pattern 110a and is “disposed along the boundaries of patterns 110a, a POSITA would have understood layer 220 is *peripheral*:

Fig. 1

Peripheral Isolation Element

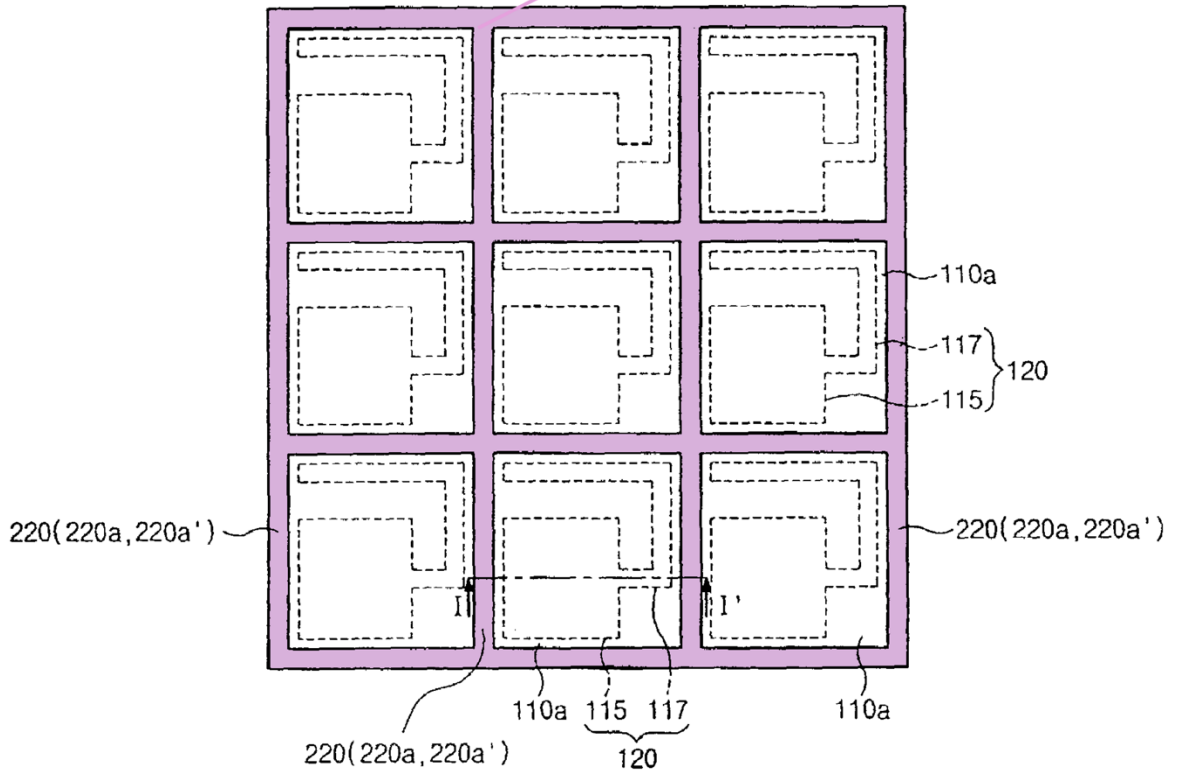
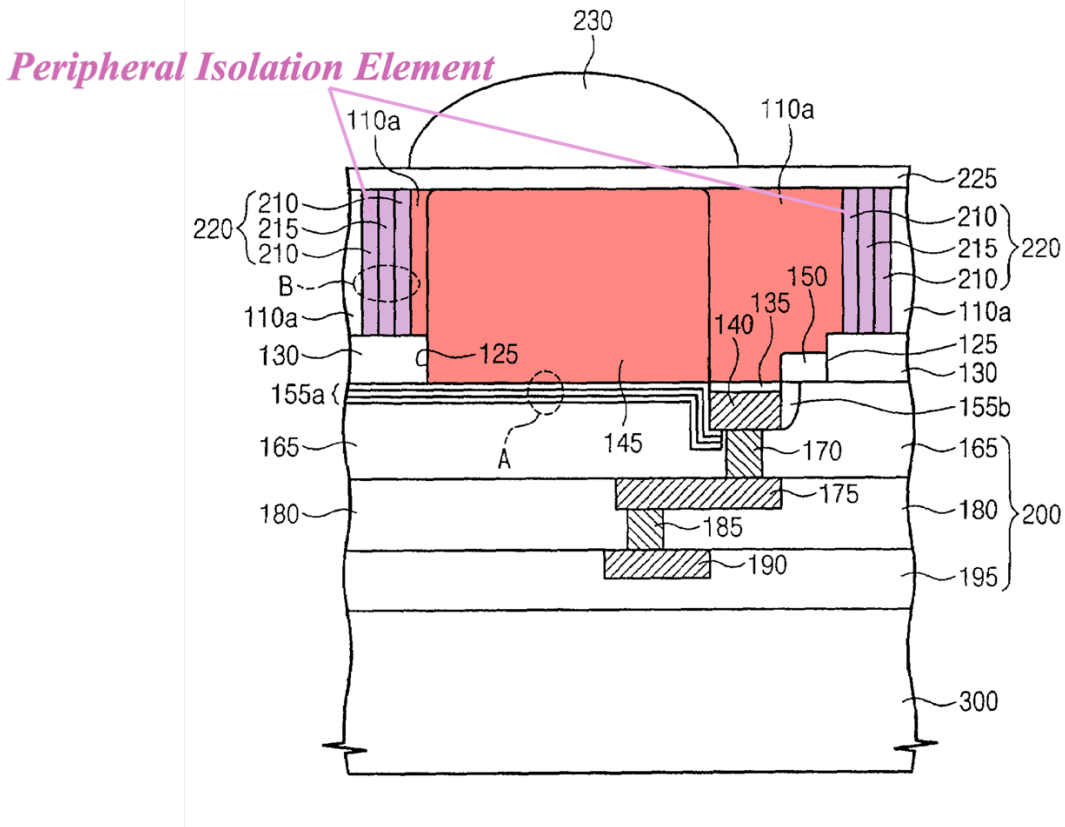


Fig. 2



138. Further regarding sidewall multi-layered reflection layer 220, Hwang-099 states that “all of the pixel semiconductor patterns 110a can thus be separated by the sidewall multi-layered reflection layer 220.” *Hwang-099*, 6:19-24. Thus, sidewall multi-layer reflection layer 220 *at least partially separate[s] said two adjacent light sensitive pixels.*

139. The '359 Patent describes “[i]n some aspects, the isolation element 214 can be designed to function as a Bragg reflector.” ’359 Patent, 8:35-36. “In other words, the isolation element includes a high refractive index material sandwiched

between two low[er] refractive index materials[.]” ’359 Patent, 8:40-43. As discussed below for Claim 1[e], Hwang-099 teaches sidewall multi-layered reflection layer 220 comprising a high refractive index layer 215 disposed between two low refractive index layers 210. *Hwang-099*, 9:58-66 (“In particular, the refractive index of the first sidewall reflection layer 210 can be lower than the refractive index[] of the...second sidewall reflection layer 215.”)

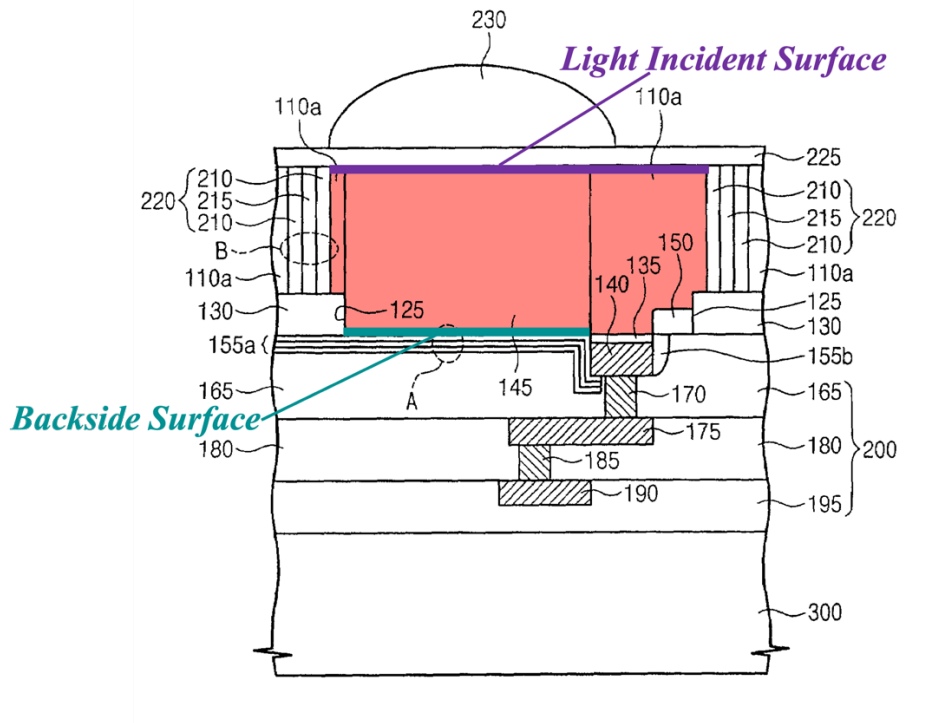
140. Sidewall multi-layered reflection layer 220 is also an *isolation element* because it optically isolates adjacent pixel semiconductor patterns 110a from each other. “The sidewall multi-layered reflection layer 220 minimizes incidence of the light...on the photodiode 145 within another pixel semiconductor pattern 110a. In other words, the sidewall multi-layered reflection layer 220 minimizes incidence of the light incident on a photodiode 145 that it encloses from being incident on other pixels.” *Hwang-099*, 10:28-40. Because the sidewall layer 220 prevent lights from being incident on a photodiode 145 (disposed in pattern 110a) from being incident on “other pixels,” sidewall layer 220 is optically isolating. To the extent it is contended that the claimed *isolation element* must be electrically isolating, *Hwang-099* teaches sidewall layer 220 is also electrically insulating because it comprises either silicon oxide or air, which are both electrically insulating materials. *Hwang-099*, 10:48-60. These insulating materials extend to form a complete electrically-insulating barrier between the semiconductor portions of the pixels, as shown in Fig.

2, from the light-incident surface to the “device isolation pattern 130” (*Hwang-099*, 10:61-62), which uses the same insulating oxide as layer 210. *Hwang-099*, 14:14-16.

E. 1[d] “each of said **pixels** having at least one doped region disposed on at least one of the **light incident surface** and the **backside surface**,”

141. *Hwang-099* teaches *each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface*, namely the n-type doped region photodiode 145. *Hwang-099*, 5:59–6:6 (“The photodiodes are regions doped with a second conductive dopant.”, “...the second conductive dopant being an N-type dopant.”). As shown below in Figure 2, photodiode 145 is disposed on each of the **light incident surface** and the **backside surface**, thus photodiode 145 is *at least one doped region disposed on at least one of the light incident surface and the backside surface*.

Fig. 2



142. Furthermore, as can be seen from Fig. 1, each pixel has a doped semiconductor pattern 110a. *Hwang-099*, 5:57-63, Fig. 1, and each pattern 110a has a corresponding doped region 145. *Hwang-099*, 5:47-63, Fig. 1 (“Each pixel semiconductor pattern 110a has a photodiode 145 disposed therein...”).

143. The doped semiconductor regions form boundaries for both the light incident surface and the backside surface, and thus the doped regions are “on” these surfaces. Notably, this is the same sense in which doped layers are “on” the respective surfaces in the '359 patent. *'359 Patent*, 7:6-9, 11:15-19.

F. 1[e] “wherein the peripheral isolation element comprises at least two materials having different indices of refraction,”

144. Hwang-099 teaches that the *peripheral isolation element* (Hwang-099’s sidewall multi-layered reflection layer 220) *comprises at least two materials having different indices of refraction*, namely the materials of layers 210 and 215 of the sidewall layer 220. Per Hwang-099, “sidewall multi-layered reflection layer 220 includes a first sidewall reflection layer 210 and a second sidewall reflection layer 215” where “the refractive index of the first sidewall reflection layer 210 is different from the refractive index[] of the...second sidewall reflection layer 215.” *Hwang-099*, 9:58-65, 2:1-6, 3:3-5, 3:41-43, 4:16-18, 6:11-13, 9:41–10:5.

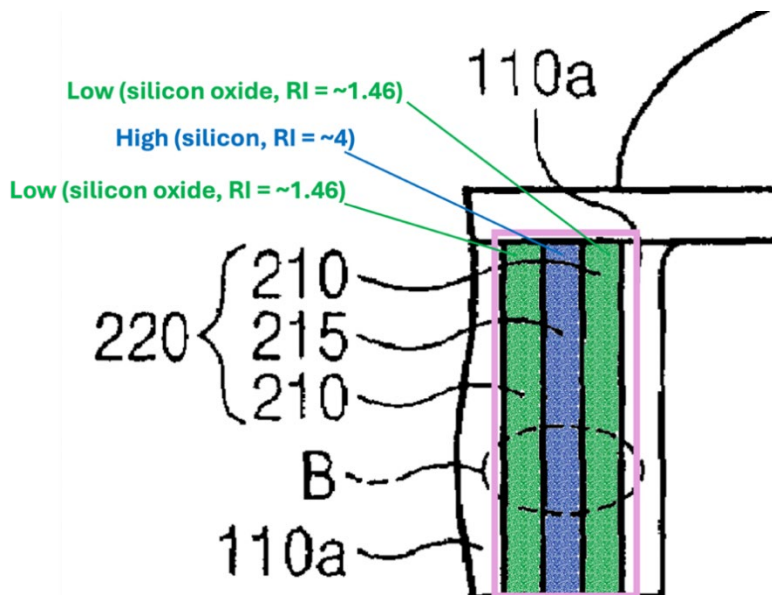
145. The sidewall layers 210 are silicon oxide or air, and the sidewall layer 215 is silicon. *Hwang-099*, 10:48-60. Per Hwang-099, silicon oxide has a refractive index of “approximately 1.46” while silicon has refractive index of “approximately 4.” *Hwang-099*, 9:28-30. Air has a refractive index of approximately 1. *Hwang-099*, 10:2-4. Thus, because Hwang-099 teaches that layers 210 may be comprised of air or silicon oxide, both materials having a different refractive index than silicon layer 215, Hwang-099 teaches *wherein the peripheral isolation element comprises at least two materials having different indices of refraction*.

- G. 1[f] “wherein said **peripheral isolation element** comprises a **first**, a **second** and a **third layer**, wherein said **third layer** is disposed between said **first and second layers**, and wherein each of said **first and second layer** exhibits an index of refraction less than an index of refraction of said **third layer**.”

146. As explained above at Claim 1[e], Hwang-099 teaches that sidewall layer 220 (*peripheral isolation element*) comprises at least two sidewall layers 210 and one sidewall layer 215. *See* Claim 1[e]. Hwang-099 specifically teaches layer 220 “having a second sidewall reflection layer 215 interposed between two first sidewall reflection layers 210,” where layers 210, 215 are “respectively formed of a silicon oxide layer and a silicon layer[.]” *Hwang-099*, 10:48-55. Layers 210/215 may be “stacked in an alternating manner a plurality of times[.]” and “both the layers of the sidewall multi-layered reflection layer 220 contacting the pair of neighboring pixel semiconductor patterns 110 can be the first sidewall reflection layer 210.” *Hwang-099*, 10:6-17.

147. As shown below, because layer 215 (**third layer**) of Silicon (RI=4) is sandwiched between layers 210 (**first and second layers**) of silicon oxide (RI=1.46), Hwang-099 teaches wherein said **peripheral isolation element** comprises a **first**, a **second** and a **third layer**, wherein said **third layer** is disposed between said **first and second layers**.

148. Sidewall layer 210, comprised of silicon, has a “refractive index of approximately 4,” per Hwang-099. *Hwang-099*, 9:29-30. Sidewall layers 210, comprised of silicon oxide, has a “refractive index of approximately 1.46,” per Hwang-099, which is less than 4. *Hwang-099*, 9:28-29. Because the refractive index of silicon oxide layers 210 (*first and second layers*) is less than the refractive index of silicon layer 210 (*third layer*), Hwang-099 teaches *wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer.*



Hwang-099, Fig. 2, 9:28-30.

H. Claim 2: “The device of claim 1, wherein the index of refraction of at least one of said first and second layer is at least 0.2 lower relative to the refractive index of the third layer.”

149. Hwang-099 teaches claim 2. Specifically, Hwang-099 teaches that the first and second layers (210) can be composed of silicon oxide (which a POSITA would have understood to mean SiO₂, *see* ¶85, above) or air, while the middle layer can be composed of silicon. *Hwang-099*, 10:2-5. Hwang-099 further teaches that air has a refractive index of 1.0 (*Hwang-099*, 10:2-5), that silicon oxide has a refractive index of approximately 1.46 (*Hwang-099*, 9:28-29), and silicon has a refractive index of approximately 4 (*Hwang-099*, 9:29-30). There is thus a refractive index difference between the third (middle) layer and the first and second (outside) layers of at least 2.64. A POSITA would thus have immediately understood Hwang-099 to be teaching that the index of refraction of at least one of said first and second layer is at least 0.2 lower relative to the refractive index of the third layer.

I. Claim 3. “The device of claim 1, wherein at least of one of said at least two materials comprises silicon dioxide.”

150. Hwang-099 states that the first and second layers (layers 210) are “silicon oxide” (*Hwang-099*, 10:2-3), which a POSITA would have understood to be the common oxide of silicon, silicon dioxide, from its given refractive index (approximately 1.46). *Hwang-099*, 9:28-29. *See* ¶85, above.

J. Claim 4. “The device of claim 1, wherein at least one of said first and second layers comprises silicon dioxide.”

151. Both the first and second layers of Hwang-099 comprise silicon oxide, which a POSITA would have understood to be silicon dioxide for the reasons I provide under claim 3, above. *Hwang-099*, 2:20-22, 9:58-10:5.

K. Claim 7. “The device of claim 1, wherein said peripheral isolation element comprises an oxide.”

152. *See* claim 3. Hwang-099’s first and second layers are silicon oxide. *Hwang-099*, 9:29-30.

L. Claim 10. “The device of claim 1, wherein the peripheral isolation element comprises at least one material having an index of refraction of less than about 2.1.”

153. *See* claim 3. Hwang-099’s first and second layers are silicon oxide with a refractive index of approximately 1.46. *Hwang-099*, 9:28-30.

M. Claim 18[Pre] “An imager device, comprising:”,

154. *See* claim 1, limitation 1[Pre].

N. “18[a] “at least two adjacent light sensitive image sensor pixels”

155. *See* claim 1, limitation 1[a].

O. 18[b] “each having a light incident surface, and a backside surface opposite the light incident surface;”

156. *See* claim 1, limitation 1[b].

P. 18[c] “a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween, said isolation element comprising at least two materials having different indices of refraction,”

157. *See* discussion under claim 1, limitation [1c], which recites “a peripheral isolation element at least partially separating said two adjacent light sensitive pixels” and limitation [1e], which recites “wherein the peripheral isolation element comprises at least two materials having different indices of refraction”. Present limitation 18[c] changes “partially separating” to “separating”, which is already addressed under element 1[c]. Present limitation 18[c] also recites the statement of intent “so as to reduce optical crosstalk therebetween”. *Hwang-099* teaches this intended effect. *Hwang-099*, 10:19-40. *Hwang-099* states:

“The sidewall multi-layered reflection layer 220 minimizes incidence of the light (reflected by the base multilayered reflection layer 155a at the first and second boundary surfaces) on the photodiode 145 within another pixel semiconductor pattern 110a. In other words, the sidewall multilayered reflection layer 220 minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels. Therefore, interference of the image sensor can be minimized, and image distortion can be minimized.”

Hwang-099, 10:19-27 (Emphasis added); *see also Hwang-099*, 15:42-48. Thus, *Hwang-099* teaches that the sidewall multi-layered reflection layer 220 (i.e. the **peripheral isolation element**) minimizes the amount of light that escapes a pixel to enter a neighboring pixel, which is **optical crosstalk**. *'359 Patent*, 6:51-52; *Hwang-*

099, 10:19-40. Hwang-099 thus teaches that the element 220 **reduces optical crosstalk between adjacent pixels.** (*Id.*).

Q. 18[d] “at least one doped region disposed on at least one of the light incident surface and the backside surface,”

158. *See* claim 1, limitation 1[d].

R. 18[e] “wherein said peripheral isolation element comprises a first, a second and a third layer, wherein said third layer is disposed between said first and second layers, and wherein each of said first and second layers exhibits an index of refraction less than an index of refraction of said third layer.”

159. *See* claim 1, limitation 1[f].

S. CLAIMS 38 AND 45

160. Claims 38 and 45 are dependent from claims 1 and 18, respectively, and recite “each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said backside surface, wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”

161. *See* claim 1, discussion under limitations 1[a]-[b], regarding the limitation each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said

backside surface. The semiconductor portions are semiconductor regions 110a and 145. *Hwang-099*, 5:47-58.

162. Regarding the limitation wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels, *Hwang-099*'s sidewall multi-layered reflection layer 220 isolates the semiconductor portions both because it isolates each pixel optically, and because it isolates each pixel electrically, as discussed under claim 1, limitation 1[c]. *Hwang-099*, 9:58-10:5, 10:19-40, Abstract; *compare '359 Patent*, 10:20-22.

163. Sidewall layer 220 is also isolates adjacent pixels electrically because it comprises either silicon oxide or air, which are both electrically insulating materials. *Hwang-099*, 10:48-60. These insulating materials extend to form a complete electrically-insulating barrier between the semiconductor portions of the pixels, as shown in Fig. 2, from the light-incident surface to the "device isolation pattern 130" (*Hwang-099*, 10:61-62), which uses the same insulating oxide as layer 210. *Hwang-099*, 14:14-16. This electrically isolates the semiconductor portions of adjacent pixels from one another.

164. The portions of *Hwang-099* discussed above apply to each pixel in an array (*Hwang-099*, 5:47-55, Figs. 1-2, 4:59-63), and thus apply to *each of said at least two adjacent light sensitive image sensor pixels*.

T. CLAIMS 39 AND 46

165. Claims 39 and 46 are dependent from claims 38 and 45, respectively, and recite “said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”

166. *See* the discussion under claim 1, limitation 1[c] and claim 38. Hwang-099’s reflection layer 220 *isolates* the semiconductor portions 110a and 145 *optically* because they surround these portions and prevent light from traveling from one pixel to an adjacent pixel. *Hwang-099*, 10:19-40, 5:47-6:23, Figs. 1 and 2.

U. CLAIMS 40 AND 47

167. Claims 40 and 47 are dependent from claims 38 and 46, respectively, and recite “said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”

168. *See* the discussion under 38. Hwang-099’s reflection layer 220 *isolates* the semiconductor portions 110a and 145 *electrically* because they surround these portions with electrically insulating materials, such as silicon dioxide or air, and extend from the light-incident surface to the device isolation pattern 130. *Hwang-099*, 5:47-6:23, 10:61-62, 10:19-40, Figs. 1 and 2.

V. CLAIMS 42 AND 49

169. Each of claims 42 and 49 recites that “said at least two pixels are formed monolithically in a common semiconductor substrate.” The ’359 patent states “the

term ‘monolithic’ refers to an electronic device in which electronic components are formed on the same substrate.” ’359 Patent, 5:19-21, 5:47-6:23. In Hwang-099, the pixels are formed on the same semiconductor substrate. *Hwang-099*, 5:52-58, Fig. 1.

170. Claims 42 and 49 depend from claims 1 and 18, respectively, and further recite “said at least two adjacent light sensitive image sensor pixels...are isolated from one another by said peripheral isolation element.” Regarding this language, see above under claim 38. *Hwang-099*, 5:52-6:23, 9:25-34, 10:6-18, 10:19-40, Figs. 1 and 2.

W. CLAIMS 43 AND 50

171. Claims 43 and 50 are dependent from claims 1 and 18, respectively, and recite “said peripheral isolation element is a trench isolation element.”

172. The ’359 Patent defines “trench isolation features” to be the same as “isolation elements”. ’359 Patent, 7:41-44 (“Regarding isolation elements, also referred to herein as trench isolation features....”). Hwang-099’s sidewall multi-layered reflection layers 220 is thus a trench isolation element because it is an isolation element (*See* claim 1, limitation 1[c]).

173. To the extent that trench implies a location, Hwang-099 teaches that the sidewall multi-layered reflection layers 220 are arranged in vertical spaces in semiconductor portion 110a (*see* element 205 in Fig. 13 and element 206 in Fig. 16).

174. To the extent “trench isolation element” implies a process and is limiting (this being a device claim), or a physical shape, Hwang-099 teaches that its sidewall multi-layered reflection layers 220 are formed by etching trenches (e.g. trench 125) and grooves that are relatively deeper than they are wide (which qualify as trenches) and filling them with sidewall material to form an overall structure 220 that is trench-shaped. (e.g. *Hwang-099*, Figs. 13-16, 18-21, 12:42-61, 13:29-49, 14:3-22, 14:50-15:7. This is notably similar to the method used in the ’359 Patent. *’359 Patent*, 12:41-43.

X. CLAIMS 44 AND 51

175. Claims 44 and 51 are dependent from claims 1 and 18, respectively, and recite said peripheral isolation element has a width in a range from about 100 nm to about 50 microns.”

176. Hwang-099 provides an example thickness of each of the two layers 210 of 550 Angstroms (55 nm) and of layer 215 of 500 Angstroms (50 nm), for a combined 160 nm. *Hwang-099*, 10:54-55. Furthermore, Hwang-099 teaches that additional layers 210 and 215 can be provided, increasing the thickness to, for example, 255 nm with five layers. *Hwang-099*, 12:62-13:3.

Y. CLAIMS 52 AND 58

177. Claims 52 and 58 are dependent from claims 38 and 45, respectively, and recite “at least one of the first layer and the second layer of said peripheral

isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials.”

178. *See* the discussion under claim 1, limitation 1[e]. The semiconductor portions comprise silicon (*Hwang-099*, 5:54-57), while the first and second layers 210 comprise silicon oxide (*Hwang-099*, 10:2-3).

Z. CLAIMS 56 AND 62

179. Claims 56 and 62 are dependent from claims 1 and 18, respectively, and recite “the peripheral isolation element comprises a light trapping material filling a trench.”

180. *Hwang-099*’s sidewall multi-layered reflection layers 220 exhibit vertical material layers 210 and 215 (meaning that they **fill a trench**), where the material layers serve to trap light within a pixel. *Hwang-099*, 9:58-63, 10:6-10, 5:47-51, 6:4-23, Figs. 1 and 2. Layer 220 “includes layers with different respective refractive indexes.” *Hwang-099*, 9:52-53. Layer 220 “includes a first sidewall reflection layer 210 and a second sidewall reflection layer 215” where “[t]he refractive index of the first sidewall reflection layer 210 is different from the refractive indexes of the pixel semiconductor pattern 110a and the second sidewall reflection layer 215.” *Hwang-099*, 9:58-63. “[T]he portion of the light reflected toward the sidewall multi-layered reflection layer 220 from the light reflected by the first and second boundary surfaces is incident again on the photodiode 145 so that

absorption efficiency of external light is increased.” *Hwang-099*, 10:31-35. Thus, layer 220 is *light trapping* because it reflects light incident on the boundary surfaces of layer 220 onto photodiode 145.

AA. CLAIM 57 AND 63

181. Claims 57 and 63 depend from claims 56 and 62, respectively, and recite “the trench is one of a shallow trench and a deep trench.”

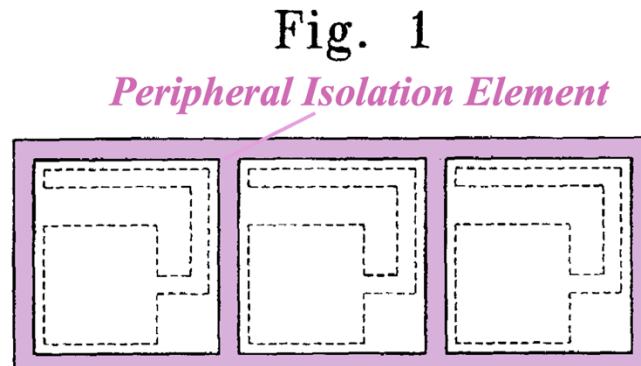
182. *Hwang-099*’s trenches qualify as deep trenches, because they extend from the light-incident surface to the isolation element 130 (as shown in, e.g., Fig. 2) or to the backside surface (e.g. Fig. 6) as discussed under claim 5. *Hwang-099*, 10:61-62 (Fig. 2), 12:25-31 (Fig. 6).

BB. CLAIM 67 AND 73

183. Claims 67 and 73 are dependent from claims 1 and 18, respectively, and recite “said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.” *Hwang-099*, 10:19-40.

184. *See* claim 1, limitation 1[c], discussing the reflective properties of *Hwang-099*’s reflection layers 220. These layers are configured to reflect light incident thereon from any of said two *adjacent light sensitive pixels back to that pixel*. *Hwang-099*, 10:19-40; 15:42-48. For example, layers 220 (purple in the annotated figure below) separating the leftmost pixel from the center pixel in Fig. 1,

below, reflect light incident from the left back into the left pixel and light incident from the right back into the right pixel:



CC. CLAIMS 68 AND 74

185. Claims 68 and 74 are dependent from claims 67 and 73, respectively, and recite “the peripheral isolation element is further configured to optically isolate said two adjacent light sensitive pixels.”

186. *See* the discussion under claim 39. Optical isolation occurs between *adjacent pixels* because of the placement of sidewall layer 220, as shown in Figs. 1 and 2. *Hwang-099*, 5:47-51, 6:4-6, 6:11-19, 10:19-40, Figs. 1 and 2.

DD. CLAIMS 69 AND 75

187. Claims 69 and 75 are dependent from claims 68 and 74, respectively, and recite “the peripheral isolation element is further configured to electrically isolate said two adjacent light sensitive pixels.”

188. See the discussion under claim 40 and claim 1, limitation 1[c]. Electrical isolation occurs between *adjacent pixels*, because of the placement of sidewall layer 220, as shown in Figs. 1 and 2. *Hwang-099*, 5:47-51, 6:4-6, 6:17-23, Figs. 1 and 2.

IX. OPINIONS REGARDING GROUND 2: CLAIMS 1-5, 7, 10, 18, 23, 38-40, 42-47, 49-64, 67-70, 73-75, AND 80-83 WERE OBVIOUS OVER HWANG-099

189. The above-referenced claims were obvious over Hwang-099. In my obviousness analysis, I provide specific opinions regarding claims 3-5, 23, 53-56, 59-60, 61-62, 64, 70, and 80-83, divided into subgroups based on the similarity of their limitations. The remaining claims are those discussed above in my analysis for Ground 1. These claims would also have been obvious based on the analysis proposed below for specific claims. For example, the analysis for claims 3 and 4 proposes that it was obvious to use silicon dioxide for Hwang-099's silicon oxide. Because this change would not affect the analysis of other claims discussed under Ground 1, those claims would likewise have been obvious.

A. CLAIMS 3 AND 4

190. Claims 3-4 are dependent claims that recite the use of silicon dioxide. Hwang-099 specifically teaches that the first and second layers of claim (layers numbered 210 in Hwang-099) are silicon oxide, which (under Ground 1), is silicon dioxide (SiO₂). However, it would also have been *obvious* to use SiO₂, based on

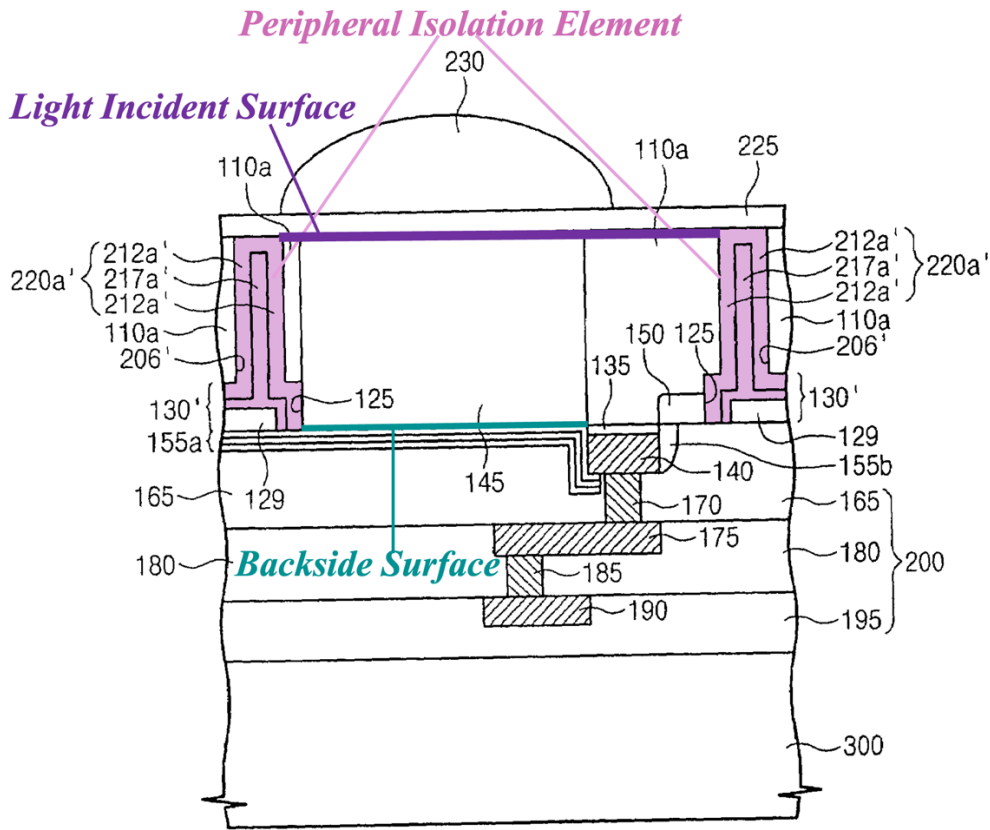
several things. First, Hwang-099 suggests using SiO₂ as the particular silicon oxide by noting that silicon oxide has a refractive index of approximately 1.46 (*Hwang-099*, 9:28-29), which corresponds to the refractive index of SiO₂. *See above*, ¶85. This would have suggested to a POSITA that what Hwang-099 meant by “silicon oxide” was SiO₂. Furthermore, SiO₂ was, in the relevant timeframe, by far the most stable and commonly-used oxide of silicon in semiconductor fabrication. It would have made sense to use SiO₂ as the first and second layers (210) of Hwang-099, because of its excellent chemical stability and electrically-insulating properties. A POSITA would have had a reasonable expectation of success (“REOS”) because SiO₂ was the most commonly-used oxide in semiconductor fabrication and has the refractive index of approximately 1.46 desired by Hwang-099. Because the remaining Ground 1 Claims do not require a specific oxide, they would also be rendered obvious by this modification.

B. CLAIMS 5 AND 23

191. Claim 5 recites “the device of claim 1, wherein the isolation element extends substantially from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.” Claim 23 is similar. It would have been obvious to extend Hwang-099’s sidewall multi-layered reflection layer 220 from the light incident surface to the backside surface (through element 130) in order to increase its reflective properties to the lower boundary of the pixel

semiconductor, in order to further reduce optical cross-talk. Specifically, A POSITA would have found it obvious and been motivated to modify Figure 2's device isolation pattern 130 such that first and second layers 210, 215 of reflection layer 220 extend through pattern 130 such that sidewall layer 220 *extends substantially from the light incident surface to the backside surface*, per the Figure 6 embodiment. *Hwang-099*, 1:31-47. In the Figure 6 embodiment, Hwang-099 teaches device isolation pattern 130' "include[s] **extended portions of the first and second sidewall reflection layers 212a' and 217a'.**" *Hwang-099*, 12:26-28, Figure 6. Hwang-099 proposes Figure 6 as an alternative to the Fig. 2 embodiment. *Hwang-099*, 4:61-63, 5:5-7.

Fig. 6



192. A POSITA would have been motivated and found it obvious to modify the device isolation pattern 130 of the FIG. 2 embodiment such that portions of the first and second sidewalls layers 210/215 would extend through device isolation pattern 130 and completely cover the peripheral sidewall of pixel semiconductor pattern 110a. For example, Hwang-099 discusses the desire for increased spectral sensitivity of the image sensor and notes problems associated with long-wavelength light (such as red light):

“Spectral sensitivity is one of crucial characteristics of an image sensor. The higher the percentage of incident light absorbed by the photodiode, the higher the spectral sensitivity. An increase in the spectral sensitivity leads to an increase in light sensitivity of the image sensor to external light, giving the image sensor favorable properties. However, there are many factors that can reduce the spectral sensitivity of the image sensor, such as the configuration of the image sensor, the wavelengths of incident light, etc. For example, many specific elements of an image sensor, such as its lines, can prevent light from being freely incident. Also, the amount of light absorbed by the photodiode can be reduced according to the wavelength of the light. For example, with a longer wave length, light penetration through the photodiode increases. Thus, regions of light with a long wavelength (in the red spectrum, for example) are likely not to be absorbed completely by the photodiode, thus reducing the spectral sensitivity.”

Hwang-099 at 1:30-47.

193. The modified device isolation pattern 130, having extended layers 215 and 210, would therefore possess the same *light trapping* ability as the sidewall multi-layered reflection layer 220 due to the alternating layers of materials with different refractive indexes reflecting light back into the photodiode, but with the increased performance capabilities for longer wavelength light due to the layered materials extending deeper into the semiconductor pattern 110a substrate and photodiode 145.

194. In more detail, a POSITA would also understand that, by replacing the single layer 130 in Fig. 2 with alternating layers of materials with different refractive indexes (labeled 130' in Fig. 6), the reflectivity and spectral selectivity in the lower section of sidewall surrounding the pixel would be increased. That is, replacing element 130 with multiple alternating layers in 130' forms a Bragg reflector, and relative to the single layer shown in Fig. 2, a multi-layer Bragg reflector will increase the number of photons returned to the photodiode from the lower part of the sidewall.

195. A POSITA would have been motivated to make this modification to increase the surface area of light trapping material covering the peripheral sidewall. By increasing the surface area of the peripheral sidewall that is covered by the light trapping material, light that is incident over the entirety of the peripheral sidewall will be reflected back toward the photodiode, just as the sidewall multi-layered reflection layer 220 functions to do. The modification would have had a reasonable expectation of success, at least because Hwang-099 provides methods for manufacturing a device isolation 130 having extended portions of sidewall multi-layered reflection layer 220. *Hwang-099* at 14:3-22, 12:35-13:3.

196. The modification would have given device isolation pattern 130 the same light trapping ability as layer 220 due to the difference in refractive indexes between the first and second layers 210, 215. A POSITA would have understood increasing the surface area of the light-trapping material on the peripheral sidewall—

already suggested by Hwang-099 Fig. 6—would predictably increase the amount of light reflected back into the pixel, thereby providing the benefit of increasing the number of photons returned to the photodiode. There would have been a reasonable expectation of success at least because Hwang-099 provides methods for manufacturing an isolation pattern 130' having first and second sidewall reflection layers. *Hwang-099*, 14:3-22, 12:35–13:3. The remaining Ground 1 Claims permit the peripheral isolation element to extend from the light incident surface to the backside surface, and would thus also be rendered obvious by this modification.

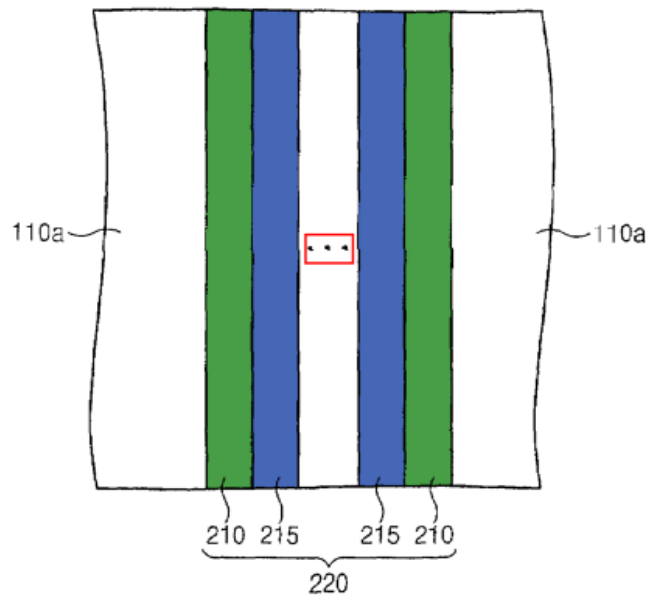
C. CLAIMS 53-54 AND 59-60

197. Claims 53 and 59 require that “the first layer and the second layer of said peripheral isolation element comprise different materials”, while claims 54 and 59 require that “the peripheral isolation element comprises at least three materials”. These claims would have been obvious over Hwang-099.

198. Hwang-099 teaches that its sidewall multi-layered reflection layer 220 (peripheral isolation element) Hwang-099 can have five layers. *Hwang-099*, 12:62-13:3; Furthermore, Hwang-099 teaches that its peripheral isolation element has multiple sets of alternating layers of low- and high-refractive index materials. *Hwang-099*, 2:16-29, 4:12-15, 6:11-13, 10:7-12, 11:47-52, 12:62-65, 14:66-15:4, Fig. 4. Specifically, layers 210/215 may be “stacked in an alternating manner a plurality of times[,]” and “both the layers of the sidewall multi-layered reflection

layer 220 contacting the pair of neighboring pixel semiconductor patterns 110 can be the first sidewall reflection layer 210.” *Hwang-099*, 10:6-17. The alternating layers could be formed by forming multiple grooves 205 and filling them with SiO₂, as shown in Fig. 13. *Hwang-099*, 12:62-13:3. Such an arrangement of reflection layer 220 is shown in Fig. 4 of *Hwang-099*, reproduced here with color annotations:

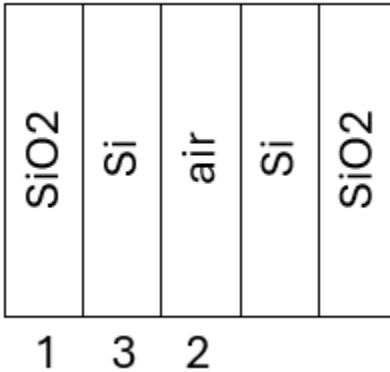
Fig. 4



Hwang-099, Fig. 4, 9:37-10:18. The ellipsis (...) indicates that additional layers pairs can be inserted. *Hwang-099*, 10:6-19.

199. *Hwang-099* further teaches that its lower-refractive index layers are, for example, silicon oxide or air. *Hwang-099*, 10:2-4, 4:3-4, 13:9-16. It would have been obvious, based on *Hwang-099*'s suggestion, that in a five-layer (or more) structure, both silicon oxide and air could be used, for example in the following

relationship, where the first, second, and third layers of the claims have been labeled 1, 2, and 3:



200. Hwang-099 teaches a sidewall layer 220 having five layers, that its layers should have multiple sets of alternating layers of low- and high-refractive index materials (*Hwang-099*, claim 4, *see also* 2:16-29, 4:12-15, 10:6-12, 11:47-52, 12:62-13:3, 14:66-15:4) and to use silicon for high-refractive-index layers and either silicon oxide or air for the low-refractive-index layers. Because of this, there were only a finite number of predictable alternatives for Hwang-099's five-layer sidewall 220, which would have led to predictable results.

201. The addition of an air layer, as suggested by Hwang-099 would further have been motivated by the desire to optimize the sidewall 220 in order to minimize interference and image distortion. *Hwang-099*, 10:19-40, 12:62-65. The design of such a structure would have been routine to a POSITA, who would have had a reasonable expectation of success, including for expected advantages.

202. The arrangement meets claims 53 and 59, because the first and second layers comprise different materials (SiO_2 and air). The arrangement also meets claims 54 and 60, because there are at least three materials (SiO_2 , Si, and air). The “at least two materials” also have different refractive indices (1.46 and 1.76) as required by claims 1 and 18. *Hwang-099*, 9:25-30, 10:2-4. The remaining ground 1 claims permit such a peripheral isolation element, and would thus also be rendered obvious by this modification.

203. There would have been a reasonable expectation of success, including for the expected benefits, at least because it would have merely required forming an additional groove 205' while manufacturing *Hwang-099*'s device, which a POSITA would understand how to do given *Hwang-099* already discloses forming such grooves.

D. CLAIMS 55, 61, 80-83

204. These claims require the peripheral isolation element to have additional layers. Claims 55 and 61 depend from claims 1 and 18, respectively, and recite “the peripheral isolation element comprises more than three layers”. Claims 80 and 82 depend from claims 1 and 18, respectively, and recite “the peripheral isolation element comprises five layers”.

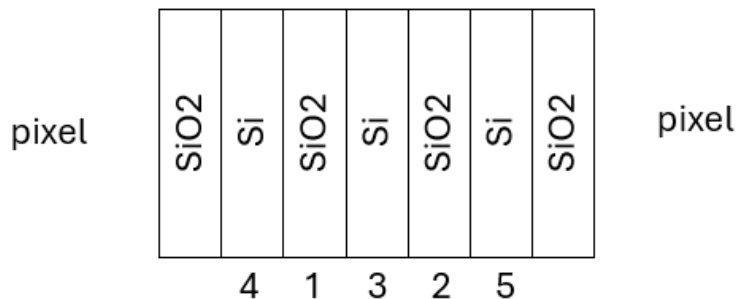
205. *Hwang-099* renders these claims obvious. As discussed above in ¶¶198-0 under claim 53 above, *Hwang-099* teaches that its sidewall multi-layered

reflection layer 220 (peripheral isolation element) can have **five layers**. *Hwang-099*, 12:62-13:3, *Hwang-099* also discusses having *pairs* of layers, with one lower-refractive-index layer paired with one higher-refractive-index layer, alternating a plurality of times, *e.g.* 2:16-29, 4:12-15, 10:7-12, 11:47-52, 14:66-15:4, claim 4. An arrangement with three such *pairs* of layers would have six total layers, for example.

206. Claims 55, 61, 80 and 82 (requiring, simply “more than three” or “five” layers) would have been obvious as a routine modification according to the express teachings of *Hwang-099* to have multiple sets of alternating layers of low- and high-refractive index materials. *Hwang-099*, claim 4, *see also* 2:16-29, 4:12-15, 10:6-12, 11:47-52, 12:62-13:3, 14:66-15:4. *Hwang-099* teaches that the silicon oxide (low refractive index) and Si (high refractive index) layers can be “alternatingly stacked a plurality of times on the sidewall of the pixel semiconductor pattern.” *Hwang-099*, claim 4, *see also* 2:16-29, 4:12-15, 10:7-12, 11:47-52, 12:62-65, 14:66-15:4. This includes arrangements “in an odd 5-layer or higher configuration.” *Hwang-099*, 11:49-52. Thus, *Hwang-099* would already have suggested an arrangement with more than three layers, which would have been further motivated by the desire to optimize the dimensions of the sidewall 220 in order to minimize interference and image distortion. *Hwang-099*, 10:19-40, 12:62-65. A POSITA would have had the requisite skill to design *Hwang-099*’s sidewall reflecting element by adjusting the

layers to optimize performance for particular applications with predictable results and a reasonable expectation of success (including for expected advantages).

207. Claims 81 and 83 depend from claims 80 and 82, respectively, and further recite that “the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second layer and the other one of said adjacent pixels.” These claims are obvious for similar reasons, using a reflecting layer 220 having four pairs of layers. In Hwang-099, for the case where four alternating pairs of layers (*e.g.* four grooves in Fig. 13) are used, Hwang-099’s layer 220 would have the following structure, with layer numbers at the bottom corresponding to the claim language:



This meets claims 81 and 83, and would have been obvious based on Hwang-099’s express suggestions and the desire to increase reflecting layer 220’s performance, as discussed above. The numbering layers leaves the first, second and third layers the same as discussed under claims 1 and 18 under my analysis for Ground 1, but merely

adds layers to the outside. A POSITA would have seen a benefit to adding layers to Hwang's Bragg reflector, in order to increase the optical isolation between pixels by increasing the overall reflectivity of the layer, and would have had a reasonable expectation of success in achieving this benefit. *Hwang-099*, 9:19-24. The remaining Ground 1 Claims permit multiple layers in the peripheral isolation element, and would thus also be rendered obvious by this modification.

E. CLAIMS 56 AND 62

208. Claims 56 and 62 depend from claims 1 and 18, respectively, and recite that the peripheral isolation element “comprises a light trapping material filling a trench.” *Hwang-099* renders obvious having its peripheral isolation element (reflecting layer 220) comprising material filling a trench, as discussed below under claim 64 (¶¶209-211). The material is light-trapping because it reflects light from a pixel, incident upon reflecting layer 220, back into the pixel. *Hwang-099*, 10:19-40, 15:42-48.

F. CLAIMS 64 AND 70

209. Claims 64 and 70 are dependent from claims 1 and 18, respectively, and recite “said peripheral isolation element comprises a trench isolation element formed by filling a trench with said first, said second, and said third layers.”

210. As discussed above under Ground 1, claim 43, the '359 Patent defines “trench isolation features” to be the same as “isolation elements” *'359 Patent*, 7:41-

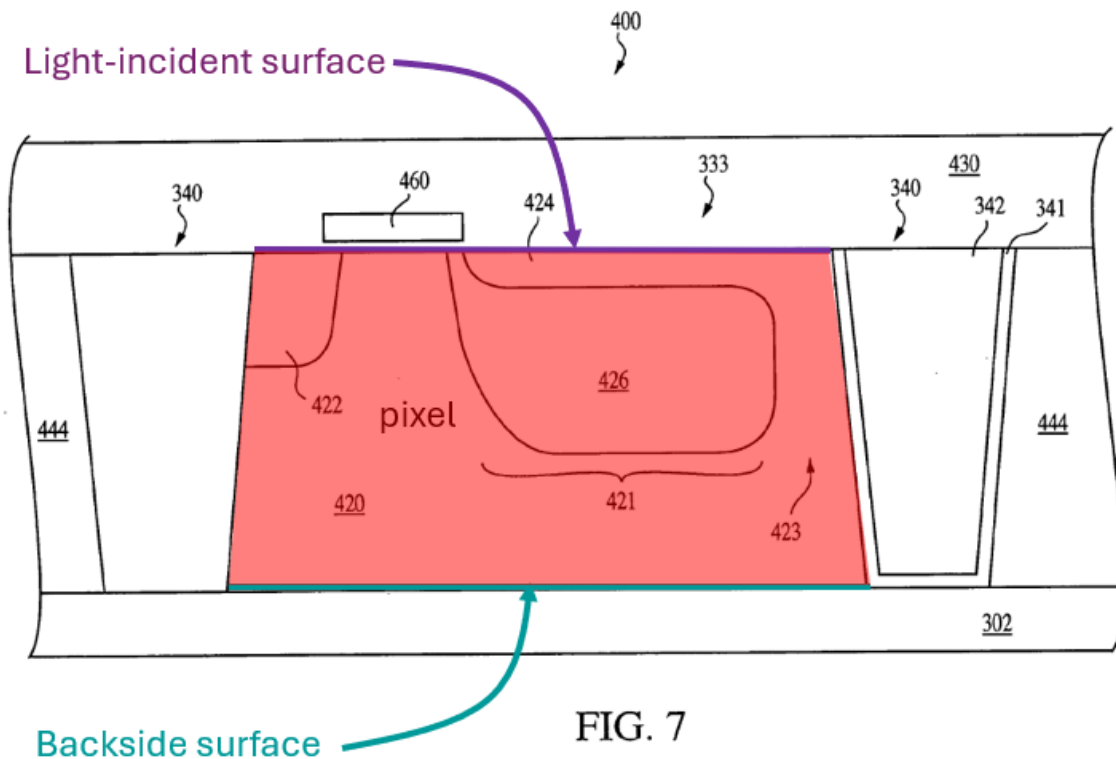
43), which Hwang-099 teaches in the form of its sidewall multi-layered reflection layers 220. *Hwang-099*, Figs. 1 and 2, ¶¶0051-0052.

211. The further claim recites a trench isolation element formed by filling a trench with said first, said second, and said third layers. Hwang-099 teaches this. Hwang-099's sidewall multi-layered reflection layers 220 are formed trench filling. In particular, Hwang-099 teaches alternate methods of forming its layers 220 in the context of Figs. 15-16 wherein a trench 206 is formed, or Figs. 20-22, wherein trenches 125 and 206' are formed, followed by filling with material to form the first and second layers, followed by filling with material to form the third (middle) layer. *Hwang-099*, 13:26-49, Figs. 15 and 16, A POSITA would have been motivated to use these alternate methods of formation by the express teaching of Hwang-099, and a POSITA would have had a REOS, at least because Hwang-099 teaches the manufacturing process for each of the disclosed forming methods. *Hwang-099*, 13:20-49, 14:38-15:32. The remaining Ground 1 claims are device claims that do not require a different formation method, and would thus be rendered obvious by this modification.

X. OPINIONS REGARDING GROUND 3: CLAIMS 5, 23, 38-40, 43, 45-47, 50, 65-66, 68-69, 71-72, AND 74-75 WERE OBVIOUS OVER HWANG-099 AND COLE.

212. The above-referenced claims would have been obvious over Hwang-099 and Cole (Ex. 1071).

213. Like the '359 patent, Cole teaches isolation structures for pixels in image sensors. *Cole*, Title, Abstract, ¶0001. An exemplary structure is illustrated in annotated Fig. 7 below, which shows a pixel (red) with a photodiode, light-incident and backside surfaces, and an isolation structures 340 at the periphery:



Cole, Fig. 7, ¶0044.

214. Several embodiments of Cole relate to isolation structures between a photodiode array and peripheral circuitry, the purpose of these structures is to stop photons and electrons from crossing to/from pixels—similar to the peripheral isolation elements of the '359 patent and sidewall layer 220 of Hwang-099. *Cole*, Title, ¶0030. Cole furthermore stresses the need to separate *individual pixels* from one another to avoid optical and electrical crosstalk *between pixels*:

“A photon impinging on a particular pixel of a photosensitive device may diffuse to an adjacent pixel, resulting in detection of the photon by the wrong pixel, i.e. cross-talk. Therefore, **CMOS image sensor pixels must be isolated from one another to avoid pixel cross talk**. In the case of CMOS image sensors, which are intentionally fabricated to be sensitive to light, **it is advantageous to provide both electrical and optical isolation between pixels.**”

Cole, ¶0005 (Emphasis added).

215. Cole further teaches an embodiment (Fig. 6, below) in which a peripheral isolation element has three different layers of materials (shown in blue, green and light green) having different refractive indices to reflect light. *Cole*, ¶¶0042, 0044.

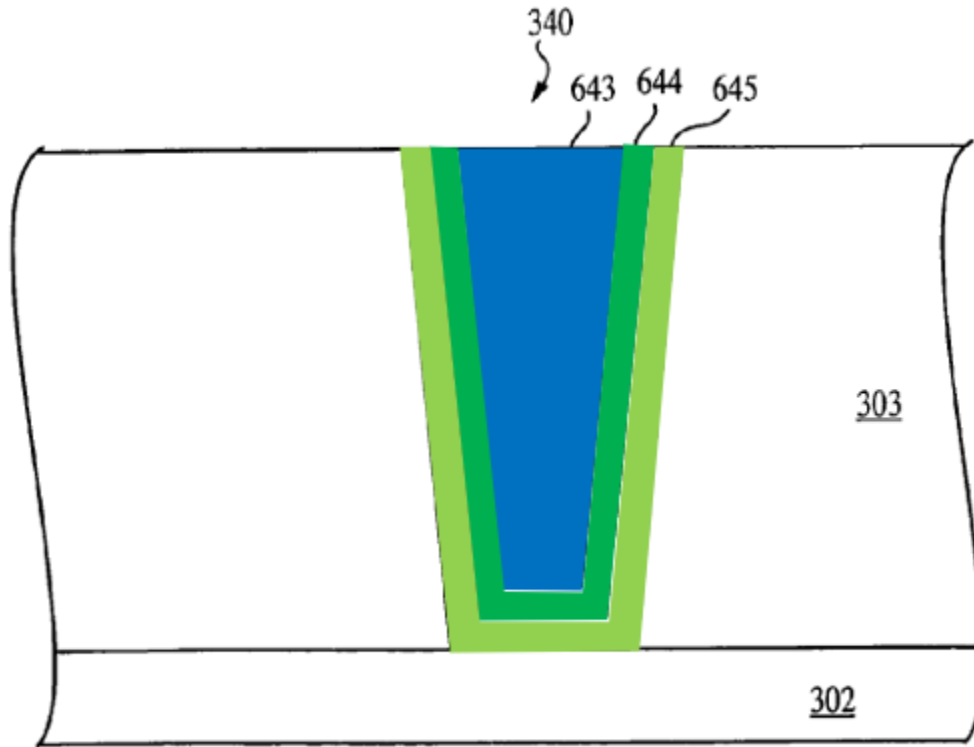


FIG. 6

Cole, ¶¶0042, 0044.

216. *Cole* teaches various techniques that provide for electrical and optical isolation at the periphery of pixels, but which apply differently to different sets of dependent claims. Therefore, the reasoning supporting obviousness will be described with respect to different groups of claims.

A. ISOLATION CLAIMS 5, 23, 38-40, 43, 45-47, 50, 68-69, 74-75

217. These claims require that the peripheral isolation element provide “isolation” generally (38, 45), a “trench” isolation element (43, 50), optical isolation (39, 46, 68, 74), and/or electrical isolation (40, 47, 69, 75). Claims 5 and 23,

furthermore, require the peripheral isolation element to “extends substantially from the light incident surface to the backside surface”.

218. Hwang-099 teaches or renders obvious these claims as discussed above in Grounds 1 and/or 2. These claims would also have been obvious, however, in view of Cole. Specifically, Cole teaches that “it is advantageous to provide both electrical and optical isolation between pixels” in order to prevent color mixing. *Cole*, ¶0005. This was also a goal of Hwang-099. *Hwang-099*, 10:28-40. Cole further teaches methods for achieving optical and electrical isolation, specifically by forming a “trench” isolation structure *Cole*, ¶0030) that extends entirely through the epitaxial layer (the layer where the photodiode is formed) to the base layer *Cole*, ¶0034), as shown in Fig. 7, reproduced again here:

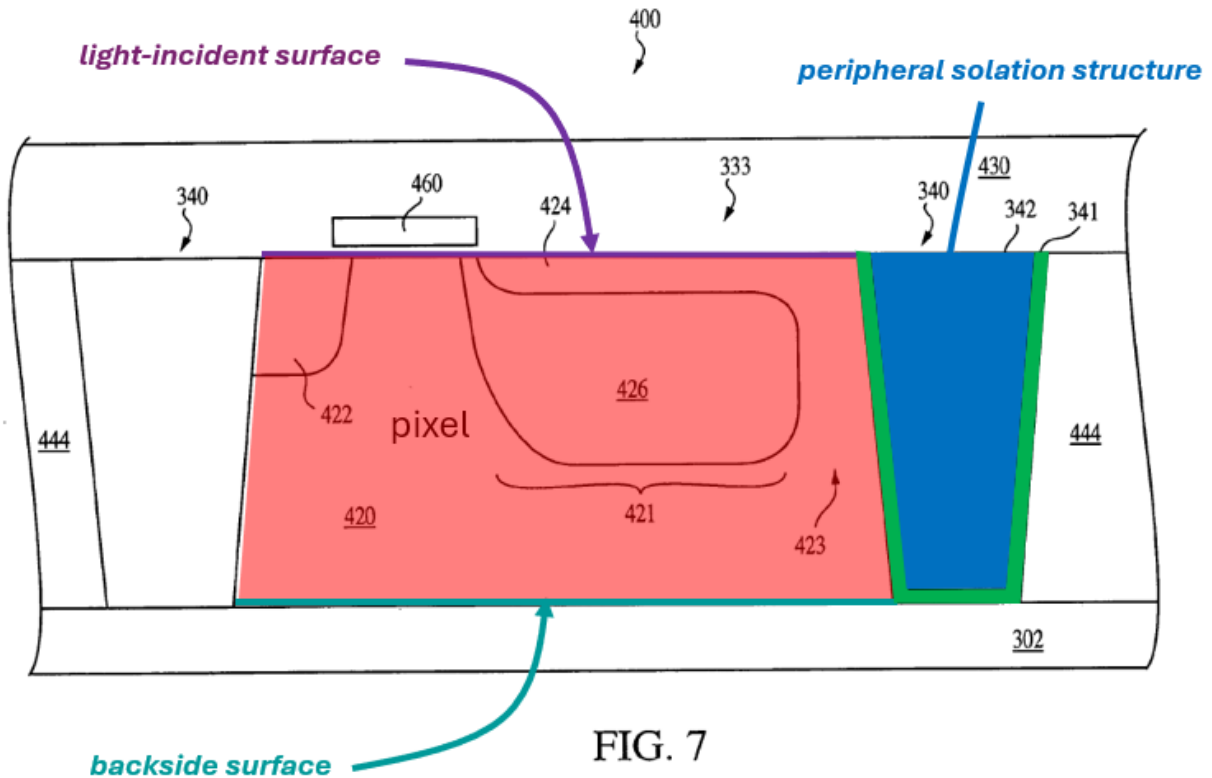


FIG. 7

Cole, Fig. 7, ¶0044. The trench 340 includes “a thermal oxide” that is “grown in trench 340 prior to deposition of material 341, providing an additional barrier to electrons.” *Cole*, ¶0035.

219. Based on these teachings, a POSITA would have been motivated to form Hwang-099’s trench isolation structure to extend from the light-incident surface to the backside surface (meeting claims 5 and 23), and to ensure that it provides sufficient isolation, thereby improving similar isolation structures in the same way. As I discuss above in ¶¶191-196, Hwang-099 already teaches a peripheral isolation structure that extends from the light-emitting surface to the backside surface and uses silicon oxide in its outside layers, as discussed above in

Ground 2, claim 5. *Hwang-099*, Fig. 6, 11:57-12:31. It would further have been obvious based on *Cole* to use a trench isolation structure to separate pixels that is sufficiently deep and sufficiently insulating “**to provide both electrical and optical isolation between pixels**”. *Cole*, ¶0005. A POSITA would have had a reasonable expectation of success in so doing, including for the expected benefits of reducing optical and electrical crosstalk (*Cole*, ¶0005), at least because *Cole* teaches forming a trench extending to the backside surface and from the predictable nature of the materials and etching processes involved. *Cole*, ¶¶0038-0039. The techniques for trench formation were widely-used and well-understood in the semiconductor industry, allowing for control of depth of trench structures by various techniques. *Cole*, ¶0038 (“Trench 340 can be formed by techniques known in the art, such as an anisotropic etch through a mask....”); *Hwang-099*, 3:60-67.

B. CLAIMS 65-66, 71-72

220. Claims 65 and 71 recite a peripheral isolation element with a depth of 100 nm to 50 microns, corresponding to a 500-fold range of depth. Claims 66 and 72 (dependent from claims 66 and 71, respectively) recite a width of 100 nm to 10 microns.

221. Regarding claims 66 and 72, *Hwang-099* already teaches a width of its sidewall reflecting structure of 160 nm, and thus teaches the limitations of claims 66

and 72, as discussed above under Ground 1, claim 44. *Hwang-099*, 10:48-60. *Hwang-099*, however, does not expressly discuss the depth.

222. The recited depth range of claims 65 and 71 would have been obvious in view of Cole. Cole teaches isolation structures at the periphery of pixels, and emphasizes the need to separate pixels to avoid optical and electrical crosstalk. *Cole*, ¶¶0005. Cole further teaches that to prevent photons and electrons from crossing the isolation structures, the structures “are deep, extending to a depth of at least about 0.5 micrometers”, with exemplary depths of 4 to 6 microns, “sufficiently deep to prevent photons or charge carriers from reaching array 333”. *Cole*, ¶¶0030, 0034. A POSITA would have been motivated, based on Cole, to use such exemplary depths sufficient to prevent photons and charge carriers from crossing them, and would have had a reasonable expectation of success in doing so, including for the expected benefits. This was at least because the techniques for trench formation were widely-used and well-understood in the semiconductor industry, allowing for control of depth of trench structures by various techniques. *Cole*, ¶0038 (“Trench 340 can be formed by techniques known in the art, such as an anisotropic etch through a mask....”); *Hwang-099*, 3:60-67.

XI. OPINIONS REGARDING GROUND 4: CLAIMS 6, 8, 11, 24, 30, 32, 34, 36, 53-54, 59-60, 80 AND 82 WERE OBVIOUS OVER HWANG-099 AND SHINOHARA.

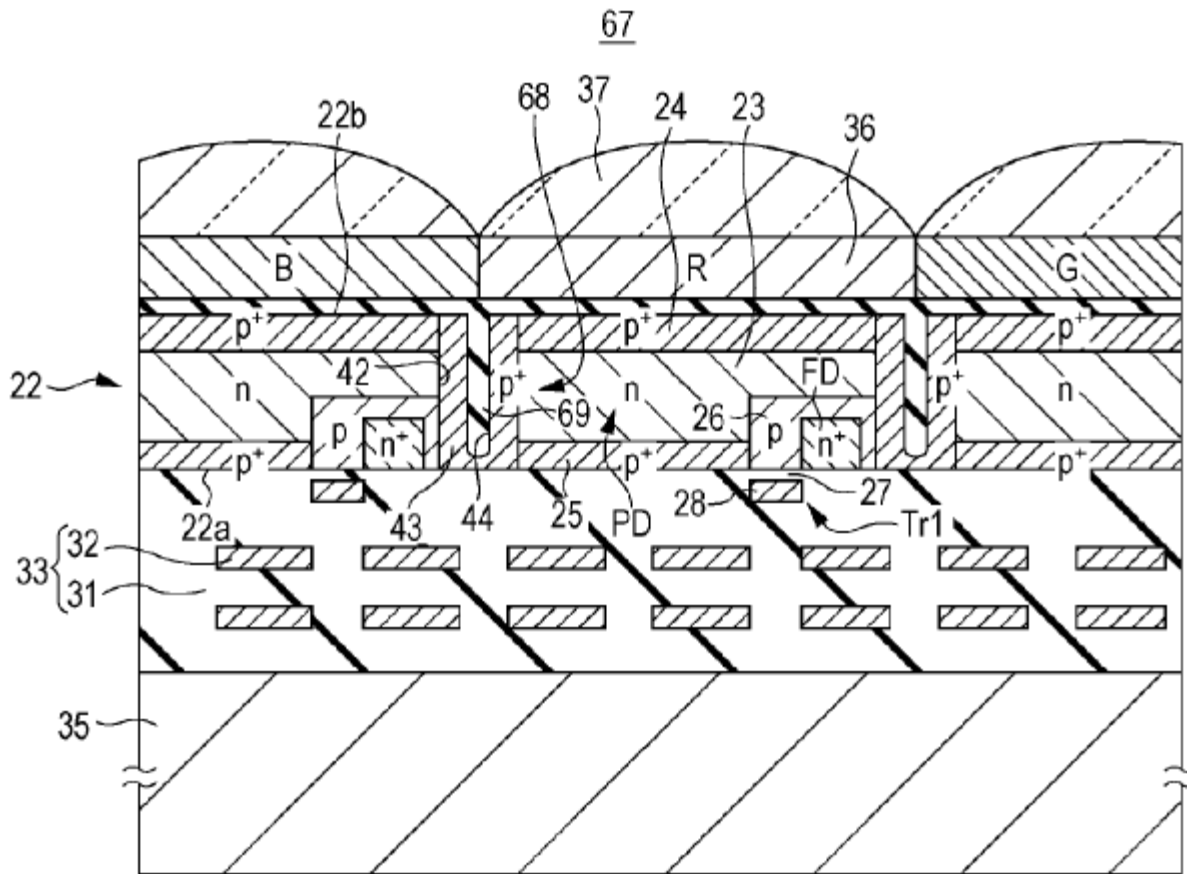
223. The above-reference claims would have been obvious over Hwang-099 and Shinohara (Ex. 1068).

224. Claims 6, 8, 11, 24, 30, 32, 33, and 36 recite the use of certain materials in the peripheral isolation element, while claims 53-54 and 59-60 recite the use of *multiply types* of materials in the peripheral isolation element, while claims 80 and 82 recite peripheral isolation elements with five layers. *Shinohara* (Ex. 1068) specifically teaches that the claimed materials are used in a reflecting layer between pixels, and teaches that such materials are used as substitutes for or together with silicon oxide. *Shinohara*, ¶¶0060, 0065, 0091.

225. While Hwang-099 does not expressly teach the use of the materials recited in claims 6, 8, 11, 24, 30, 32-34, and 36-37, Shinohara specifically teaches that such materials can be used in a reflecting layer between pixels, and teaches that such materials can be used as substitutes for or together with silicon oxide.

226. Like Hwang-099 and the '359 patent, Shinohara teaches a “solid-state imaging device” having pixels. *Shinohara*, Abstract. A cross-sectional view of a pixel (with neighboring pixels to the right and left) is provided in Fig. 9A, reproduced here:

FIG. 9A



Shinohara, Fig. 9A. In Fig. 9A, there are portions of three pixels shown, each overlain by a hemispherical micro-lens at the top of the Figure. *Shinohara*, ¶¶0059, 0092.

227. Between pixels, *Shinohara* teaches having “an element isolation region 68 for isolating pixels....” *Shinohara*, ¶0090. The element isolation region is formed of alternating layers of silicon (43) and an oxide or nitride film (69). *Shinohara*, ¶¶0097, 0094. The purpose of the element isolation region is to prevent optical and electrical cross-talk between pixels, similar to the peripheral isolation

element of the '359 patent and the sidewall multi-layered reflection layer 220 of Hwang-099. Shinohara explains:

“According to the solid-state imaging device 67 of the second embodiment, the p-type semiconductor layer 43 having the void 44 is formed in the trench 42, and the insulating film 69 is further filled in the void 44, so that the element isolation region 68 is formed. Since the insulating film 69 is filled in the void 44, adjacent pixels are further electrically insulated from each other, thereby suppressing the leakage of photoelectrically converted charge into an adjacent pixel. In addition, since the filled **insulating film 69 has a refractive index different from that of the p-type semiconductor layer 43**, even if inclined incident light is incident thereon, the light is not photoelectrically converted in an adjacent pixel after passing through the element isolation region 68. That is, inclined incident **light is reflected at the interface between the silicon and the insulating film and does not leak outside from the pixel**, and hence no color mixture occurs.”

Shinohara, ¶0094.

228. Shinohara teaches that its layer 69 can be made from silicon oxide or nitride, or, if a negative fixed charge is desired, from any of “hafnium dioxide (HfO₂), dialuminum trioxide(Al₂O₃), ditantalum pentaoxide (Ta₂O₅), and dilanthanum trioxide (La₂O₃)....” *Shinohara*, ¶0092.

229. It would have been obvious and a POSITA would have been motivated to use the oxides specified by Shinohara in the layers 210 of the sidewall reflecting element 220 of Hwang-099, for two independent reasons. **First**, the isolation

element of Shinohara plays a role in the device similar to Hwang-099's peripheral isolation element. *Hwang-099*, 6:19-23, 9:58-66, 10:14-18; *Shinohara*, ¶0094. Moreover, Hwang-099 repeatedly stresses the general concept of a peripheral isolation element with alternating layers of different refractive indices to produce reflection. *Hwang-099*, 2:1-3, 2:10-13, 3:41-43, 4:1-2, 4:16-18, 6:11-13, 9:52-53, 9:60-63, 10:7-10, 11:22-30, 11:66-12:7, claims 2, 3, 12. For its relatively higher-refractive-index layers Hwang-099 suggests using silicon, while for the lower-refractive-index layers the electrically-insulating materials silicon oxide and air. *Hwang-099*, 6:11-13, 9:28-30, 10:2-5. Shinohara expressly teaches that, in such structures, either silicon oxide (as used in Hwang-099) or hafnium dioxide (HfO_2), dialuminum trioxide (Al_2O_3), ditantalum pentaoxide (Ta_2O_5), dilanthanum trioxide (La_2O_3) would be appropriate for layer 69, because these layers provide both electrical insulation and a refractive index contrast with silicon. *Shinohara*, ¶¶0092-0094.

230. A POSITA would have known that the refractive index of Al_2O_3 in approximately the middle of the visible spectrum was approximately 1.7 (*Aguilar-Frutis*, Ex. 1077, p. 1700), the refractive index of Ta_2O_5 was approximately 2 (*Kasano*, Ex. 1064, ¶¶0024-0025), the refractive index of HfO_2 was approximately 2 (*Iida*, Ex. 1078, ¶¶0051, 0088), and the refractive index of La_2O_3 was approximately 1.8 (*He*, Ex 1079, p. G132).

231. Thus, a POSITA would have found it appropriate to use these oxides as substitutes for Hwang-099's lower-refractive index layers 210 (the first and second layers of the claims) because they are suitably-insulating oxides with refractive indices lower than Hwang-099's silicon layers (RI is approximately 4), *Hwang-099*, 9:28-30, that were already being used in a peripheral isolation element in Shinohara. There would have been predictable results.

232. **Second**, a POSITA would have expected benefits from using the oxides suggested by Shinohara in the layers 210 of Hwang-099's sidewall reflecting element 220. Specifically, Shinohara teaches that these oxides can provide a negative fixed charge, which has a hole-pinning effect in the adjacent p-type layer 43. *Shinohara*, ¶¶0092, 0095. The hole pinning effect, as referred to in Shinohara, means the use of a fixed negative charge to cause an accumulation of positive charges in the silicon near the oxide layer. The positive charge accumulation region is formed in the vicinity of the interface between the silicon layer and the insulating layer and causes a bending the energy bands near the interface. This is useful, because the interface between the insulating layer and silicon otherwise has the potential to create interface states that can promote the generation of mobile electrons, even in the absence of incident light. The hole-pinning effect suppresses these electrons, thereby reducing dark current. A POSITA would have expected the hole-pinning effect to suppress the generation of white spots and dark current (as

taught by Shinohara), and to improve quantum efficiency and operation speed. *Shinohara*, ¶0095. Shinohara furthermore teaches that layers with different refractive indices ensures that “no color mixture occurs”. *Shinohara*, ¶¶0091, 0095.

233. A POSITA would have had a reasonable expectation of success in using hafnium dioxide (HfO_2), dialuminum trioxide (Al_2O_3), and ditantalum pentaoxide (Ta_2O_5), dilanthanum trioxide (La_2O_3) in Hwang-099, including to achieve advantages taught in Shinohara, based on the widespread and predictable use of insulating oxides in the semiconductor industry, the teachings of Hwang-099 and Shinohara to use insulating oxides in peripheral isolation elements, and because these were well-known materials in semiconductor fabrication, with established deposition techniques. *Shinohara*, ¶0091; *Callegari*, 4:66-5:8, 7:1-31.

A. CLAIMS 6, 11, 30, 32, 34, 36

234. Claims 6 and 11 recite the use of Al_2O_3 in the first or second layers (claim 6) or “any of aluminum oxide and hafnium oxide” in the peripheral isolation element (claim 11). Claims 30 and 34 recite the use of tantalum oxide in the peripheral isolation element. Claims 32 and 36 recite the use of lanthanum oxide in the peripheral isolation element. It would have been obvious to use any of aluminum oxide, hafnium oxide, tantalum oxide, and lanthanum oxide in the first and second layers 210 of Hwang-099’s sidewall reflecting element (peripheral isolation

element) 220 for the reasons provided above in ¶¶225-233. *Shinohara*, ¶¶0092-0095.

B. CLAIM 8: “The device of claim 1, wherein said peripheral isolation element provides a passivating negative charge.”

235. *Shinohara* teaches that its oxides in its layer 69 can have a negative fixed charge, which suppresses dark current and is thus a passivating negative charge. *Shinohara*, ¶¶0092, 0095. A POSITA would have been motivated to use any of hafnium dioxide, dialuminum trioxide, ditantalum pentaoxide, and dilanthanum trioxide in Hwang-099’s sidewall reflecting element (peripheral isolation element) 220 for the well-known and predictable hole-pinning effect that suppresses the generation of white spots and dark current as discussed above in ¶232.

C. CLAIMS 24, 53-54, 59-60, 80, AND 82

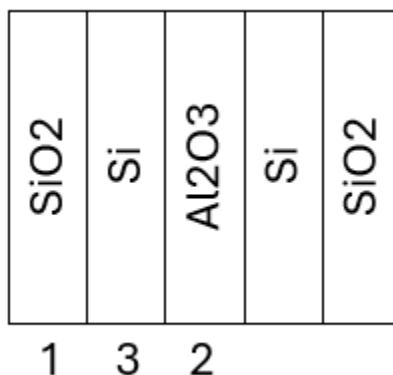
236. Claim 24 (dependent on claim 18) requires that “said at least two materials comprises silicon dioxide and aluminum oxide”, where claim 18 specifies that the peripheral isolation element comprises two materials with different indices of refraction. Claims 53 and 59 require that “the first layer and the second layer of said peripheral isolation element comprise different materials”. Claims 54 and 60 require that “the peripheral isolation element comprises at least three materials”, while claims 80 and 82 require “the peripheral isolation element comprises five layers”. These claims would have been obvious over Hwang-099 and *Shinohara*.

As discussed above under Ground 1, claim 55, Hwang-099 teaches that its sidewall multi-layered reflection layer 220 (peripheral isolation element) having **five layers**. *Hwang-099*, 12:67-13:3; *see also Hwang-099* discussing multiple sets of layers alternating a plurality of times, e.g. 2:16-29, 4:12-15, 10:7-12, 11:47-52, 14:66-15:4, claim 4. Hwang-099 specifically teaches a five-layer embodiment made from three grooves 205, which are filled with silicon oxide, forming a sidewall layer 220 with SiO-Si-SiO-Si-SiO structure. *Hwang-099*, 12:62-13:3. It would have been obvious based on Hwang-099 and Shinohara that in a five-layer (or more) structure, both silicon oxide and aluminum oxide (Al_2O_3) would be used with Al_2O_3 in the middle. Shinohara further teaches that it was advantageous to use an Al_2O_3 layer between two silicon layers to provide a negative fixed charge, and hole-pinning effect. *Shinohara*, ¶¶0091, 0095, Figs. 9A-9B. Based on these suggestions, it would have been obvious to form Hwang-099's sidewall layer 220 with five layers, but replace the middle silicon oxide layer with Al_2O_3 , corresponding to Shinohara's structure (Si- Al_2O_3 -Si) with two outer layers of silicon oxide. This would have had the advantage, taught by Shinohara, of providing a negative-fixed-charge layer to produce a pinning effect to suppress the generation of white spots and dark current, as taught by Shinohara. *Shinohara*, ¶0094, 0091.

237. A POSITA would have been further motivated by the desire to optimize the performance of sidewall 220. *Hwang-099*, 10:19-40, 12:62-13:3; *Shinohara*,

¶0094. The design of such a structure would have been routine to a POSITA, who would have had a reasonable expectation of success at least because forming Al_2O_3 layers was well-known, including for expected advantages.

238. In the combination, the first, second and third layers would be as shown here:



239. The combination meets claim 24, because Hwang-099's peripheral isolation element would have "at least two materials with different refractive indices that comprise silicon dioxide and aluminum oxide" ($\text{RI} \approx 1.46$ and 1.7 , respectively). The combination also meets claims 53 and 59, because the first and second layers comprise different materials (silicon oxide and Al_2O_3). The combination also meets claims 54 and 60, because the first and second layers are different materials. The combination meets claims 80 and 82, because the structure has five layers.

XII. OPINIONS REGARDING GROUND 5: CLAIMS 12-17, 19-22, 25-29, 65-66, 71-72, AND 76-79 WERE OBVIOUS OVER HWANG-099 AND CAREY.

240. The above-referenced claims were obvious over Hwang-099 and Carey (Ex. 1069). References to Carey are to the added page numbers:line numbers, for example 024:15-16 means page 024, lines 15-16.

241. Claims 12-17, 19-22, 26-29, and 76-79 are dependent claims that recite various “textured regions”, which Hwang-099 does not expressly disclose (claims 25, 65-66 and 71-72 do not recite textured layers, and will be addressed separately below). Carey, however, discloses the advantageous use of textured regions within image-sensor pixels, allowing them to be thinner. A POSITA would have found it obvious to add textured regions to the pixels of Hwang-099 in the various manners suggested by Carey.

242. Carey is directed to High-Speed Photosensitive Devices and Associated Methods. *Carey*, Title. The photosensitive devices of Carey include imaging devices having an array of pixels, just like Hwang-099 and the '359 patent. *Carey*, e.g. Figs. 13 and 14, 024:15-16, 022:15-16. Like Hwang-099 and the '359 patent, Carey teaches pixels with photodiodes, where the photodiodes have peripheral isolation structures between adjacent pixels to lower optical crosstalk, preferably using total internal reflection. *Carey*, 026:14-34, 011:14-19.

243. Within such devices, Carey teaches the use of textured regions on surfaces. *Carey*, Abstract. Textured surfaces, according to Carey, “refer to a surface having a topology with nano- to micron-sized surface variations”—similar to the definition of the ’359 patent. *Carey*, 006:33-007:9; ’359 *Patent*, 4:40-43.

244. Carey teaches that its textured surfaces have a variety of benefits. *Carey*, 009:13-19, 010:7-15, 011:11-22, 012:18-29, 014:15-20, 015:26-34, 017:18-19, 021:21-25, 025:9-17, 026:18-21, 026:25-27, 027:6-13. To explain Carey’s disclosure of the benefits, it is useful to explain certain aspects of the basic functioning of a silicon-based photodiode. Photodiodes work by creating charged particles (which can be measured) from the absorption of light passing through them. The light must travel some distance to be absorbed, however, and the average distance light must travel before being absorbed depends on its wavelength. This means that short-wavelength light (*e.g.* blue light) will tend to be absorbed in the upper portion of the device, while longer-wavelength light (*e.g.* red, or in particular, infra-red) may pass through the entire thickness of a device without being absorbed. *Carey*, 009:13-19. This, in turn, could require a minimum device thickness for devices that need to be sensitive to long-wavelength light. *Carey*, 011:8-11.

245. Carey’s Textured regions can help with this problem, according to Carey, by diffusely scattering (or diffusing) long-wavelength light. *Carey*, 011:11-22. When scattered, the light will take on a different direction, potentially increasing

its path-length through the silicon, and giving it a better chance of being absorbed. (*Id.*). According to Carey, this can increase the sensitivity of the device to longer wavelengths, allow the device to be thinner, and increase the operation speed of the device. (*Id.*). To achieve these benefits, Carey teaches placing its textured regions on the front surface, back surface, and/or peripheral isolation elements of the device. *Carey*, 016:9-12, 022:10-11.

246. A POSITA would have had a reasonable expectation of success in combining Carey with Hwang-099. At the level of generality of the claims of the '359 patent, the art was predictable. Furthermore, both the '359 patent and Carey provide a broad description of their textured layers (*Carey*, 006:33-007:9; '359 *Patent*, 4:40-43), and each states that their textured layers can be produced via a variety of standard techniques used in semiconductor processing. *Carey*, 006:33-007:20; '359 *Patent*, 4:40-57. Each refers to and incorporates the same three prior-art patents as illustrative of techniques for forming textured layers. *Carey*, 016:26-29; '359 *Patent*, 15:13-18. The evidence thus shows that a POSITA would reasonably have expected success in making textured regions within Hwang-099's device, and in achieving the advantages taught by Carey.

248. A POSITA would have been motivated to include a *textured region*, per Carey, coupled to the *light incident surface* to increase the sensitivity, speed and light collection efficiency of Hwang-099's pixel. Carey, 009:13-19, 010:7-15, 011:11-22, 012:18-29, 014:15-20, 015:26-34, 017:18-19, 021:21-25, 025:9-17, 026:18-21, 026:25-27, 027:6-13. It was well-known that "[i]ncident light to a planar surface of silicon reflects, and reflected light does not contribute to the photocurrent." Mita, p. 2. Carey's textured regions on the light incident surface are a well-known approach to increase the amount of light collected by semiconductor devices. A POSITA would have known that adding a textured region coupled to Hwang-099's *light incident surface* would have diffusely scattered incident light such that less light was reflected off the light incident surface, thereby increasing the collection efficiency of Hwang-099's *pixel*. A POSITA would have understood that, in modifying silicon surfaces to form Carey textured regions, it would have been advisable to provide a thin passivating layer. The modification is application of a known technique (adding a textured region to the light incident surface) to a known device (image sensor) ready for improvement to yield the predictable result of increasing light collection efficiency.

249. A POSITA would have also been motivated to modify Hwang-099's *backside surface* to *comprise Carey's textured region*. Providing a textured region on the backside surface would have enhanced internal reflection of incident light

within Hwang-099's pixel. A POSITA would have understood that compared to a smooth surface, a Carey textured region would have diffusely scattered incident light thereby increasing the path length of light throughout the geometry of the pixel. Further, a POSITA would have appreciated that the Carey textured region would have worked in conjunction with Hwang-099's base multi-layered reflection layer to increase the amount of incident light reflected toward photodiode 145, in part by increasing the range of angles that light reflects back into the pixel. A POSITA would have understood that, in modifying silicon surfaces to form Carey textured regions, it would have been advisable to provide a thin passivating layer. The modification would have predictably increased the quantum efficiency of Hwang-099's pixel. The modification is nothing more than application of a known technique (providing a textured region) to a known device (image sensor) in the same way.

250. The modification would have had additionally a reasonable expectation of success because methods of texturing materials were well-known. *Konno* at 14:38-45; *Smith* at 3:31-35.

B. CLAIM 13: "The device of claim 12, wherein said textured region is coupled to the light incident surface."

251. It was obvious to use a Carey textured region in a pixel of Hwang-099's device **coupled to the light incident surface**, for the reasons discussed above under claim 12. Carey states that "[t]he textured region can be associated with the surface

nearest the impinging electromagnetic radiation....”, and can be paired with an antireflection layer. *Carey*, 016:9-10, Fig. 6, 021:10-20. By scattering light passing through the light-incident layer, light travels on a longer path through the device, increasing efficiency. *Carey*, 011:11-22. *Carey* furthermore teaches that textured regions near the surface of a layer are said to be “coupled” to the layer. *Carey*, Abstract, 012:18-20

C. CLAIM 14: “The device of claim 13, wherein said light incident surface comprises said textured region.”

252. *See* claim 13. The Hwang-099-Carey combination teaches the light-incident surface *compris[ing] the textured region* as shown in Fig. 6. *Carey*, Fig. 6, 021:10-13

D. CLAIM 15: “The device of claim 13, wherein said textured region comprises a textured film layer.”

253. *Carey*’s Fig. 6 shows a **textured** region that is also a **film layer**. *Carey*, Fig. 6, 021:10-16. For example, in Fig. 7 of *Carey*, textured region 78—which is the same as textured region 68 in Fig. 6 but placed at the backside of the device—is referred to interchangeably as both a “textured region” and a “textured layer”. *Carey*, Fig. 7, 021:15-16. The term “film” simply means a thin layer and applies generally to semiconductor layers.

E. CLAIM 16: “The device of claim 15, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”

254. Carey teaches that layer 68 in Fig. 6 comprises “silicon material”.

Carey, 021:10-13. Carey further states:

“Various types of silicon materials are contemplated, and any such material that can be incorporated into an optoelectronic device is considered to be within the present scope. In one aspect, for example, the silicon material is monocrystalline. In another aspect, the silicon material is multicrystalline. In yet another aspect, the silicon material is microcrystalline.”

Carey, 015:14-18. “Multicrystalline” and “microcrystalline” are both forms of polycrystalline silicon, *i.e.*, *polysilicon*. Based on Carey’s teaching, it would have been obvious to use polysilicon on the light-incident surface of the device to form a textured layer, because it was a commonly-used material in semiconductor manufacturing having known deposition and structuring methods. Polycrystalline is expressly suggested by Carey, and could have been predictably implemented with a reasonable expectation of success for similar reasons.

F. CLAIM 17: “The device of claim 12, wherein said backside surface comprises said textured region.”

255. *See* claim 12. Carey teaches that the **backside surface can comprise the textured region** as shown, *e.g.*, in Carey’s Figs. 2 and 7. *Carey*, Fig. 2, 012:10-29, Fig. 7, 021:13-20, 016:13-15, 027:4-5. A POSITA would have found this

arrangement desirable in order to reflect and scatter light at the backside surface, such that the path light travels back through the device is increased in length, increasing efficiency. *Carey*, 011:11-012:29.

G. CLAIM 19: “The device of claim 18, wherein at least one of said light incident surface and said backside surface of at least one of said two adjacent light sensitive pixels comprises a textured region.”

256. *See* the discussion above under claims 12-13, and 17.

H. CLAIM 20: “The device of claim 19, wherein said textured region is a textured film layer.”

257. *See* claim 15. *Carey*’s backside textured region 78 (Fig. 7) is also referred to interchangeably as both a “textured region” and a “textured layer”, where a POSITA would understand that a layer is a *film*. *Carey*, Fig. 7, 021:15-16.

I. CLAIM 21: “The device of claim 20, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”

258. *See* the discussion above under claim 16, which applies here for similar reasons.

J. CLAIM 22: “The device of claim 19, wherein said textured region reflects at least a portion of light internally incident thereon into the at least one pixel.”

259. *See* claim 16 and claim 22, above. *Carey* explains this with respect to Fig. 2, which shows a cross-section of a pixel, and is reproduced here:

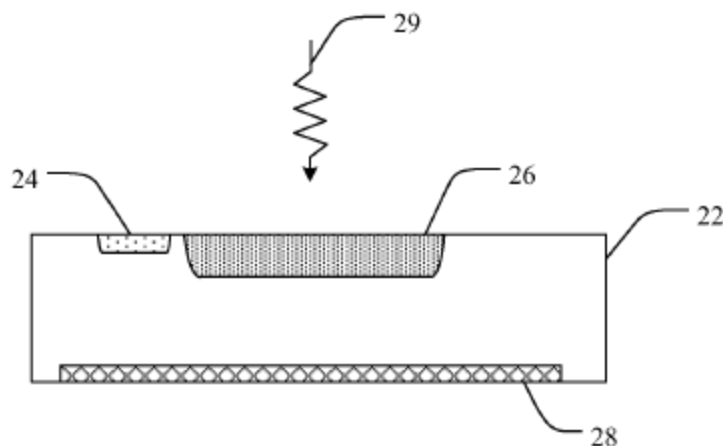


FIG. 2

Carey, Fig. 2. In Fig. 2, light 29 impinges on the front surface of the device, partially passing through the device to reach a textured region 28 on the backside of the device. Carey, 012:10-29. Carey explains:

“The optoelectronic device can also include a **textured region 28** coupled to the silicon material 22 and positioned to interact with incoming electromagnetic radiation 29. In this case, the textured region is located on a side of the silicon material that is opposite to the first doped region 24 and the second doped region 26. **Electromagnetic radiation that passes through the silicon material to contact the textured region can be reflected back through the silicon material, thus effectively increasing the absorption path length** of the silicon material.”

Carey, 012:18-29 (Emphasis added). Thus, Carey expressly teaches for backside textured regions that **said textured region reflects at least a portion of light internally incident thereon into the at least one pixel.**

K. CLAIM 25: “The device of claim 19, wherein said at least two pixels are formed monolithically in a common semiconductor substrate.”

260. See Ground 1, claims 42 and 49. *Hwang-099*, 5:52-58. *Hwang-099* already teaches this claim element, but it is dependent on claim 19, which requires a textured layer. The combination with *Carey* would not change the fact that *Hwang-099*'s pixels are formed monolithically in a common semiconductor substrate.

L. CLAIM 26: “The device of claim 19, wherein the textured region is formed by laser radiation.”

261. *Carey* teaches that its textured regions can be **formed by laser radiation** *Carey*, 006:33-7:9, 016:16-018:10. *Carey* states expressly that “[o]ne effective method of producing a textured region is through laser processing.” *Carey*, 016:18-19. *Carey* teaches laser radiation as one of a finite number of alternatives for the formation of textured regions, and it could have been carried out predictably with a reasonable expectation of success, based on *Carey*'s direct teachings.

M. CLAIM 27: “The device of claim 12, wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.”

262. *Carey* teaches that **reactive ion etching, chemical etching, nanoimprinting, and material deposition** can be used to form a textured region. *Carey*, 016:16-19, 007:1-3, 007:13-15. It would have been obvious to use any of these methods, based on *Carey*'s express teachings, and because *Carey* teaches each

of these methods is one of a finite number of alternatives for the formation of textured regions, which would have been carried out predictably with a reasonable expectation of success, based on Carey's direct teachings.

N. CLAIM 28: "The device of claim 12, wherein the textured region is formed by laser radiation."

263. *See* claim 26.

O. CLAIM 29: "The device of claim 12, wherein said textured region is coupled to the backside surface."

264. *See* the discussion above under claim 17, which is narrower. *Carey*, Fig. 2, 012:10-29, Fig. 7, 021:13-20, 016:13-15, 027:4-5.

P. CLAIM 65 AND 71

265. Claims 65 and 71 depend from claims 64 and 70, respectively, and recite "said trench isolation element has a depth in a range of about 100 nm to about 50 microns."

266. The combination rendered claim 65 obvious, because Carey teaches a depth of the silicon photodiode of about 1 to 50 microns, and it would have been obvious to have Hwang-099's trench isolation element run for this entire depth or a substantial portion of it.

267. Specifically, Carey teaches that the silicon material for its photodiode can have "a thickness of from about 1 μm to about 50 μm ." *Carey*, 013:26-27. Such thicknesses have the advantage of increasing operation speeds. *Carey*, 010:1-15.

The “silicon material” is the material in which the photodiode is fashioned, and is equivalent to the silicon material in which photodiodes are formed (145) in Hwang-099. *Carey*, 012:18-20; *Hwang-099*, 5:55-58, Fig. 2. The thickness of this layer is approximately the depth of Hwang-099’s peripheral isolation element 220, because it extends from the light-incident surface to the isolation layer 130. Hwang-099, Fig. 2. *Carey* further teaches that the silicon material of a typical photodiode might be 100 microns, but that thinner depths can be used with textured regions, which effectively increase the path length of traversing long-wavelength radiation. *Carey*, 009:13-010:15. Using thinner materials has the advantage of increasing operation speeds. *Carey*, 010:1-15. Thus, it would have been obvious to use *Carey*’s suggested silicon depth of 1 to 50 microns as the depth of Hwang-099’s sidewall reflecting layers 220.

268. Furthermore, it would have been obvious for Hwang-099’s sidewall multi-layered reflection layer 220 to extend from the light incident surface to the backside surface (i.e. the depth of the silicon material 145, or 1 to 50 microns per *Carey*) for the reasons provided above under Ground 2, claims 5 and 23. There would have been a REOS for the combination, at least because *Carey* teaches forming methods for the photodiode thickness (depth), where again, the silicon material for the photodiode is the same material as for the formed trench in Hwang-099.

Q. CLAIM 66 AND 72

269. Claims 66 and 72 depend from claims 65 and 71, respectively, and recite “said trench isolation element has a width in a range of about 100 nm to about 10 microns.” Hwang-099 teaches this limitation as discussed under Ground 1, claim 44.

R. CLAIM 76 AND 78

270. Claims 76 and 78 depend from claims 1 and 18, respectively, and recite “the peripheral isolation element comprises a textured region.”

271. Carey teaches that the peripheral isolation element comprises its textured region in a dielectric material:

“Furthermore, **an isolation structure 57 can be positioned between the photodiodes to electrically and/or optically isolate the photodiodes from one another.** In another aspect, the photodiode array can be electronically coupled to electronic circuitry to process the signals generated by each photodiode. Various types of isolation structures are contemplated, and any such isolation is considered to be within the present scope. The isolation structure can be shallow or deep trench isolation. Furthermore, the isolation structure can include depths between traditional shallow and deep isolation, depending on the device design. Isolation structures can include **dielectric materials**, reflective materials, conductive materials, and combinations thereof, **including textured regions** and other light diffusing features. Thus the isolation structure can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device.”

Carey, 022:2-4 (Emphasis added). It would have been obvious based on Carey's suggestion (and the reasons discussed above ¶¶241-246 to use an **isolation element with a textured region**, *e.g.*, in Hwang-099's silicon oxide layers, because these are obviously silicon dioxide (as explained above under Ground 1, claim 3 and Ground 2, claim 3), a well-known dielectric material. Furthermore, a POSITA would expect a Carey textured region as part of the peripheral isolation element to scatter incident light, causing a longer path length through the device and increasing efficiency when light reflects off the peripheral isolation element. Carey, 011:11-012:29. Carey, 011:11-012:29. Thus, a POSITA would have been motivated to improve similar isolation elements in the same way, and there would have been a reasonable expectation of success, including for the expected benefits, at least because methods of texturing materials were well-known and it would have merely required texturing grooves 205' in which the layers of sidewall multi-layered reflection layer 220 (*peripheral isolation element*) are formed.

S. CLAIM 77 AND 79

272. Claims 77 and 79 depend from claims 1 and 18, respectively, and recite “the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.”

273. See claim 76. Based on Carey’s suggestion to place textured regions in dielectric layers of peripheral isolation layers and the advantages of textured layers discussed in Carey, it would have been obvious and a POSITA would have been motivated to place Carey textured regions at the interface between Hwang-099’s silicon oxide layers and the respectively-nearest pixel regions (*i.e., between the second layer and the other one of said adjacent pixels and between the first layer and one of said adjacent pixels*), to cause diffuse scattering of light back into the pixel to occur at each such interface. A POSITA would have had a reasonable expectation of success, for the reasons discussed under claims 76 and 78, above.

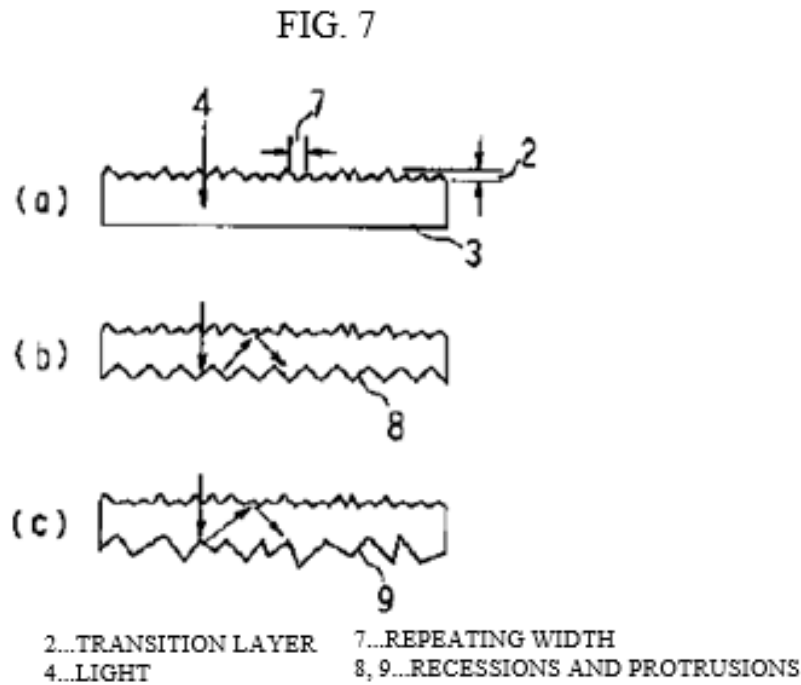
XIII. OPINIONS REGARDING GROUND 6: CLAIMS 12-17, 19-22, 25, 27, AND 29 WERE OBVIOUS OVER HWANG-099 AND UEMATSU

274. The above-referenced claims would have been obvious over Hwang-099 (as in Ground 2) and Uematsu (Ex. 1070).

275. Claims 12-17, 19-22, and 27 and 29 recite textured layers (claim 25 does not, but is dependent from claim 19).. Hwang-099 does not teach textured regions, but Uematsu does. It would have been obvious to use the textured regions of Uematsu in Hwang-099 for the reasons set forth below.

276. Uematsu is directed to photodetectors for detecting incoming light. Uematsu, Abstract, Title, ¶0001. Uematsu teaches that the efficiency of the conversion of light to electric charges “can be increased by effectively introducing

light into the substrate and confining the light inside the substrate without allowing it to escape to the outside of the substrate.” *Uematsu*, ¶0002. To confine light into the substrate, Uematsu teaches forming certain textured regions (in Uematsu, “recesses and protrusions”) on the light-incident and backside surfaces, as shown, for example, in Figs. 7(b)-(c), reproduced here:

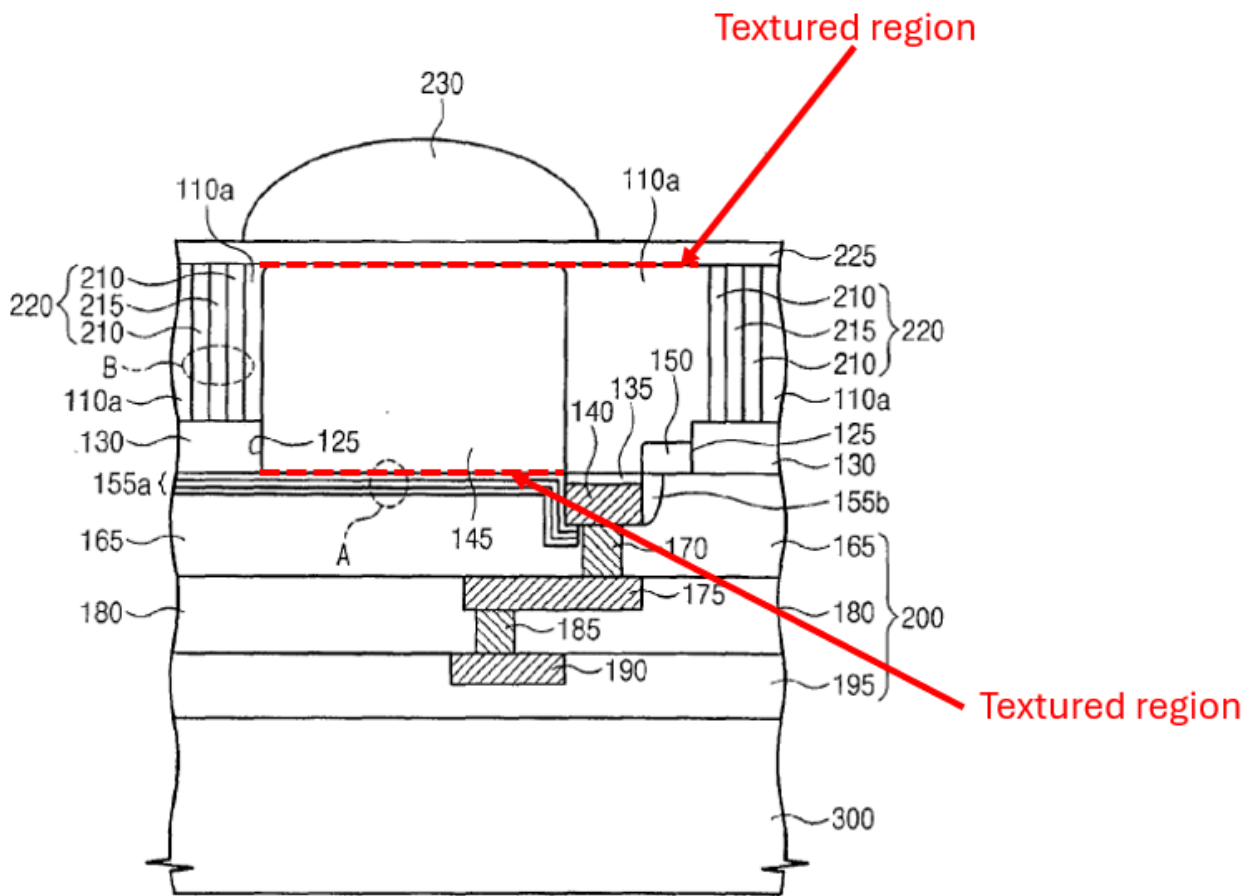


Uematsu, Fig. 7, ¶¶0017-0018. As shown in Fig. 7, by forming layers of Uematsu in the specific manner Uematsu suggests, one can achieve an advantageous increase in the internal path length of the light, increasing efficiency. *Uematsu*, ¶¶0017-0018.

277. In addition to rationales supporting obvious that are specific to certain claims and provided below for those claims, it would have been obvious to a POSITA to use textured Uematsu’s regions at the light-incident and/or backside

surfaces of Hwang-099's pixel to trap light within the pixel and increase the pixel's efficiency, as taught by Uematsu. *Uematsu*, ¶¶0014, 0018, 0024-0027, Fig. 12. A POSITA would have been motivated to provide textured regions of Uematsu at Hwang-099's light-incident and/or backside layers, as shown here:

Fig. 2



278. A POSITA would have found it obvious to use one or both of these Uematsu textured regions to increase efficiency, as taught by Uematsu, with a REOS at least because Uematsu teaches standard formation techniques for its textured

regions, and states that they can be “easily formed”. *Uematsu*, ¶¶0019-0022. In Hwang-099, it would have been obvious based on Uematsu to form its textured regions either in the silicon of layers 110a/145 itself, or as an additional film on the surfaces of these layers. *Uematsu*, ¶¶0019-0022.

A. CLAIM 12: “The device of claim 1, wherein at least one of said two adjacent light sensitive pixels comprises a textured region.”

279. It would have been obvious to incorporate Uematsu’s textured region in at least one pixel of Hwang-099’s device, at the light-incident and or backside surface, based on Uematsu, as discussed above in ¶¶274-279.

280. A POSITA would additionally have been motivated to include a *textured region*, per Carey, coupled to the *light incident surface* to increase the light collection efficiency of Hwang-099’s *pixel*. It was well-known that “[i]ncident light to a planar surface of silicon reflects, and reflected light does not contribute to the photocurrent.” *Mita*, p. 2. Textured regions per Uematsu on the light incident surface a well-known approach to increase the amount of light collected by semiconductor devices. A POSITA would have known that adding Uematsu’s textured region coupled to Hwang-099’s *light incident surface* would have diffusely scattered incident light such that less light was reflected off the light incident surface, thereby increasing the collection efficiency of Hwang-099’s *pixel*. The modification is application of a known technique (adding a textured region to the light incident

surface per Uematsu) to a known device (image sensor) ready for improvement to yield the predictable result of increasing light collection efficiency. The modification would have had a reasonable expectation of success because methods of forming textured regions coupled to the light incident surface were well-known.

281. A POSITA would additionally have been motivated to modify Hwang-099's *backside surface to comprise Carey's textured region*. A POSITA would have been motivated to provide a backside layer comprising a textured layer in Hwang-099's pixel to scatter light back into the pixel and thus improve efficiency, improving similar pixels in the same way. *Uematsu*, ¶¶0017-0018, 0027. Providing a textured region on the backside surface would have enhanced internal reflection of incident light within Hwang-099's pixel. *Uematsu*, ¶0018, Fig. 7. A POSITA would have understood that compared to a smooth surface, an Uematsu textured region would have diffusely scattered incident light, thereby increasing the path length of light throughout the geometry of the pixel. Further, a POSITA would have appreciated that the textured region would have worked in conjunction with Hwang-099's base multi-layered reflection layer to increase the amount of incident light reflected toward photodiode 145, in part by increasing the range of angles at which light reflects back into the pixel. Thus, the modification would have predictably increased the quantum efficiency of Hwang-099's pixel. The modification is nothing more

than application of a known technique (providing a textured region per Uematsu) to a known device (image sensor) in the same way.

282. The modification would have had a reasonable expectation of success because methods of texturing materials were well-known. *Konno* at 14:38-45; *Smith* at 3:31-35. Additionally, a POSITA would understand how to further alter texture geometry such that light reflection is optimized.

B. CLAIM 13: “The device of claim 12, wherein said textured region is coupled to the light incident surface.”

283. *See* claim 12’s mapping. It would have been obvious to incorporate Uematsu’s textured region in at least one pixel of Hwang-099’s device *coupled to the light incident surface*. Uematsu teaches that the textured region can be formed in the light-incident surface in a manner that facilitates internal reflection to increase efficiency. *Uematsu*, ¶¶0017-0018; Abstract, Figs. 7-12, ¶¶0006, 0012, 0017-0022, 0026, 0052-0053.

C. CLAIM 14: “The device of claim 13, wherein said light incident surface comprises said textured region.”

284. *See* claim 13, above. The combination teaches that the light-incident surface can *comprise* the textured region. *Uematsu*, ¶0006 (“recesses and protrusions provided on the substrate front surface”); *see also Uematsu*, ¶¶0017-0022, Figs. 7-12.

D. CLAIM 15: “The device of claim 13, wherein said textured region comprises a textured film layer.”

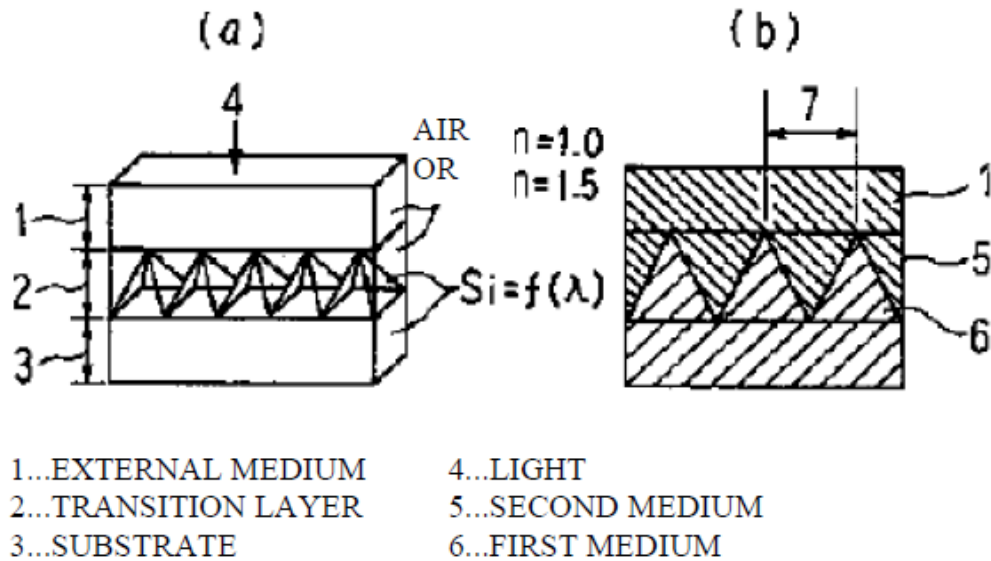
285. *See* claim 14. Uematsu teaches that its front-surface textured region can be “minute recesses and protrusions 11’ of irregular sizeformed by a deposited **film** using CVD (chemical vapor deposition).” *Uematsu*, ¶¶0021, Fig. 9. It would have been obvious to do so because Uematsu expressly teaches it. *Id.* Moreover, Uematsu teaches the method as one of a finite number of alternatives for the formation of textured regions, which would have been carried out predictably, with a REOS based on Uematsu’s direct teachings. A POSITA would have been motivated to use this method disclosed by Uematsu to achieve the efficiency advantages described by Uematsu. *Uematsu*, ¶¶0017-0018, Fig. 7.

E. CLAIM 16: “The device of claim 15, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”

286. *See* claim 15. Uematsu teaches that the “material of the film that was used was a material that is transparent and has a relatively high refractive index such as ITO or ZnO₂.” *Uematsu*, ¶¶0021. Such a layer comprises the metals Indium and Tin, or Zirconium. Uematsu also teaches that “the spaces between the minute recesses and protrusions 11’ were filled with a filling material (not illustrated) to protect the front surface. *Id.* A material with a relatively small refractive index such

as SiO₂ was formed on the filling material by means of spin coating, CVD, or the like.” *Id.* An example of a fill material is shown in Fig. 1(b), reproduced below, where the fill material is the second medium 5:

FIG. 1



Uematsu, Fig. 1(b), ¶¶0012-0013,0021, 0008. The fill material conforms to the surface of the textured layer, and thus itself becomes a textured layer with a complementary shape. Because this layer is made from SiO₂, it also **comprises silicon dioxide**. *Uematsu*, ¶0021.

287. A POSITA would have been motivated to use this method because it is expressly disclosed by *Uematsu*, and to achieve the efficiency advantages described by *Uematsu*. *Uematsu*, ¶¶0017-0018, Fig. 7. This method of formation, moreover, is one of a finite number of known alternatives disclosed by *Uematsu* that could be

implemented without unexpected results. *Uematsu*, ¶0021, Fig. 9. For at least that reason, and from Uematsu's express disclosure, a POSITA would also have had a reasonable expectation of success.

F. CLAIM 17: “The device of claim 12, wherein said backside surface comprises said textured region.”

288. See claim 12, discussing a backside surface region.

G. CLAIM 19: “The device of claim 18, wherein at least one of said light incident surface and said backside surface of at least one of said two adjacent light sensitive pixels comprises a textured region.”

289. See claims 13 and 17.

H. CLAIM 20: “The device of claim 19, wherein said textured region is a textured film layer.”

290. See claim 15.

I. CLAIM 21: “The device of claim 20, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”

291. See claim 16.

J. CLAIM 22: “The device of claim 19, wherein said textured region reflects at least a portion of light internally incident thereon into the at least one pixel.”

292. Uematsu teaches the claimed reflection when textured layers are formed in the particular manner described by *Uematsu*. *Uematsu*, ¶¶0017-0018, 0022, Figs. 7a-c. In the Hwang-099 – Uematsu combination, textured regions at

least at the backside surface would reflect light back into Hwang-099's pixel, as shown analogously in Fig. 7(c). *Uematsu*, ¶0018.

K. CLAIM 25: “The device of claim 19, wherein said at least two pixels are formed monolithically in a common semiconductor substrate.”

293. See Ground 1, claims 42 and 49. *Hwang-099*, 5:52-58. *Hwang-099* already teaches this claim element, but it is dependent on claim 19, which requires a textured layer. The combination with *Uematsu* would not change the fact that *Hwang-099*'s pixels are formed monolithically in a common semiconductor substrate.

L. CLAIM 27: “The device of claim 12, wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.”

294. *Uematsu* teaches forming its textured region by chemical etching or material deposition. *Uematsu*, ¶¶0019, 0021-0022. A POSITA would have been motivated to use this method disclosed by *Uematsu* to achieve the efficiency advantages described by *Uematsu*. *Uematsu*, ¶¶0017-0018, Fig. 7. This method of formation, moreover, is one of a finite number of known alternatives disclosed by *Uematsu* that could be implemented without unexpected results. *Uematsu*, ¶0021, Fig. 9. For at least that reason, and because of *Uematsu*'s express disclosure, a POSITA would also have had a reasonable expectation of success.

M. CLAIM 29: “The device of claim 12, wherein said textured region is coupled to the backside surface.”

295. See claim 17. *Uematsu*, Figs. 7-12, Abstract, cl. 8, ¶¶0010, 0018-0019, 0022.

XIV. OPINIONS REGARDING GROUND 7: CLAIMS 30, 32-34, AND 36-37 WERE OBVIOUS OVER HWANG-099 AND CALLEGARI

296. The above-referenced claims were obvious over Hwang-099 (as described in Ground 1) and **Callegari** (Ex. 1074).

297. Claims 30, 32-34, and 36-37 recite the use of certain oxides, well-known for semiconductor fabrication, within the peripheral isolation element. These oxides include Tantalum oxide (claims 30 and 34), Lanthanum oxide (claims 32 and 36), and Lanthanum aluminum oxide (claims 33 and 37).

298. While Hwang does not expressly teach the use of such materials, these materials were commonly-used in semiconductor fabrication, including for image sensors, as taught by Callegari. In addition, a POSITA would have known the standard properties (such as dielectric constants and refractive indices) of these materials, as they were widely available in the literature.

299. As discussed above under Ground 1, Hwang teaches the structure of claims 1 and 18, including a peripheral isolation element. While Hwang discusses silicon, silicon Oxide and Air as example materials for its peripheral isolation element, Hwang repeatedly stresses the more general concept of a peripheral

isolation element with alternating layers of different refractive indices to produce reflection. *Hwang-099*, 2:16-29, 4:12-15, 10:7-12, 11:47-52, 14:66-15:4, claim 4. For its relatively lower refractive-index layers, Hwang suggests the *electrically-insulating* materials silicon oxide and air. *Hwang-099*, 9:58-10:5.

300. It would have been obvious to a POSITA in the relevant timeframe that there were a variety of oxide materials, commonly-used in the semiconductor arts, that provided electrical-insulation properties together with relatively low refractive indices, and were thus suitable for use in Hwang's peripheral isolation element. Callegari, for example, teaches the use of tantalum oxide, lanthanum oxide, and lanthanum aluminum oxide in semiconductor fabrication. *Callegari*, 7:17-20. Callegari states that these materials were desirable as transistor gate oxides in semiconductors, a role that requires excellent electrical insulation properties. *Callegari*, 7:11-20, 1:58-2:17. Callegari specifically teaches the use of such materials in "sensor image array optoelectronic microelectronic fabrications", which are image sensors. *Callegari*, 6:5-17, *see also* 7:11-13, 4:3-8.

301. A POSITA would have found obvious the substitution of these materials for the lower-refractive-index layers (*e.g.* the claimed "first" and "second" layers of claims 1 and 18) or the high refractive-index layer (the claimed "third" layer) of the peripheral isolation element of Hwang. This is for two reasons. First, a POSITA would have known that tantalum oxide, lanthanum oxide, and lanthanum

aluminum oxide were common oxides used in semiconductor manufacturing with high resistivities and refractive indices generally in a range between those of silicon oxide and silicon. For example, the approximate refractive indices of these materials, as compared to silicon and SiO₂, are shown in the table below:

Material	Approximate Refractive index (n)
Silicon	4
Silicon Oxide (SiO ₂)	1.46
Tantalum Oxide (Ta ₂ O ₅)	2
Lanthanum Oxide (La ₂ O ₃)	1.8
Lanthanum Aluminum Oxide (LaAlO ₃)	1.7

See ¶230, above; *Hwang-099*, 9:28-30, 9:58-10:5, Ex. 1080, p. N3.

302. A POSITA would have seen that these oxides match the requirements for Hwang’s first and second layers (having a relatively lower refractive index) and would provide electrical insulation (like air and silicon oxide). Such substitutions would therefore have been seen as the “simple substitution of one known element for another”, with predictable results. For this reason, the substitution would have been obvious. Second, a POSITA would have seen as desirable the ability to use

common oxides having somewhat different refractive indices, because this would have allowed the POSITA to tune peripheral isolation elements to particular applications. That is, by altering the refractive index of the first and second layers, or by changing materials with a similar refractive index, a POSITA would have been able to adjust a peripheral isolation element to provide better constructive interference at particular wavelengths of interest in a given application. Hwang-099 teaches that its reflective structures can be varied to optimize performance. *Hwang-099*, 3:47-53; 10:41-47.

303. A POSITA would have had a reasonable expectation of success in using tantalum oxide, lanthanum oxide, and lanthanum aluminum oxide, because these were well-known materials in semiconductor fabrication, with established deposition techniques. (*e.g. Callegari*, 4:66-5:8).

A. CLAIMS 30, 32-34, AND 36-37

304. Claims 30 and 34 recite the use of tantalum oxide in the peripheral isolation element. Claims 32 and 36 recite the use of lanthanum oxide in the peripheral isolation element. Claims 33 and 37 recite the use of Lanthanum aluminum oxide in the peripheral isolation element. It would have been obvious to use any of tantalum oxide, lanthanum oxide, and lanthanum aluminum oxide in the first and second layers 210 of Hwang's sidewall layer 220 for the reasons discussed above.

XV. OPINIONS REGARDING GROUND 8: CLAIMS 30-31 AND 34-35 WERE OBVIOUS OVER HWANG-099 AND FORBES

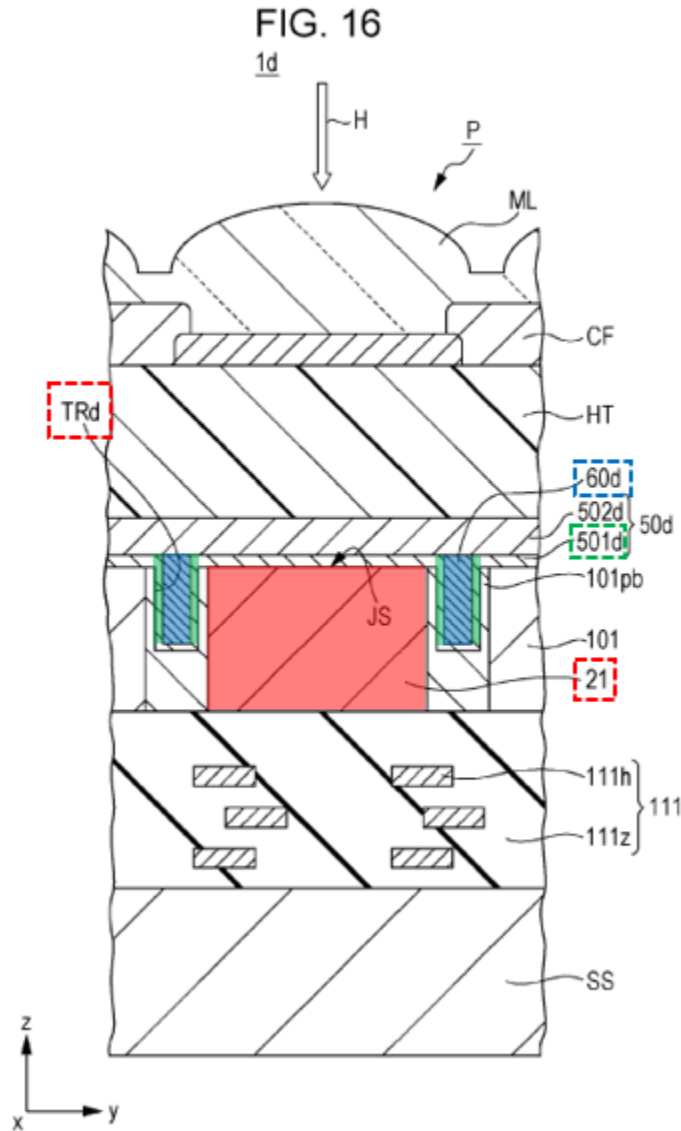
305. Claims 30-31 and 34-35 were obvious over Hwang-099 and Forbes (Ex. 1075).

306. Claims 30 and 34 require that the peripheral isolation element comprise tantalum oxide, while claims 31 and 35 further specify that the tantalum oxide comprises tantalum aluminum oxynitride (TaAlON). Like the oxides discussed under XIV, TaAlON was also a well-known oxide useful in the semiconductor arts, as taught by Forbes. *Forbes*, Title, Abstract. Forbes teaches that TaAlON films are “for use in a variety of electronic systems and devices.” *Forbes*, Abstract, ¶¶0033, 0103. The use of TaAlON as one element of a peripheral isolation element (e.g. in place of silicon oxide) would thus be a substitution of familiar elements (TaAlON for silicon oxide) having similar characteristics, according to known methods, which could be implemented with predictable results. A POSITA would have had a REOS at least because the methods of forming TaAlON were well-known and similar methods for layer formation had long been employed in semiconductor fabrication.

XVI. OPINIONS REGARDING GROUND 9: CLAIMS 1-2, 6-8, 10-11, 18, 30, 34, 38-39, 42-46, 49-52, 58, 67, AND 73 WERE OBVIOUS OVER HIYAMA

307. Hiyama teaches a solid-state imaging device. *Hiyama*, Abstract, ¶0273. Hiyama’s Fig. 16 (below) shows a cross-section of an individual pixel (photodiode

21, highlighted red) and associated components, having peripheral isolation elements (TRd) containing lower-refractive-index layers 501d (green) and a higher-refractive-index layer 60d (blue) surrounding the pixel:



308. There are two points of obviousness:

309. **First**, under claim 1, limitation 1[d] (“each of said pixels having at least one doped region disposed on at least one of the light incident surface and the

backside surface,”) and the similar claim limitation 18[d], it would have been obvious that layer 101 (which contacts both surfaces) was formed with p-type doping (such that the entire photodiode region 21 would be doped), because it was well-known that electron collection (as the minority carriers) is more efficient than hole collection in silicon, making this the common configuration for silicon-based image sensors. *See, e.g., Hwang-099, 5:52-6:6, Shinohara, ¶¶0058, Fig. 2, elements 23, 24, 25; Cole, ¶¶0045, Fig. 7, Mouli (Ex. 1010), 1:20-31, Hwang-584 (Ex. 1013) ¶¶0007-0008.* It also would have been obvious that the photodiode region 21 consisted of a region that was p-doped and a region that was n-doped, because this was necessary for the formation of a PN junction. *See ¶¶45-49, above.*

310. **Second**, under elements 1[f] and 18[f], a POSITA would have found it obvious to use the commonly-understood refractive indices for the materials of layers 501d and 60d (*see* ¶230, above, and ¶320, below) because equipment for depositing high quality layers of these materials are readily would have been applied with predictable results.

311. A POSITA would have had a reasonable expectation of success, because photodiodes in image sensors were commonly formed using a p-type layer having an n-type region within them, and the methods for producing such structures were well-known and predictable. *See, e.g., Hwang-099, 5:52-6:6, Shinohara, ¶¶0058, Fig. 2, elements 23, 24, 25; Cole, ¶¶0045, Fig. 7, Mouli (Ex. 1010), 1:20-31,*

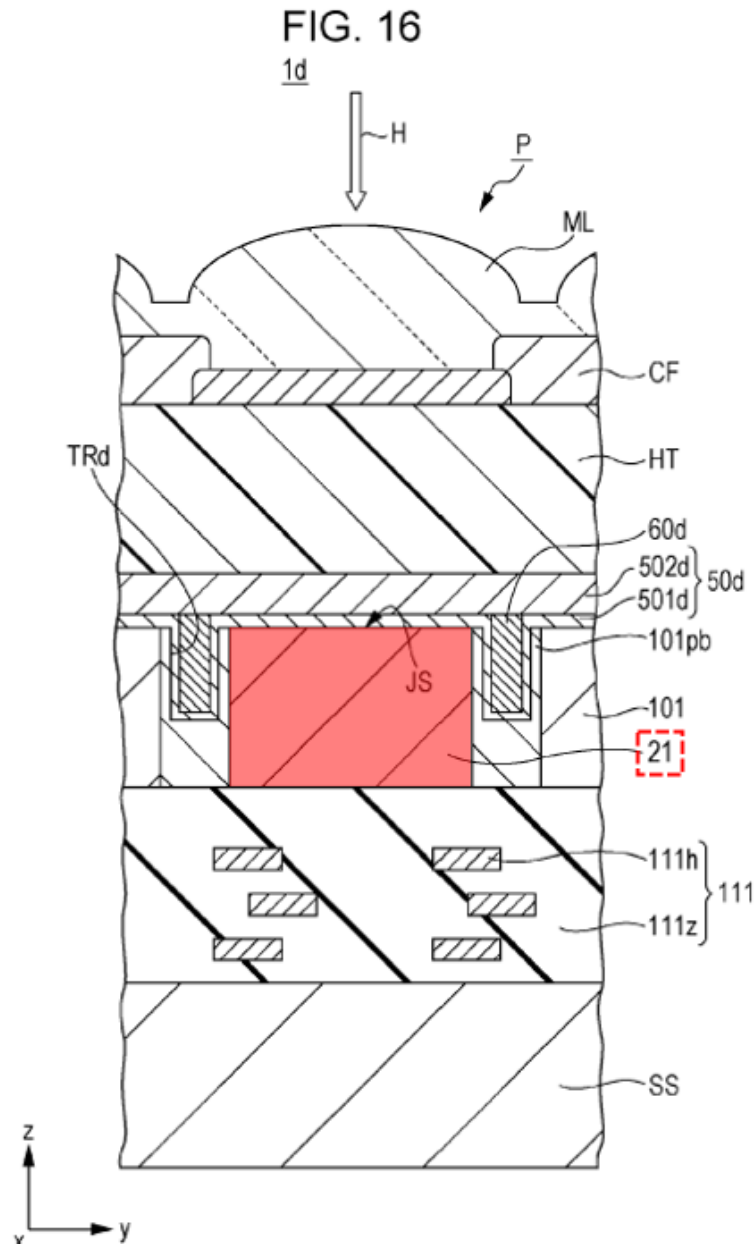
Hwang-584 (Ex. 1013) ¶¶0007-0008. A POSITA further would have had a reasonable expectation of success using the commonly-understood refractive indices for the materials in Hiyama’s filled-groove TRd, because these would have been the most typical and would have been applied with predictable results. Even if the refractive index varied somewhat from reported values, a POSITA would have reasonably expected success in achieving the claimed invention and the benefits of optical isolation, because of the relative large differences in refractive indices between these materials.

A. 1[Pre] “An imager device, comprising:”

312. Hiyama teaches an *imager device* in the form of a solid-state imaging device. *Hiyama*, Abstract, ¶0273. Hiyama’s fourth embodiment, related to Figure 16, is relevant. *Hiyama*, ¶0273. Hiyama’s fourth embodiment (Fig. 16), is based on its first embodiment, and thus the description of the first embodiment applies to Fig. 16, except as Hiyama explains. *Hiyama*, ¶0275.

B. 1[a] “at least two adjacent light sensitive image sensor **pixels”**

313. Hiyama teaches *at least two adjacent ... image sensor pixels*. *Hiyama*, ¶¶0112-0114, 0294, 0081, 0182, 0213, Fig. 2, ¶¶0094, 0177. The pixel is Hiyama’s photodiode 21, as shown with red annotations in Fig. 16:

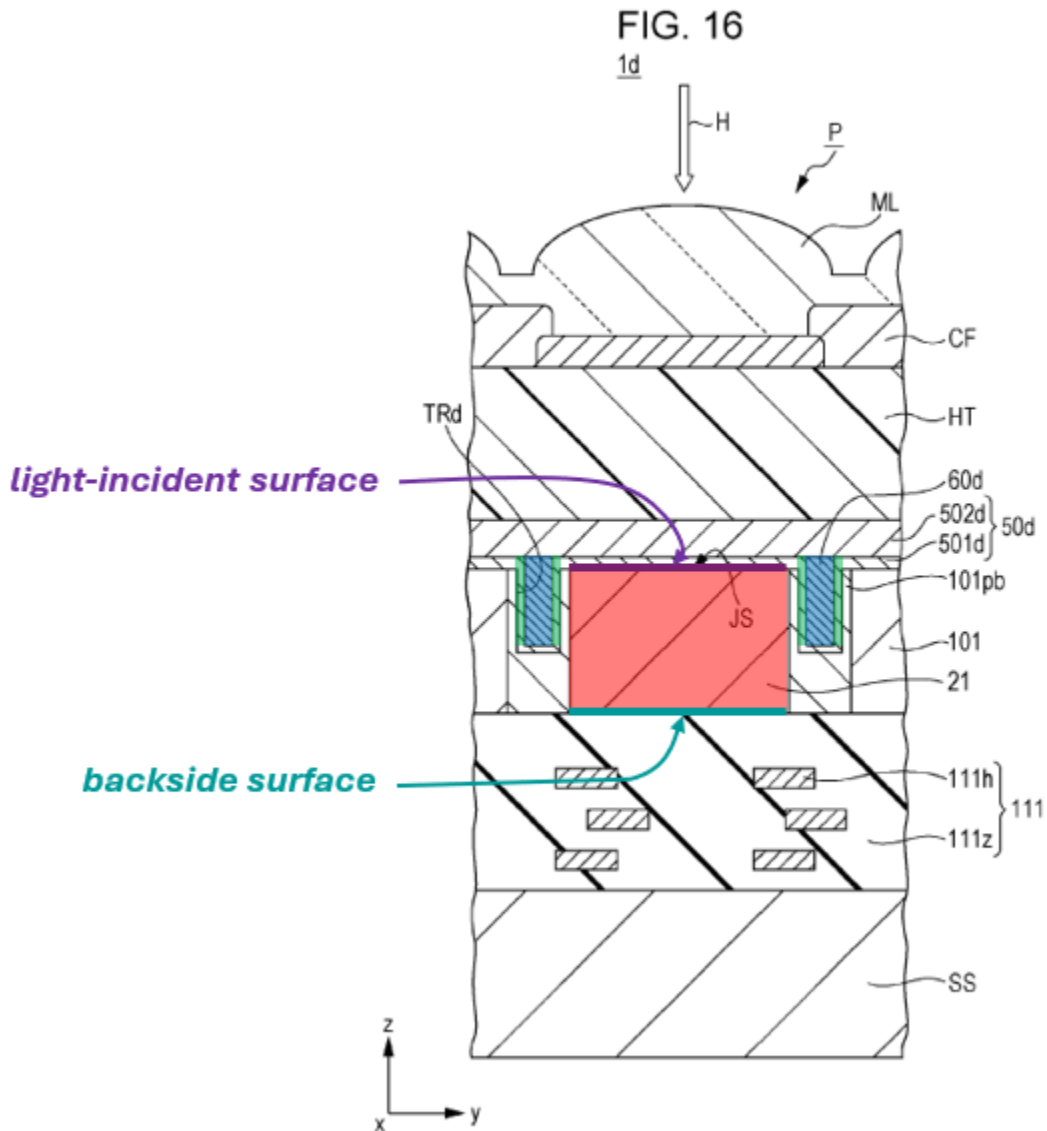


Hiyama, Fig. 16, ¶¶0075, 0112-0114.

314. The pixels are **light-sensitive**, because they are photodiodes that convert light into charge carriers. *Hiyama*, ¶0114.

C. 1[b] “each having a light incident surface, and a **backside surface** opposite the light incident surface;”

315. Each pixel has a *light incident surface*, and a *backside surface* opposite the light incident surface, as shown in Fig. 16, reproduced below with added annotations.



Hiyama, Fig. 16. In Fig. 16, “incident light H” passes through a microlens (“ML”)

and “is incident” on the “light sensing surface JS” of photodiode area 21, where it is converted to an electric signal. *Hiyama*, ¶¶0110, 0143, 0275, 0112-0114. For that reason, the surface at the top of photodiode area 21 is the *light-incident surface*, while the opposite surface is the *backside surface*.

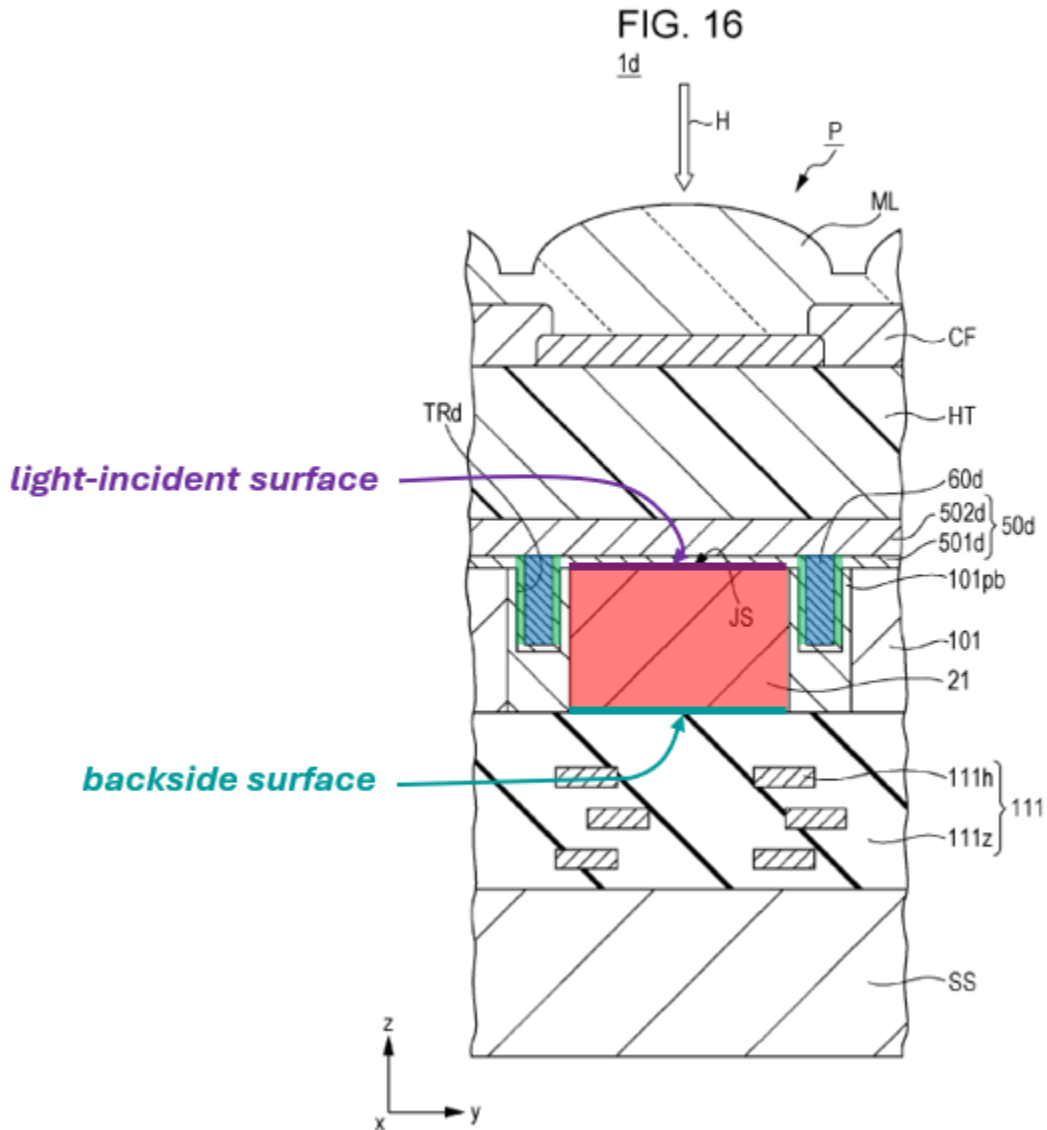
D. 1[c] “a peripheral isolation element at least partially separating said two adjacent light sensitive pixels;

316. *Hiyama* teaches a *peripheral isolation element at least partially separating said two adjacent light sensitive pixels*. Specifically, *Hiyama* teaches a groove TRd (Fig. 16, left side) that is filled with layers 501d and 60d, which is the *peripheral isolation element*. *Hiyama*, Fig. 16, ¶¶0286. The peripheral isolation element is *at least partially separating said two adjacent light sensitive pixels*, because it is formed in the “pixel separation region” 101pb of *Hiyama* (*Hiyama*, ¶¶0117, 0283-0294), which is “interposed between the plurality of pixels P” in a grid pattern. *Hiyama*, ¶0118.

317. The filled groove TRd is *peripheral* because it is located at the sides of each pixel. Further, groove TRd is an *isolation element* both because it optically and isolates neighboring pixels. *Hiyama*, ¶0294; *compare* '359 Patent, 10:20-22.

E. 1[d] “each of said **pixels** having at least one doped region disposed on at least one of the **light incident surface** and the **backside surface**,”

318. Hiyama teaches each of said pixels having at least one doped region (the photodiode 21) disposed on at least one of the *light incident surface* and the *backside surface*. *Hiyama*, ¶0117. As discussed above in ¶¶310 and 312, it would have been obvious that Hiyama’s photodiode 21 was a *doped region*. The doped region is all of layer 101 including the photodiode region 21 (shown in red in Fig. 16 below), and extends from, and thus is *disposed on*, both the *light-incident surface* to the *backside surface*:



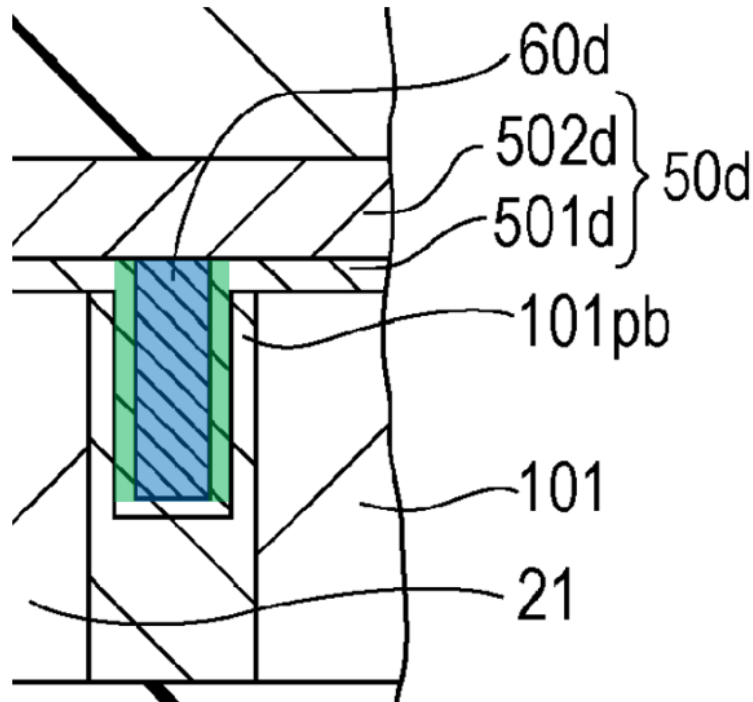
F. 1[e] “wherein the **peripheral isolation element** comprises at least two materials having different indices of refraction,”

319. Hiyama teaches that the **peripheral isolation element** (groove TRd and materials 501 and 60d) *comprises at least two materials having different indices of refraction*, specifically a high- κ dielectric such as Al_2O_3 (or HfO_2 , or Ta_2O_5) as the material of layer 501, and tungsten as the material of layer 60d. *Hiyama*, ¶¶0152,

0200. As discussed in ¶230, above, a POSITA knew that in approximately the middle of the visible spectrum, Al₂O₃ has a refractive index of approximately 1.7, HfO₂ has a refractive index of about 2, Ta₂O₅ has a refractive index of about 2, and knew that the refractive index of Tungsten was approximately 3.5 *Komuro*, Ex. 1005, ¶0137, Table I. It would have been obvious to use these standard values as I discuss above in ¶¶311-312.

- G. 1[f] “wherein said **peripheral isolation element** comprises a **first**, a **second** and a **third** layer, wherein said **third** layer is disposed between said **first** and **second** layers, and wherein each of said **first** and **second** layer exhibits an index of refraction less than an index of refraction of said **third** layer.”

320. Hiyama’s *peripheral isolation element* (groove TRd and materials 501 and 60d) has a *first*, *second* and a *third* layer, where the *first* and *second* layers are composed of the high-κ dielectric oxide of layer 501 (*e.g.*, Al₂O₃, HfO₂, or Ta₂O₅) and the *third*, middle layer is composed of Tungsten, as shown in the annotated portion of Fig. 16:



Hiyama, Fig. 16.

321. As discussed immediately above, the *first* and *second* layers (e.g. Al₂O₃, HfO₂, or Ta₂O₅) each exhibit an index of refraction (RI≈1.7, 2, and 2, respectively) less than an index of refraction of said *third* layer (Tungsten, RI≈3.5).

322. Hiyama's method of forming such *first*, *second* and *third* layers, by filling a trench with a first material 501d and then a second material 60d is similar to that of the '359 Patent, and would result in a similar layer structure to that of the '359 Patent. Compare '359 Patent, 13:12-28.

H. CLAIM 2: “The device of claim 1, wherein the index of refraction of at least one of said first and second layer is at least 0.2 lower relative to the refractive index of the third layer.”

323. As discussed above under claim 1, limitations 1[e] and 1[f], the first and second layers have an index of refraction that is at least 0.2 lower relative to the refractive index of the third layer.

I. CLAIM 6: “The device of claim 1, wherein at least one of the first and second layer comprises Al₂O₃.”

324. Hiyama teaches that the *first and second layers can comprise Al₂O₃*. *Hiyama*, ¶¶0152-0153, 0200.

J. CLAIM 7: “The device of claim 1, wherein said peripheral isolation element comprises an oxide.”

325. *See* discussion under claim 1, limitation 1[f]. *Hiyama*, ¶¶0152, 0200.

K. CLAIM 8: “The device of claim 1, wherein said peripheral isolation element provides a passivating negative charge.”

326. Hiyama teaches that “[t]he antireflection film 50J is formed by using a high dielectric having a negative fixed electric charge so that the occurrence of the dark current is suppressed”, which is a passivating negative charge, at least because it suppresses the formation of mobile electrons at the interface of the insulating layer 501d and the semiconductor layer, as I explain above in ¶232, with respect to similar fixed negative-charge structures in similar layers of Shinohara. *Hiyama*, ¶¶0078, *see also* ¶¶0143, 0216, 0250.

L. CLAIM 10: “The device of claim 1, wherein the peripheral isolation element comprises at least one material having an index of refraction of less than about 2.1.”

327. See claim 1, limitation 1[f].

M. CLAIM 11: “ The device of claim 1, wherein the peripheral isolation element comprises any of aluminum oxide and hafnium oxide.”

328. See claim 1, limitation 1[f]. *Hiyama*, ¶¶0152, 0200.

N. CLAIM 18

329. Claim 18 is nearly identical to claim 1, with three exceptions.

330. **First**, the language of claim limitation 1[d] has been moved to appear earlier in claim 18 than in claim 1, but this does not change the mapping.

331. **Second**, the language in claim limitation 1[c] has been changed as follows in claim 18: “~~at least partially~~ separating said at least two adjacent light sensitive pixels”. *Hiyama* meets the modified claim language for the same reasons explained above under claim 1, because the filled-groove TRd separates at least two adjacent pixels. *Hiyama*, ¶¶0117-0118, Fig. 16.

332. **Third**, claim 18 requires that the peripheral isolation element must “reduce optical crosstalk therebetween”, where therebetween means between pixels. *Hiyama* teaches this. *Hiyama*, ¶0294. The difference in refractive index between layers 501d and 60d (e.g. between Al_2O_3 at $\text{RI} \approx 1.7$ and Tungsten at $\text{RI} \approx 3.5$) leads to reflection of light from the filled-groove TRd back into the pixel. Specifically, the

difference in refractive index of the layers, would have produced a reflective structure, as I explain above in ¶68, that would have the effect of reflecting light incident upon the filled-groove TRd back into the pixel from which it originated.

O. CLAIMS 42 AND 49

333. Claims 42 and 49 recite at least two pixels are formed monolithically in/on a common semiconductor substrate. Hiyama teaches that its pixels are formed *monolithically in and on a common substrate*, as that term is used in the '359 patent. '359 Patent, 5:19-21; *Hiyama*, ¶0004 (“a plurality of pixels is arranged on a surface of a substrate”); *see also* ¶¶0093-0095, 0112-0113. The pixels are formed in semiconductor layer 101 and on the semiconductor substrate. *Hiyama*, ¶¶0075, 0107, 0289.

334. Claims 42 and 49 further recite that the pixels are isolated from one another by said peripheral isolation element. Hiyama teaches this, as discussed above under claim 1, limitation 1[c] and claim 18. *Hiyama*, ¶0294.

P. CLAIMS 30 AND 34

335. Claims 30 and 34 depend from claims 1 and 18, and recite the peripheral isolation element comprising tantalum oxide. Hiyama teaches this. *Hiyama*, ¶¶0152, 0200.

Q. CLAIM 38 AND 45

336. Claims 38 and 45 depend from claims 1 and 18 respectively, and recite “each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said backside surface, wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.” Hiyama teaches these claims as discussed under claim 1, limitation 1[b] (semiconductor portion 101 providing surfaces) and claim 1, limitation 1[c] (isolates the semiconductor portions of adjacent pixels). *Hiyama*, ¶0294.

R. CLAIMS 39 AND 46

337. Claims 39 and 46 recite, “said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.” As discussed above under claim 1, limitation 1[c], Hiyama teaches that filled groove TRd optically isolates adjacent pixels. *Hiyama*, ¶0294.

S. CLAIMS 43 AND 50

338. Claims 43 and 50 depend from claims 1 and 18, and recite that “said peripheral isolation element is a trench isolation element”. Hiyama teaches that this. *Hiyama*, ¶0285-0290.

T. CLAIMS 44 AND 51

339. Claims 44 and 51 depend from claims 1 and 18, and recite that the “peripheral isolation element has a width in a range from about 100 nm to about 50 microns”. Hiyama teaches that the layers 501d have a thickness of 1 to 20 nm each, while the layer 60d has a thickness of 100 to 400 nm, such that Hiyama teaches a thickness range for the filled-groove TRd of 102 to 440 nm. *Hiyama*, ¶¶0144, 0179, 0293.

U. CLAIMS 52 AND 58

340. Claims 52 and 58 depend from claims 38 and 45, and recite that the “at least one of the first layer and the second layer of said peripheral isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials”. Hiyama teaches this, because its semiconductor portions are silicon (*Hiyama*, ¶0093), but the first layer and second layer are Al₂O₃, HfO₂, or Ta₂O₅. *Hiyama*, ¶¶0152, 0200.

V. CLAIMS 64, 70

341. Claims 64 and 70 depend from claims 1 and 18, and recite that “said peripheral isolation element comprises a trench isolation element formed by filling a trench with said first, said second, and said third layers.” Hiyama teaches that its structures TRd are formed by making a groove (trench) and filling with first, second and third layers. *Hiyama*, ¶¶0288-0290.

W. CLAIMS 67 AND 73

342. Claims 67 and 73 defend from claims 1 and 18, respectively, and recite “said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.”

343. Hiyama teaches that its filled groove TRd reflects at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel. *Hiyama*, ¶0294. As I discuss above in ¶333, the difference in refractive index between layers 501d (in this instance, Al₂O₃, RI≈1.7) and 60d (RI≈3.5) leads to reflection of light from the filled-groove TRd back into the pixel.

XVII. OPINIONS REGARDING GROUND 10: CLAIMS 1, 5, 18, 23-24, 38-41, 43, 45-48, 50, 55, 68-69, 74-75, AND 80-83 WERE OBVIOUS OVER HIYAMA AND COLE.

344. The above-referenced claims were obvious over Hiyama (as applied in Ground 9) and Cole (*see* Ground 3).

345. There are two principal obviousness contentions. First, as discussed above under ¶310, it would have been obvious to form layer 101 containing photodiode 21 to be formed with p-type doping and an internal n-type region, as was commonly-known in the art. Cole provides additional motivation for this, because Cole’s pixel is formed in this well-known manner, with “a p-type surface layer 424

and an n-type photodiode region 426'' (Cole, ¶0045), as shown as red and blue regions in Fig. 7, reproduced here:

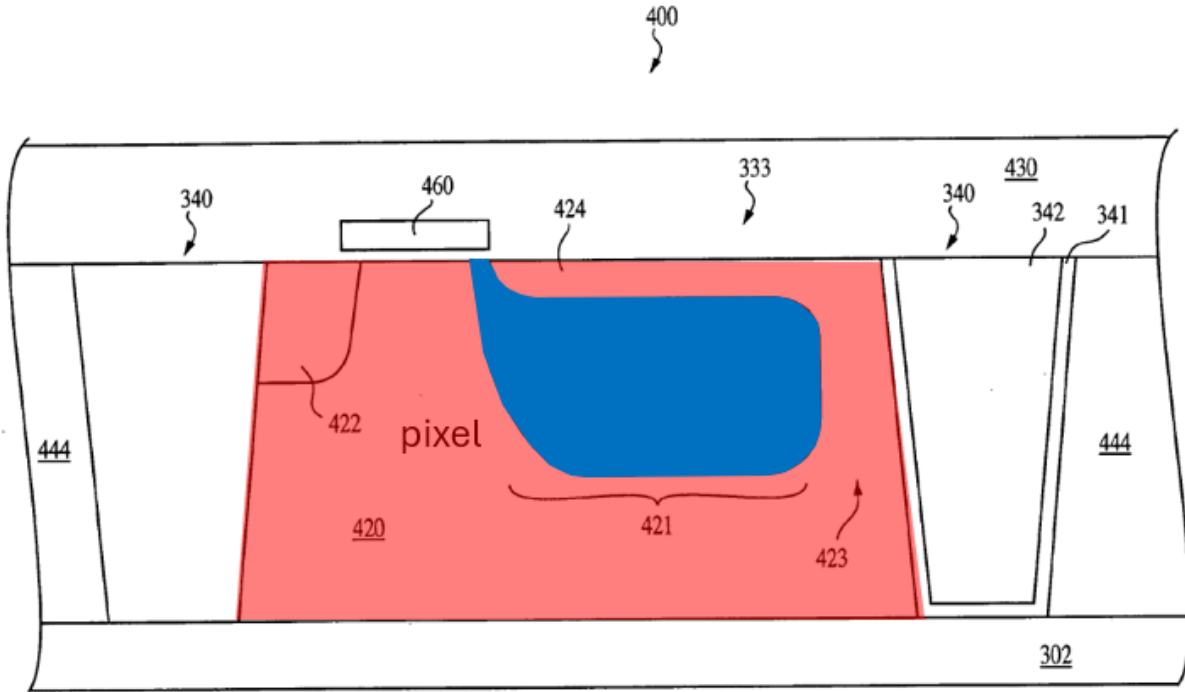


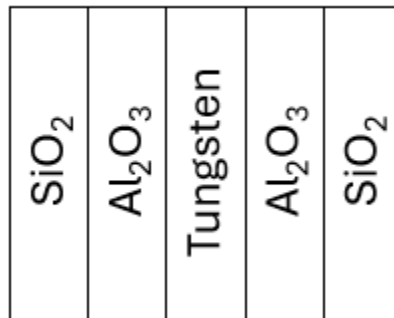
FIG. 7

Cole, Fig. 7, ¶0045.

346. Second, as discussed in ¶¶320-323, Hiyama teaches a pixel structure with peripheral isolation elements comprising a middle Tungsten layer and outer layers of Al_2O_3 , HfO_2 , or Ta_2O_5 , separating pixel photodiodes that are formed in silicon. To help prevent chemical reaction between silicon and peripheral isolation structure material, Cole teaches that it is useful to add outer thermal oxide (SiO_2) layers to the isolation structure. Cole, Abstract, ¶0039. Cole further teaches that

such outer SiO₂ layers “provid[e] an additional barrier to electrons”, meaning that they improve resistance to electrical crosstalk. *Cole*, ¶0035.

347. When using an outer thermal oxide (SiO₂) with the filled-groove structure TRd of Hiyama, the layer ordering of Hiyama’s filled groove TRd would be:



348. With this peripheral isolation structure, the core of Hiyama’s filled groove TRd (Al₂O₃ - Tungsten - Al₂O₃) remains the same. Specifically, the Al₂O₃ layers are still the “first” and “third” layers of claims 1 and 18, and the Tungsten layer is still the “second” layer (I note that certain dependent claims, below, provide for alternative mappings). This ground would add SiO₂ layers on the outside of Al₂O₃ layers of Hiyama, adjacent to the pixels, which would have been obvious for the reasons provided above.

349. *Cole* further motivates the combination with its embodiment of Fig. 6, in which a five-layer isolation structure is used, as shown here:

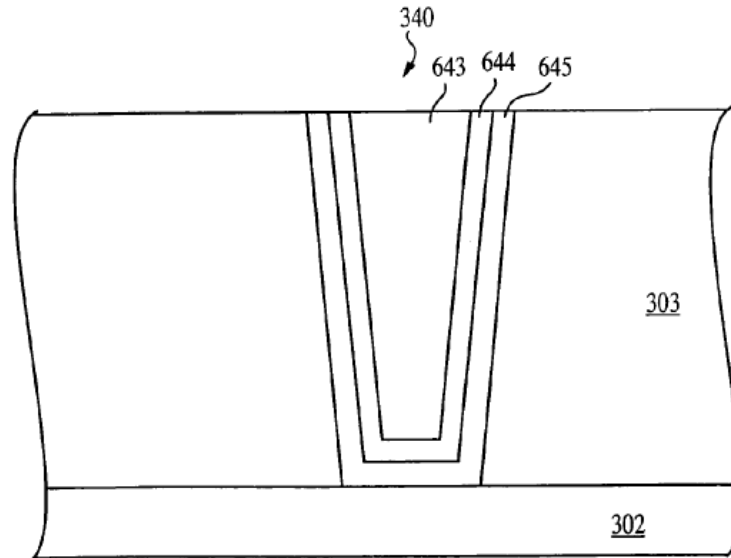


FIG. 6

Cole, Fig. 6, ¶0042. The five-layer structure uses three materials with different refractive indices, such that light is reflected away. *Cole* explains:

“FIG. 6 depicts trench 340 containing three materials 643, 644, and 645. **Materials 643, 644, and 645 have different refractive indices.** Based on the refractive indices of materials 643, 644, and 645, the layering structure of materials 643, 644, and 645 is **configured such that photons** entering the trench from peripheral circuitry (FIG. 3) **will be reflected away** from array 333. Illustratively, **material 643 has a greater refractive index than material 644, which in turn has a greater refractive index than material 645.**”

Cole, ¶0042 (Emphasis added).

350. A POSITA would have been motivated to provide for a thermal oxide (SiO_2 formed by oxidation at elevated temperature), as recommended by *Cole* (*Cole*, Abstract, ¶0039), as the outside layers of Hiyama’s isolation structure. Because both

Hiyama and Cole are formed in silicon (*Hiyama*, ¶0093; *Cole*, ¶0034), the thermal oxide would be oxidized silicon (SiO_2). Using outer SiO_2 layers would have improved electrical isolation, protected the interior materials from chemical reaction (*Cole*, ¶¶0035, 0039), and implemented Cole’s recommendation to configure a five-layer isolation structure with three materials having different refractive indices in order to reflect light, where the refractive indices are highest in the middle (Tungsten, $n=3.5$), next-highest in the Al_2O_3 layers ($n=1.7$), and lowest in the outer, SiO_2 layers ($n=1.45$). *See* ¶320, above; *Cole*, ¶0042.

351. A POSITA would have found this arrangement of Hiyama’s filled groove TRd obvious because of the expected advantages discussed by Cole, namely the protection of interior layers against chemical reaction, the increase in electrical insulation, and the ability to reflect away light by exploiting the refractive index difference of the layers, according to Cole’s statement that it is “advantageous to provide both electrical and optical isolation between pixels”, and that “image sensor pixels must be isolated from one another to avoid pixel cross talk.” *Cole*, ¶¶0005, 0035, 0039, 0045. A POSITA would have reasonably expected success in using SiO_2 in the outer layer to achieve the expected benefits, because SiO_2 was the most-commonly used oxide in semiconductor fabrication and was known to have excellent electrically insulating properties. *See* ¶190, above.

A. CLAIMS 1 AND 18

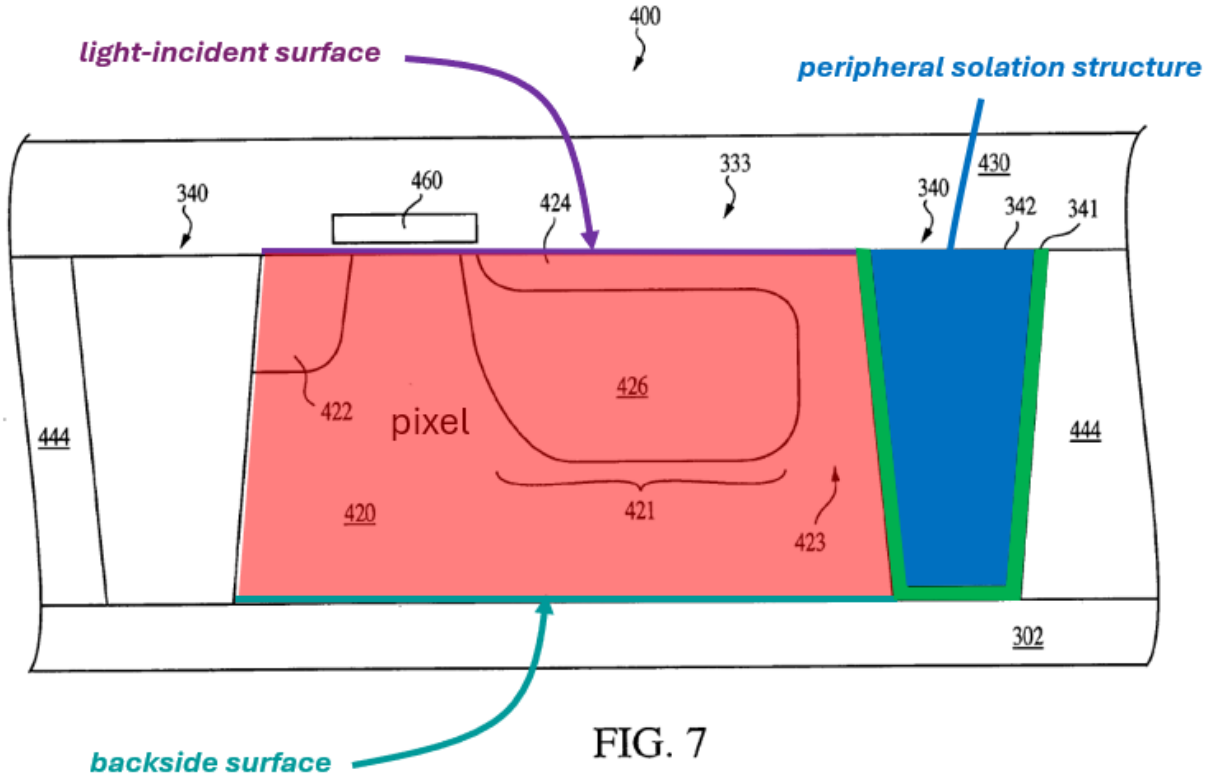
352. The combination meets claims 1 and 18 in the same manner discussed in Ground 9 (i.e., with an unaltered layer structure in Hiyama), with the exception that Cole provides further motivation for Ground 9’s obviousness analysis (¶310) with respect to the doping of Hiyama’s photodiode 21

B. ISOLATION CLAIMS 5, 23, 38-40, 43, 45-47, 50, 68-69, 74-75

353. These claims require that the peripheral isolation element provide “isolation” generally (38, 45), a “trench” isolation element (43, 50), optical isolation (39, 46, 68, 74), and/or electrical isolation (40, 47, 69, 75). Claims 5 and 23, furthermore, require the peripheral isolation element to “extends substantially from the light incident surface to the backside surface”.

354. These claims would also have been obvious over Hiyama and Cole for similar reasons as Hwang-099 and Cole. See ¶¶217-219, above. Cole teaches that “it is advantageous to provide both electrical and optical isolation between pixels” in order to prevent color mixing (Cole, ¶0005), and this goal applies equally to Hiyama. Hiyama, ¶0295. Cole further teaches methods for achieving optical and electrical isolation, specifically by forming a “trench” isolation structure (Cole, ¶0030) that extends entirely through the epitaxial layer (the layer where the

photodiode is formed) to the base layer *Cole*, ¶0034), as shown in Fig. 7, reproduced again here:



Cole, Fig. 7, ¶0044. The trench includes “a thermal oxide” that is “grown in trench 340 prior to deposition of material 341, providing an additional barrier to electrons.” *Cole*, ¶0035.

355. A POSITA would have been motivated based on these teachings to form Hiyama’s filled-groove TRd from the light-incident surface to the backside surface, and to ensure that it provides sufficient isolation. It would further have been obvious based on *Cole* to use a trench isolation structure to separate pixels that is sufficiently deep and sufficiently insulating “to provide both electrical and optical

isolation between pixels”. *Cole*, ¶0005. A POSITA would have had a reasonable expectation of success in so doing for the reasons discussed above in ¶219, including for the expected benefits of reducing optical and electrical crosstalk.

C. CLAIM 24

“24. The device of claim 18, wherein said at least two materials comprises silicon dioxide and aluminum oxide.”

356. The modified Hiyama structure renders claim 24 obvious. As discussed above in ¶¶347-352, the modified Hiyama structure would comprise both silicon dioxide (SiO_2 , $\text{RI} \approx 1.46$, *Hwang-099*, 9:28-30) and aluminum oxide (Al_2O_3 , $\text{RI} \approx 1.7$ see ¶230, above), which are materials with different refractive indices. The “thin” thermal oxide layer (*Cole*, ¶0039) would not have been expected to interfere with the negative-fixed charge of the Aluminum Oxide layer. A POSITA would have known to grow the thermal oxide thick enough such that it would contribute to the optical isolation function of Hiyama’s filled groove structure TRd.

357. I note that in Ground 9, for the independent claims, the “two materials” are Tungsten and an oxide layer, such as Al_2O_3 . See, e.g., ¶320, above, discussing claim 1, limitation 1[e]. Here, the two materials are SiO_2 and Al_2O_3 . This change, however, has no other effect on the mapping of the Hiyama reference to the independent claims.

D. CLAIMS 41 AND 48

358. Claims 41 and 48 depend from claims 38 and 47 respectively, and additionally recite that “an index of refraction of the semiconductor portion of each of said at least two adjacent image sensor pixels is different from indices of refraction of said layers of the peripheral isolation element such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.”

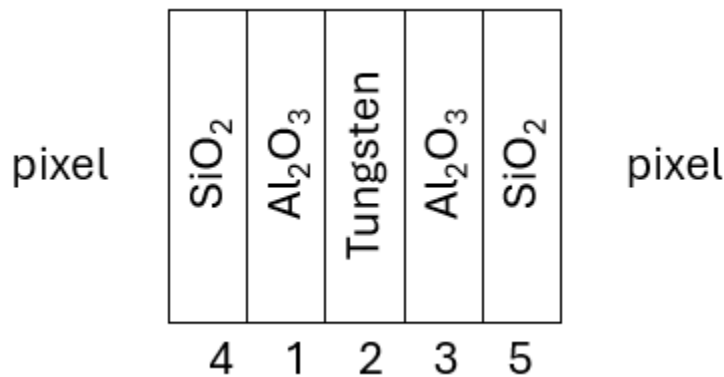
359. Hiyama teaches that the semiconductor portion 101 of the pixels is single-crystal silicon with a refractive index of approximately 3.6. *Hiyama*, ¶¶0093, 0217. The layers of the peripheral isolation element, in contrast, are Tungsten, Al₂O₃, and SiO₂, with refractive indices of approximately 3.5, 1.7, and 1.45, respectively. *See* ¶¶311, 320, and 230, above. Thus, the layers of the isolation element are different materials from the semiconductor portions of the pixels, and the refractive indices of the semiconductor portion is different from each of the layers. As taught by Cole, this arrangement of layers with different refractive indices, highest in the middle and lowest at the outsides, difference would cause a reflective surface resulting in optical isolation. *Cole*, ¶0042.

E. CLAIMS 55, 61, 80-83

360. Claims 55 and 61 depend from claims 1 and 18, respectively, and further recite that “the peripheral isolation element comprises more than three

layers”. Claims 80 and 82 depend from claims 1 and 18, respectively, and further recite that “the peripheral isolation element comprises five layers”. As discussed above, the modified Hiyama groove TRd would contain five layers.

361. Claims 81 and 83 depend from claims 80 and 82, respectively, and further recite that “the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second layer and the other one of said adjacent pixels.” In the modified Hiyama groove TRd, the first and third layers are Al_2O_3 while the second layer is Tungsten, as explained above under Grounds 7 and 8. The fourth and fifth layers, which are outside layers and thus between disposed between the [first/second] layer and one of said adjacent pixels are the SiO_2 layers, as shown in the illustration below.



XVIII. OPINIONS REGARDING GROUND 11: CLAIM 9 WAS OBVIOUS OVER HIYAMA AND WERNER

362. Claim 9 was obvious over Hiyama as discussed in XVII and Werner (Ex. 1067).

363. Claim 9 recites “[t]he device of claim 1, wherein said peripheral isolation element exhibits a surface recombination velocity as low as 10 cm/s.”

364. Surface recombination velocity (“SRV”) is a measure of the rate at which charge carriers recombine at a surface. This rate tends to be higher at the interface between two different materials, because where the materials meet, there can be defects creating interface states that make recombination more efficient. When charge-carrier recombination occurs, charge carriers that would otherwise be measured as an analog to incoming light will be rendered immobile, which in turn lowers the accuracy of the image sensor. Thus, lowering surface recombination velocity was desirable.

365. Hiyama has a material interface with the potential for defects where Hiyama’s filled-groove TRd contacts Hiyama’s silicon layer 101. As discussed above in ¶¶320-323, Hiyama teaches a peripheral isolation element that has outer layers 501d made from Al₂O₃. *Hiyama*, ¶¶0150-0152, 0200. The Al₂O₃ is deposited using Atomic Layer Deposition (ALD) *Hiyama*, ¶0196, 0218), and once deposited, forms an interface with the single-crystal silicon of layer 101. *Hiyama*, ¶0093.

366. Werner is a technical journal article that teaches using ALD to produce Al₂O₃ layers with a high negative fixed charge density of on single-crystal silicon (c-Si) to achieve surface recombination velocities of under 10 cm/s. *Werner*, Abstract, pp. 001-003, Fig. 4.

367. A POSITA would have been motivated to apply Werner in the Fig. 16 embodiment of Hiyama, to produce Al₂O₃ layers (layers 501d) with high negative fixed-charge densities and low SRVs (*e.g.* 10 cm/s). Hiyama already uses Al₂O₃ in contact with c-Si produced by ALD, and having negative fixed charges. *Hiyama*, ¶¶0143, 0150-0152, 0200, 0216, 0250. Werner demonstrates that low SRVs can be “routinely” achieved using similar techniques (*Werner*, p. 003, Abstract), and a POSITA would have found the application of those techniques obvious, and would reasonably have expected success in producing SRVs as low as 10 cm/s and thereby improving image sensor accuracy. I note that the ’359 patent implicitly relies on the prior art to produce Al₂O₃ layers with low SRVs. *’359 Patent*, 9:57-60.

XIX. CONCLUSION

1. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.



Dated: 4/16/2025

By: _____

Appendix A

Stanley Shanfield



Curriculum Vitae for Stanley Shanfield

Education:

Massachusetts Institute of Technology, Ph.D., Physics, 1981

University of California, Irvine, B.S. Cum Laude, Physics, 1977

Educational Awards:

Outstanding Research Project, U.C. Regents Award, 1977

Phi Beta Kappa, 1977

Four Year Scholarship, Tuition & Research, ERDA/DOE, 1977-1981

Hands-On Professional Expertise:

Semiconductor Physics & Chemistry
Semiconductor Fabrication: Silicon and III-V Materials
Semiconductor Device & Integrated Circuit Engineering
Semiconductor Equipment: Front & Back End
Semiconductor Packaging Design and Manufacturing
Passive Component Design and Manufacturing
RF Design and Fabrication
Digital Design & Fabrication
Semiconductor Manufacturing in Silicon and III-V Materials
MEMS Design and Fabrication: Electrical, Optical, & Sensing Devices
Fiber Optic Device Design and Fabrication
Integrated Optics & Electro-Optical Devices
Plasma Physics

Specialized Training:

Global Positioning Electronics, Systems and Components
Six Sigma Semiconductor Manufacturing
Microwave Engineering
US Patent Law in Technology
Patent Application and Prosecution
Semiconductor Plasma Processing
Thin Film Physics and Technology
MEMS-based Gyroscopes and Accelerometers
Thermoelectric Materials & Technology
Phased Array Radar Engineering
Antennas and Electromagnetic Propagation
Solid State Optical Devices
Fiber Optic Communication System Operation
HALT and HAST Reliability Testing Methods

Professional Experience:

Draper Laboratory Cambridge, MA

2003 – present

Division Leader, Advanced Hardware Development Distinguished Member of Technical Staff Technical Director

Led division (about 80 staff) in re-invigorating multi-chip integrated circuit module facility, more than doubling associated revenues in two years. By most accounts, made division a viable business & technological entity again. Invented & led implementation of an ultra-miniature electronics fabrication technology which became a top laboratory priority. Led team in realization & fabrication of a newly designed precision MEMS-based gyroscope and associated ASIC. Found funding and led team in developing a miniature power source with energy density at least two orders of magnitude higher than any source previously built. Developed fabrication technology for semiconductor-based low phase noise oscillator design, allowing for receiver operation with extremely low signal strength. Many awards received, most recently, the Draper 2010 Distinguished Performance Award, and 2010 Best Patent Award.

Clarendon Photonics Newton, MA

2001 – 2003

Director, Packaging & Integration

30 person photonic chip startup with \$18 million 2nd round funding. Invented and productized new, low cost and reliable semiconductor processing, packaging and pig-tailing technology for optical add-drop multiplexer. Established assembly and packaging process, and developed control electronics. Partner with Micron Technologies, using their R&D semiconductor facility.

AXSUN Technologies Bedford/Billerica, MA

1999 – 2001

Vice President, Operations 1999 – 2000

Initially three staff members with \$6 million funding. Designed, fabricated and productized AXSUN's micro-electromechanical (MEM) Fabry-Perot optical filter. Patents granted on semiconductor processing and control electronics. Completed facility and semiconductor processing design, then completely equipped. Raised 2nd round funding for \$36 million. Established process and fabrication facility in Belfast, Northern Ireland for producing thick oxide silicon-on-insulator material.

Director, Manufacturing & Wafer Fab Technology

2000 – 2001

After 3rd round funding, led device manufacturing, creating wafer fab and assembly infrastructure; hired 70+ people, led production. Delivered first generation product for revenue to multiple customers. Converted pure technology to dominant company revenue with high yield.

Company purchased by Volcano Technologies, San Diego.

Raytheon Corporation Lexington/Andover, MA

1985 - 1999

Manager, Semiconductor Operations

1996 – 1999

Built and led a 300 employee, \$60 million revenue 24/7 semiconductor development and manufacturing operation resulting from the consolidation of a number of smaller organizations. Key player in technological development and recipient of Raytheon's 6 Sigma Leadership training. Decision maker in Texas Instrument group acquisition, providing significant expert opinion on semiconductor and design facilities. Obtained state-of-art yields using best available steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for-steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for-manufacturing circuit design and layout methodology.

Research Laboratory Manager

1992 – 1996

Leader of a 90 employee development and contract research organization in high performance semiconductor devices and circuits, measurement, assembly and wafer fab. Led a team which invented and implemented a major revenue generating technology (\$.100 million) based on semiconductor device development (pseudomorphic high electron mobility transistor). Increased outside research funding by 50% in 3 years through superior technical performance relative to competitors.

Section Manager, Semiconductors & ICs

1985 – 1992

Led a MM-Wave Circuit and Module Development program over 2 years, leading to production win of a satellite terminal electronics generating \$320 million in sales. Developed processes for fabricating high power, high frequency multi-function integrated circuits, and combining high performance digital and analog devices in a single integrated circuit.

Spire Corporation Bedford, MA

1981 – 1984

**Staff Scientist
Senior Staff Scientist**

Developed new methods for low temperature deposition of plasma-assisted CVD epitaxial silicon. Wrote joint papers with MIT professor, and had process adopted by equipment manufacturers. Built, operated and characterized ion-assisted deposition system for making coating for semiconductor and machine tool industries. Process eventually purchased by Kennametal, Inc.

Publications

Restricted Publications & Reports

Process Sequence for Formation of Ultra-High Density Multi-Chip Modules:

A high yield, low cost method for creating a system-in-a-package consisting of numerous semiconductor die, passive components, and sensors. Process formed basis for new (2008) facility.

Design and Method of Fabrication of Ultra-High Density Radioisotope Power Source:

In test, a miniature power source that achieves energy density more than 1000X the best chemical battery. Method uses planar semiconductor processing of bulk thermoelectric materials.

Design and Method of Achieving Extremely Low Crystal Oscillator Phase Noise:

Method developed for very low power refrigeration of quartz or sapphire crystal resonators, resulting in extremely low phase noise oscillators. The low phase noise allows extremely high sensitivity in digital receivers, including GPS receivers, leading to use in extremely low signal conditions.

Design, Evaluation & Production of MEMS-based Fabry-Perot Interferometer:

Design and method for ultra-compact spectral analyzer made using semiconductor and optical thin film processing.

Design & Evaluation of Ultra-Fast Control Electronics for Integrated Optical Multiplexer:

Design and performance evaluation of silicon-based integrated optical multiplexer using chip-based local heating

Design and Fabrication of Q-band MILSTAR Communications Terminal Transmitter:

Record power and efficiency 44 GHz transmitter design using new transistor design, and combined waveguide

Key Publications (selected)

Process Characterization of PSG and BPSG Plasma Deposition, J. Electrochem. Soc., Volume 131, Issue 9, pp. 2202-2203

A double-recessed Al_{0.24}GaAs/In_{0.16}GaAs pseudomorphic HEMT for Ka- and Q-band power Applications, Electron Device Letters, IEEE, Volume 14, Issue 9, pp. 456 - 458

Formation of Thick Metal Structures on GaAs MMICs Using Image Reversal Lithography and Evaporated Metal Deposition, J. Electrochem. Soc., Volume 136, Issue 9, pp. 2687-2690

Contact Hole Etching in Load-Locked Hexagonal Reactive Ion Etch System, J. Electrochem. Soc., Vol. 131, No. 8, 1984

An AlGaAs/InGaAs pseudomorphic high electron mobility transistor with Improved Breakdown Voltage for X and Ku-band power applications, Microwave Theory and Techniques, IEEE Transactions on, Volume 41, Issue 5, May 1993, pp. 752 - 759

Hot-electron-induced Degradation of Metal-Semiconductor Field-Effect Transistors, Integrated Circuit Symposium, 1994. Technical Digest 1994., 16th Annual Volume , Issue , 16-19 Oct. 1994, pp. 259

Ion Beam Deposition of Cubic Boron Nitride, J. Vac. Sci. Technol. A Volume 1, Issue 2, pp. 323-325

Patents**US Patent 6504235 - Passivation layer and process for semiconductor devices**

Method of coating semiconductor devices that prevented parametric shift in electrical performance. Solved key processing problem.

US Patent 4440108 - Ion Beam Deposition Apparatus

Design of equipment for deposition of thin films in the presence of ion bombardment. System produced thin films of interest for mechanical, electrical and optical properties and was sold as an equipment product.

US Patent 6525880 - Integrated Tunable Fabry-Perot filter and Method of Making Same

Design and method for fabricating very small, very high performance variable optical filter using semiconductor fabrication technology. In current use in fiber optical networks, chemical sensors, and 3-D medical imaging applications.

US Patent 5175020 - Boron Nitride Films and Process of Making Same

Ion assisted deposition of ultra-hard cubic boron nitride films for semiconductor and machine tool applications. Significant use in both areas.

US Patent 4526673 - Coating Method

Method for deposition of thin films used in semiconductor device fabrication. Method based on direct control of the kinetics of thin film deposition.

US Patent 7727806 - Systems and Methods for High Density Multi-Component Modules

Method for fabrication of electronic modules using multiple thinned integrated circuits, patterned multi-level interconnects, passive electronic components, and sensors

US Patent Application 2009/TBD - Devices, systems, and methods for controlling the temperature of resonant elements

Devices and systems for achieving low phase noise crystal oscillators using unique low power thermoelectric structures

Expert Witness Experience:

See attachment

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