

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Apple Inc. and Sony Group Corporation,
Petitioners

v.

SiOnyx LLC,
(record) Patent Owner

Inter Partes Review Case No. IPR2025-00845
U.S. Patent No. 10,224,359

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,224,359**

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I. INTRODUCTION

IPR is requested of Claims 1-83 of USPN 10,224,359. As shown, independent claims 1 and 18 are anticipated by Hwang-099 (Ground 1) and additionally rendered obvious by Hiyama alone (Ground 9).

II. LEVEL OF SKILL OF A POSITA

For purposes of this IPR, Petitioners apply SiOnyx’s proposed level of skill, namely having “at least a bachelor’s degree in electrical engineering, materials science, or physics (or an equivalent degree), at least two years of experience in optoelectronics, and at least three years of work experience in semiconductor manufacturing...[A] master’s degree or Ph.D. in a relevant field may substitute for some work experience or vice versa.” Ex. 1014, 20.

III. REQUIREMENTS UNDER 37 C.F.R. §42.104

A. Grounds for Standing Under 37 C.F.R. §42.104(a)

Petitioners certify the ’359 Patent is eligible for IPR.

B. Identification of Challenge Under 37 C.F.R. §42.104(b)

Claims 1-83 are unpatentable over the following prior art and Grounds:

Reference	Name	Exhibit	Prior art date	Cited on ’359 patent?
USPN 7,675,099	Hwang-099	1004	3/9/2010 102(b)	NO
US Pub. 2011/0241148	Hiyama	1066	3/24/2011 102(e) 10/6/2011 102(a)	YES

Werner, et al.	Werner	1067	2010 102(b) ¹	NO
US Pub. 2012/0033119	Shinohara	1068	8/2/2011 102(e) 2/9/2012 102(a)	NO
PCT Pub. WO2011/160130	Carey	1069	6/18/2010 102(e) 12/22/2011 102(a)	NO
JPH06-244444	Uematsu	1070	9/2/1994 102(b)	YES
US Pub. 2006/0286766	Cole	1071	12/21/2006 102(b)	YES
USPN 6,395,650	Callegari	1074	5/28/2002 102(b)	NO
US Pub. 2008/0121962	Forbes	1075	5/29/2008 102(b)	NO

¹ Werner published in APPLIED PHYSICS LETTERS, Volume 97, Issue 16 dated October 18, 2010. *See Werner*. Werner was publicly accessible before the critical date of the '359 patent at least because Werner was indexed and shelved in the Penn State University Library in October 2010. Munford Dec. (Ex. 1073), ¶9.

Ground	Grounds of Unpatentability
1	Claims 1-4, 7, 10, 18, 38-40, 42-47, 49-52, 56-58, 62-63, 67-69, and 73-75 are anticipated by Hwang-099.
2	Claims 1-5, 7, 10, 18, 23, 38-40, 42-47, 49-64, 67-70, 73-75, and 80-83 were obvious over Hwang-099.
3	Claims 5, 23, 38-40, 43, 45-47, 50, 65-66, 68-69, 71-72, and 74-75 were obvious over Hwang-099 and Cole.
4	Claims 6, 8, 11, 24, 30, 32, 34, 36, 53-54, 59-60, 80 and 82 were obvious over Hwang-099 and Shinohara.
5	Claims 12-17, 19-22, 25-29, 65-66, 71-72, and 76-79 were obvious over Hwang-099 and Carey.
6	Claims 12-17, 19-22, 25, 27, and 29 were obvious over Hwang-099 and Uematsu.
7	Claims 30, 32-34, and 36-37 were obvious over Hwang-099 and Callegari.
8	Claims 30-31 and 34-35 were obvious over Hwang-099 and Forbes.
9	Claims 1-2, 6-8, 10-11, 18, 30, 34, 38-39, 42-46, 49-52, 58, 64, 67, 70 and 73 were obvious over Hiyama.
10	Claims 1, 5, 18, 23-24, 38-41, 43, 45-48, 50, 55, 61, 68-69, 74-75, and 80-83 were obvious over Hiyama and Cole.
11	Claim 9 was obvious over Hiyama and Werner.

C. Claim Construction Under 37 C.F.R. §42.104(b)(3)

Petitioners do not believe claim construction is necessary to apply the claims to the present prior art.² In Samsung's co-pending ITC investigation, the ITC issued an Order construing certain claim terms. Ex. 1014.

IV. ANALOGOUS ART

The prior art is analogous, because it is in the same field as the '359 Patent, namely semiconductor devices for detecting light. '359 Patent, 6:48-52, 7:64-66; *Hwang-099*, Abstract; *Hiyama*, ¶¶0002; *Shinohara*, Title, ¶¶0092-0095; *Carey*, Abstract, Title; *Uematsu*, Title, Abstract; *Cole*, Title, Abstract; *Callegari*, 6:5-16; *Werner*, Abstract; *Forbes*, Abstract, ¶¶0003-004; *Dec.*, ¶¶76-123.

The prior art is also reasonably pertinent to at least one problem facing the '359 Patent's inventors, namely the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light. '359 Patent, 1:24-37, 6:13-25; *Hwang-099*, 10:19-40; *Hiyama*, ¶¶0294-0295; *Werner*, Abstract; *Shinohara*, ¶¶0092-0095; *Carey*, 022:2-14, 026:14-34; *Uematsu*, Title, Abstract; *Cole*, ¶¶0005, 0042; *Callegari*, Title, Abstract, 6:5-16, 7:1-31; *Forbes*, Abstract, ¶¶0033, 0103; *Dec.*, ¶¶76-123.

² Petitioners' application of prior art to the Challenged Claims is not a waiver of any argument in litigation regarding a claim term's construction or indefiniteness.

**V. DETAILED EXPLANATION OF THE REASONS FOR
UNPATENTABILITY**

**Ground 1. Claims 1-4, 7, 10, 18, 38-40, 42-47, 49-52, 56-58, 62-63, 67-69, and
73-75 are anticipated by Hwang-099**

CLAIM 1

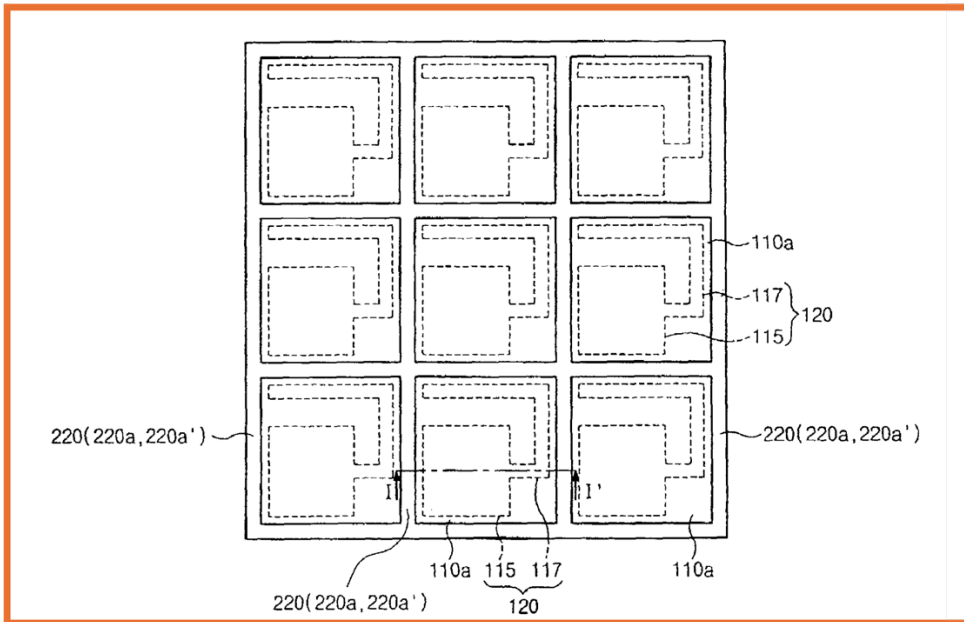
1[Pre] “An imager device, comprising:”

Hwang-099 (Ex. 1004) teaches an *imager device*³ in the form of an image sensor, as shown, *e.g.*, in Fig. 1. *Hwang-099*, Title, 1:14-18, Fig. 1; *Dec.*, ¶¶125-126.

³ Claim language provided in italics. All drawing annotations added. Claim language in colored font maps to same-colored regions in the annotated drawings. Citations to a claim limitation and/or section number are to the limitation’s mapping in this Petition and are incorporated by reference, including the Motivations to Combine (MTC) and showing of reasonable expectation of success (REOS) provided in the cross-referenced section. All REOS include the benefits described for the respective MTC. All emphases added unless otherwise noted.

Imager Device

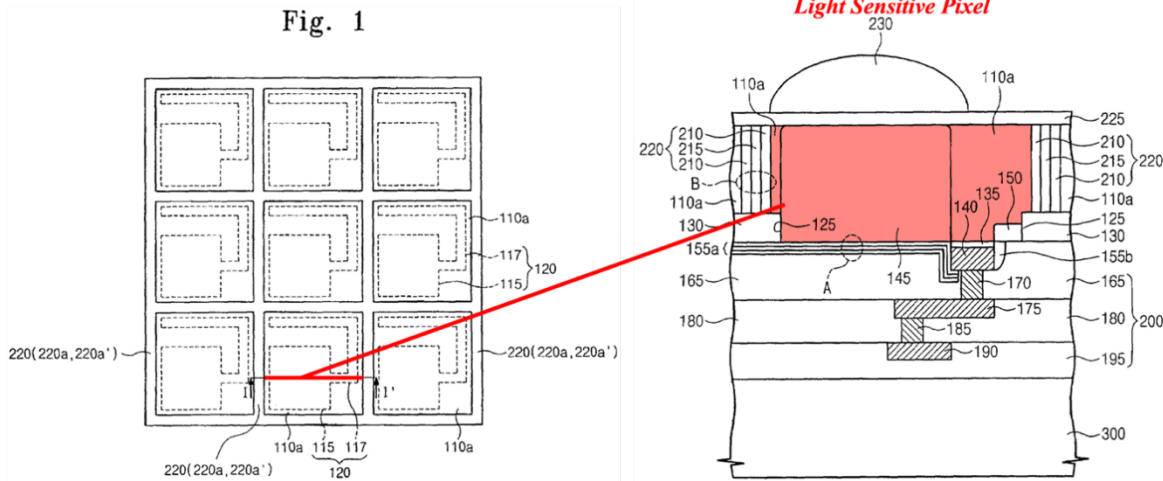
Fig. 1



Dec., ¶126.

*1[a] “at least two adjacent light sensitive image sensor **pixels**”*

Hwang-099 teaches *at least two adjacent light sensitive image sensor **pixels***, namely at least the portion comprising pixel semiconductor patterns 110a and photodiodes 145 formed therein, shown in annotated Figs. 1-2:

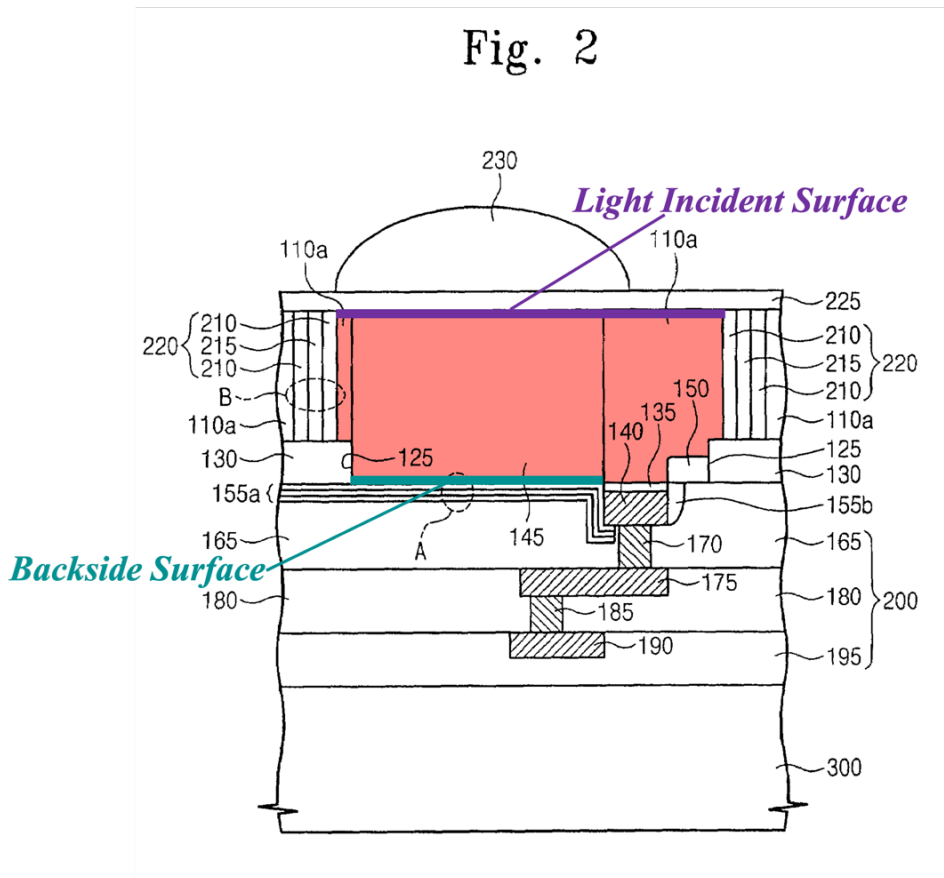


Dec., ¶127. Fig. 1’s image sensor comprises a plurality of pixel semiconductor patterns 110a arranged two-dimensionally in rows/columns; each pattern 110a has a photodiode 145 disposed therein. *Hwang-099*, Figs. 1-2, 5:47-58. Each pixel is a light-sensitive image sensor pixel because it allows collection of electron-hole pairs generated by absorbed light, thus converting light into an electrical signal. *Hwang-099*, 5:52–6:4, 1:23-29, 10:36-40, 1:52-54, 1:14-29; Dec., ¶¶127-128. There are at least two adjacent light sensitive image sensor pixels as shown in Fig. 1. Dec., ¶¶128-133. Pixel semiconductor pattern 110a is a part of a pixel. *Hwang-099*, 5:52-57; Dec., ¶¶128-133. *Hwang-099* calls 110a “pixel semiconductor patterns” and teaches that pixel semiconductor patterns 110a are separated by a reflection layer 220 to minimize incident light on “neighboring pixels”. *Hwang-099*, 10:28-40, 15:42-48; Dec., ¶¶128-133. Layer 220 completely separates the pixels because layer 220 “surround[s] the pixel semiconductor patterns 110a” and is “formed between a

pair of neighboring pixel semiconductor patterns 110a[,]” per Fig. 1. *Hwang-099*, 12:42-53, 3:60-67; *Dec.*, ¶¶128-133.

1[b] “each having a **light incident surface**, and a **backside surface** opposite the **light incident surface**;”

Hwang’s pixel semiconductor pattern 110a and photodiode 145, which is “disposed” within pattern 110a (collectively, one **pixel**), “have first and second surfaces in parallel, *i.e.*, that face one another.” *Hwang-099*, 5:57-58, 6:37-38, 6:61-65; *Dec.*, ¶¶134-135. These are the **light-incident surface** and a **backside surface**, as shown in annotated Fig. 2:



Dec., ¶¶134-135; Claim 1[a]. In annotated Fig. 2, above, at least the portion of the first surface of 110a/145 as annotated is a bottom surface (*backside surface*) because it “is more proximate to the substrate 300[,]” and at least the portion of the second surface of 110a/145 as annotated is a top surface (*light incident surface*) because it receives incident light. *Hwang-099*, 6:38-40, 8:20-22, 9:6-7, 1:14-18; *Dec.*, ¶¶134-135. Because the top/second and bottom/first surfaces of pattern 110a “face one another” and are “parallel,” the surfaces are *opposite*. *Hwang-099*, 6:37-38; *Dec.*, ¶¶134-135.

Because Fig. 2 of *Hwang-099* is a cross-section of Fig. 1, a POSITA would have understood that *each of the pixels* in Fig. 1 similarly comprise a *light incident surface* and a *backside surface* opposite the *light incident surface*. *Dec.*, ¶136.

1[c] “a peripheral isolation element at least partially separating said two adjacent light sensitive pixels;”

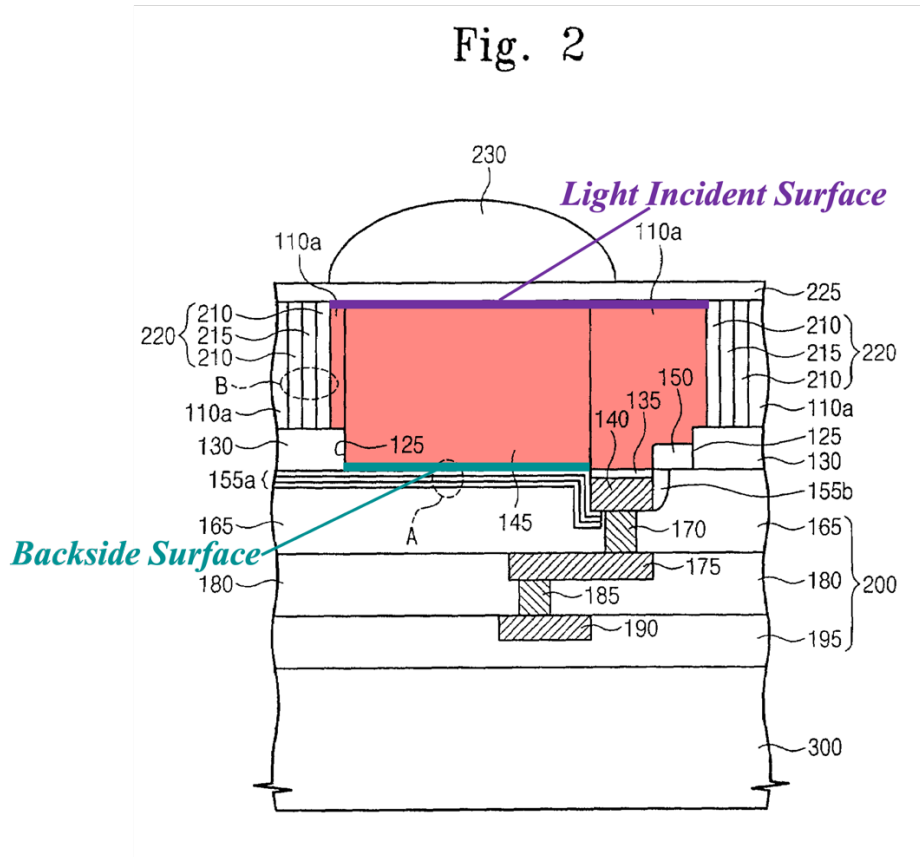
Hwang-099 teaches a *peripheral isolation element at least partially separating said two adjacent light sensitive pixels*, namely “[s]idewall multi-layered reflection layer 220 [that] encloses the side walls of the pixel semiconductor patterns 110a.” *Hwang-099*, 6:15-23 (further disclosing layer 220 separating patterns 110a and “disposed along the boundaries” of the patterns), 6:32-36, 3:63-67, Fig. 1; *Dec.*, ¶1367. Because layer 220 “encloses” pattern 110a and is “disposed along the boundaries of patterns 110a, layer 220 is *peripheral*:

Hwang-099 further teaches that sidewall multi-layer reflection layer 220 *at least partially separate[s] said two adjacent light sensitive pixels*. Hwang-099, 6:19-24 (“all of the pixel semiconductor patterns 110a can thus be separated by the sidewall multi-layered reflection layer 220.”); Dec., ¶¶138-140.

Hwang-099’s reflection layer 220 is an *isolation element* because it optically isolates adjacent pixel semiconductor patterns 110a from each other. *C.f.* ’359 Patent, 6:20-22; Dec., ¶¶138-140. Hwang-099’s sidewall layer 220 prevents light incident on a first photodiode 145 (disposed in pattern 110a) from being incident on “other pixels,” and is thus optically isolating. Hwang-099, 10:19-27, 15:42-48; Dec., ¶¶138-140. To the extent SiOnyx argues that electrical isolation is required, Hwang-099 teaches it by providing insulating silicon oxide from the light-incident surface to the isolation layer 130. Hwang-099, Fig. 2. Dec., ¶¶138-140.

1[d] “each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface,”

Hwang-099 teaches such a *doped region*, namely the n-type doped region photodiode 145. Hwang-099, 5:59–6:6; Dec., ¶141. As shown below in Fig. 2, n-type doped photodiode 145 is disposed on each of the **light incident surface** and the **backside surface**, thus photodiode 145 is *at least one doped region disposed on at least one of the light incident surface and the backside surface*.



Dec., ¶¶141-142.

The doped regions 145 form boundaries for both the light incident surface and the backside surface, and thus the doped regions 145 are “on” these surfaces. Dec., ¶143. Notably, this is the same sense in which doped layers are “on” the respective surfaces in the ’359 patent. ’359 Patent, 7:6-9, 11:15-19; Dec., ¶143.

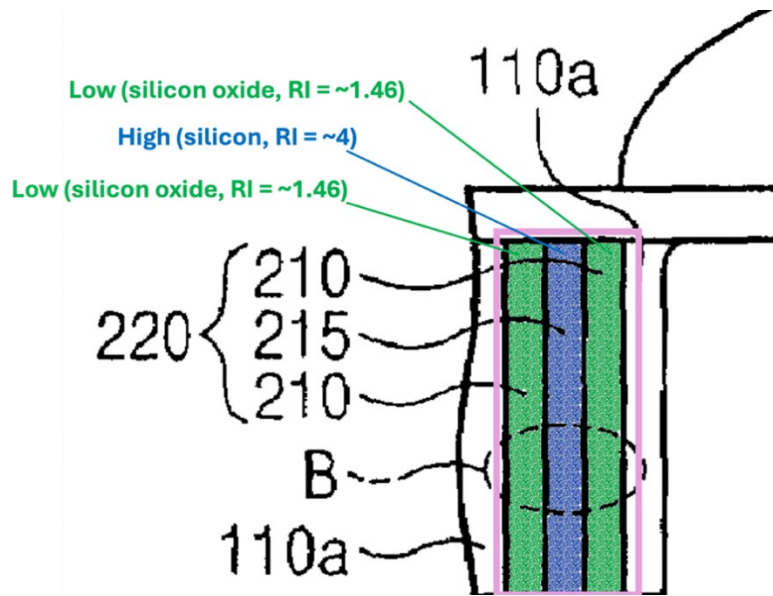
1[e] “wherein the peripheral isolation element comprises at least two materials having different indices of refraction,”

Hwang-099 teaches that the *peripheral isolation element* (Hwang-099’s sidewall multi-layered reflection layer 220) *comprises at least two materials having*

different indices of refraction, namely the materials of layers 210 and 215 of the sidewall layer 220. *Hwang-099*, 9:58-65, 2:1-6, 3:3-5, 3:41-43, 4:16-18, 6:11-13, 9:41-10:5; *Dec.*, ¶144. The sidewall layers 210 are silicon oxide or air, and the sidewall layer 215 is silicon. *Hwang-099*, 10:48-60. Per *Hwang-099*, silicon oxide has a refractive index of “approximately 1.46”, air has a refractive index of 1, while silicon has refractive index of “approximately 4.” *Hwang-099*, 9:28-30, 10:2-4. *Hwang-099* thus teaches *wherein the peripheral isolation element comprises at least two materials having different indices of refraction.* *Dec.*, ¶145.

1[f] “wherein said peripheral isolation element comprises a first, a second and a third layer, wherein said third layer is disposed between said first and second layers, and wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer.”

As explained under limitation 1[e], *Hwang-099* teaches that sidewall layer 220 (*peripheral isolation element*) comprises at least two layers 210 and one layer 215. *Hwang-099* teaches that “sidewall reflection layer 215 [is] interposed between two first sidewall reflection layers 210,” where layers 210, 215 are “respectively formed of a silicon oxide layer and a silicon layer[.]” *Hwang-099*, 10:48-55. As shown below, because layer 215 (*third layer*) of silicon (RI=4) is sandwiched between layers 210 (*first and second layers*) of silicon oxide (RI=1.46), *Hwang-099* teaches limitation 1[f].



Hwang-099, Fig. 2, 9:28-30; *Dec.*, ¶¶146-148.

CLAIM 2

See claim 1[e]-[f]’s mappings. There is a refractive index difference of at least 0.2 between Hwang-099’s first and second layers of silicon oxide ($n \approx 1.46$), and the third layer of silicon ($n \approx 4$). *Dec.*, ¶149.

CLAIM 3

A POSITA would have understood that Hwang-099’s “silicon oxide” layers 210 were silicon dioxide (an extremely common oxide of silicon), from its disclosed refractive index (approximately 1.46). *Hwang-099*, 9:28-29; *Dec.*, ¶150.

CLAIM 4

See claims 1, 3’s mappings. Layers 210 are the first and second layers, per claim 1[f]’s mapping. *Dec.*, ¶151.

CLAIM 7

See claim 1[e]’s mapping. *Dec.*, ¶152.

CLAIM 10

Hwang-099’s first and second layers are silicon oxide with a refractive index of approximately 1.46, *less than about 2.1*. *Hwang-099*, 9:28-30; *Dec.*, ¶153.

CLAIM 18

18[Pre] “An imager device, comprising:”

See claim 1[Pre]’s mapping. *Dec.*, ¶154.

18[a] “at least two adjacent light sensitive image sensor pixels”

See claim 1[a]’s mapping. *Dec.*, ¶155.

18[b] “each having a light incident surface, and a backside surface opposite the light incident surface;”

See claim 1[b]’s mapping. *Dec.*, ¶156.

18[c] “a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween, said isolation element comprising at least two materials having different indices of refraction,”

See claim 1[c], 1[e]’s mappings discussing the peripheral isolation element separating adjacent pixels and having materials with different refractive indices. Additionally, Hwang-099 teaches claim 18[c]’s *so as to reduce optical crosstalk*

therebetween: “[T]he sidewall ... minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels ... and image distortion can be minimized.” *Hwang-099*, 10:19-40, 15:42-48; *Dec.*, ¶157; *cf.* ’359 *Patent*, 6:51-52.

18[d] “at least one doped region disposed on at least one of the light incident surface and the backside surface,”

See claim 1[d]’s mapping. *Dec.*, ¶158.

18[e] “wherein said peripheral isolation element comprises a first, a second and a third layer, wherein said third layer is disposed between said first and second layers, and wherein each of said first and second layers exhibits an index of refraction less than an index of refraction of said third layer.”

See claim 1[f]’s mapping. *Dec.*, ¶159.

CLAIMS 38, 45

Regarding the *semiconductor portion providing said light incident surface and said backside surface*, see claim 1[a]-[b]’s mappings. The semiconductor portions are semiconductor regions 110a, 145. *Hwang-099*, 5:47-58; *Dec.*, ¶¶160-161.

Regarding the *peripheral isolation element isolat[ing] the semiconductor portions* of adjacent pixels, *Hwang-099*’s sidewall layer 220 *isolates the semiconductor portions* both because it isolates each pixel ***optically***, as discussed

under claim 1[c]’s mapping. *Hwang-099*, 9:58-10:5, 10:19-40, Abstract; *Dec.*, ¶162; *cf.* ’359 *Patent*, 10:20-22.

Hwang-099’s reflection layer 220 also *isolates* the semiconductor portions 110a, 145 *electrically* because they surround these portions with electrically insulating materials, such as silicon dioxide or air, and extend from the light-incident surface to the device isolation pattern 130. *Hwang-099*, 10:19-40, 5:47-6:23, 10:61-62, Figs. 1-2; *Dec.*, ¶163.

Hwang-099’s cited teachings apply to each pixel in an array (*Hwang-099*, 5:47-55, Figs. 1-2, 4:59-63), and thus apply to *each of said at least two adjacent light sensitive image sensor pixels*. *Dec.*, ¶164.

CLAIMS 39, 46

See claim 38’s mapping. *Dec.*, ¶¶165-166.

CLAIMS 40, 47

See claim 38’s mapping. *Dec.*, ¶¶167-168.

CLAIMS 42, 49

The ’359 patent states “the term ‘monolithic’ refers to an electronic device in which electronic components are formed on the same substrate.” ’359 *Patent*, 5:19-21. In *Hwang-099*, the pixels are formed on the same substrate. *Hwang-099*, 5:52-58; Fig. 1, *Dec.*, ¶¶169-170.

The pixels are also isolated from one another by said peripheral isolation

element, per claim 38's mapping. *Hwang-099*, 5:52-6:23, 9:25-34, 10:6-18, 10:19-40, Figs. 1-2; *Dec.*, ¶¶169-170.

CLAIMS 43, 50

The '359 Patent defines "trench isolation features" to be the same as "isolation elements". '359 *Patent*, 7:42-44 ("Regarding isolation elements, also referred to herein as trench isolation features...."). *Hwang-099*'s sidewall multi-layered reflection layer 220 is thus a trench isolation element because it is an isolation element (*See* claim 1[c]'s mapping). *Dec.*, ¶¶171-172.

To the extent that "trench" implies a location, *Hwang-099* teaches that sidewall multi-layered reflection layers 220 are arranged in vertical spaces in semiconductor portion 110a (*see* Fig. 13, element 205, Fig. 16, element 206). *Dec.*, ¶173.

Finally, to the extent "trench" implies a process or a physical shape, *Hwang-099* teaches sidewall multi-layered reflection layers 220 are formed by etching trenches (*e.g.*, trench 125) and grooves that are relatively deeper than they are wide (*i.e.*, trenches), filling them with sidewall material, to form an overall structure 220 that is trench-shaped. *Hwang-099*, Figs. 13-16, 18-21, 12:42-61, 13:29-49, 14:3-22, 14:50-15:7. This is notably similar to the method used in the '359 Patent. '359 *Patent*, 12:41-43; *Dec.*, ¶174.

CLAIMS 44, 51

Hwang-099 provides an example thickness of each of the two layers 210 of 550 Angstroms (55 nm) and of layer 215 of 500 Angstroms (50 nm), for a combined 160 nm. *Hwang-099*, 10:54-55; *Dec.*, ¶¶175-176.

CLAIMS 52, 58

See Ground 1, claim 1[e]'s mapping. The semiconductor portions comprise silicon (*Hwang-099*, 5:54-57), while the first and second layers 210 comprise silicon oxide (*Hwang-099*, 10:2-3). *Dec.*, ¶¶177-178.

CLAIMS 56, 62

Hwang-099's sidewall multi-layered reflection layers 220 exhibit vertical material layers 210 and 215 (meaning that they **fill a trench**), where the material layers serve to trap light within a pixel. *Hwang-099*, 9:58-63, 10:6-10, 5:47-51, 6:4-6, 6:9-11, 6:19-23, Figs. 1 and 2. Layer 220 is *light trapping* because it reflects light incident on the boundary surfaces of layer 220 onto photodiode 145. *Hwang-099*, 9:52-10:35. *Dec.*, ¶¶179-180.

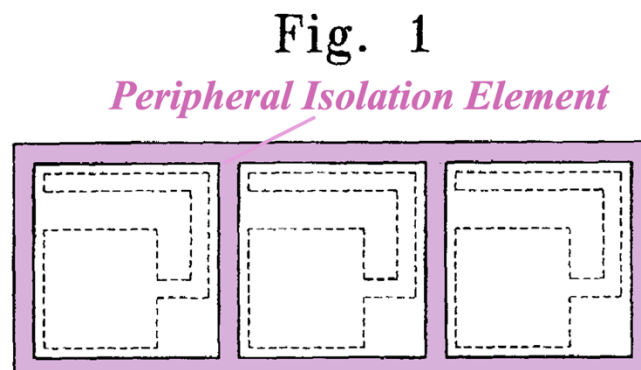
CLAIM 57, 63

Hwang-099's trenches qualify as deep trenches, because they extend from the light-incident surface to the isolation element 130. *Hwang-099*, 10:61-62 (Fig. 2), 12:25-31 (Fig. 6); *Dec.*, ¶¶181-182.

CLAIM 67, 73

See claim 1[c]'s mapping, discussing the reflective properties of Hwang-099's

reflection layers 220. These layers are configured to reflect light incident thereon from any of said two *adjacent light sensitive pixels back to that pixel*. *Hwang-099*, 10:19-40, 15:42-48. For example, layers 220 separating the leftmost pixel from the center pixel in Fig. 1, below, reflect light incident from the left back into the left pixel and light incident from the right back into the right pixel:



Dec., ¶¶183-184.

CLAIMS 68, 74

See claim 39's mapping. Optical isolation occurs between *adjacent pixels* because of the placement of sidewall layer 220, as shown in Figs. 1 and 2. *Hwang-099*, 5:47-51, 6:4-6, 6:11-19, 10:19-40, Figs. 1 and 2; *Dec.*, ¶¶185-186.

CLAIMS 69, 75

See claim 40's mapping. Electrical isolation occurs between *adjacent pixels*, because of the placement of sidewall layer 220, as shown in Figs. 1 and 2. *Hwang-099*, 5:47-51, 6:4-6, 6:17-23, Figs. 1 and 2; *Dec.*, ¶¶187-188.

Ground 2. Claims 1-5, 7, 10, 18, 23, 38-40, 42-47, 49-64, 67-70, 73-75, and 80-

83 were obvious over Hwang-099

This Ground challenges all claims challenged in Ground 1, and certain additional claims. Obviousness arguments are provided only for a subset of the claims, namely 3-5, 23, 53-56, 59-60, 61-62, 64, 70, and 80-83, divided into subgroups based on the similarity of their limitations. The obviousness arguments for these subgroups of claims, however, involve simple modifications of Hwang-099 that would also meet the remaining claims challenged in Ground 1 but not otherwise addressed in each subgroup. *Dec.*, ¶189.

CLAIMS 3-4

Claims 3-4 recite the use of silicon dioxide. Hwang-099 teaches the first and second layers (layers numbered 210 in Hwang-099) are silicon oxide, which Petitioners contend (under Ground 1), is silicon dioxide (SiO₂). However, it would also have been *obvious* to use SiO₂. Hwang-099 teaches that silicon oxide has a refractive index of approximately 1.46 (*Hwang-099*, 9:28-29), which matches the refractive index of SiO₂. *Dec.*, ¶190 (*citing Maltison, Komuro*). A POSITA would have been motivated to use SiO₂ because it was the most stable and commonly-used silicon oxide in semiconductor fabrication, providing desirable electrical insulating properties. *Dec.*, ¶190. A POSITA would have had a reasonable expectation of success (“REOS”) at least because SiO₂ is the most commonly-used oxide in semiconductor fabrication and has the refractive index of approximately 1.46 desired

by Hwang-099. *Dec.*, ¶190. Because the remaining Ground 1 Claims do not require a specific oxide, they would also be rendered obvious by this modification. *Dec.*, ¶190.

CLAIMS 5, 23

It would have been obvious to extend Hwang-099's sidewall multi-layered reflection layer 220 from the light incident surface to the backside surface (through element 130) to increase its reflective properties to the lower boundary of the pixel semiconductor, to further reduce optical cross-talk. *Dec.*, ¶191.

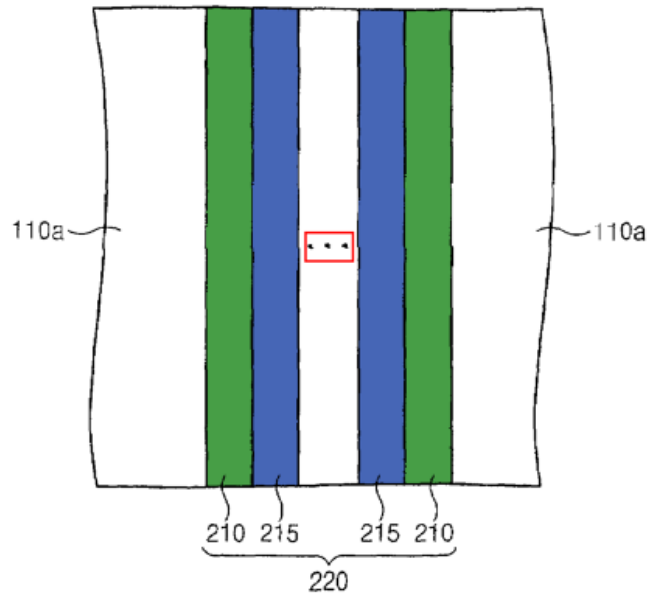
Specifically, a POSITA would have found it obvious to modify Fig. 2's device isolation pattern 130 such that first and second layers 210, 215 of reflection layer 220 extend through pattern 130 such that sidewall layer 220 *extends substantially from the light incident surface to the backside surface*, per the Fig. 6 embodiment. In the Fig. 6 embodiment, Hwang-099 teaches device isolation pattern 130' "include[s] **extended portions of the first and second sidewall reflection layers 212a' and 217a'.**" *Hwang-099*, 12:26-28, Fig. 6. Hwang-099 proposes Fig. 6 as an alternative to the Fig. 2 embodiment. *Hwang-099*, 4:61-63, 5:5-7; *Dec.*, ¶191 (*citing Hwang-099*, 1:31-48).

6—would predictably increase the amount of light reflected back into the pixel, thereby providing the benefit of increasing the number of photons returned to the photodiode. *Dec.*, ¶¶192-196. There would have been a REOS at least because Hwang-099 provides methods for manufacturing an isolation pattern 130 having first and second sidewall reflection layers. *Hwang-099*, 14:3-22, 12:35–13:3; *Dec.*, ¶¶192-196. The remaining Ground 1 Claims permit the peripheral isolation element to extend from the light incident surface to the backside surface, and would thus also be rendered obvious by this modification. *Dec.*, ¶196.

CLAIMS 53-54, 59-60

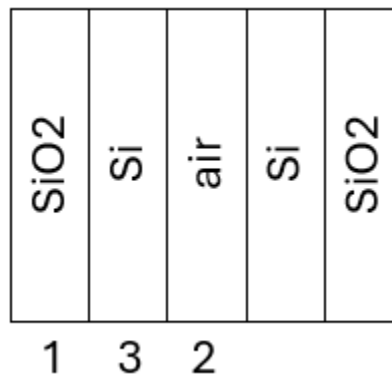
Hwang-099 teaches sidewall layer 220 having multiple pairs of alternating layers of low- and high-refractive index materials. *Hwang-099*, 2:16-29, 4:12-15, 6:11-13, 10:7-12, 11:47-52, 12:62-65, 14:66-15:4, Fig. 4; *Dec.*, ¶¶197-198. Fig. 4 illustrates this arrangement of reflection layer 220:

Fig. 4



Hwang-099, Fig. 4, 9:37-10:18; *Dec.*, ¶198.

Hwang-099 further teaches that its lower-refractive index layers are silicon oxide or air. *Hwang-099*, 10:2-4, 4:3-4, 13:9-16; *Dec.*, ¶199. It would have been obvious, based on *Hwang-099*'s suggestion, that in a five-layer (or more) structure, both silicon oxide and air would be used, for example, in the following relationship, where the first, second, and third layers of the claims have been labeled 1, 2, and 3:



Dec., ¶199. Hwang-099 teaches a sidewall layer 220 having five layers, that its layers should have multiple sets of alternating layers of low- and high-refractive index materials (*Hwang-099*, claim 4, *see also* 2:16-29, 4:12-15, 10:6-12, 11:47-52, 12:62-13:3, 14:66-15:4) and to use silicon for high-refractive-index layers and either silicon oxide or air for the low-refractive-index layers. Because of this, there were only a finite number of predictable alternatives for Hwang-099's five-layer sidewall 220, which would have led to predictable results. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 421 (2007). *Dec.*, ¶200.

The addition of an air layer, as suggested by Hwang-099, would further have been motivated by the desire to optimize the sidewall 220 in order to minimize interference and image distortion. Hwang-099, 10:19-40, 12:62-65. The design of such a structure would have been routine to a POSITA, who would have had a reasonable expectation of success, including for expected advantages. *Dec.*, ¶201. There would have been REOS at least because it would have merely required forming an additional groove 205' while manufacturing Hwang-099's device, which a POSITA would understand how to do given Hwang-099 already discloses forming such grooves. *Dec.*, ¶201.

The arrangement meets claims 53 and 59, because the first and second layers comprise different materials (SiO₂ and air). The arrangement also meets claims 54 and 60, because there are at least three materials (SiO₂, Si, and air). *Dec.*, ¶¶202-

203. The “at least two materials” also have different refractive indices (1.46 and 1) as required by claims 1 and 18. *Hwang-099*, 9:25-30, 10:2-4; *Dec.*, ¶¶202-203. The Remaining Ground 1 Claims permit such a peripheral isolation element, and would thus also be rendered obvious by this modification. *Dec.*, ¶¶202-203.

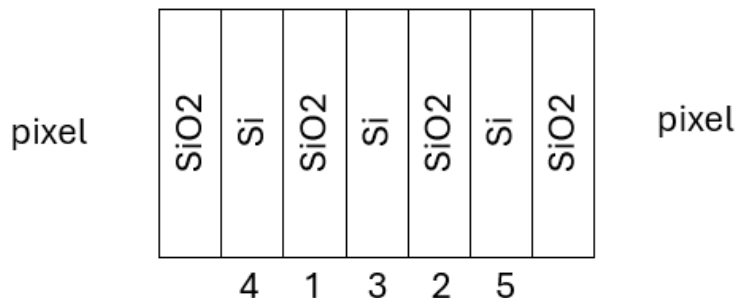
CLAIMS 55, 61, 80-83

These claims recite the peripheral isolation element having additional layers. *Hwang-099* renders these claims obvious. As explained immediately above for claim 55, *Hwang-099* teaches sidewall layer 220 having multiple **pairs** of alternating layers of low- and high-refractive index materials. *Hwang-099*, 2:16-29, 4:12-15, 6:11-13, 10:7-12, 11:47-52, 12:62-65, 14:66-15:4, Fig. 4; *Dec.*, ¶¶204-205. An arrangement with three such **pairs** of layers would have **six total layers**, for example. *Hwang-099* also teaches that its reflecting element 220 can be formed “in an **odd 5-layer or higher** configuration.” *Hwang-099*, 11:49-52; *Dec.*, ¶¶204-205.

Claims 55, 61, 80, and 82 require “more than three” or “five” layers. Should SiOnyx argue *Hwang-099* does not expressly disclose a five-layer arrangement, despite the teachings described above, it would have been obvious as a routine modification, motivated by the express teachings of *Hwang-099*, to have five layers of alternating low- and high-refractive index materials. *Hwang-099*, 11:49-52; *Dec.*, ¶206. Such arrangements would have been further motivated by the desire to optimize the dimensions of the sidewall 220 to minimize interference and image

distortion, which a POSITA would have expected to improve with increasing layer numbers. *Hwang-099*, 10:19-40, 12:62-65; *Dec.*, ¶206. A POSITA would have had the skill to design Hwang-099's sidewall reflecting element by adjusting the layers to optimize performance for particular applications with predictable results and a REOS. *Dec.*, ¶206.

Regarding claims 81, 83, Dr. Shanfield provides a figure explaining what the claimed alternating layers of low and high refractive indices, *i.e.*, SiO₂ and Si, would look like. As discussed above, Hwang-099 expressly teaches a 5-layer or higher configuration. Therefore, it would have been obvious and a POSITA would have been motivated to use Hwang-099 with a reflecting layer 220 having *four pairs* of layers with alternating low-high indices of refraction, as shown in Dr. Shanfield's depiction, below (layer numbers at the bottom corresponding to the claim language):



Dec., ¶207. This meets claims 81 and 83, and would have been obvious based on Hwang-099's express suggestions and the desire to increase reflecting layer 220's performance, as discussed above. *Dec.*, ¶207. The remaining Ground 1 Claims permit multiple layers in the peripheral isolation element, and would thus also be

rendered obvious by this modification. *Dec.*, ¶207.

CLAIMS 56, 62

Hwang-099 renders obvious having its peripheral isolation element (reflecting layer 220) comprising material filling a trench, as discussed above for claim 64's mapping, immediately below. The material is light-trapping because it reflects light from a pixel, incident upon reflecting layer 220, back into the pixel. *Hwang-099*, 10:19-40, *Dec.*, ¶208.

CLAIMS 64, 70

As discussed for Ground 1, claim 43's mapping, the '359 Patent defines "trench isolation elements" to be the same as "isolation elements" ('359 Patent, 7:41-43), which Hwang-099 teaches in the form of its sidewall multi-layered reflection layers 220. *Hwang-099*, Figs. 1 and 2, 5:57-60, 6:4-6, 6:7-6:23; *Dec.*, ¶¶209-210.

Hwang-099 also teaches and renders obvious the process limitation. Hwang-099's sidewall multi-layered reflection layers 220 are formed by trench filling. In particular, Hwang-099 teaches alternate methods of forming its layers 220 in the context of Figs. 15-16 wherein a trench 206 is formed, or Figs. 20-22, wherein trenches 125 and 206' are formed, followed by filling with material to form the first and second layers, followed by filling with material to form the third (middle) layer. *Hwang-099*, 13:26-49, Figs. 15 and 16; *Dec.*, ¶211. A POSITA would have been

motivated to use these alternate methods of formation by the express teaching of Hwang-099, and a POSITA would have had a REOS, at least because Hwang-099 teaches the manufacturing process for each of the disclosed forming methods. *Hwang-099*, 13:20-49, 14:38-15:32; *Dec.*, ¶211. The Remaining Ground 1 Claims are device claims that do not require a different formation method, and would thus be rendered obvious by this modification. *Dec.*, ¶211.

Ground 3. Claims 5, 23, 38-40, 43, 45-47, 50, 65-66, 68-69, 71-72, and 74-75 were obvious over Hwang-099 and Cole.

Like the '359 Patent, Cole (Ex. 1071) teaches isolation structures for pixels in image sensors. *Cole*, Title, Abstract, ¶0001; *Dec.*, ¶¶212-213. An exemplary structure is illustrated in Fig. 7 below, which shows a pixel (red) with a photodiode, light-incident and backside surfaces, and isolation structures 340 at the periphery:

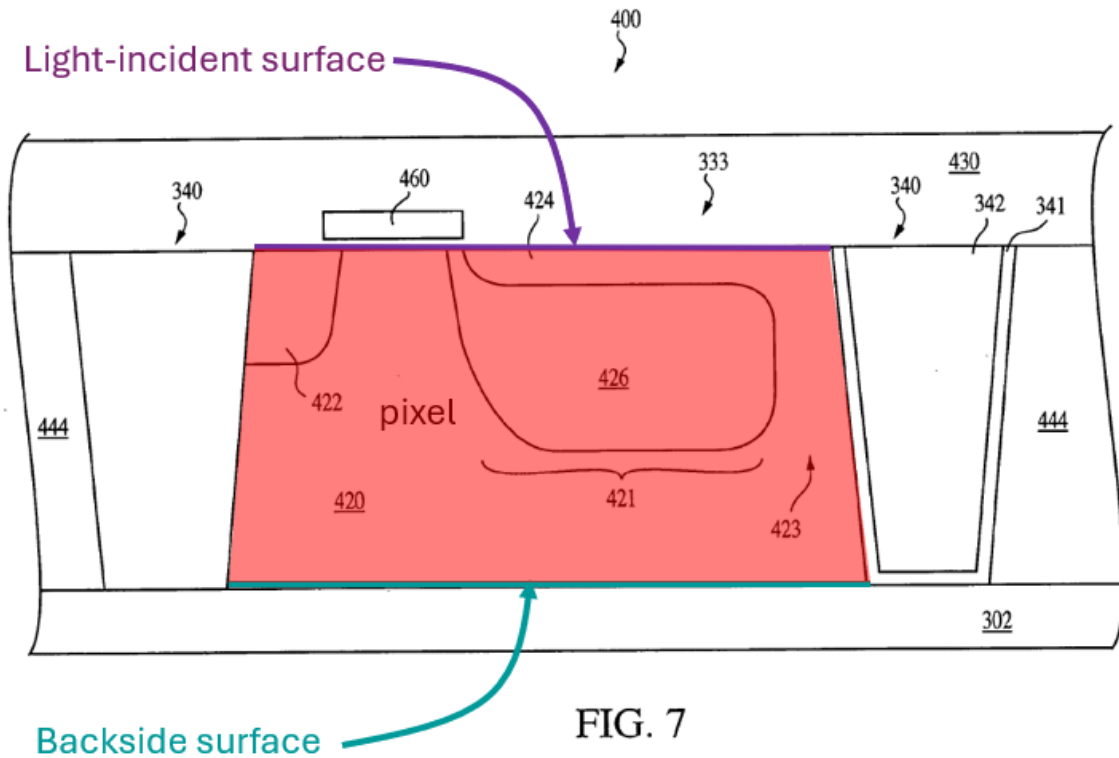


FIG. 7

Cole, Fig. 7, ¶0044; *Dec.*, ¶213.

Although several embodiments of *Cole* relate to isolation structures between a photodiode array and peripheral circuitry, the purpose of these structures is to stop photons and electrons from crossing to/from pixels—similar to the peripheral isolation elements of the '359 Patent and sidewall layer 220 of *Hwang-099*. *Cole*, Title, ¶0030; *Dec.*, ¶214. *Cole* furthermore stresses the need to separate *individual pixels* from one another to avoid optical and electrical crosstalk *between pixels*: “CMOS image sensor pixels **must be isolated** from one another to avoid pixel cross talk....it is advantageous to provide **both electrical and optical isolation between pixels.**” *Cole*, ¶0005 (Emphases added); *Dec.*, ¶214.

Cole teaches an embodiment (Fig. 6, below) in which a peripheral isolation element has three different materials (shown in blue, green, and light green) having different refractive indices to reflect light. *Cole*, ¶¶0042, 0044; *Dec.*, ¶215.

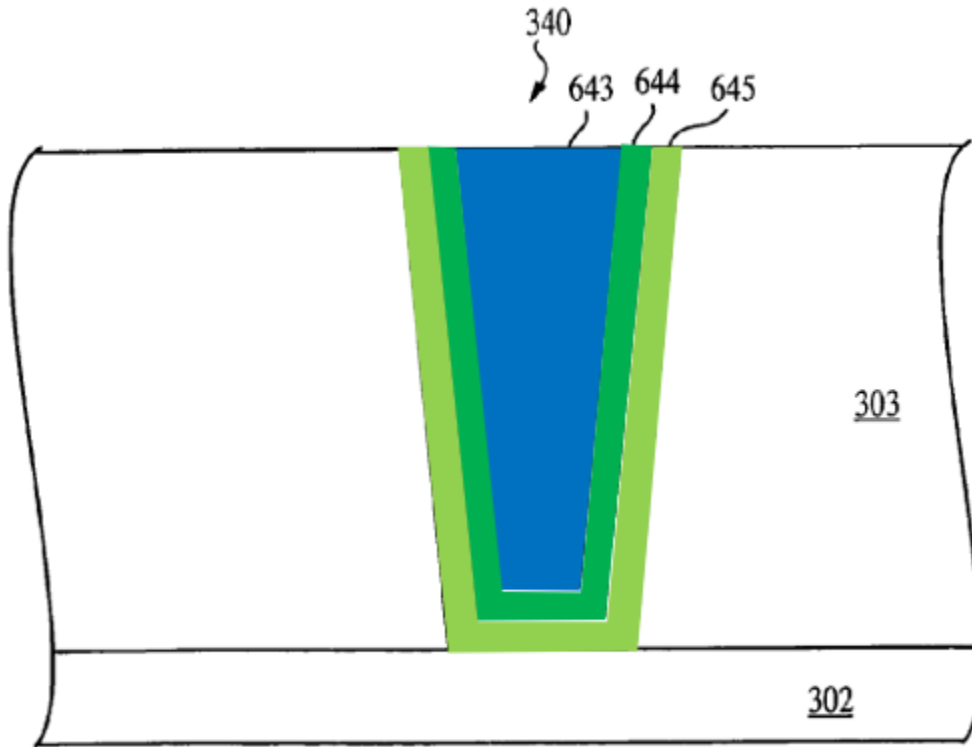


FIG. 6

Cole, ¶¶0042, 0044; *Dec.*, ¶215.

Cole teaches various techniques that provide for electrical and optical isolation at the periphery of pixels, but which apply differently to different sets of dependent claims. Therefore, the reasoning supporting obviousness will be described with respect to different groups of claims. *Dec.*, ¶216.

ISOLATION CLAIMS 5, 23, 38-40, 43, 45-47, 50, 68-69, 74-75

These claims require the peripheral isolation element provide “isolation” generally (38, 45), a “trench” isolation element (43, 50), optical isolation (39, 46, 68, 74), and/or electrical isolation (40, 47, 69, 75). Claims 5 and 23 require the peripheral isolation element to “extend[] substantially from the light incident surface to the backside surface”. Hwang-099 teaches or renders obvious these claims as discussed above in Grounds 1 and/or 2. Additionally, these claims were obvious over Hwang-099 in view of Cole. *Dec.*, ¶¶217-218.

Cole teaches that “it is advantageous to provide both electrical and optical isolation between pixels” to prevent color mixing. *Cole*, ¶0005; *Dec.*, ¶218. Cole further teaches methods for achieving optical and electrical isolation, specifically by forming a “trench” isolation structure 340 (*Cole*, ¶0030) that extends entirely through the epitaxial layer (the layer where the photodiode is formed) to the base layer (*Cole*, ¶0034), as shown in Fig. 7:

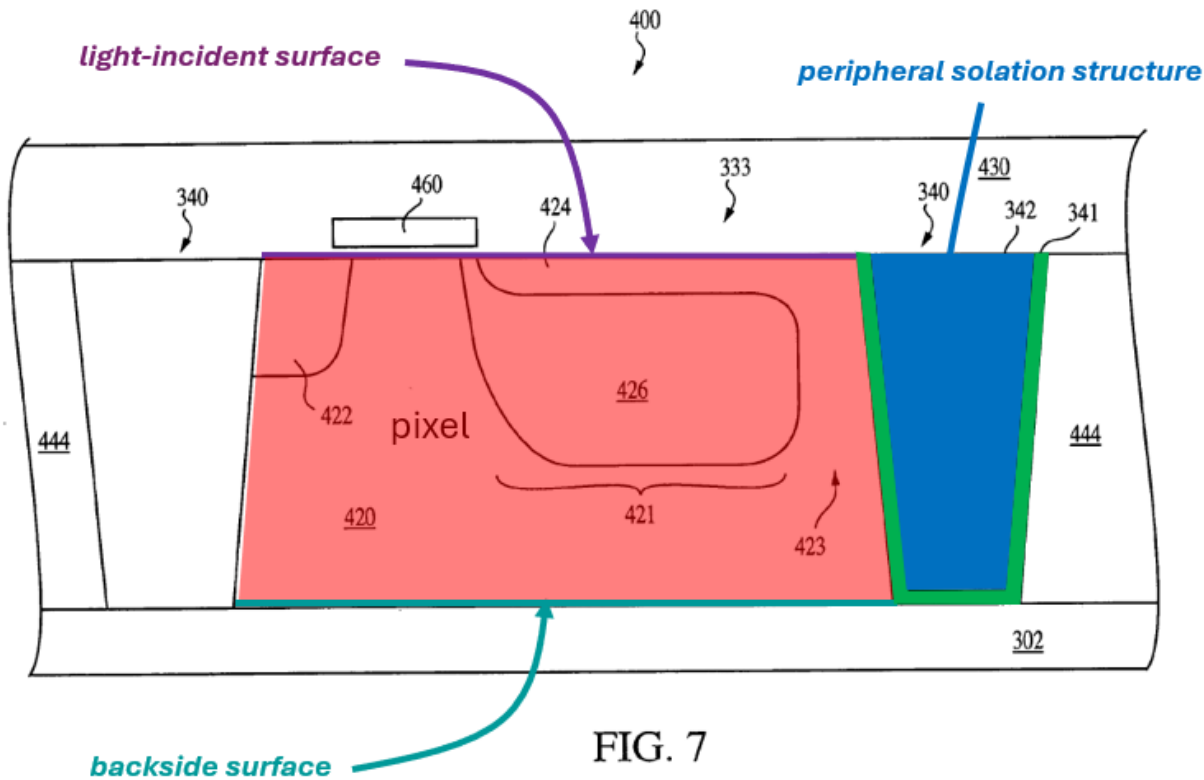


FIG. 7

Cole, Fig. 7, ¶0044; *Dec.*, ¶218. The trench 340 includes “a thermal oxide” that is “grown in trench 340 prior to deposition of material 341, providing an additional barrier to electrons.” *Cole*, ¶0035; *Dec.*, ¶218.

Based on these teachings, a POSITA would have been motivated to form Hwang-099’s trench isolation structure to extend from the light-incident surface to the backside surface (claims 5, 23), and to ensure that it provides sufficient isolation, thereby improving similar isolation structures in the same way. *Dec.*, ¶219. Hwang-099 already teaches (in reference to Hwang-099’s Fig. 6) a peripheral isolation structure that extends from the light-emitting surface to the backside surface and uses silicon oxide in its outside layers, as discussed above in Ground 2, claim 5.

Hwang-099, Fig. 6, 11:57-12:31. It would further have been obvious, based on Cole, to use a trench isolation structure that is sufficiently deep and insulating “to provide both electrical and optical isolation between pixels”. *Cole*, ¶0005; *Dec.*, ¶219. A POSITA would have had a REOS, at least because the techniques for trench formation were widely-used and well-understood in the semiconductor industry, allowing for control of depth of trench structures by various techniques. *Cole*, ¶0038 (“Trench 340 can be formed by techniques known in the art, such as an anisotropic etch through a mask...”); *Hwang-099*, 3:60-67, *Dec.*, ¶219.

CLAIMS 65-66, 71-72

Regarding claims 66 and 72, *Hwang-099* teaches a width of its sidewall reflecting structure of 160 nm and thus teaches the limitations of claims 66 and 72, as discussed above under Ground 1, claim 44. *Hwang-099*, 10:48-60; *Dec.*, ¶¶220-221. *Hwang-099*, however, does not expressly discuss the depth. *Dec.*, ¶221.

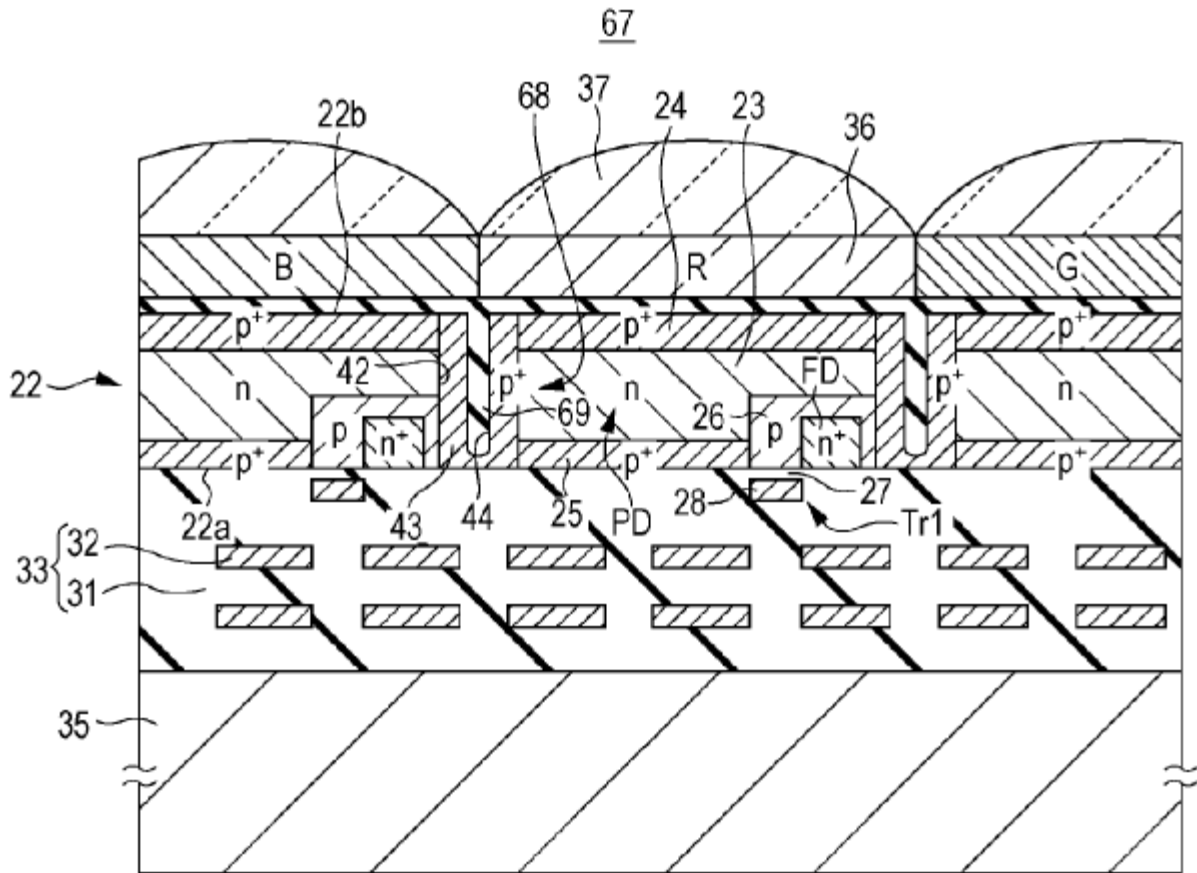
The recited depth range of claims 65 and 71 would have been obvious in view of Cole. Cole teaches isolation structures at the periphery of pixels and emphasizes the need to separate pixels to avoid optical and electrical crosstalk. *Cole*, ¶0005; *Dec.*, ¶222. Cole further teaches that to prevent photons and electrons from crossing the isolation structures, the structures “are deep, extending to a depth of at least about 0.5 micrometers”, with exemplary depths of 4 to 6 microns, “sufficiently deep to prevent photons or charge carriers from reaching array 333”. *Cole*, ¶¶0030, 0034;

Dec., ¶222. A POSITA would have found it obvious, based on Cole, to use such exemplary depths sufficient to prevent photons and charge carriers from crossing them, and would have had a REOS for the same reasons discussed above for the isolation claims. *Dec.*, ¶222.

Ground 4. Claims 6, 8, 11, 24, 30, 32, 34, 36, 53-54, 59-60, 80 and 82 were obvious over Hwang-099 and Shinohara.

Like Hwang-099 and the '359 patent, Shinohara (Ex. 1068) teaches a “solid-state imaging device” having pixels. *Shinohara*, Abstract; *Dec.*, ¶¶223-224. A cross-sectional view of a pixel (with neighboring pixels to the right and left) is provided in Fig. 9A:

FIG. 9A



Shinohara, Fig. 9A; Dec., ¶¶225-226.

Between pixels, Shinohara teaches having “an element isolation region 68 for isolating pixels....” *Shinohara*, ¶0090. The element isolation region is formed of alternating layers of silicon (43) and an oxide or nitride film (69). *Shinohara*, ¶¶0097, 0094. The purpose of the element isolation region is to prevent optical and electrical cross-talk between pixels. *Shinohara*, ¶0094; Dec., ¶227.

Shinohara teaches that layer 69 is made from silicon oxide or nitride, or, if a negative fixed charge is desired, from any of “hafnium dioxide (HfO₂), dialuminum

trioxide(Al_2O_3), ditantalum pentaoxide (Ta_2O_5), and dilanthanum trioxide (La_2O_3)....” *Shinohara*, ¶0091; *Dec.*, ¶228.

In addition to rationales that are specific to certain claims and provided under those claims, below, a POSITA would have been motivated to use the oxides specified by Shinohara in Hwang-099’s layers 210 of the sidewall reflecting element 220 for two independent reasons. **First**, the isolation element of Shinohara plays a role in the device similar to Hwang-099’s peripheral isolation element. *Hwang-099*, 6:19-23, 9:58-66, 10:14-18; *Shinohara*, ¶0094; *Dec.*, ¶¶229-231. Shinohara expressly teaches that, in such structures, either silicon oxide (as used in Hwang-099) or hafnium dioxide (HfO_2), dialuminum trioxide (Al_2O_3), ditantalum pentaoxide (Ta_2O_5), dilanthanum trioxide (La_2O_3) were useful. *Shinohara*, ¶¶0091-0094; *Dec.*, ¶¶229-231. A POSITA further would have recognized that these oxides were suitable for Hwang-099’s lower-refractive index layers 210 (the first and second layers of the claims) because these layers provide both electrical insulation and a refractive index contrast with silicon. *Shinohara*, ¶¶0091-0094; *Dec.*, ¶¶229-231 (*citing Aguilar-Frutis, Kasano, Iida, He*).

Second, a POSITA would have expected benefits from using the oxides suggested by Shinohara in the layers 210 of Hwang-099’s sidewall reflecting element 220. *Dec.*, ¶¶232-233. Specifically, Shinohara teaches that these oxides can provide a negative fixed charge, which has a beneficial hole-pinning effect that

suppresses the generation of white spots and dark current. *Shinohara*, ¶¶0091, 0095; *Dec.*, ¶¶232-233.

A POSITA would have had a REOS at least because methods of forming various oxide layers used by Shinohara were well-known and could have been predictably implemented by a POSITA. *Shinohara*, 0091; *Dec.*, ¶¶232-233 (*citing Callegari*).

CLAIMS 6, 11, 30, 32, 34, 36

It would have been obvious to use any of aluminum oxide, hafnium oxide, tantalum oxide, and lanthanum oxide in the first and second layers 210 of Hwang-099's sidewall reflecting element (peripheral isolation element) 220 for the reasons provided above on pages 42-45. *Shinohara*, ¶¶0091-0095; *Dec.*, ¶234.

CLAIM 8

Shinohara teaches that its oxides in its layer 69 can have a negative fixed charge, which suppresses dark current and is thus a passivating negative charge. *Shinohara*, ¶¶0091, 0095; *Dec.*, ¶235. A POSITA would have been motivated to use one of Shinohara's oxides with a negative fixed charge for the reasons discussed above on pages 42-45. *Dec.*, ¶235.

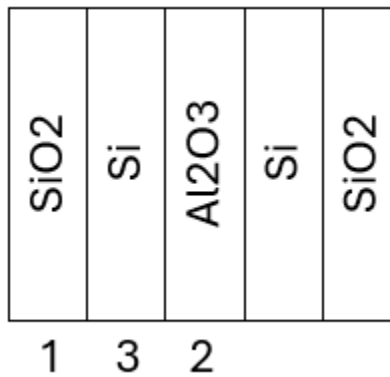
CLAIMS 24, 53-54, 59-60, 80, 82

These claims would have been obvious over Hwang-099 and Shinohara. As discussed above under Ground 2, claim 55, Hwang-099 teaches sidewall multi-

layered reflection layer 220 (peripheral isolation element) having **five layers**. *Hwang-099*, 12:67-13:3, 2:16-29, 4:12-15, 10:7-12, 11:47-52, 14:66-15:4, claim 4; *Dec.*, ¶236. *Hwang-099* specifically teaches a five-layer embodiment made from three grooves 205, which are filled with silicon oxide, forming a sidewall layer 220 with SiO₂-Si-SiO₂-Si-SiO₂ structure. *Hwang-099*, 12:62-13:3. It would have been obvious, based on *Hwang-099* and *Shinohara*, that in a five-layer (or more) structure, both silicon oxide and aluminum oxide (Al₂O₃) could be used with Al₂O₃ in the middle. *Shinohara* further teaches that it was advantageous to use an Al₂O₃ layer between two silicon layers to provide a negative fixed charge. *Shinohara*, ¶0091, Figs. 9A-9B; *Dec.*, ¶236. Based on these suggestions, it would have been obvious to form *Hwang-099*'s sidewall layer 220 with five layers but replace the middle silicon oxide layer with Al₂O₃, corresponding to *Shinohara*'s structure (Si-Al₂O₃-Si) with two outer layers of silicon oxide. *Dec.*, ¶236. This would have had the advantage, taught by *Shinohara*, of providing a negative-fixed-charge layer to produce a pinning effect to suppress the generation of white spots and dark current, as taught by *Shinohara*. *Shinohara*, ¶0094, 0091. *Dec.*, ¶236.

The design of such a structure would have been routine to a POSITA, who would have had a REOS at least because forming Al₂O₃ layers could have been done well-known techniques. *Shinohara*, ¶0091; *Dec.*, ¶237.

In the combination, the first, second and third layers would be as shown here:



Dec., ¶238.

The combination meets claim 24, because Hwang-099’s peripheral isolation element would have “at least two materials with different refractive indices that comprise silicon dioxide and aluminum oxide” (RI≈1.46 and 1.7, respectively). The combination also meets claims 53 and 59, because the first and second layers comprise different materials (silicon oxide and Al₂O₃). The combination also meets claims 54 and 60, because the first and second layers are different materials. *Dec.*, ¶239. The combination meets claims 80 and 82, because the structure has five layers. *Dec.*, ¶239.

Ground 5. Claims 12-17, 19-22, 25-29, 65-66, 71-72, and 76-79 were obvious over Hwang-099 and Carey.

Carey (Ex. 1069)⁴ teaches photosensitive devices including imaging devices having an array of pixels made from photodiodes, just like Hwang-099 and the '359 patent. *Carey*, e.g., Figs. 13 and 14, 024:15-16, 022:15-16; 026:14-34, 011:14-19; *Dec.*, ¶¶240-242.

Within such devices, Carey teaches the use of textured regions on surfaces. *Carey*, Abstract; *Dec.*, ¶243. Textured surfaces, according to Carey, “refer to a surface having a topology with nano- to micron-sized surface variations”—the same definition as the '359 patent. *Carey*, 006:33-007:9; '359 *Patent*, 4:40-43; *Dec.*, ¶243.

In addition to rationales that are specific to certain claims and provided under those claims, below, it would have been obvious to utilize Carey’s textured surfaces for the express benefits taught by Carey. *Carey*, 009:13-19, 010:7-15, 011:11-22, 012:18-29, 014:15-20, 015:26-34, 017:18-19, 021:21-25, 025:9-17, 026:18-21, 026:25-27, 027:6-13; *Dec.*, ¶¶244-246. Carey’s textured regions are said to work by scattering long-wavelength light. *Carey*, 011:11-22; *Dec.*, ¶¶244-246. When scattered, the light will take on a different direction, potentially increasing its path-

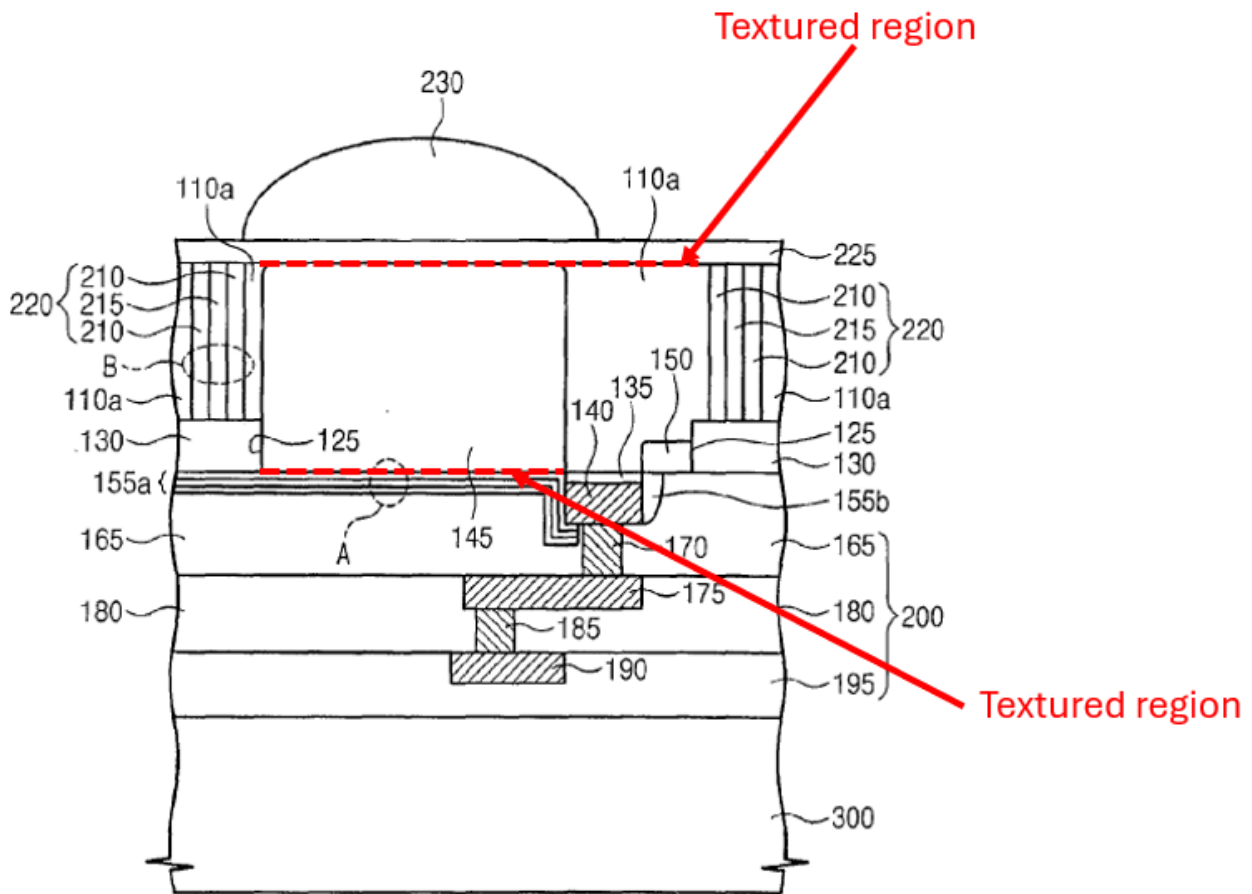
⁴ To assist in the Board’s review, the Petitioners have added line numbers to Carey in the left margin of Ex. 1069. References are added to page numbers:line numbers.

length through the silicon, and giving it a better chance of being absorbed. *Id.* According to Carey, this can increase the sensitivity of the device to longer wavelengths, allow the device to be thinner, and increase the operation speed of the device. *Id.* A POSITA would have had a REOS in using Carey's textured regions with Hwang-099 because Carey teaches a variety of well-understood methods for doing so. *Carey*, 016:16-25. *Dec.*, ¶¶244-246.

CLAIM 12

It was obvious to use a Carey textured region in a pixel of Hwang-099's device, for the reasons discussed on pp. 48-49. Specifically, it would have been obvious to add such a textured region at the light-incident surface and/or backside surface of Hwang-099's pixel, as shown here:

Fig. 2



Dec., ¶247.

A POSITA would have been motivated to include a *textured region*, per Carey, coupled to the *light incident surface* to increase the sensitivity, speed and light collection efficiency of Hwang-099's pixel. Carey, 009:13-19, 010:7-15, 011:11-22, 012:18-29, 014:15-20, 015:26-34, 017:18-19, 021:21-25, 025:9-17, 026:18-21, 026:25-27, 027:6-13; Dec., ¶248. Per Dr. Shanfield, it was well-known that “[i]ncident light to a planar surface of silicon reflects, and reflected light does not contribute to the photocurrent.” Dec., ¶248 (*citing Mita*). Carey's textured

regions on the light incident surface are a well-known approach to increase the amount of light collected by semiconductor devices. *Dec.*, ¶248. Per Dr. Shanfield, a POSITA would have known that adding a Carey textured region coupled to Hwang-099's *light incident surface* would have diffusely scattered incident light such that less light was reflected off the light incident surface, thereby increasing the collection efficiency of Hwang-099's *pixel*. *Dec.*, ¶248. The modification is application of a known technique (adding a Carey textured region to the light incident surface) to a known device (image sensor) ready for improvement to yield the predictable result of increasing light collection efficiency. *Dec.*, ¶248. The modification would have had a REOS because methods of forming Carey textured regions coupled to the light incident surface were well-known. *Dec.*, ¶¶248-250 (citing *Konno, Smith*).

A POSITA would have also been motivated to modify Hwang-099's *backside surface* to *comprise Carey's textured region*. Per Dr. Shanfield, providing such a textured region on the backside surface would have enhanced internal reflection of incident light within Hwang-099's *pixel*. *Dec.*, ¶¶249-250. A POSITA would have understood that compared to a smooth surface, a Carey textured region would have diffusely scattered incident light thereby increasing the path length of light throughout the geometry of the *pixel*. *Dec.*, ¶¶249-250. Further, a POSITA would have appreciated that Carey's textured region would have worked in conjunction

with Hwang-099's base multi-layered reflection layer to increase the amount of incident light reflected toward photodiode 145, in part by increasing the range of angles that light reflects back into the pixel. *Dec.*, ¶¶249-250. Thus, the modification would have predictably increased the quantum efficiency of Hwang-099's pixel. *Dec.*, ¶¶249-250. The modification is nothing more than an application of a known technique (providing a Carey textured region) to a known device (image sensor) in the same way. *Dec.*, ¶¶249-250.

CLAIM 13

It was obvious to use a Carey textured region in a pixel of Hwang-099's device *coupled to the light incident surface*, for the reasons discussed above under claim 12. Carey states that “[t]he textured region can be associated with the surface nearest the impinging electromagnetic radiation...”, and can be paired with an antireflection layer. *Carey*, 016:9-10, Fig. 6, 021:10-20. By scattering light passing through the light-incident layer, light travels on a longer path through the device, increasing efficiency. *Carey*, 011:11-22; *Dec.*, ¶251. Carey furthermore teaches that its textured regions near the surface of a layer are said to be “coupled” to the layer. *Carey*, Abstract, 012:18-20; *Dec.*, ¶251.

CLAIM 14

See claim 13's mapping. The Hwang-099-Carey combination teaches the light-incident surface *compris[ing] the textured region* as shown in Fig. 6. *Carey*,

Fig. 6, 021:10-13; *Dec.*, ¶252.

CLAIM 15

Carey's Fig. 6 shows a *textured* region that is also a *film layer*. *Carey*, Fig. 6, 021:10-16; *Dec.*, ¶253. For example, in Fig. 7 of Carey, textured region 78—which is the same as textured region 68 in Fig. 6 but placed at the backside of the device—is referred to interchangeably as both a “textured region” and a “textured layer”. *Carey*, Fig. 7, 021:15-16. A POSITA would understand a layer is a *film*. *Dec.*, ¶253.

CLAIM 16

Carey teaches that layer 68 in Fig. 6 comprises “silicon material”. *Carey*, 021:10-13. Carey states that “[v]arious types of silicon materials are contemplated, including “multicrystalline” and “microcrystalline”. *Carey*, 015:14-18. “Multicrystalline” and “microcrystalline” are both forms of polycrystalline silicon, *i.e.*, *polysilicon*. *Dec.*, ¶254. Based on Carey's teaching, it would have been obvious to use polysilicon on the light-incident surface of the device to form a textured layer, because it was a commonly-used material in semiconductor manufacturing having known deposition and structuring methods, expressly suggested by Carey, and could have been predictably implemented with a REOS for the same reasons. *Dec.*, ¶254.

CLAIM 17

See claim 12's mapping. Carey teaches the *backside surface* can comprise the *textured region* as shown, *e.g.*, in Carey's Figs. 2 and 7. *Carey*, Fig. 2, 012:10-29,

Fig. 7, 021:13-20, 016:13-15, 027:4-5; *Dec.*, ¶255. A POSITA would have found this arrangement desirable to scatter light at the backside surface, such that the path light travels back through the device is longer, increasing efficiency. *Carey*, 011:11-012:29; *Dec.*, ¶255.

CLAIM 19

See claims 12-13 and 17's mapping. *Dec.*, ¶256.

CLAIM 20

See claim 15's mapping. *Carey*'s backside textured region 78 (Fig. 7) is also referred to interchangeably as both a "textured region" and a "textured *layer*", where a POSITA would understand a layer is a *film*. *Carey*, Fig. 7, 021:15-16; *Dec.*, ¶257.

CLAIM 21

See claim 16 and 20's mapping. *Dec.*, ¶258.

CLAIM 22

See claim 19's mapping. *Dec.*, ¶259.

Carey, Fig. 2 illustrates a pixel's cross-section:

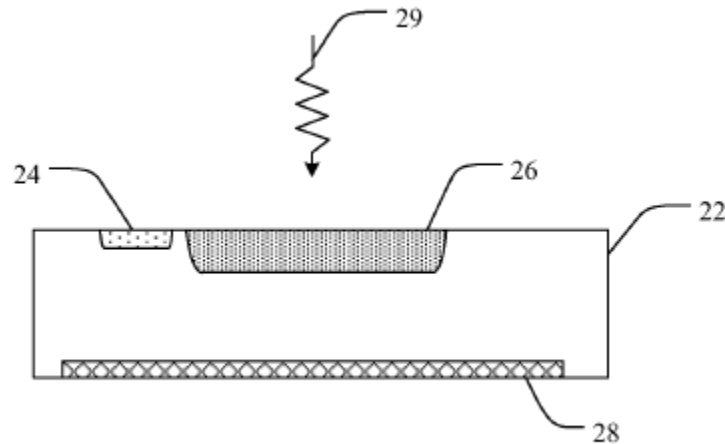


FIG. 2

Carey, Fig. 2; Dec., ¶259. In Fig. 2, light 29 impinges on the front surface of the device, and “[e]lectromagnetic radiation that passes through the silicon material to contact the textured region can be reflected back through the silicon material, thus effectively increasing the absorption path length of the silicon material.” Carey, 012:10-29; Dec., ¶259.

CLAIM 25

See Ground 1, claims 42 and 49’s mappings. Hwang-099, 5:52-58; Dec., ¶260.

CLAIMS 26, 28

Carey teaches that textured regions “can be formed by the irradiation of a laser pulse or laser pulses.” Carey, 006:33-7:10; 016:16-018:10; Dec., ¶¶261, 263. It would have been obvious to modify Hwang-099 to form the textured region via laser radiation do so because Carey expressly motivates the forming technique. *Id.* Moreover, Carey teaches laser radiation as one of a finite number of alternatives for

the formation of textured regions, which would have been carried out predictably, with a REOS based on Carey's direct teachings. *Dec.*, ¶¶261, 263. *See KSR*, 550 U.S. at 421.

CLAIM 27

Carey teaches using *reactive ion etching, chemical etching, nanoimprinting, and material deposition* to form a textured region. *Carey*, 016:16-19, 007:1-3, 007:13-15; *Dec.*, ¶262. It would have been obvious to do so because Carey expressly motivates the combination and using the claimed forming method. *Id.* Moreover, Carey teaches these methods as few of a finite number of alternatives for the formation of textured regions, which would have been carried out predictably, with a REOS based on Carey's direct teachings. *Dec.*, ¶262. *See KSR*, 550 U.S. at 421.

CLAIM 29

See claim 17's mapping. *Carey*, Fig. 2, 012:10-29, Fig. 7, 021:13-20, 016:13-15, 027:4-5; *Dec.*, ¶264.

CLAIM 65, 71

Claims 65 and 71 depend from claims 64 and 70, respectively, and recite "said trench isolation element has a depth in a range of about 100 nm to about 50 microns." *Dec.*, ¶265.

Carey teaches a depth of the silicon photodiode of about 1 to 50 microns, and it would have been obvious to have Hwang-099's trench isolation element run for

this entire depth or a substantial portion of it. *Dec.*, ¶¶266-267.

Specifically, Carey teaches that the silicon material for its photodiode can have “a thickness of from about 1 μm to about 50 μm .” *Carey*, 013:26-27. Such thicknesses have the advantage of increasing operation speeds. *Carey*, 010:1-15; *Dec.*, ¶267. The “silicon material” is the material in which the photodiode is fashioned and is equivalent to the silicon material in which photodiodes are formed (145) in Hwang-099, which governs the depth of Hwang-099’s sidewall reflecting layers 220. *Carey*, 012:18-20; *Hwang-099*, 5:55-58, Fig. 2; *Dec.*, ¶267.

Furthermore, it would have been obvious for Hwang-099’s sidewall multi-layered reflection layer 220 to extend from the light incident surface to the backside surface (*i.e.*, the depth of the silicon material 145, or 1 to 50 microns per Carey) for the reasons provided above under Ground 2, claims 5 and 23. There would have been a REOS for the combination, at least because Carey teaches forming methods for the photodiode thickness (depth), where again, the silicone material for the photodiode is the same material as for the formed trench in Hwang-099. *Dec.*, ¶268.

CLAIM 66, 72

Hwang-099 teaches the claimed width as discussed under Ground 1, claim 44. *Dec.*, ¶269.

CLAIM 76, 78

Carey teaches that the peripheral isolation element comprises its textured

region in a dielectric material. *Carey*, 022:2-4; *Dec.*, ¶¶270-271. It would have been obvious based on Carey's suggestion to use an *isolation element with a textured region, e.g.*, in Hwang-099's silicon oxide layers, because these were obviously silicon dioxide (as explained above under Ground 1, claim 3 and Ground 2, claim 3), a well-known dielectric. *Dec.*, ¶271. Furthermore, a POSITA would expect a Carey textured layer as part of Hwang-099's peripheral isolation element to scatter incident light, causing a longer path length through the device and increasing efficiency when light reflects off the peripheral isolation element. *Carey*, 011:11-012:29; *Dec.*, ¶271. Thus, a POSITA would have been motivated to improve similar isolation elements in the same way, and there would have been a REOS at least because methods of texturing materials were well-known, and it would have merely required texturing grooves 205' in which the layers of sidewall multi-layered reflection layer 220 (*peripheral isolation element*) are formed. *Dec.*, ¶271.

CLAIMS 77, 79

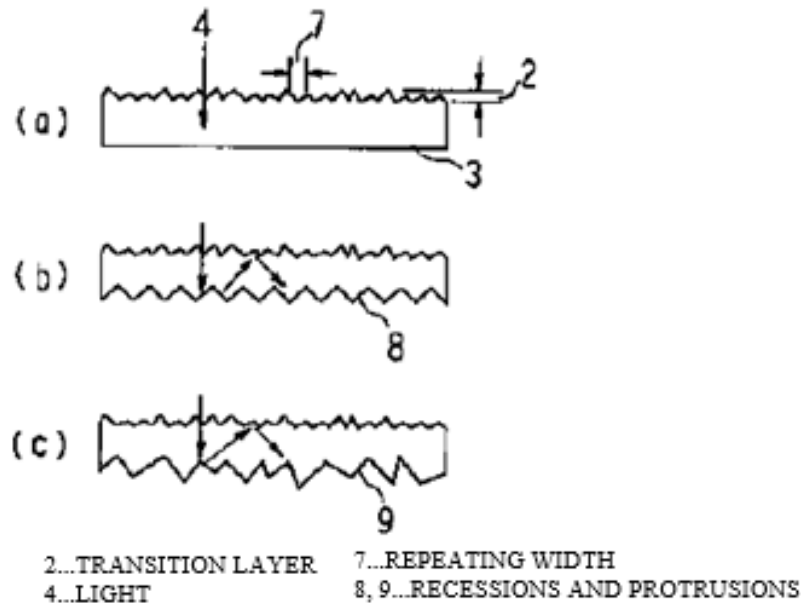
See claim 76. Based on Carey's suggestion to place textured layers in dielectric layers of peripheral isolation layers and the advantages of textured layers discussed in Carey, it would have been obvious, and a POSITA would have been motivated to place textured layers at the interface between Hwang-099's silicon oxide layers and the respectively-nearest pixel regions (*i.e., between the second layer and the other one of said adjacent pixels and between the first layer and one of said*

adjacent pixels), to cause diffuse scattering of light back into the pixel to occur at each such interface. *Dec.*, ¶¶272-273. A POSITA would have had a REOS, for the reasons discussed under claims 76 and 78, above. *Dec.*, ¶273.

Ground 6. Claims 12-17, 19-22, 25, 27, and 29 were obvious over Hwang-099 and Uematsu

Uematsu (Ex. 1070) is directed to photodetectors for detecting incoming light. *Uematsu*, Abstract, Title, ¶0001; *Dec.*, ¶¶274-276. Uematsu teaches that the efficiency of the conversion of light to electric charges “can be increased by effectively introducing light into the substrate and confining the light inside the substrate without allowing it to escape to the outside of the substrate.” *Uematsu*, ¶0002; *Dec.*, ¶276. To confine light into the substrate, Uematsu teaches forming certain textured regions (in Uematsu, “recesses and protrusions”) on the light-incident and backside surfaces, as shown, for example, in Figs. 7(b)-(c):

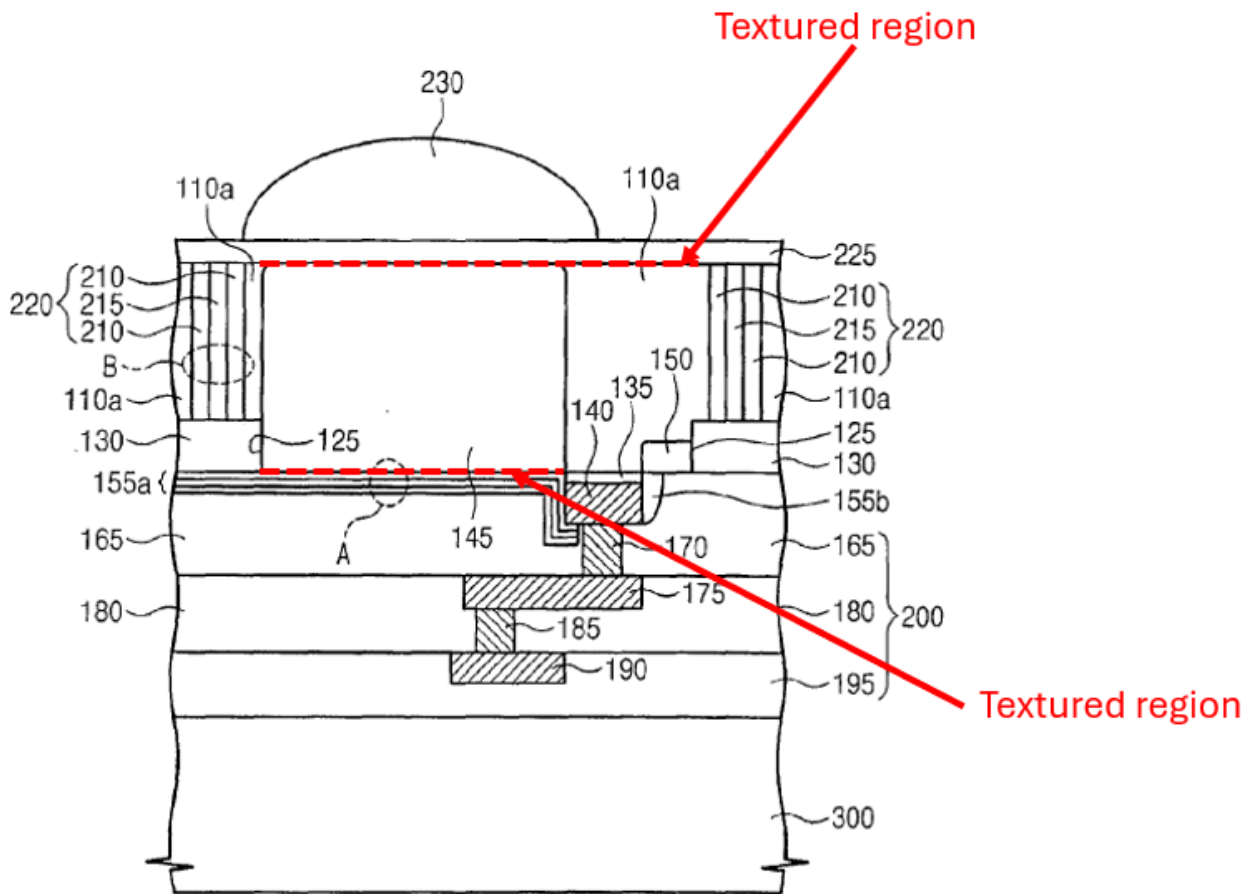
FIG. 7



Uematsu, Fig. 7, ¶¶0017-0018; *Dec.*, ¶276. As shown in Fig. 7, by forming layers of *Uematsu* in the specific manner *Uematsu* suggests, one can achieve an advantageous increase in the internal path length of the light, increasing efficiency. *Uematsu*, ¶¶0017-0018; *Dec.*, ¶276.

In addition to rationales that are specific to certain claims and provided under those claims, below, it would have been obvious to a POSITA to use *Uematsu*'s textured regions at the light-incident and/or backside surfaces of *Hwang-099*'s pixel to trap light within the pixel and increase the pixel's efficiency, as taught by *Uematsu*. *Uematsu*, ¶¶0014, 0018, 0024-0027, Fig. 12. A POSITA would have been motivated to provide textured regions of *Uematsu* at *Hwang-099*'s light-incident and/or backside layers, as shown here:

Fig. 2



Dec., ¶277.

A POSITA would have found it obvious to use one or both of these textured regions to increase efficiency, as taught by Uematsu, with a REOS at least because Uematsu teaches standard formation techniques for its textured regions, and states that they can be “easily formed”. *Uematsu*, ¶¶0019-0022; *Dec.*, ¶278. In Hwang-099, it would have been obvious based on Uematsu to form textured layers either in the silicon of layers 110a/145 itself, or as an additional film on the surfaces of these layers. *Uematsu*, ¶¶0019-0022; *Dec.*, ¶278.

CLAIM 12

It would have been obvious to incorporate Uematsu's textured region in at least one pixel of Hwang-099's device, at the light-incident and/or backside surface, based on Uematsu, as discussed above on pp. 59-61. *Dec.*, ¶279.

A POSITA would have been motivated to include a *textured region*, per Uematsu, coupled to the *light incident surface* to increase the light collection efficiency of Hwang-099's *pixel*. Per Dr. Shanfield, it was well-known that “[i]ncident light to a planar surface of silicon reflects, and reflected light does not contribute to the photocurrent.” *Dec.*, ¶280 (citing *Mita*). Textured regions on the light incident surface a well-known approach to increase the amount of light collected by semiconductor devices. *Dec.*, ¶280. Per Dr. Shanfield, a POSITA would have known that adding Uematsu's textured region coupled to Hwang-099's *light incident surface* would have diffusely scattered incident light such that less light was reflected off the light incident surface, thereby increasing the collection efficiency of Hwang-099's *pixel*. *Dec.*, ¶280. The modification is application of a known technique (adding a textured region to the light incident surface per Uematsu) to a known device (image sensor) ready for improvement to yield the predictable result of increasing light collection efficiency. *Dec.*, ¶¶280-282. The modification would have had a REOS because methods of forming textured regions coupled to the light incident surface were well-known. *Dec.*, ¶¶280-282 (citing *Konno, Smith*).

A POSITA would have been motivated to modify Hwang-099's *backside surface to comprise textured region*, per Uematsu. A POSITA would have been motivated to provide a backside layer comprising Uematsu's textured layer in Hwang-099's pixel to scatter light back into the pixel and thus improve efficiency, improving similar pixels in the same way. *Uematsu*, ¶¶0017-0018, 0027; *Dec.*, ¶¶281-282. Per Dr. Shanfield, providing a textured region on the backside surface would have enhanced internal reflection of incident light within Hwang-099's pixel. *Uematsu*, ¶0018, Fig. 7; *Dec.*, ¶¶281-282. A POSITA would have understood that compared to a smooth surface, Uematsu's textured region would have diffusely scattered incident light, thereby increasing the path length of light throughout the geometry of the pixel. *Dec.*, ¶¶281-282. Further, a POSITA would have appreciated that Uematsu's textured region would have worked in conjunction with Hwang-099's base multi-layered reflection layer to increase the amount of incident light reflected toward photodiode 145, in part by increasing the range of angles at which light reflects back into the pixel. *Dec.*, ¶¶281-282. Thus, the modification would have predictably increased the quantum efficiency of Hwang-099's pixel. *Dec.*, ¶¶281-282. The modification is nothing more than application of a known technique (providing a textured region per Uematsu) to a known device (image sensor) in the same way. *Dec.*, ¶¶281-282.

CLAIM 13

See claim 12's mapping. It would have been obvious to incorporate Uematsu's textured region in at least one pixel of Hwang-099's device *coupled to the light incident surface*. Uematsu teaches that the textured layer can be formed in the light-incident surface in a manner that facilitates internal reflection to increase efficiency. *Uematsu*, ¶¶0017-0018; *Dec.*, ¶283.

CLAIM 14

See claim 13's mapping. The combination teaches that the light-incident surface can *comprise the textured region*. *Uematsu*, ¶0006 (“recesses and protrusions provided on the substrate front surface”); ¶¶0017-0024, Figs. 7-12; *Dec.*, ¶284.

CLAIM 15

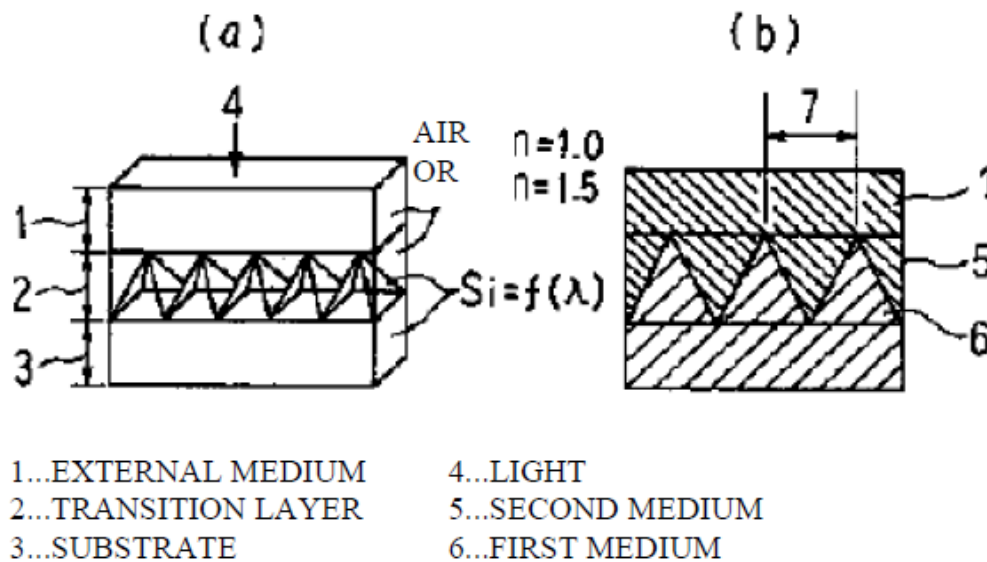
See claims 13's mapping. Uematsu teaches that its front-surface textured region can be “minute recesses and protrusions 11' of irregular size...formed by a deposited **film** using CVD (chemical vapor deposition).” *Uematsu*, ¶0021, Fig. 9; *Dec.*, ¶285. It would have been obvious to do so because Uematsu expressly teaches it. *Id.* Moreover, Uematsu teaches the method as one of a finite number of alternatives for the formation of textured regions, which would have been carried out predictably, with a REOS based on Uematsu's direct teachings. *Dec.*, ¶285. See *KSR*, 550 U.S. at 421. A POSITA would have been motivated to use this method

disclosed by Uematsu to achieve the efficiency advantages described by Uematsu.
Uematsu, ¶¶0017-0018, Fig. 7; *Dec.*, ¶285.

CLAIM 16

See claim 15’s mapping. Per Uematsu, “material of the film that was used was a material that is transparent and has a relatively high refractive index such as ITO or ZnO₂.” *Uematsu*, ¶0021; *Dec.*, ¶286. Such a layer comprises the *metals* indium and tin or zirconium. Uematsu also teaches using a fill material over the texturing. *Id.* The fill material can be SiO₂ formed by spin coating, CVD, or the like. *Id.* An example of a fill material (second medium 5) is shown in Fig. 1(b):

FIG. 1



Uematsu, Fig. 1(b), ¶¶0012-0013, 0021, 0008; *Dec.*, ¶286. The fill material conforms to the surface of the textured layer, and thus itself becomes a textured layer

with a complementary shape. *Dec.*, ¶286. A POSITA would have been motivated to use this method because it is expressly disclosed by Uematsu for the light-transparency of the materials, and to achieve the efficiency advantages described by Uematsu. *Uematsu*, ¶¶0017-0018, Fig. 7; *Dec.*, ¶287. This method of formation, moreover, is one of a finite number of known alternatives disclosed by Uematsu that would be implemented without unexpected results. *KSR*, 550 U.S. 398, 417-21. *Uematsu*, ¶0021, Fig. 9; *Dec.*, ¶287. A POSITA would also have had a REOS for at least these reasons, and because of Uematsu's express recommendation. *Dec.*, ¶287.

CLAIM 17

See claim 12's mapping, discussing a backside surface comprising a textured region. *Dec.*, ¶288.

CLAIM 19

See the mappings of claims 12-13 and 17. *Dec.*, ¶289.

CLAIM 20

See claim 15 and 19's mapping. *Dec.*, ¶290.

CLAIM 21

See claim 16 and 20's mapping. *Dec.*, ¶291.

CLAIM 22

See claim 19's mapping. *Dec.*, ¶292.

Uematsu teaches the claimed reflection when textured layers are formed in the particular manner described by *Uematsu*. *Uematsu*, ¶¶0017-0018, 0022, Figs.

7a-c; *Dec.*, ¶292. In the Hwang-099–Uematsu combination, textured regions at least at the backside surface would reflect light back into Hwang-099’s pixel, as shown analogously in Fig. 7(c). *Uematsu*, ¶0018. *Dec.*, ¶292.

CLAIM 25

See Ground 1, claims 42 and 49’s mappings. *Hwang-099*, 5:52-58; *Dec.*, ¶293.

CLAIM 27

Uematsu teaches forming its textured region by chemical etching or material deposition. *Uematsu*, ¶¶0019, 0021-0022; *Dec.*, ¶294. A POSITA would have been motivated to use this method based on the express teaching of Uematsu, and to achieve the efficiency advantages described by Uematsu. *Uematsu*, ¶¶0017-0018, Fig. 7; *Dec.*, ¶294. This method of formation, moreover, is one of a finite number of known alternatives disclosed by Uematsu that could be implemented without unexpected results. *KSR*, 550 U.S. 398, 417-21. *Uematsu*, ¶0021, Fig. 9; *Dec.*, ¶294. For at least those reasons, and because of Uematsu’s express teaching, a POSITA would also have had a REOS. *Dec.*, ¶294.

CLAIM 29

See claim 17’s mapping. *Uematsu*, Figs. 7-12, Abstract, cl. 8, ¶¶0010, 0018-0019, 0022; *Dec.*, ¶295.

Ground 7. Claims 30, 32-34, 36-37 were obvious over Hwang-099 and

Callegari

The above-referenced claims were obvious over Hwang-099 (as described in Ground 1) and Callegari (Ex. 1074). *Dec.*, ¶296.

Claims 30, 32-34, and 36-37 recite the use of certain oxides, well-known for semiconductor fabrication, within the peripheral isolation element. These oxides include tantalum oxide (claims 30 and 34), lanthanum oxide (claims 32 and 36), and lanthanum aluminum oxide (claims 33 and 37). *Dec.*, ¶297.

It would have been obvious to a POSITA that there were a variety of oxide materials commonly-used in the semiconductor arts that provided electrical-insulation properties together with relatively low refractive indices and were thus suitable for use in Hwang's peripheral isolation element. *Dec.*, ¶¶298-300. Callegari, for example, teaches the use of tantalum oxide, lanthanum oxide, and lanthanum aluminum oxide in semiconductor fabrication. *Callegari*, 7:17-20; *Dec.*, ¶¶298-300. Callegari states that these materials were desirable as transistor gate oxides in semiconductors, a role that requires excellent electrical insulation properties. *Callegari*, 7:11-20, 1:58-2:17; *Dec.*, ¶¶298-300. Callegari specifically teaches the use of such materials in "sensor image array optoelectronic microelectronic fabrications", which are image sensors. *Callegari*, 6:5-17, *see also* 7:11-13, 4:3-8; *Dec.*, ¶¶298-300.

A POSITA would have found obvious the substitution of these materials for

the lower-refractive-index layers (*e.g.*, the claimed “first” and “second” layers of claims 1 and 18) of the peripheral isolation element of Hwang-099, based on their known insulating properties and refractive indices that would have made them obvious alternatives to silicon oxide in Hwang-099. *Callegari*, 4:66-5:8; *Dec.*, ¶¶301-303. The use of these oxides as one element of a peripheral isolation element (*e.g.* in place of silicon oxide) would thus be a substitution of familiar elements (tantalum oxide, lanthanum oxide, or lanthanum aluminum oxide for silicon oxide) having similar characteristics, according to known methods, and implemented with predictable results. *See KSR*, 550 U.S. at 414, 417. A POSITA would have had a REOS in using tantalum oxide, lanthanum oxide, and lanthanum aluminum oxide because these were well-known materials in semiconductor fabrication, with established deposition techniques. *Dec.*, ¶¶301-303.

CLAIMS 30, 32-34, 36-37

It would have been obvious to use any of tantalum oxide, lanthanum oxide, and lanthanum aluminum oxide in the first and second layers 210 of Hwang-099’s layer 220 for the reasons immediately above (pp. 68-68). *Dec.*, ¶304.

Ground 8. Claims 30-31, 34-35 were obvious over Hwang-099 and Forbes

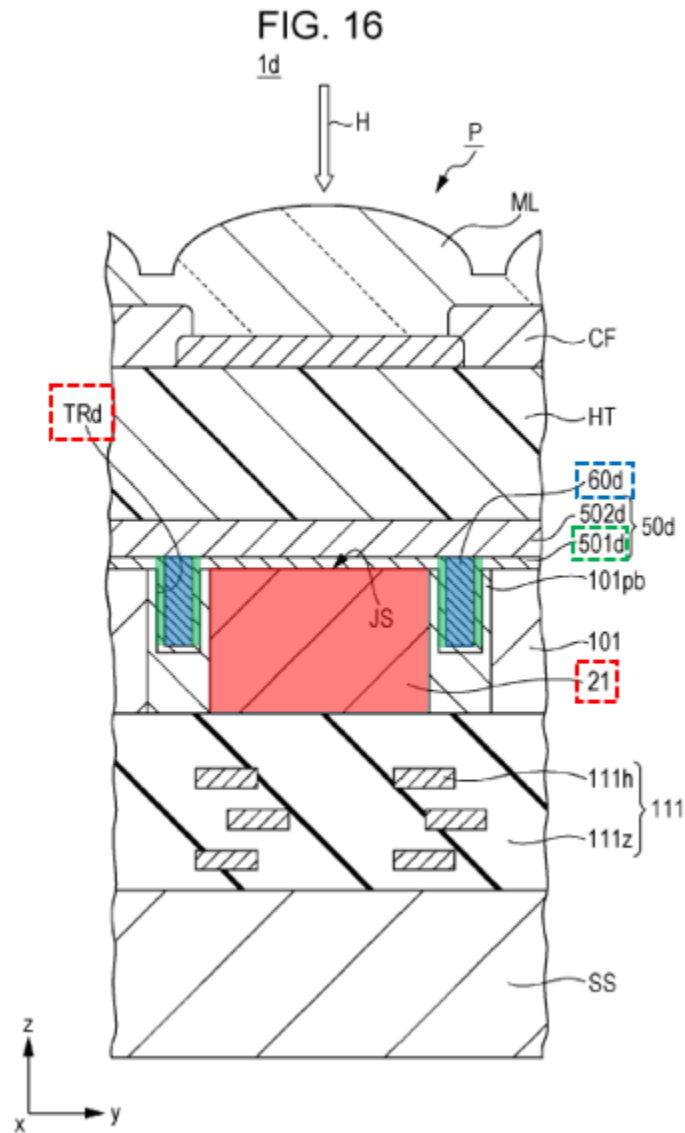
Claims 30-31 and 34-35 were obvious over Hwang-099 (as discussed in Ground 1) and Forbes (Ex. 1075). *Dec.*, ¶305.

Claims 30 and 34 require that the peripheral isolation element comprise

tantalum oxide, while claims 31 and 35 further specify that the tantalum oxide comprises tantalum aluminum oxynitride (TaAlON). Like the oxides discussed under Ground 7, TaAlON was also a well-known oxide useful in the semiconductor arts, as taught by Forbes. *Forbes*, Title, Abstract. Forbes teaches that TaAlON films are “for use in a variety of electronic systems and devices.” *Forbes*, Abstract, ¶¶0033, 0103; *Dec.*, ¶306. The use of TaAlON as one element of a peripheral isolation element (e.g. in place of silicon oxide) would thus be a substitution of familiar elements (TaAlON for silicon oxide) having similar characteristics, according to known methods, which could be implemented with predictable results. *See KSR*, 550 U.S. at 414, 417. A POSITA would have had a REOS at least because the methods of forming TaAlON were well-known and similar methods for layer formation had long been employed in semiconductor fabrication. *Dec.*, ¶306.

Ground 9. Claims 1-2, 6-8, 10-11, 18, 30, 34, 38-39, 42-46, 49-52, 58, 64, 67, 70 and 73 were obvious over Hiyama

Hiyama teaches a solid-state imaging device. *Hiyama*, Abstract, ¶0273; *Dec.*, ¶307. Hiyama’s Fig. 16 (below) shows a cross-section of an individual pixel (photodiode 21, highlighted red) and associated components, having peripheral isolation elements (TRd) containing lower-refractive-index layers 501d (green) and a higher-refractive-index layer 60d (blue) surrounding the pixel:



Dec., ¶307.

Hiyama nearly anticipates the challenged claims. This Ground is presented as one of obviousness for two principal reasons. *Dec.*, ¶308.

First, under claim 1[d] (“each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface,”) and the similar claim 18[d], it would have been obvious that layer 101 (which contacts

both surfaces) was formed with p-type doping (such that the entire photodiode 21 was doped) because this was standard for most image sensors. *Dec.*, ¶309 (citing *Hwang-099*, 5:52-6:6, *Shinohara*, ¶0058, Fig. 2, elements 23, 24, 25; *Cole*, ¶0045, Fig. 7, *Mouli* (Ex. 1010), 1:20-31, *Hwang-584* (Ex. 1013, ¶¶0007-0008)). It also would have been obvious that the photodiode region 21 consisted of a region that was p-doped and a region that was n-doped, because this was necessary for a PN junction in a photodiode. *Dec.*, ¶309.

Second, under claims 1[f], 18[f], a POSITA would have found it obvious to use known refractive indices for the materials of layers 501d and 60d, because these would have been the typical and would have been applied with predictable results. *Dec.*, ¶310; (citing *Aguilar-Frutis*, *Komuro*); *See KSR*, 550 U.S. 398, 417-21.

A POSITA would have had a REOS, because photodiodes in image sensors were commonly formed using a p-type layer having an n-type region within them, and the methods for producing such structures were well-known and predictable. *See, e.g.*, *Hwang-099*, 5:52-6:6, *Shinohara*, ¶0058, Fig. 2, elements 23, 24, 25; *Cole*, ¶0045, Fig. 7, *Mouli* (Ex. 1010), 1:20-31, *Hwang-584* (Ex. 1013) ¶¶0007-0008. A POSITA further would have had a REOS using known refractive indices for the materials in Hiyama's filled-groove TRd, because these would have been the typical and would have been applied with predictable results. *Dec.*, ¶311.

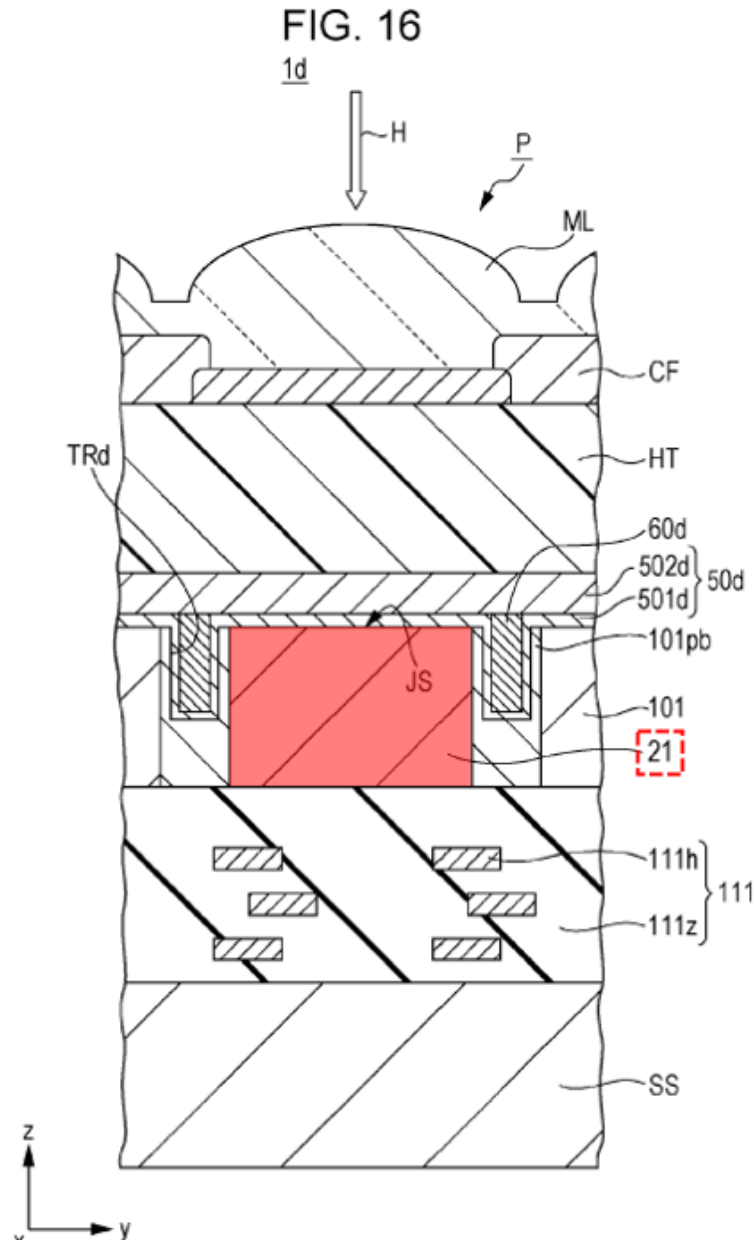
CLAIM 1

1[Pre] “An imager device, comprising:”

Hiyama teaches an *imager device* in the form of a solid-state imaging device. *Hiyama*, Abstract, ¶0273; *Dec.*, ¶312. Hiyama’s fourth embodiment (Fig. 16) is based on its first embodiment, and thus the description of the first embodiment applies to Fig. 16, except as Hiyama explains. *Hiyama*, ¶¶0273- 0275; *Dec.*, ¶312.

1[a] “at least two adjacent light sensitive image sensor **pixels**”

Hiyama teaches *at least two adjacent ... image sensor **pixels***. *Hiyama*, ¶¶0112-0114, 0294, 0081, 0182, 0213, Fig. 2, ¶¶0094, 0177; *Dec.*, ¶313. The pixel is Hiyama’s photodiode 21, as shown in Fig. 16:

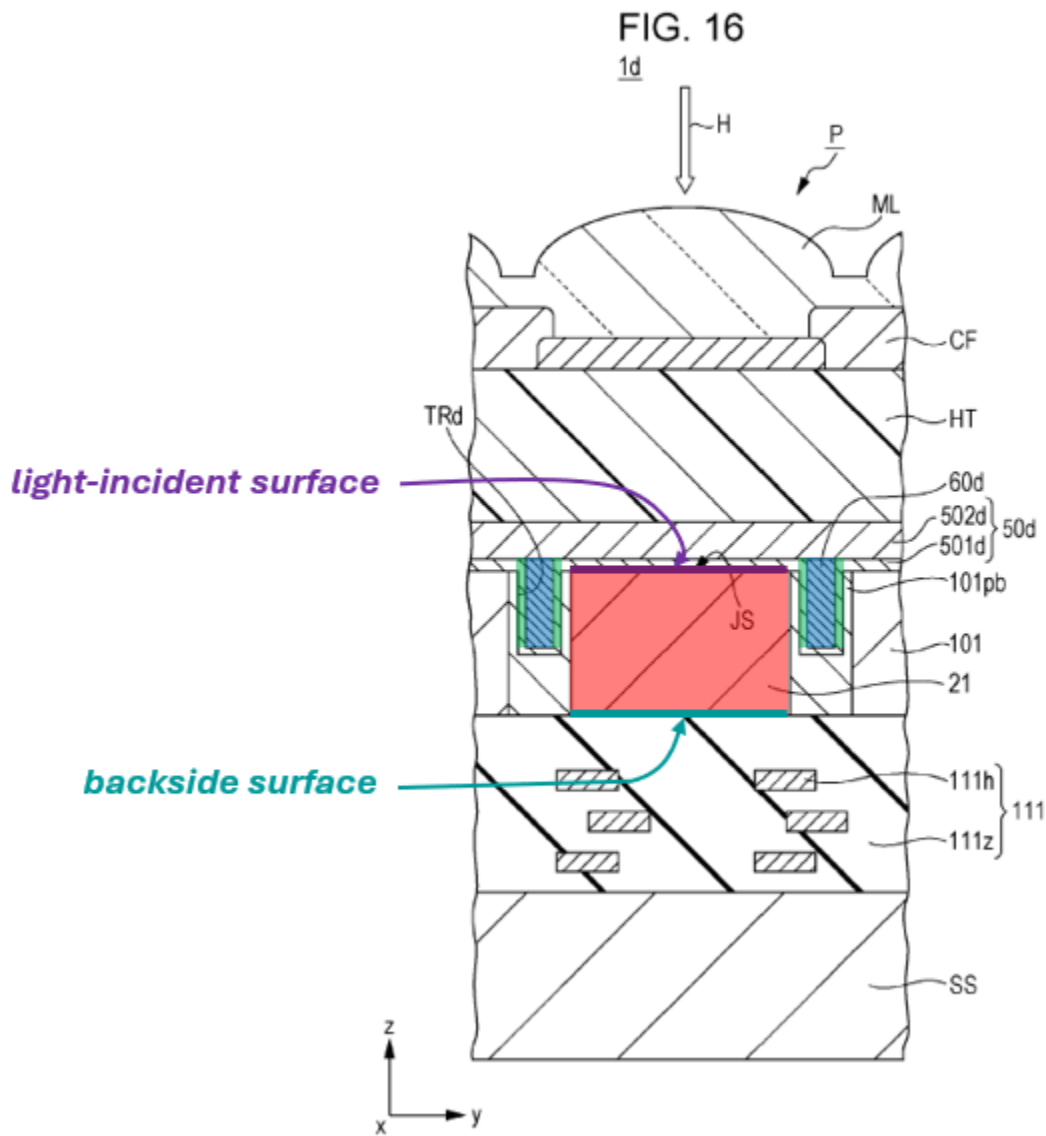


Hiyama, Fig. 16, ¶¶0075, 0112-0114; Dec., ¶313.

The pixels are *light-sensitive* because they are photodiodes that convert light into charge carriers. Hiyama, ¶0114; Dec., ¶314.

1[b] “each having a light incident surface, and a backside surface opposite the light incident surface;”

Fig. 16 illustrates the claimed surfaces:



Hiyama, Fig. 16; *Dec.*, ¶315. In Fig. 16, “incident light H” passes through a microlens (“ML”) and “is incident” on the “light sensing surface JS” of photodiode area 21, where it is converted to an electric signal. *Hiyama*, ¶¶0110, 0143, 0275, 0112-0114; *Dec.*, ¶315. For that reason, the surface at the top of photodiode area 21 is the *light-incident surface*, while the opposite surface is the *backside surface*.

Dec., ¶315.

1[c] “a peripheral isolation element at least partially separating said two adjacent light sensitive pixels;

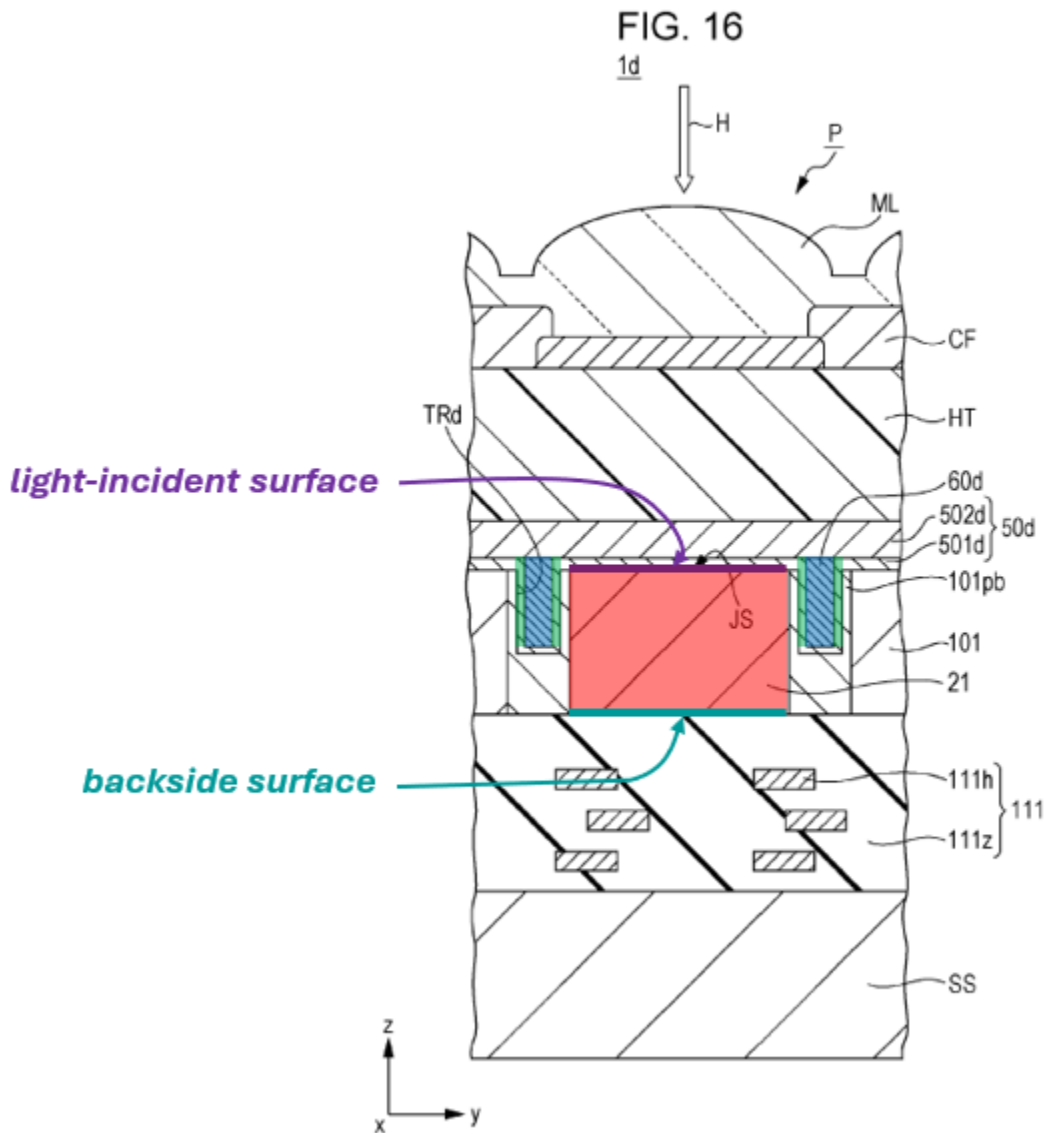
Hiyama teaches ***a peripheral isolation element at least partially separating said two adjacent light sensitive pixels***. Specifically, Hiyama teaches a groove TRd (Fig. 16, label on left side) that is filled with layers 501d and 60d, which comprises the ***peripheral isolation element***. *Hiyama*, Fig. 16, ¶0286; *Dec.*, ¶316. The peripheral isolation element is *at least partially separating said two adjacent light sensitive pixels*, because it is formed in the “pixel separation region” 101pb of Hiyama (*Hiyama*, ¶¶0117, 0283-0294), which is “interposed between the plurality of pixels P” in a grid pattern. *Hiyama*, ¶0118; *Dec.*, ¶316.

The filled groove TRd is peripheral because it is located at the sides of each pixel. *Dec.*, ¶317. Further, groove TRd is an isolation element because it optically isolates neighboring pixels (*Hiyama*, ¶¶0294, 0150-0152); *Dec.*, ¶317 (*citing* ’359 Patent, 10:20-22).

1[d] “each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface,”

Hiyama teaches each of said pixels having at least one doped region (the photodiode 21) disposed on at least one of the ***light incident surface*** and the

backside surface. Hiyama, ¶0117. As discussed above on pp. 71-72 it was obvious to have the pixel be a *doped region*. The doped region is all of layer 101 including the photodiode 21 (shown in red in Fig. 16 below), and extends from, and thus is *disposed on*, both the *light-incident surface* to the *backside surface*:



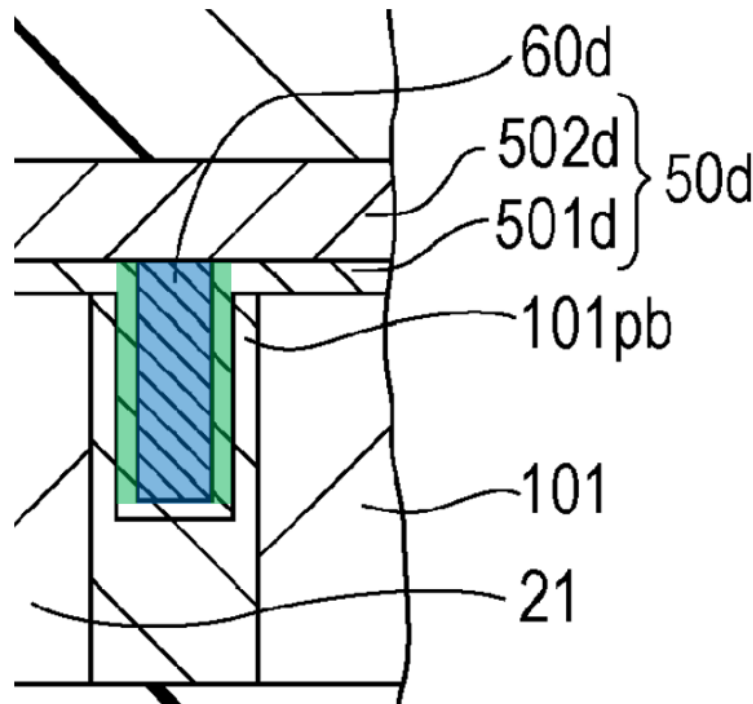
Dec., ¶318.

1[e] “wherein the peripheral isolation element comprises at least two materials having different indices of refraction,”

Hiyama teaches that *the peripheral isolation element* (groove TRd and materials 501 and 60d) *comprises at least two materials having different indices of refraction*, specifically a high- κ dielectric such as Al_2O_3 (or HfO_2 , or Ta_2O_5) as the material of layer 501, and tungsten as the material of layer 60d. *Hiyama*, ¶¶0152, 0200; *Dec.*, ¶319. In approximately the middle of the visible spectrum, Al_2O_3 has a refractive index of 1.7, HfO_2 has a refractive index of about 2.0, Ta_2O_5 has a refractive index of about 2.1, while the refractive index of Tungsten is about 3.5. *Dec.*, ¶319; (citing *Aguilar-Frutis, Komuro, Kasano, Iida*).

1[f] “wherein said peripheral isolation element comprises a first, a second and a third layer, wherein said third layer is disposed between said first and second layers, and wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer.”

Hiyama’s *peripheral isolation element* (groove TRd and materials 501 and 60d) has a *first, second and a third layer*, where the *first* and *second* layers are composed of the high- κ dielectric oxide of layer 501 (*e.g.*, Al_2O_3 , HfO_2 , or Ta_2O_5) and the *third*, middle layer is composed of tungsten, as shown in the annotated portion of Fig. 16:



Hiyama, Fig. 16; *Dec.*, ¶320.

As discussed immediately above, the *first* and *second* layers (e.g., Al_2O_3 , HfO_2 , or Ta_2O_5) exhibit an index of refraction less than an index of refraction of said *third* layer (Tungsten). *Dec.*, ¶321. Hiyama's method of forming such *first*, *second* and *third* layers, by filling a trench with a first material 501d and then a second material 60d is similar to that of the '359 patent, and would result in a similar layer structure. *Compare '359 Patent*, 13:12-28; *Dec.*, ¶322.

CLAIM 2

As discussed above under Ground 9, claims 1[e]-[f], the first and second layers have an index of refraction that is at least 0.2 lower relative to the refractive index of the third layer. *Dec.*, ¶323.

CLAIM 6

Hiyama teaches that the *first and second layers can comprise Al₂O₃*. Hiyama, ¶¶0152-0153, 0200; Dec., ¶324.

CLAIM 7

See Ground 9, claim 1[f]’s mapping. Hiyama, ¶¶0152, 0200; Dec., ¶325.

CLAIM 8

Hiyama teaches that “[t]he antireflection film 50J is formed by using a high dielectric having a **negative fixed electric** charge so that the occurrence of the dark current is suppressed”, which is a *passivating negative charge*. Hiyama, ¶0078, see also ¶¶0143, 0216, 0250; Dec., ¶326.

CLAIM 10

See Ground 9, claim 1[f]’s mapping. Dec., ¶327.

CLAIM 11

See Ground 9, claim 1[f]’s mapping. Hiyama, ¶¶0152, 0200; Dec., ¶328.

CLAIM 18

Claim 18 is nearly identical to claim 1, with three exceptions. Dec., ¶329.

First, the language of claim 1[d] has been moved to appear earlier in claim 18 than in claim 1, but this does not change the mapping. Dec., ¶330.

Second, the language in claim 1[c] has been changed as follows in claim 18: “~~at least partially~~ separating said at least two adjacent light sensitive pixels”. Hiyama meets the modified claim language for the same reasons explained above

under claim 1[c], because the filled-groove TRd separates at least two adjacent pixels. *Hiyama*, ¶¶0117-0118, Fig. 16; *Dec.*, ¶331.

Third, claim 18 requires that the peripheral isolation element must “reduce optical crosstalk therebetween”, where “therebetween” means between pixels. *Hiyama* teaches this. *Hiyama*, ¶0294; *Dec.*, ¶332. Per Dr. Shanfield, the difference in refractive index between layers 501d and 60d leads to reflection of light from the filled-groove TRd back into the pixel. *Dec.*, ¶332.

CLAIMS 30, 34

These claims recite the peripheral isolation element comprising tantalum oxide. *Hiyama* teaches this. *Hiyama*, ¶¶0152, 0200; *Dec.*, ¶335.

CLAIM 38, 45

Hiyama teaches these claims as discussed under claim 1[b] (semiconductor portion 101 providing surfaces) and claim 1[c] (isolates the semiconductor portions of adjacent pixels). *Hiyama*, ¶0294; *Dec.*, ¶336.

CLAIMS 39, 46

Hiyama teaches that filled groove TRd optically isolates pixels. *Hiyama*, ¶0294; *Dec.*, ¶337.

CLAIMS 42, 49

Hiyama teaches that its pixels are formed *monolithically in and on a common substrate*, as that term is used in the '359 patent. '359 Patent, 5:19-21; *Hiyama*,

¶0004 (“a plurality of pixels is arranged on a surface of a substrate”); *see also* ¶¶0093-0095, 0112-0113; *Dec.*, ¶333. The pixels are formed in semiconductor layer 101 and on the semiconductor substrate. *Hiyama*, ¶¶0075, 0107, 0289; *Dec.*, ¶333.

Hiyama further teaches the pixels are isolated from one another by said peripheral isolation element, per claims 1[c]’s mapping. *Hiyama*, ¶0294; *Dec.*, ¶334.

CLAIMS 43, 50

Hiyama teaches that said peripheral isolation element is a trench isolation element. *Hiyama*, ¶¶0285-0290; *Dec.*, ¶338.

CLAIMS 44, 51

Hiyama teaches the layers 501d have a thickness of 1 to 20 nm each, while the layer 60d has a thickness of 100 to 400 nm, such that Hiyama teaches a thickness range for the filled-groove TRd of 102 to 440 nm. *Hiyama*, ¶¶0144, 0179, 0293; *Dec.*, ¶339.

CLAIMS 52, 58

Hiyama teaches claims 52 and 58 because its semiconductor portions are silicon (*Hiyama*, ¶0093), but the first layer and second layer are Al₂O₃, HfO₂, or Ta₂O₅. *Hiyama*, ¶¶0143, 0145, 0200; *Dec.*, ¶340.

CLAIMS 64, 70

Hiyama teaches that its structures TRd are formed by making a groove (trench) and filling with first, second and third layers. *Hiyama*, ¶¶0288-0290; *Dec.*,

¶341.

CLAIMS 67 AND 73

Hiyama teaches that its filled groove TRd reflects at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel. *Hiyama*, ¶0294; *Dec.*, ¶342. Per Dr. Shanfield, the difference in refractive index between layers 501d and 60d leads to reflection of light from the filled-groove TRd back into the pixel. *Dec.*, ¶343.

Ground 10. Claims 1, 5, 18, 23-24, 38-41, 43, 45-48, 50, 55, 61, 68-69, 74-75, and 80-83 were obvious over Hiyama and Cole.

Cole is summarized under Ground 3. Petitioners present two obviousness contentions. First, Cole provides additional motivation for the contention of Ground 9 that it would have been obvious to form Hiyama's layer 101 with p-type doping and an n-type internal region because Cole's pixel is formed with "a p-type surface layer 424 and an n-type photodiode region 426" (*Cole*, ¶0044), shown as red and blue regions in Fig. 7:

TRd of Hiyama, the layer ordering of Hiyama's filled groove TRd would be:

SiO ₂	Al ₂ O ₃	Tungsten	Al ₂ O ₃	SiO ₂
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Dec., ¶347. With this peripheral isolation structure, the core of Hiyama's filled groove TRd (Al₂O₃-Tungsten-Al₂O₃) remains the same. Specifically, the Al₂O₃ layers are still the "first" and "third" layers of claims 1 and 18, and the tungsten layer is still the "second" layer (Petitioner notes that certain dependent claims, below, provide for alternative mappings). This ground would add SiO₂ layers on the outside of Al₂O₃ layers of Hiyama, adjacent to the pixels, which would have been obvious for the reasons provided above. *Dec.*, ¶348.

Cole further motivates the combination with its embodiment of Fig. 6, in which a five-layer isolation structure is used:

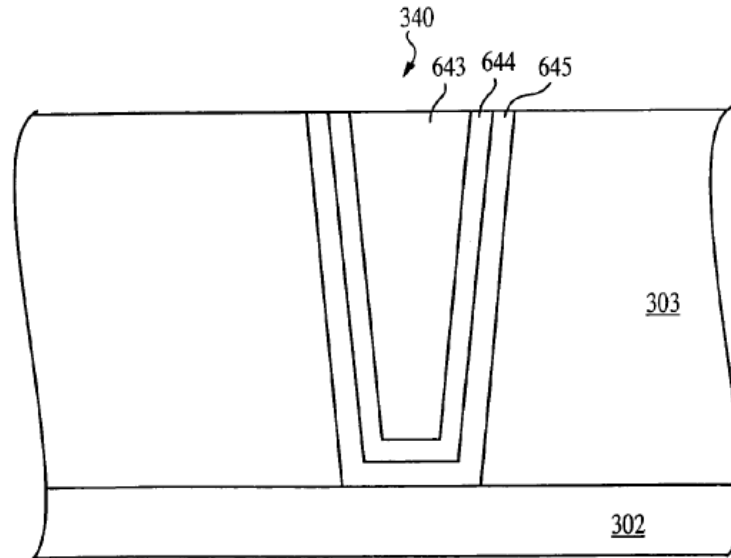


FIG. 6

Cole, Fig. 6, ¶0042; *Dec.*, ¶349. *Cole* explains, “[m]aterials 643, 644, and 645 have different refractive indices”, where 643 has the highest, 644 the next highest, and 645 the lowest, such that the structure reflects away photons. *Cole*, ¶0042; *Dec.*, ¶349.

A POSITA would have been motivated to provide for a thermal oxide (SiO_2 formed by oxidation at heat), as expressly recommended by *Cole* (*Cole*, Abstract, ¶0039), as the outside layers of Hiyama’s isolation structure. *Dec.*, ¶350. Using outer SiO_2 layers would have improved electrical isolation, protected the interior materials from chemical reaction (*Cole*, ¶¶0035, 0039), and implemented *Cole*’s recommendation to configure a five-layer isolation structure with three materials having different refractive indices in order to reflect light, where the refractive indices are highest in the middle (tungsten, $n=3.5$), next-highest in the Al_2O_3 layers

($n=1.76$), and lowest in the outer, SiO₂ layers ($n=1.45$). *Cole*, ¶0042; *Dec.*, ¶350. A POSITA would have reasonably expected success in using SiO₂ in the outer layer because the use of SiO₂ as a thermal oxide and in peripheral isolation elements was well-known and predictable. *Dec.*, ¶351.

CLAIMS 1, 18

The combination meets claims 1 and 18 in the same manner discussed in Ground 9 (i.e., with an unaltered layer structure in Hiyama), with the exception that Cole provides further motivation for Ground 9's obviousness argument (pp. 71-72) with respect to the doping of Hiyama's photodiode 21. *Dec.*, ¶352.

ISOLATION CLAIMS: 5, 23, 38-40, 43, 45-47, 50, 68-69, 74-75

The isolation claims would have been obvious over Hiyama in view of Cole for the reasons provided under Ground 3, pp. 36-41. Specifically, Cole motivates extending isolation structures (like Hiyama's filled groove TRd) from Hiyama's light-incident surface to the backside surface, to ensure that Hiyama's peripheral isolation element (TRd) electrically and optically isolates adjacent pixels. Cole, ¶¶0005, 0038-0039, 0042, 0045, Figs. 6, 7; *Dec.*, ¶¶353-354. The analysis under Ground 3 (with the exception of the reference to Hwang-099's Fig. 6) does not change with Hiyama as the base reference, because both Hwang-099 and Hiyama are similar image sensors having arrays of pixels with the need to avoid crosstalk. *Hwang-099*, 10:19-40; *Hiyama*, ¶0294; *Dec.*, ¶¶354-355. Petitioners thus

incorporate the motivations and rationale for obviousness provided in Ground 3.
Dec., ¶¶354-355.

CLAIM 24

The modified Hiyama structure meets claim 24 because it has both silicon dioxide and aluminum oxide in the peripheral isolation element. This structure would also meet independent claim 18, and in particular limitation 18[c], because these two materials have different indices of refraction (1.45 and 1.7, respectively).
Dec., ¶¶356-357.

CLAIMS 41, 48

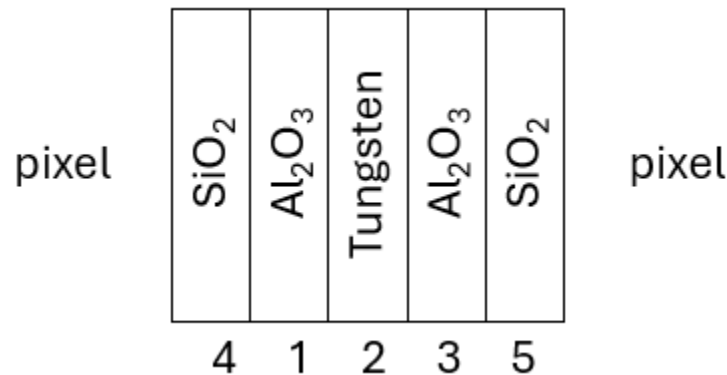
Hiyama teaches semiconductor portion 101 of the pixels is single-crystal silicon with a refractive index of 3.6. *Hiyama*, ¶¶0093, 0217; *Dec.*, ¶358. The layers of the peripheral isolation element, in contrast, are tungsten, Al₂O₃, and SiO₂, with refractive indices of 3.5, 1.7, and 1.45, respectively. *Dec.*, ¶359. As taught by Cole, the different refractive indices, highest in the middle and lowest at the outsides, would cause a reflective surface, resulting in optical isolation. *Cole*, ¶0042; *Dec.*, ¶359.

CLAIMS 55, 61, 80-83

Regarding claims 55, 61, 80 and 82, the modified Hiyama groove TRd described above would contain five layers. *Dec.*, ¶360.

Regarding claims 81 and 83, in the modified Hiyama groove TRd described

above, the first and third layers are Al_2O_3 , while the second layer is tungsten, as explained above under Grounds 9. The fourth and fifth layers, which are outside layers and thus disposed between the [first/second] layer and one of said adjacent pixels, are the SiO_2 layers, as shown in the illustration below. *Dec.*, ¶361.



Dec., ¶361.

Ground 11. Claim 9 was obvious over Hiyama and Werner

Claim 9 was obvious over Hiyama and Werner (Ex. 1067). *Dec.*, ¶¶362-363.

Surface recombination velocity (“SRV”) is a measure of the rate at which charge carriers recombine at a surface. This rate tends to be higher at the interface between two different materials, because where the materials meet, there can be defects creating interface states that make recombination more efficient. When charge-carrier recombination occurs, charge carriers that would otherwise be measured as an analog to incoming light will be rendered immobile, which in turn lowers the accuracy of the image sensor. Thus, lowering surface recombination

velocity was desirable. *Dec.*, ¶364.

Hiyama has a material interface with the potential for defects where Hiyama's filled-groove TRd contacts Hiyama's Silicon layer 101. As discussed above under Ground 4, claim 6, and claim 1 element [1d], Hiyama teaches a peripheral isolation element that has outer layers 501d made from Al₂O₃. *Hiyama*, ¶¶0150-0152, 0200. The Al₂O₃ is deposited using Atomic Layer Deposition (ALD). *Hiyama*, ¶0196, 0218, and once deposited, forms an interface with the single-crystal Silicon of layer 101. *Hiyama*, ¶0093. *Dec.*, ¶365.

Werner is a technical journal article that teaches using ALD to produce Al₂O₃ layers with a high negative fixed charge density of on single-crystal Silicon (c-Si) to achieve surface recombination velocities of under 10 cm/s. *Werner*, Abstract, pp. 1-3, Fig. 4; *Dec.*, ¶366.

It would have been obvious to apply Werner in the Fig. 16 embodiment of Hiyama, to produce Al₂O₃ layers (layers 501d) with high negative fixed-charge densities and low SRVs (*e.g.*, 10 cm/s). Hiyama already uses Al₂O₃ in contact with c-Si produced by ALD, and having negative fixed charges. *Hiyama*, ¶¶0143, 0150-0152, 0200, 0216, 0250. Werner demonstrates that low SRVs can be "routinely" achieved using similar techniques. *Werner*, p. 3, Abstract. A POSITA would have found the application of those techniques desirable, and would have a REOS in producing SRVs as low as 10 cm/s and thereby improving image sensor accuracy,

at least because the ALD-based methods were well-known and predictable. '359
Patent, 9:57-60; *Dec.*, ¶367.

VI. DISCRETIONARY DENIAL

A. General Plastic

General Plastic factor 1 (GP1) outweighs the other factors unless the same petitioner (or petitioner having a significant relationship to that petitioner) previously filed a petition against the same claim(s). *GP*, 4; *Valve*, IPR2019-00062, Paper 11, 9-10; *Videndum*, IPR2023-01218, Paper 12, 6. Samsung is the first petitioner (IPR2025-00162 and -00163); Apple/Sony is the second.

Apple/Sony began independently preparing this IPR in September 2024 and was not involved with Samsung's IPR. *fubotv*, IPR2024-00919, Paper 14, 27-28; *Luminex*, IPR2024-00101, Paper 20, 9.

Apple/Sony are not Samsung's co-defendants. Their respective petitions result from SiOnyx's litigations. *Ancora*, IPR2021-00663, Paper 17, 10-11.

Sony supplies Samsung and Apple. At the same time, Sony and Samsung offer competing image-sensors. SiOnyx accuses Sony's and Samsung's image sensors in Samsung's litigation, but a different Sony (and other suppliers') sensor(s) in Apple's litigation. Exs. 1015, 1016; Ex. 1065, 1-2; Ex. 1017, 1. Thus, Sony has a "strong and independent interest" in invalidating this patent. *Luminex*, 14; *Samsung*, IPR2022-00615, Paper 20, 17-18. Apple has its own interest as a direct competitor

of Samsung defending litigation involving different products. *Ford*, IPR2023-00763, Paper 28, 3; *Greenthread*, IPR2024-00551, Paper 26, 10.

Sony is not an exclusive supplier. Thus, Sony has no exclusive relationship with Samsung—there is no proxy relationship. *Luminex*, 11; *WesternGeco*, 889 F.3d at 1321-22.

Neither Sony nor Apple is indemnifying Samsung, nor would that create an RPI/proxy relationship. *Luminex*, IPR2024- 00101, Paper 20, 12-13.

The petition Samsung ranked first, IPR2025-00162, presents different principal prior and different secondary references, except for the Shinohara reference. Samsung's second-ranked petition does rely on Hwang-099 as a principal reference, but not Hiyama, and has only one secondary reference in common (Shinohara). Hwang-099 does not demonstrate copying. *Signify*, IPR2023-00213, Paper 16, n.13; *Theta*, IPR2024-00819, Paper 12, 17; *Ascend*, IPR2024-00948, Paper 10, 32-34.

Consequently, GP1 is unmet, ending the analysis. However, the other factors all favor institution.

GP2: Apple/Sony independently identified Hwang-099 and started preparing this IPR before Samsung's IPR was filed.

GP3: PO has not filed a preliminary response in Samsung's IPR.

GP4-5: Apple/Sony started this Petition after Apple was sued. This technology

is complex, and the prior art is extensive. Petitioners know of no case finding 6-7 months an undue delay in filing.

GP6-7: This Petition is not redundant, respecting the Board's finite resources. No roadblocks prevent a timely decision. *Honda*, IPR2018-00348, Paper 10, 19-20.

GP8-9: not applicable, as denial would prejudice Petitioners. *Id.*, 20-21.

B. Advanced Bionics

Advanced Bionics/Becton Dickinson favor institution—*Advanced Bionics* Part 1 is unsatisfied.

The unpatentability bases here are materially different from Samsung's, as discussed under GP-1, above. Although Samsung presented Hwang-099 as a principal reference in its lower-priority petition, its IPR is pending, so none are considered "previously...presented[.]" *Verizon Connect*, IPR2023-01162, Paper 12, 16-18; *Alivacor*, IPR2023-00950, Paper 12, 51-54.

Of the nine references applied herein, six were not of record in the application that issued as the '359 patent. The two that were of record (Hiyama and Uematsu) were not discussed during prosecution, and were cited together with hundreds of other references. This petition, furthermore, demonstrates that the claims issued erroneously over the cited Hiyama art, and would not have been allowed over the uncited Hwang-099 prior art.

C. Fintiv

The parallel litigation against Apple only is early; there is no ITC litigation against Apple/Sony. A Scheduling Order was entered in February. No trial date is set. Discovery just commenced. Claim construction has not begun and a hearing is not until November. Dispositive motions are not due until September 2026. (Ex. 1018, 1; Ex. 1019, 15-16). A trial is likely as late as February 2027. (Ex. 1020, 36). Combined with the Petition's strength, *Fintiv* favors institution.

Pursuant to the Office's Interim Process Concerning Institution published March 26, 2025, Petitioners reserve the right to address in further briefing any discretionary denial issues raised by SiOnyx.

II. CONCLUSION

Petitioners respectfully request IPR of the Challenged Claims.

Respectfully submitted,

Date: April 16, 2025

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III. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1)

A. Real Party-In-Interest

Petitioners Apple Inc. and Sony Group Corporation are the real parties-in-interest. 37 C.F.R. § 42.8(b)(1). The other real parties-in-interest are Sony Semiconductor Solutions Corporation, Sony Semiconductor Manufacturing Corporation, Sony Corporation, Sony Corporation of America, and Sony Electronics Inc.

B. Related Matters

1. District Court Litigation Matters

The '359 Patent is presently the subject of a patent infringement lawsuit filed against Petitioner Apple Inc.:

SiOnyx, LLC v. Apple Inc., No. 1:24-cv-12354 (D. Mass. Sept. 12, 2024).

Additionally, Patent Owner has filed the following district court action against third-party Samsung:

SiOnyx, LLC v. Samsung Elecs. Co., Ltd., No. 2:24-cv-00291 (E.D. Tex. Apr. 30, 2024).

2. ITC Matters

Patent Owner maintains the following ITC action against third-party Samsung:

In the Matter of Certain Sensors with Pixels and Products Containing the Same, USITC Inv., No. 337-TA-1403, Apr. 30, 2024.

3. IPR Matters

Third-party Samsung has filed the following IPRs, each challenging Claims 1-30, 32, 34, 36, 38-83 of the '359 Patent:

Samsung Elecs. Co., Ltd. v. SiOnyx, LLC, IPR2025-00162 (PTAB Nov. 29, 2024) and IPR2025-00163 (PTAB Nov. 29, 2024).

C. Lead and Back-Up Counsel

Petitioners provide the following designation and service information for lead and back-up counsel. 37 C.F.R. §§ 42.8(b)(3) and (b)(4).

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing petition for *inter partes* review, together with all exhibits and other documents filed therewith, was served by USPS – Express Mail or service of equivalent reliability on April 16, 2025, on the Patent Owner’s counsel of record at the United States Patent & Trademark Office having the following address:

Troutman Pepper Locke LLP (Rochester)
70 Linden Oaks
Suite 210
Rochester, NY 14625
UNITED STATES

Date: April 16, 2025

/Matthew A. Smith/ (RN 49,003)

CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the foregoing petition for *inter partes* review contains 13,990 words according to the word processing program used to prepare it.

Date: April 16, 2025

/Matthew A. Smith/ (RN 49,003)

CLAIM LISTING APPENDIX

U.S. Patent No. 10,224,359 for Claims 1-83

Claim Designation	Claim Language
1[Pre]	“[1a]An imager device, comprising:”
1[a]	“at least two adjacent light sensitive image sensor pixels
1[b]	“each having a light incident surface, and a backside surface opposite the light incident surface;”
1[c]	“a peripheral isolation element at least partially separating said two adjacent light sensitive pixels;
1[d]	“each of said pixels having at least one doped region disposed on at least one of the light incident surface and the backside surface,”
1[e]	“wherein the peripheral isolation element comprises at least two materials having different indices of refraction,”
1[f]	“wherein said peripheral isolation element comprises a first, a second and a third layer, wherein said third layer is disposed between said first and second layers, and wherein each of said first and second layer exhibits an index of refraction less than an index of refraction of said third layer.”
2	“2. The device of 1, wherein the index of refraction of at least one of said first and second layer is at least 0.2 lower relative to the refractive index of the third layer.”
3	“3. The device of 1, wherein at least one of said at least two materials comprises silicon dioxide.”
4	“4. The device of 1, wherein at least one of said first and second layers comprises silicon dioxide.”
5	“5. The device of 1, wherein the isolation element extends substantially from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.”
6	“6. The device of 1, wherein at least one of the first and second layer comprises Al ₂ O ₃ .”
7	“7. The device of 1, wherein said peripheral isolation element comprises an oxide.”
8	“8. The device of 1, wherein said peripheral isolation element provides a passivating negative charge.”

9	“9. The device of 1, wherein said peripheral isolation element exhibits a surface recombination velocity as low as 10 cm/s.”
10	“10. The device of 1, wherein the peripheral isolation element comprises at least one material having an index of refraction of less than about 2.1.”
11	“11. The device of 1, wherein the peripheral isolation element comprises any of aluminum oxide and hafnium oxide.”
12	“12. The device of 1, wherein at least one of said two adjacent light sensitive pixels comprises a textured region.”
13	“13. The device of 12, wherein said textured region is coupled to the light incident surface.”
14	“14. The device of 13, wherein said light incident surface comprises said textured region.”
15	“15. The device of 13, wherein said textured region comprises a textured film layer.”
16	“16. The device of 15, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”
17	“17. The device of 12, wherein said backside surface comprises said textured region.”
18[Pre]	“An imager device, comprising:”
18[a]	“at least two adjacent light sensitive image sensor pixels”
18[b]	“each having a light incident surface, and a backside surface opposite the light incident surface;”
18[c]	“a peripheral isolation element separating said at least two adjacent light sensitive pixels so as to reduce optical crosstalk therebetween, said isolation element comprising at least two materials having different indices of refraction,”
18[d]	“at least one doped region disposed on at least one of the light incident surface and the backside surface,”
18[e]	“wherein said peripheral isolation element comprises a first, a second and a third layer, wherein said third layer is disposed between said first and second layers, and wherein each of said first and second layers exhibits an index of refraction less than an index of refraction of said third layer.”
19	“19. The device of 18, wherein at least one of said light incident surface and said backside surface of at least one of

	said two adjacent light sensitive pixels comprises a textured region.”
20	“20. The device of 19, wherein said textured region is a textured film layer.”
21	“21. The device of 20, wherein said textured film layer comprises any of silicon dioxide, silicon nitride, amorphous silicon, polysilicon, a metal and combinations thereof.”
22	“22. The device of 19, wherein said textured region reflects at least a portion of light internally incident thereon into the at least one pixel.”
23	“23. The device of 18, wherein the peripheral isolation element extends from the light incident surface to the backside surface of at least one of said two adjacent light sensitive pixels.”
24	“24. The device of 18, wherein said at least two materials comprises silicon dioxide and aluminum oxide.”
25	“25. The device of 19, wherein said at least two pixels are formed monolithically in a common semiconductor substrate.”
26	“26. The device of 19, wherein the textured region is formed by laser radiation.”
27	“27. The device of 12, wherein the textured region is formed by one of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.”
28	“28. The device of 12, wherein the textured region is formed by laser radiation.”
29	“29. The device of 12, wherein said textured region is coupled to the backside surface.”
30	“30. The device of 1, wherein said peripheral isolation element comprises tantalum oxide.”
31	“31. The device of 30, wherein said tantalum oxide comprises tantalum aluminum oxynitride.”
32	“32. The device of 1, wherein said peripheral isolation element comprises lanthanum oxide.”
33	“33. The device of 32, wherein said lanthanum oxide comprises lanthanum aluminum oxide.”

34	“34. The device of 18, wherein said peripheral isolation element comprises tantalum oxide.”
35	“35. The device of 34, wherein said tantalum oxide comprises tantalum aluminum oxynitride.”
36	“36. The device of 18, wherein said peripheral isolation element comprises lanthanum oxide.”
37	“37. The device of 36, wherein said lanthanum oxide comprises lanthanum aluminum oxide.”
38	“38. The device of 1, wherein each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface and said backside surface, wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”
39	“39. The device of 38, wherein said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”
40	“40. The device of 38, wherein said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”
41	“41. The device of 38, wherein an index of refraction of the semiconductor portion of each of said at least two adjacent image sensor pixels is different from indices of refraction of said layers of the peripheral isolation element such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.”
42	“42. The device of 1, wherein said at least two adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate and are isolated from one another by said peripheral isolation element.”
43	“43. The device of 1, wherein said peripheral isolation element is a trench isolation element.”
44	“44. The device of 1, wherein said peripheral isolation element has a width in a range from about 100 nm to about 50 microns.”
45	“45. The device of 18, wherein each of said at least two adjacent light sensitive image sensor pixels comprises a semiconductor portion providing said light incident surface

	and said backside surface, wherein said peripheral isolation element isolates the semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”
46	“46. The device of 45, wherein said peripheral isolation element optically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”
47	“47. The device of 46, wherein said peripheral isolation element electrically isolates said semiconductor portions of said at least two adjacent light sensitive image sensor pixels.”
48	“48. The device of 47, wherein an index of refraction of the semiconductor portion of each of said at least two adjacent image sensor pixels is different from indices of refraction of said layers of the peripheral isolation element such that light incident from each of said semiconductor portions on said peripheral isolation element is reflected, thereby providing optical isolation between the pixels.”
49	“49. The device of 18, wherein said at least two adjacent light sensitive image sensor pixels are formed monolithically on a common semiconductor substrate and are isolated from one another by said peripheral isolation element.”
50	“50. The device of 18, wherein said peripheral isolation element is a trench isolation element.”
51	“51. The device of 18, wherein said peripheral isolation element has a width in a range from about 100 nm to about 50 microns.”
52	“52. The imager device of 38, wherein at least one of the first layer and the second layer of said peripheral isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials.”
53	“53. The imager device of 1, wherein the first layer and the second layer of said peripheral isolation element comprise different materials.”
54	“54. The imager device of 1, wherein the peripheral isolation element comprises at least three materials.”
55	“55. The imager device of 1, wherein the peripheral isolation element comprises more than three layers.”
56	“56. The imager device of 1, wherein the peripheral isolation element comprises a light trapping material filling a trench.”

57	“57. The imager device of 56, wherein the trench is one of a shallow trench and a deep trench.”
58	“58. The imager device of 45, wherein at least one of the first layer and the second layer of the peripheral isolation element and said semiconductor portion of each of said at least two adjacent pixels comprise different materials.”
59	“59. The imager device of 18, wherein the first layer and the second layer of said peripheral isolation element comprise different materials.”
60	“60. The imager device of 18, wherein the peripheral isolation element comprises at least three materials.”
61	“61. The imager device of 18, wherein the peripheral isolation element comprises more than three layers.”
62	“62. The imager device of 18, wherein the peripheral isolation element comprises a light trapping material filling a trench.”
63	“63. The imager device of 62, wherein the trench is one of a shallow trench and a deep trench.”
64	“64. The imager device of 1, wherein said peripheral isolation element comprises a trench isolation element formed by filling a trench with said first, said second, and said third layers.”
65	“65. The imager device of 64, wherein said trench isolation element has a depth in a range of about 100 nm to about 50 microns.”
66	“66. The imager device of 65, wherein said trench isolation element has a width in a range of about 100 nm to about 10 microns.”
67	“67. The imager device of 1, wherein said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.”
68	“68. The imager device of 67, wherein the peripheral isolation element is further configured to optically isolate said two adjacent light sensitive pixels.”
69	“69. The imager device of 68, wherein the peripheral isolation element is further configured to electrically isolate said two adjacent light sensitive pixels.”
70	“70. The imager device of 18, wherein said peripheral isolation element comprises a trench isolation element formed

	by filling a trench with said first, said second, and said third layers.”
71	“71. The imager device of 70, wherein said trench isolation element has a depth in a range of about 100 nm to about 50 microns.”
72	“72. The imager device of 71, wherein said trench isolation element has a width in a range of about 100 nm to about 10 microns.”
73	“73. The imager device of 18, wherein said peripheral isolation element is configured to reflect at least a portion of light incident thereon from any of said two adjacent light sensitive pixels back to that pixel.”
74	“74. The imager device of 73, wherein the peripheral isolation element is further configured to optically isolate said two adjacent light sensitive pixels.”
75	“75. The imager device of 74, wherein the peripheral isolation element is further configured to electrically isolate said two adjacent light sensitive pixels.”
76	“76. The imager device of 1, wherein the peripheral isolation element comprises a textured region.”
77	“77. The imager device of 1, wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.”
78	“78. The imager device of 18, wherein the peripheral isolation element comprises a textured region.”
79	“79. The imager device of 18, wherein the peripheral isolation element further comprises a first textured region between the first layer and one of said adjacent pixels and a second textured region between the second layer and the other one of said adjacent pixels.”
80	“80. The imager device of 1, wherein the peripheral isolation element comprises five layers.”
81	“81. The imager device of 80, wherein the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second layer and the other one of said adjacent pixels.”

82	“82. The imager device of 18, wherein the peripheral isolation element comprises five layers.”
83	“83. The imager device of 82, wherein the five layers include the first layer, the second layer, the third layer, a fourth layer disposed between the first layer and one of said adjacent pixels and a fifth layer disposed between the second layer and the other one of said adjacent pixels.”

TABLE OF EXHIBITS

Exhibit numbers are chosen to match, to the extent possible, exhibit numbering in prior-filed, related IPR2025-00689.

Exhibit	Description
1001	U.S. Patent No. 10,224,359 (“the ’359 Patent”)
1002	File History of the ’359 Patent (Application No. 15/216,244)
1003	Declaration of Dr. Stanley Shanfield (“Dec.”)
1004	U.S. Patent No. 7,675,099 to Hwang et al. (“Hwang-099”)
1005	U.S. Patent Publication No. 2010/0302432 to Komuro (“Komuro”)
1006	Not submitted
1007	U.S. Patent Publication No. 2011/0019050 to Yamashita (“Yamashita”)
1008	U.S. Patent No. 7,709,775 to Konno et al. (“Konno”)
1009	U.S. Patent Publication No. 2009/0160000 to Kim (“Kim”)
1010	U.S. Patent No. 7,492,027 to Mouli (“Mouli”)
1011	Not submitted
1012	U.S. Patent Publication No. 2007/0108476 to Hong (“Hong”)
1013	Certified English Translation of Korean Patent No. 10-0688584 to Hwang (“Hwang-584”)
1014	Certain Sensors with Pixels and Products Containing the Same, Inv. No. 337-TA-1403, USITC Pub. 841145, Order No. 36: Construing Certain Claim Terms (January 15, 2025)

1015	SiOnyx, LLC vs. Samsung Electronics, CO., LTD. et al., Case No. 2:24-cv-00291-JRG (EDTX, Dkt. No. 4-9)
1016	SiOnyx, LLC vs. Samsung Electronics, CO., LTD. et al., Case No. 2:24-cv-00291-JRG (EDTX, Dkt. No. 4-10)
1017	SiOnyx, LLC v. Apple, Inc., Case No. 1:24-cv-12354 (D. Mass, Dkt. No. 22-4)
1018	SiOnyx, LLC v. Apple, Inc., Case No. 1:24-cv-12354 (D. Mass, Dkt. No. 53)
1019	SiOnyx, LLC v. Apple, Inc., Case No. 1:24-cv-12354 (D. Mass, Dkt. No. 51)
1020	D. Mass Local Patent Rules
1021	S. M. Sze & Kwok Ng, Physics of Semiconductor Devices (3rd ed. 2007) (“Sze”)
1022	James R. Janesick, Scientific Charge-Coupled Devices (2001) (“Janesick”)
1023	Alistair Sproul, Solar Cells: Resources for the Secondary Science Teacher, University of New South Wales (2003) (“Sproul”)
1024	U.S. Patent Publication No. 2007/0190681 to Lee et al. (“Lee”)
1025	R. Daniel McGrath, Image Sensor Technology, in Single-Photon Imaging 27 (Peter Seitz & Albert JP Theuwissen eds., 2011) (“McGrath”)
1026	Christopher Shea, A Silicon p-i-n detector for a hybrid CMOS imaging system, Rochester Institute of Technology, https://repository.rit.edu/theses/7116 (2012) (“Shea”)
1027	Photodiode Characteristics and Applications, OSI Optoelectronics (2005) (“OSI Whitepaper”)
1028	H. A. Macleod, Thin-Film Optical Filters (3rd ed. 2001) (“Macleod”)

1029	Misha Boroditsky, Regina Ragan & Eli Yablonovitch, Absorption Enhancement in Ultra-Thin Textured AlGaAs Films, 57 Solar Energy Materials and Solar Cells 1 (1999) (“Boroditsky”)
1030	Jan Provoost and Piet De Moor, Backside-illuminated image sensors: Optimizing manufacturing for a sensitivity payoff, https://www.vision-systems.com/print/content/16744520 (2011, retrieved February 24, 2025) (“Provoost”)
1031	A. Tournier et al., R 5 Pixel-to-Pixel Isolation by Deep Trench Technology : Application to CMOS Image Sensor (2011) (“Tournier”)
1032	Vyshnavi Suntharalingam, Dennis D. Rathman, Gregory Prigozhin, Steven Kissel, and Mark Bautz, Back-illuminated three-dimensionally integrated CMOS image sensors for scientific applications, Proc. SPIE 6690, Focal Plane Arrays for Space Telescopes III, 669009 (2007) (“Suntharalingam”)
1033	U.S. Patent No. 6,888,214 to Mouli et al. (“Mouli-214”)
1034	Kyriaki Minoglou et al., Reduction of Electrical Crosstalk in Hybrid Backside Illuminated CMOS Imagers Using Deep Trench Isolation, in IEEE 2008 International Interconnect Technology Conference 129 (2008) (“Minoglou”)
1035	U.S. Patent No. 6,710,370 to Street et al. (“Street”)
1036	U.S. Patent Publication No. 2004/0251513 to Su et al. (“Su”)
1037	Maximillian A. Perez et al., Rubidium Vapor Cell with Integrated Bragg Reflectors for Compact Atomic MEMS, 154 Sensors and Actuators A: Physical 295 (2009) (“Perez”)
1038	I. H. Malitson, Interspecimen Comparison of the Refractive Index of Fused Silica*,†, J. Opt. Soc. Am. 55 (1965) (“Malitson”)
1039 - 1047	Not submitted

1048	Yoshio Mita et al., Deep-Trench Vertical Si Photodiodes for Improved Efficiency and Crosstalk, 13 IEEE Journal of Selected Topics in Quantum Electronics 386 (2007) (“Mita”)
1049 - 1063	Not submitted
1064	U.S. Patent Publication No. 2008/0265349 to Kasano et al. (“Kasano”)
1065	Joint Statement Identifying Accused Products, In the Matter of Certain Sensors with Pixels and Products Containing the Same, USITC Inv., No. 337-TA-1403, Jan. 31, 2025 (Redacted)
1066	U.S. Patent Publication No. 2011/0241148 (“Hiyama”)
1067	Werner, et al., Very low surface recombination velocities on p- and n-type c-Si by ultrafast spatial atomic layer deposition of aluminum oxide, Appl. Phys. Lett. 97, 162103 (2010) (“Werner”)
1068	U.S. Patent Publication No. 2012/0033119 (“Shinohara”)
1069	PCT Pub. WO2011/160130 (“Carey”)
1070	Certified Translation of JPH06-244444 (“Uematsu”)
1071	U.S. Patent Publication No. 2006/0286766 (“Cole”)
1072	Not submitted
1073	Declaration of June Munford
1074	U.S. Patent No. 6,395,650 (“Callegari”)
1075	U.S. Patent Publication No. 2008/0121962 (“Forbes”)
1076	U.S. Patent No. 7,135,350 (“Smith”)
1077	M. Aguilar-Frutis, et al., Optical and electrical properties of aluminum oxide films deposited by spray pyrolysis, Appl. Phys. Lett., 72, 1700 (1998) (“Aguilar-Frutis”)

1078	U.S. Patent Publication No. 2011/0156186 A1 (“Iida”)
1079	Weiming He, et al., Atomic Layer Deposition of Lanthanum Oxide Films for High-k Gate Dielectrics, Electrochemical and Solid-State Letters, 7(7), G131 (2004) (“He”)
1080	Meza-Rocha, et al., Characterization of Lanthanum-Aluminum Oxide Thin Films Deposited by Spray Pyrolysis , ECS Journal of Solid State Science and Technology, 3 (2) N1-N6 (2014) (“Meza-Rocha”)
1081	U.S. Patent Publication No. 2011/002589 (“Hibbeler”)
1082	U.S. Patent No. 8,357,984 (“Mao”)