

Invalidity of U.S. Patent No. 10,877,233 (the “’233 Patent”) in View of

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

DS250DF810 was published in October 2019. DS250DF810 qualifies as prior art under at least 35 U.S.C. § 102(a) (AIA).

The Administrative Law Judge has not yet construed the claims and therefore the meaning of the terms in the claims has yet to be resolved. The support identified here for limitations of the Asserted Claims of the ’233 Patent is responsive to Complainant’s apparent infringement contentions in its Complaint, which Respondents disagree with. As such, nothing in Respondents’ claim charts should be construed as an admission regarding infringement, either literally or under the doctrine of equivalents, or as an admission regarding Respondents’ understanding of the proper scope of the Asserted Claims of the ’233 Patent.

All cross-references should be understood to include material that is cross-referenced within the cross-reference. Where a particular Figure is cited, the citation should be understood to encompass the caption and description of the Figure as well as any text relating to or describing the Figure. Conversely, where particular text referring to a Figure is cited, the citation should be understood to include the Figure as well. Respondents reserve the right to rely on additional citations or sources of evidence that also may be applicable, or that may become applicable in light of claim construction, changes in Complainant’s infringement and/or domestic industry contentions, and/or information obtained during discovery as the Investigation progresses.

To the extent Complainant alleges that DS250DF810 does not disclose any particular limitation of the Asserted Claims of the ’233 Patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the ’233 Patent to modify DS250DF810 and/or to combine the teachings of DS250DF810 with other prior art references, including but not limited to the prior art references cited in the Cover Pleading and the relevant section(s) of claim charts for other prior art references for the ’233 Patent in a manner that would have rendered the Asserted Claims invalid as obvious.

Because Complainant has yet to identify any limitation of the Asserted Claims of the ’233 Patent that it contends is not fully disclosed by DS250DF810, either alone or in combination with other prior art cited by Respondents, Respondents expressly reserve the right to rebut any such contention, including by identifying additional obviousness combinations, if any such contention is made by Complainant. Respondents further reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the Cover Pleading.

A. INDEPENDENT CLAIM 1

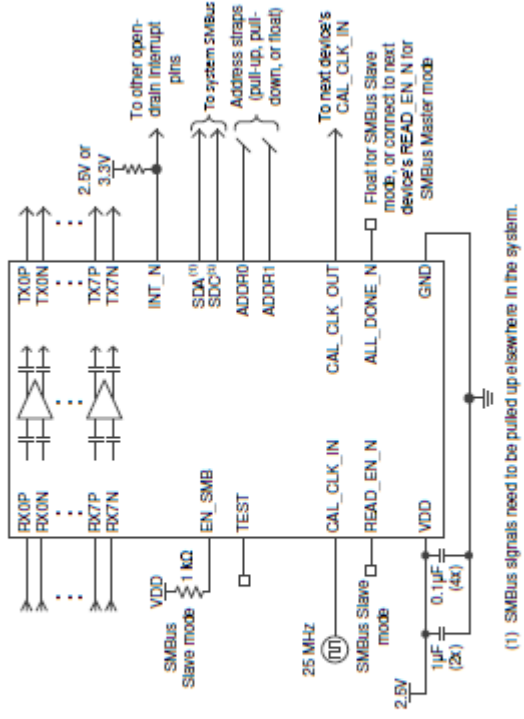
Claim 1

1 [pre] A cable that comprises:

Texas Instruments – DS250DF810 2.5 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

To the extent the preamble is limiting, DS250DF810 discloses and/or renders obvious this limitation.

4 Simplified Schematic



DS250DF810, 1.

Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

10.1 Application Information

The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

10.2 Typical Application

The DS250DF810 is typically used in the following main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port jitter cleaning / retiming for optical applications

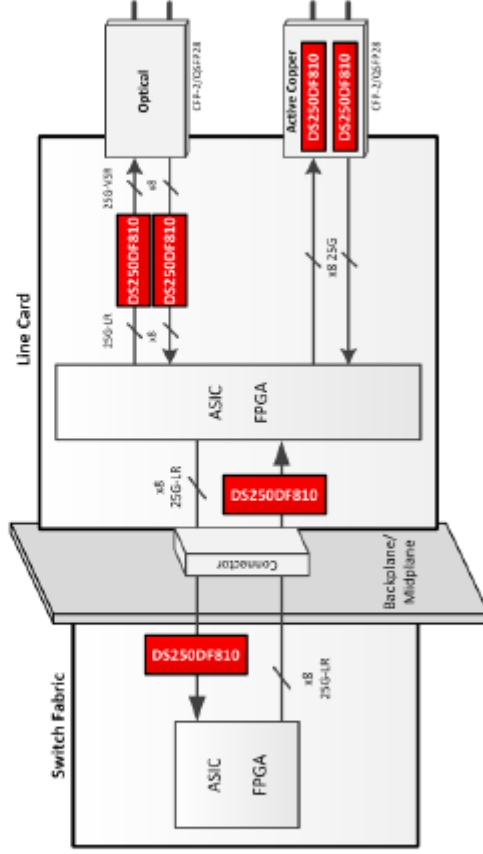


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

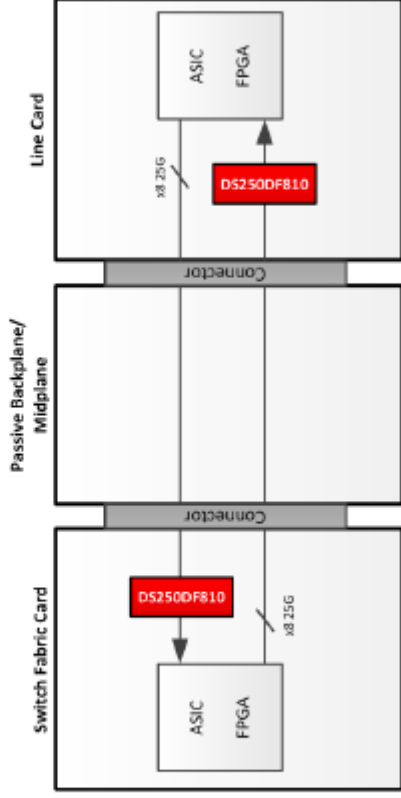


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7

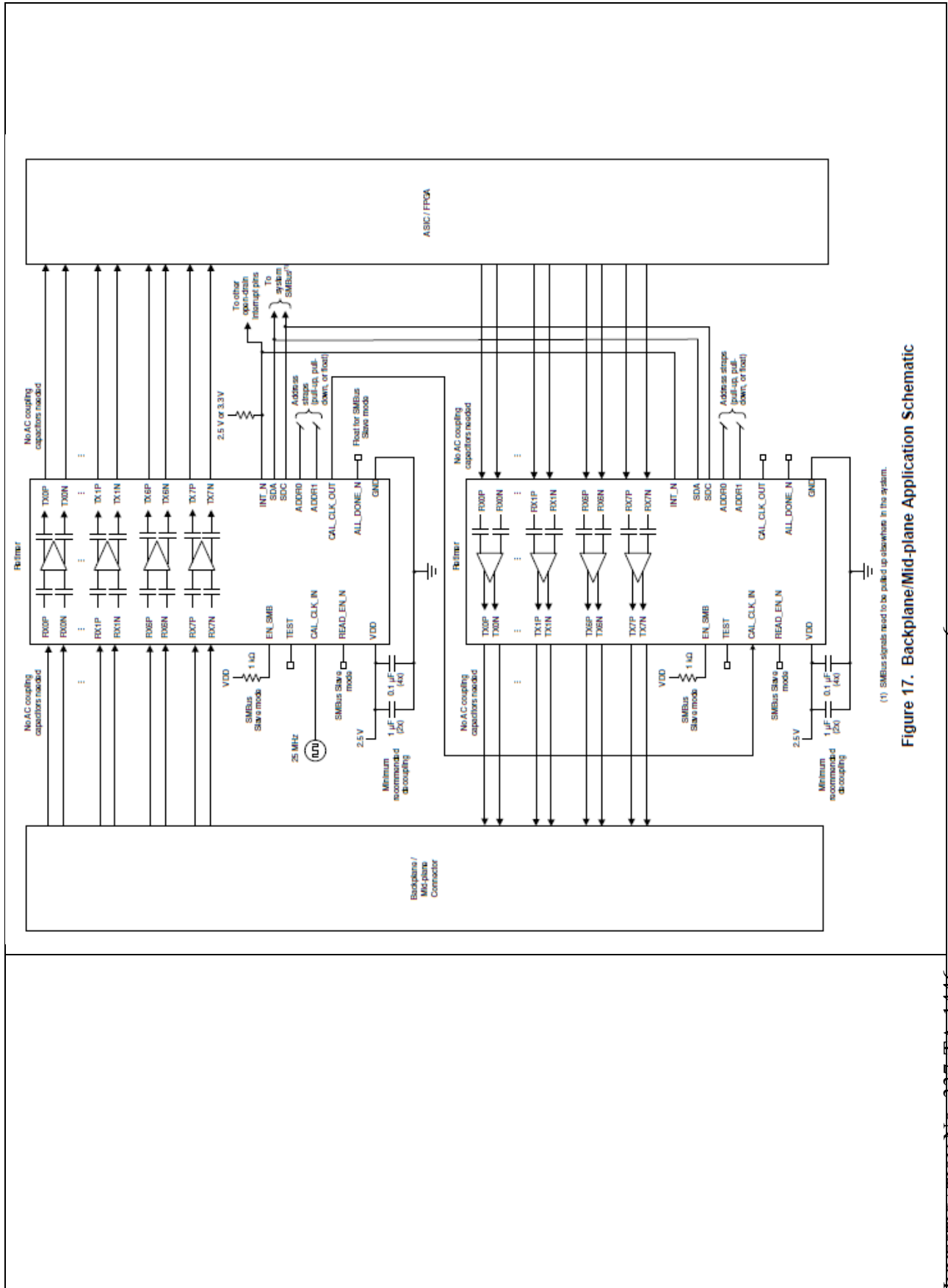


Figure 17. Backplane/Mid-plane Application Schematic

<p>Claim 1</p>	<p>Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”) DS250DF810, 79.</p> <p>To the extent that this preamble is not disclosed, either explicitly or inherently, by DS250DF810, this preamble is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>1[a] a first data recovery and remodulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;</p>	<p>DS250DF810 discloses and/or renders obvious this limitation.</p> <p>4 Simplified Schematic</p> <p>(1) SMBus signals need to be pulled up elsewhere in the system.</p>

DS250DF810, 1.

<p>Claim 1</p>	<p>Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)</p> <p>10.1 Application Information</p> <p>The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.</p> <p>10.2 Typical Application</p> <p>The DS250DF810 is typically used in the following main application scenarios:</p> <ol style="list-style-type: none"> 1. Backplane and mid-plane reach extension 2. Front-port jitter cleaning / retiming for optical applications <p>Figure 15. Typical Uses for the DS250DF810 in a System</p> <p>DS250DF810, 77.</p>
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Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

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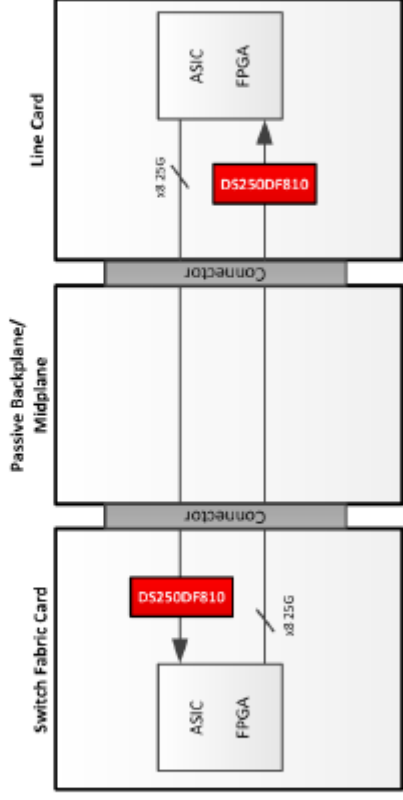


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7

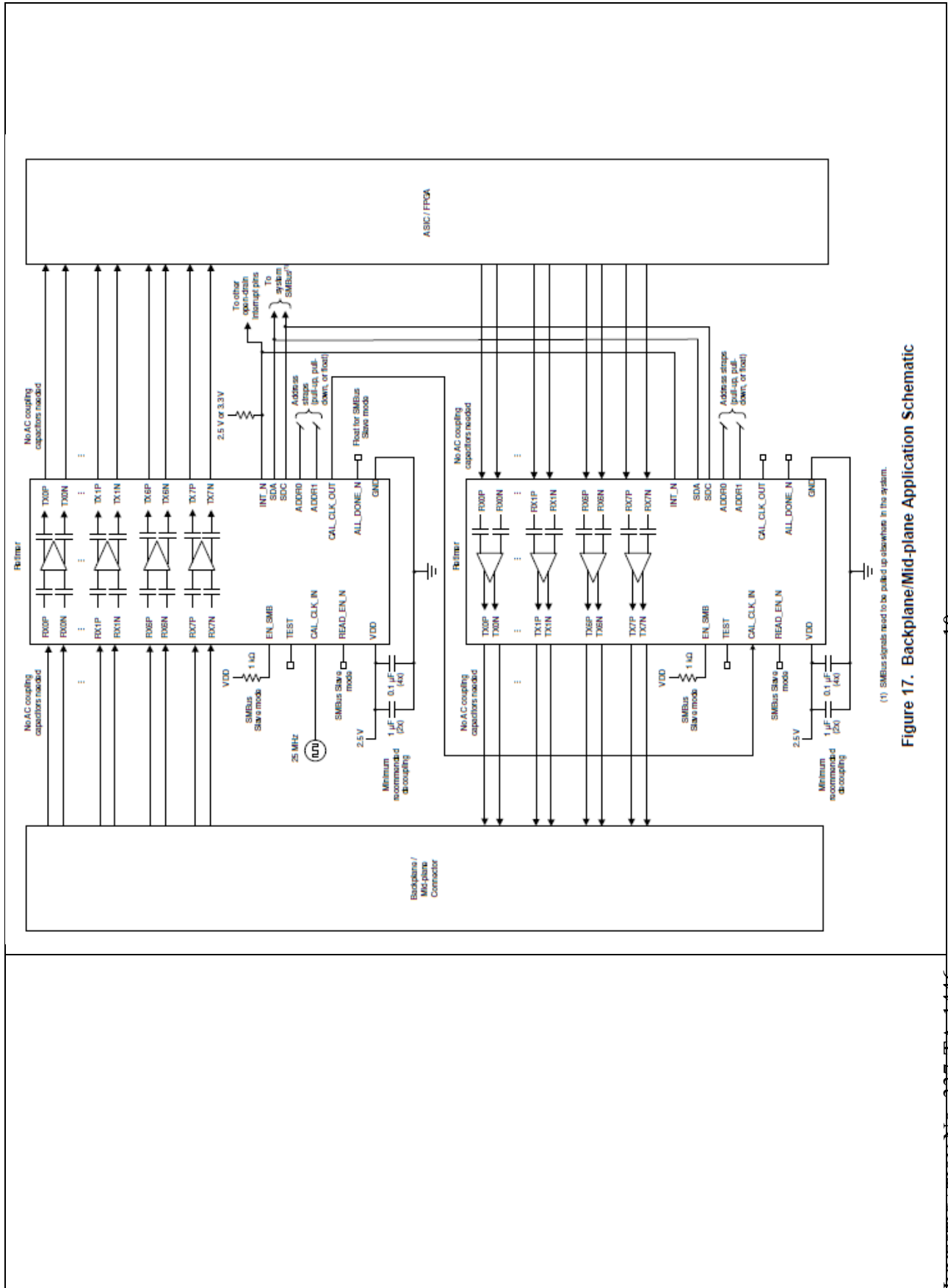


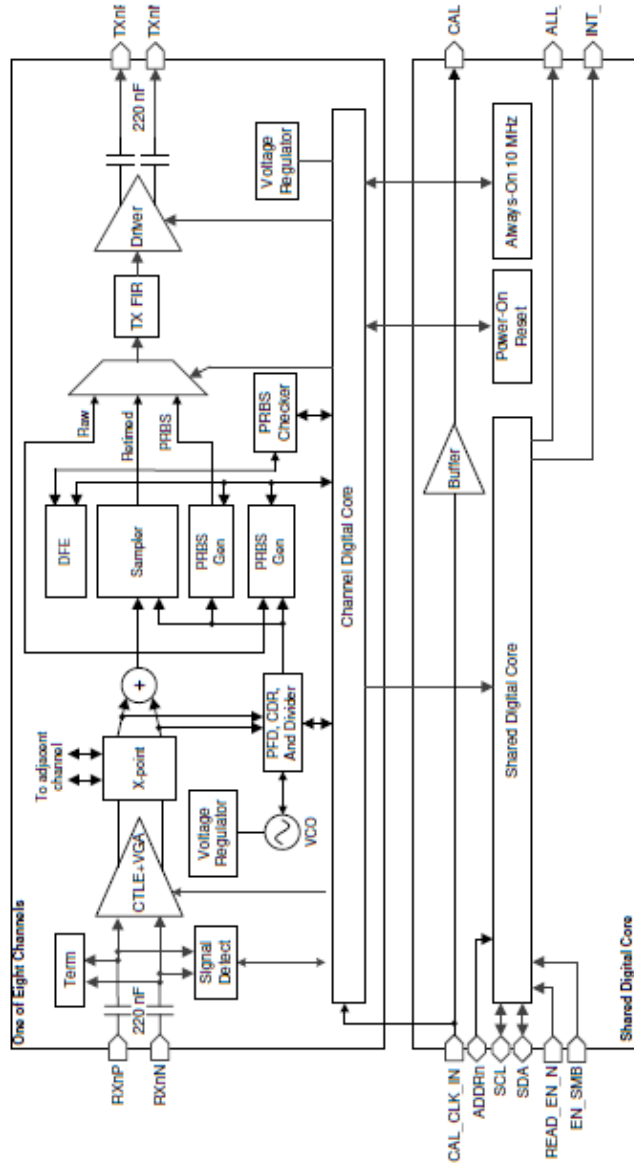
Figure 17. Backplane/Mid-plane Application Schematic

<p>Claim 1</p>	<p>Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”) DS250DF810, 79.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

9.2 Functional Block Diagram



DS250DF810, 17.

Exhibit A-7

<p>Claim 1</p>	<p>Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)</p> <p>9.3.8 Clock and Data Recovery (CDR)</p> <p>The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes.</p> <p>By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF810 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator.</p> <p>The CDR requires the following in order to be properly configured:</p> <ul style="list-style-type: none"> • 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN). • Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF810, 19.</p>
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Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

9.3.10 Differential Driver with FIR Filter

The DS250DF810 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. $C[0]$ can take on values in the range [-31, +31]. $C[-1]$ and $C[+1]$ can take on values in the range [-15, 15].

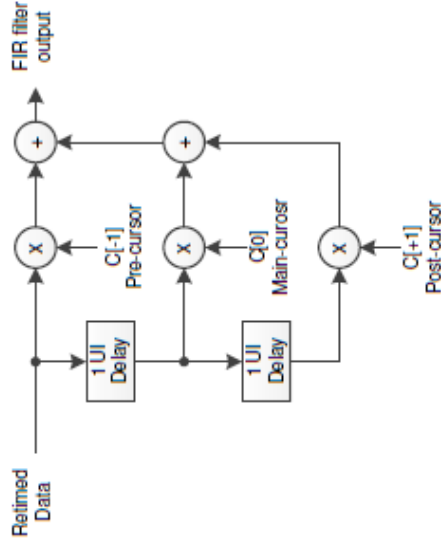


Figure 7. FIR Filter Functional Model

When utilizing the FIR filter, it is important to abide by the following general rules:

- $|C[-1]+C[0]+C[+1]| \leq 31$; the FIR tap coefficients absolute sum must be less or equal to 31)
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect, the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect, the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform in order to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
- $VOD_{low-frequency} = V_2 - V_5$
- $Rpre_{dB} = 20 * \log_{10} (V_3/V_2)$
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<p>Claim 1</p>	<p>Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”) DS250DF810, 20.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>1[b] a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and</p>	<p>DS250DF810 discloses and/or renders obvious this limitation.</p> <p>4 Simplified Schematic</p> <p>The schematic shows the DS250DF810 device with various pins and connections. On the left, there are multi-lane data paths for RX (RX0P, RX0N, RX7P, RX7N) and TX (TX0P, TX0N, TX7P, TX7N). A 2.5V or 3.3V supply is connected to the TX pins. The INT_N pin is connected to an open-drain interrupt pin. The SDA and SDC pins are connected to system SMBus address signals. The ADDR0 and ADDR1 pins are also connected to address signals. The CAL_CLK_OUT pin is connected to the next device's CAL_CLK_IN. The ALL_DONE_N pin is a float for SMBus Slave mode or connects to the next device's READ_EN_N for SMBus Master mode. The VDD pin is connected to a 2.5V supply through a 1µF capacitor (2x) and a 0.1µF capacitor (4x). The EN_SMB and TEST pins are also shown. A 25 MHz clock source is connected to the CAL_CLK_IN pin. The SMBus Slave mode is indicated by a square symbol.</p> <p>(1) SMBus signals need to be pulled up elsewhere in the system.</p>
	<p>DS250DF810, 1.</p>

Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

10.1 Application Information

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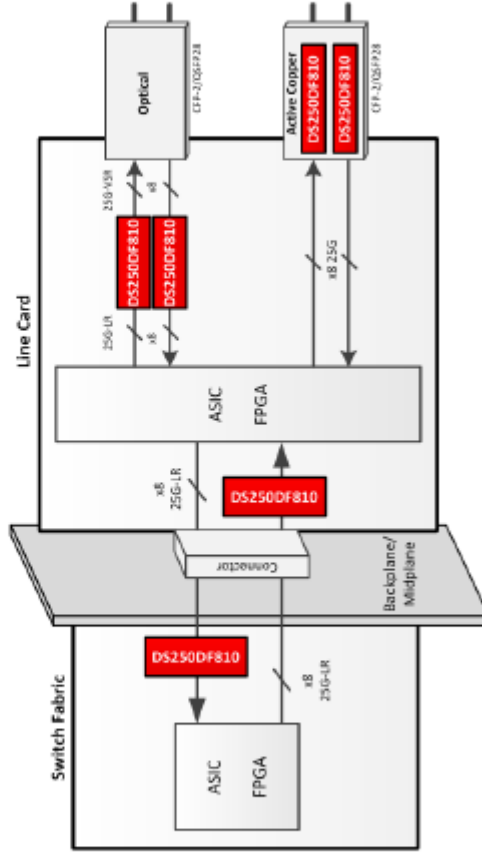


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

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Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

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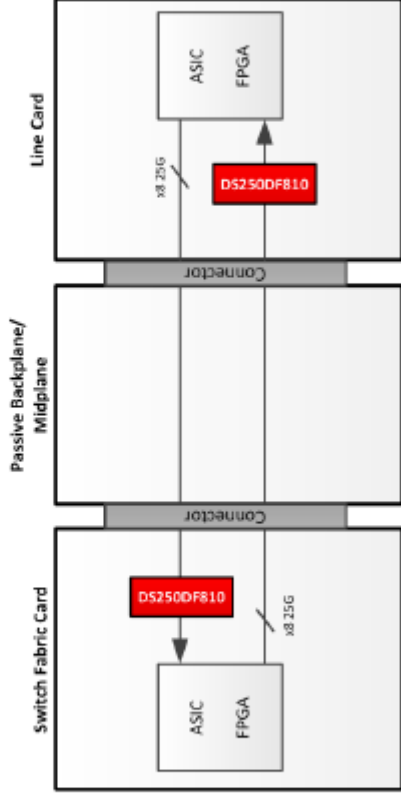


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7

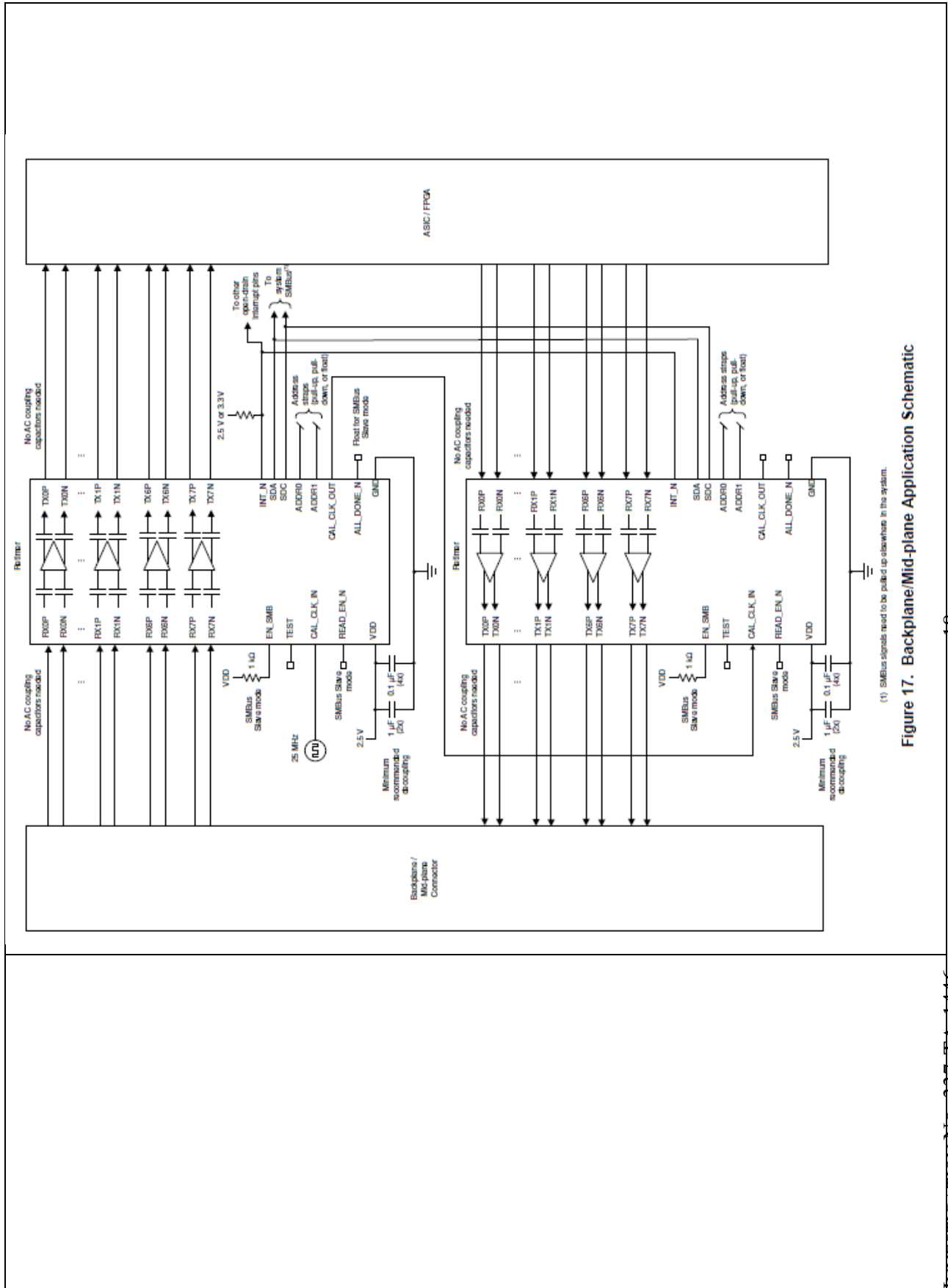


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Exhibit A-7

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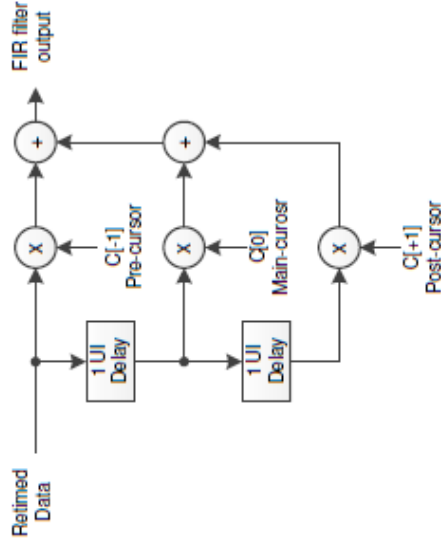


Figure 7. FIR Filter Functional Model

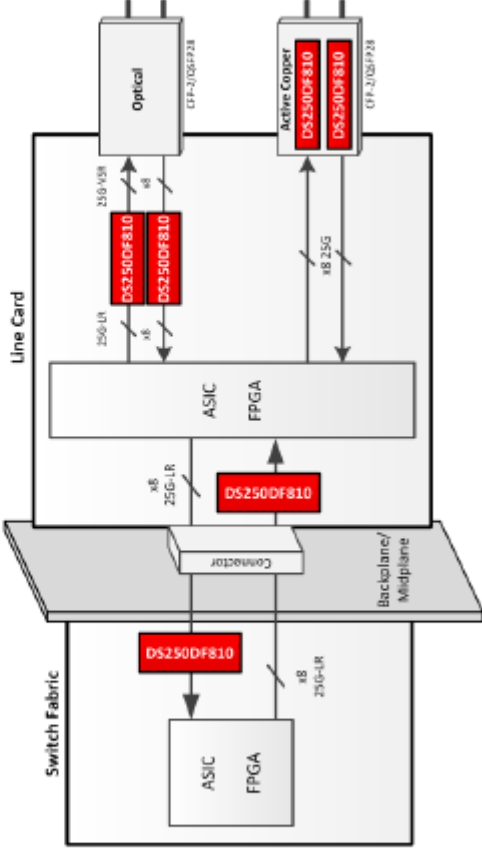
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- $\text{sgn}(C[-1])=\text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

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<p>1[c] electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,</p>	<p>DS250DF810 discloses and/or renders obvious this limitation.</p> <p>4 Simplified Schematic</p> <p>The schematic shows the DS250DF810 chip with various pins and their connections. On the left, RX0P/RX0N, RX7P/RX7N, TX0P/TX0N, and TX7P/TX7N are shown with differential pairs. A 1kΩ resistor connects VDD to EN_SMB. TEST is connected to GND. A 25 MHz clock source is connected to CAL_CLK_IN. CAL_CLK_OUT is connected to the next device's CAL_CLK_IN. READ_EN_N is connected to the next device's READ_EN_N. VDD is connected to GND with a 1μF capacitor (2x) and a 0.1μF capacitor (4x). On the right, INT_N is connected to other open-drain interrupt pins. SDA⁽¹⁾ and SDC⁽¹⁾ are connected to system SMBus. ADR0 and ADR1 are address straps (pull-up, pull-down, or float). CAL_CLK_IN is connected to the next device's CAL_CLK_IN. A note indicates that CAL_CLK_IN is float for SMBus Slave mode or connected to next device's READ_EN_N for SMBus Master mode.</p> <p>(1) SMBus signals need to be pulled up elsewhere in the system.</p>
	<p>DS250DF810, 1.</p>

<p>Claim 1</p>	<p>Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)</p> <p>10.1 Application Information</p> <p>The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.</p> <p>10.2 Typical Application</p> <p>The DS250DF810 is typically used in the following main application scenarios:</p> <ol style="list-style-type: none"> 1. Backplane and mid-plane reach extension 2. Front-port jitter cleaning / retiming for optical applications  <p>The diagram illustrates the DS250DF810's role in a system. It is divided into three main sections: Switch Fabric, Backplane/Midplane, and Line Card. In the Switch Fabric, an ASIC/FPGA block is connected to a DS250DF810 retimer via an x8 25G-LR interface. This retimer is connected to another DS250DF810 on the Backplane/Midplane via a Connector. The second retimer is then connected to an ASIC/FPGA block in the Line Card via an x8 25G-LR interface. The Line Card section includes two DS250DF810 retimers connected to an ASIC/FPGA block. One retimer is connected to an Optical component (CFP-208P28) via a 25G-LR interface, and the other is connected to an Active Copper component (CFP-208P28) via an 18.25G interface. The Optical component is further connected to a 25G-LR interface, and the Active Copper component is connected to a 25G-LR interface.</p> <p>Figure 15. Typical Uses for the DS250DF810 in a System</p> <p>DS250DF810, 77.</p>
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Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

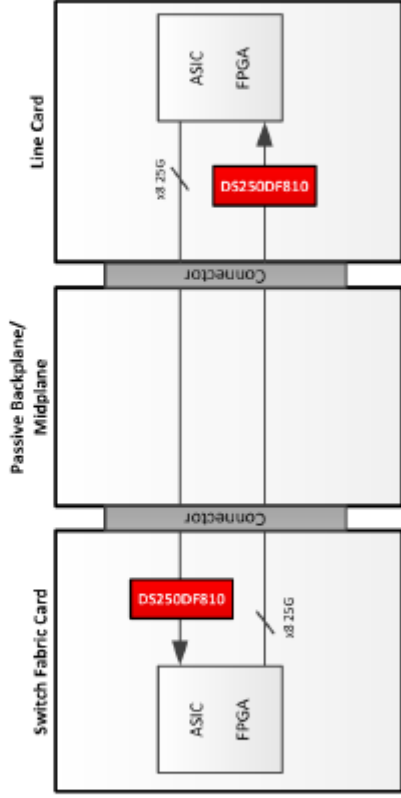


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7

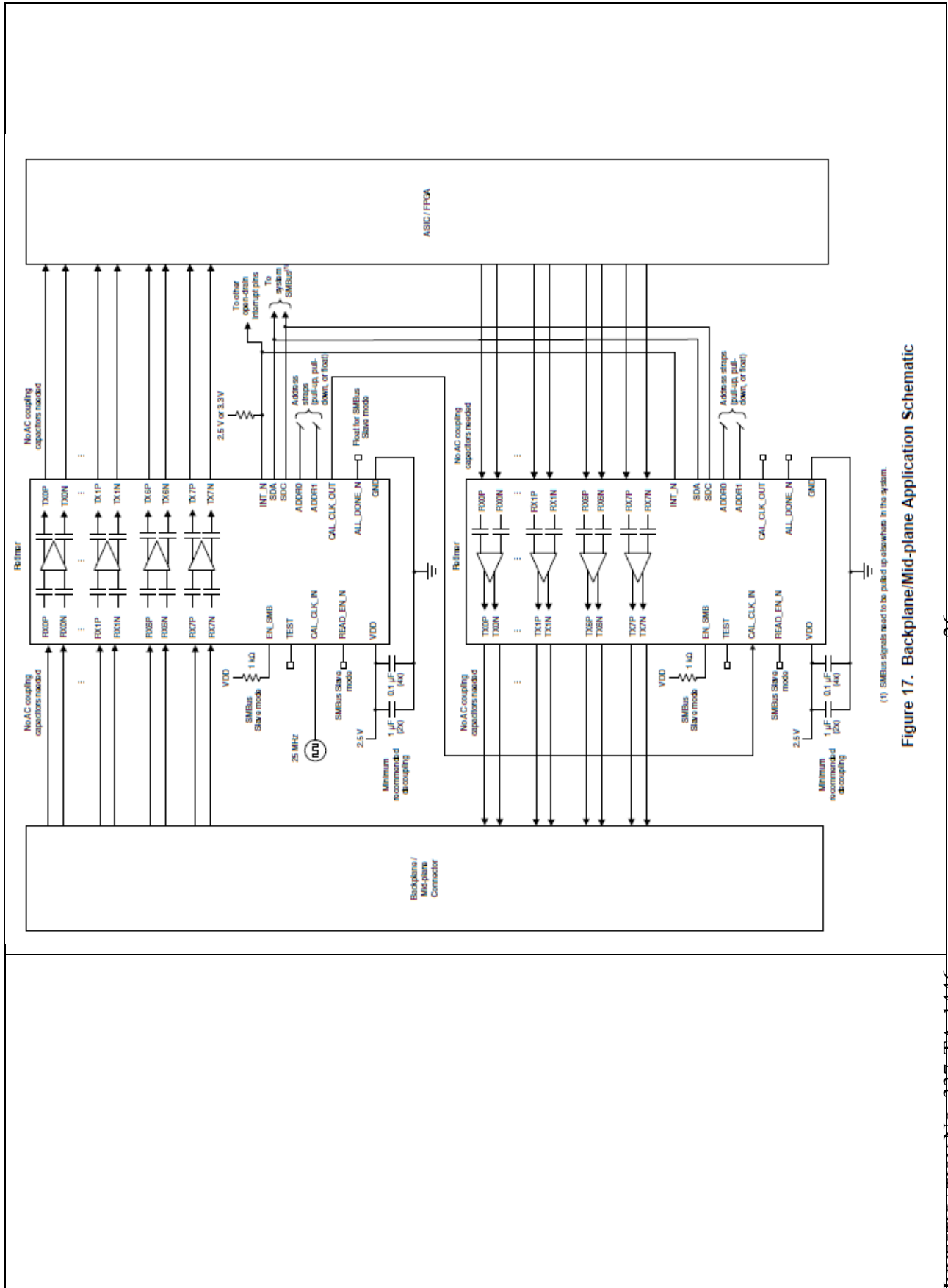


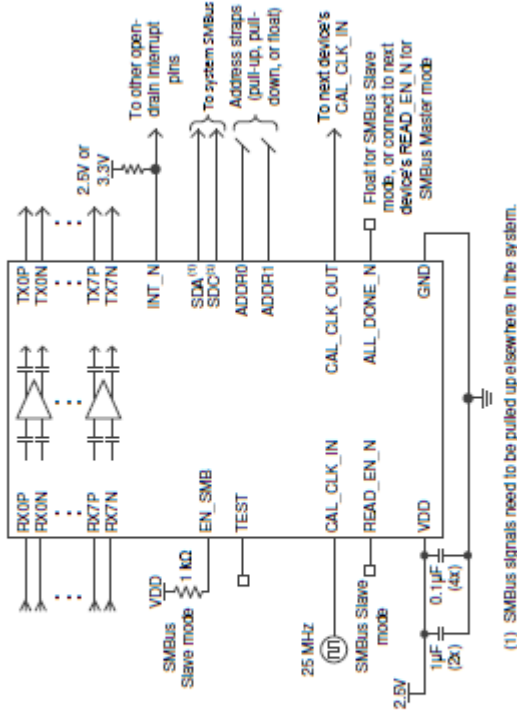
Figure 17. Backplane/Mid-plane Application Schematic

<p>Claim 1</p>	<p>Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”) DS250DF810, 79.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

4 Simplified Schematic

Claim 1
 electrical transit signals and said inbound and outbound multilane data streams for the first host interface port, and



DS250DF810, 1.

<p>Claim 1</p>	<p>Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)</p> <p>10.1 Application Information</p> <p>The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.</p> <p>10.2 Typical Application</p> <p>The DS250DF810 is typically used in the following main application scenarios:</p> <ol style="list-style-type: none"> 1. Backplane and mid-plane reach extension 2. Front-port jitter cleaning / retiming for optical applications <p>Figure 15. Typical Uses for the DS250DF810 in a System</p> <p>DS250DF810, 77.</p>
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Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

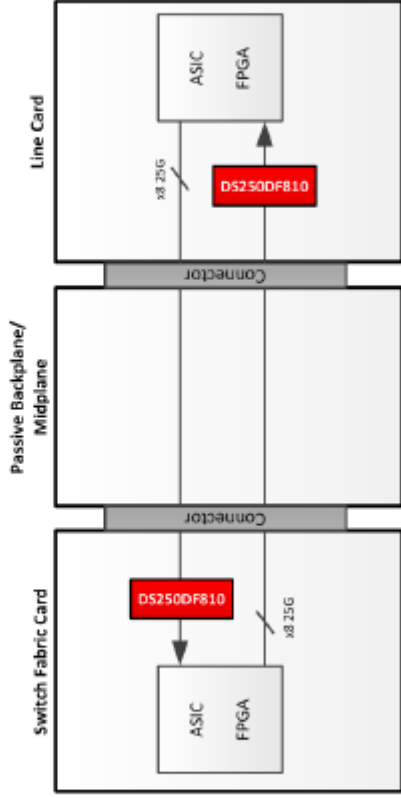
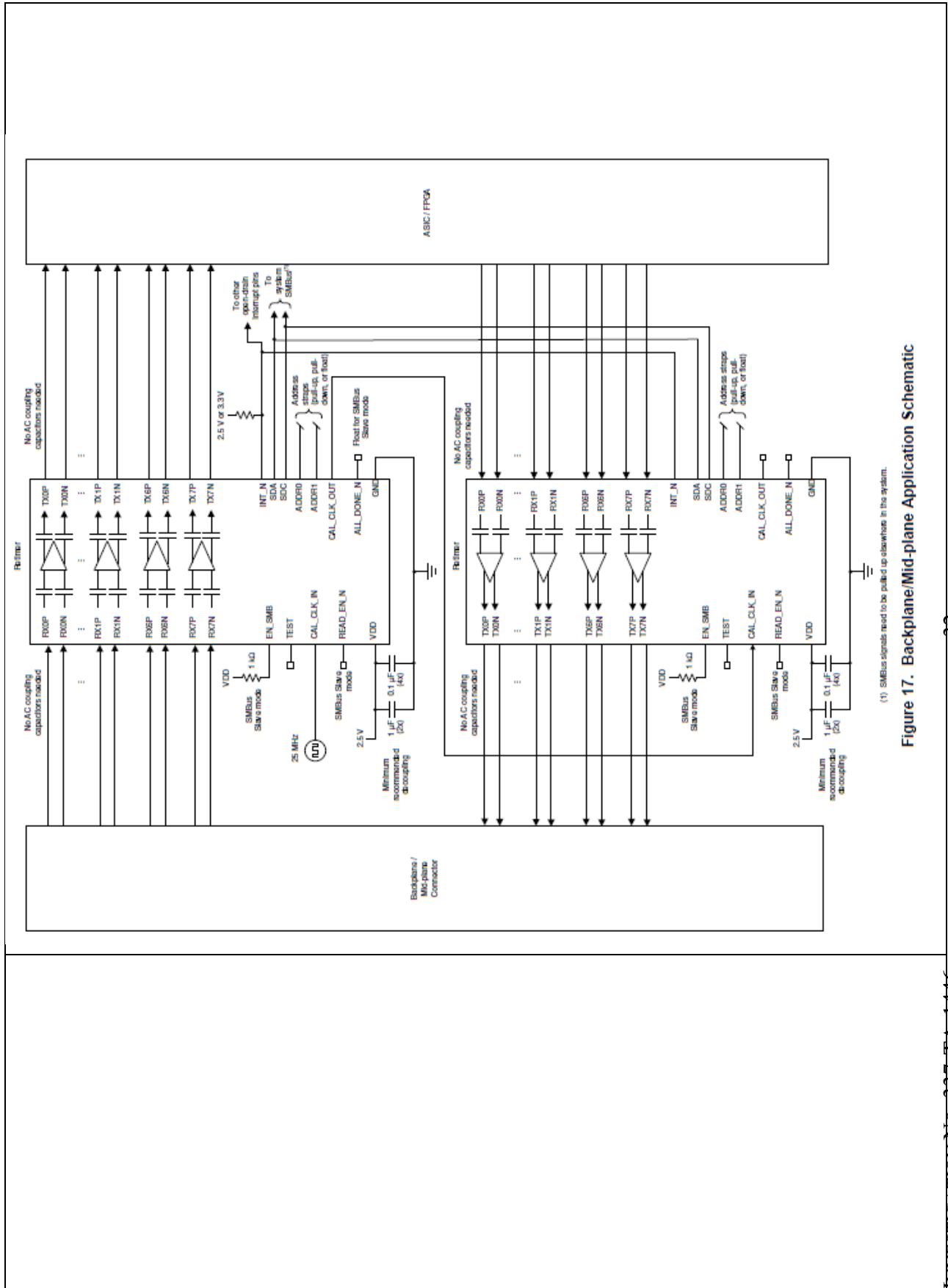


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7



(1) SMBus signals need to be pulled up elsewhere in the system.

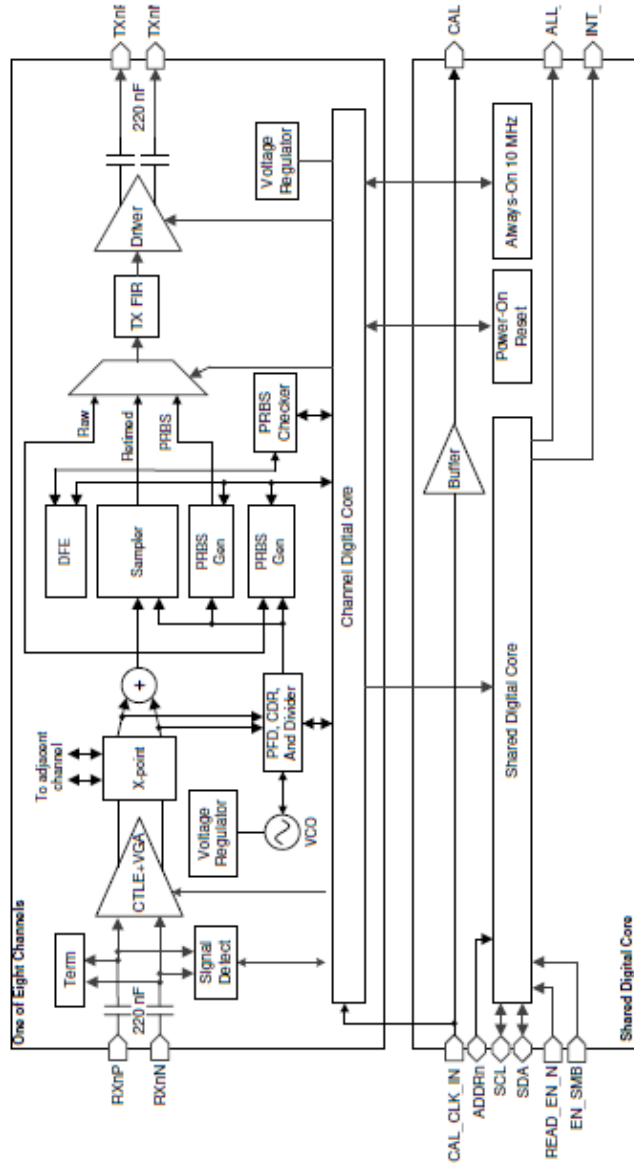
Figure 17. Backplane/Mid-plane Application Schematic

<p>Claim 1</p>	<p>Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”) DS250DF810, 79.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

9.2 Functional Block Diagram



DS250DF810, 17.

Exhibit A-7

Claim 1	<p>Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)</p> <p>9.3.8 Clock and Data Recovery (CDR)</p> <p>The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes.</p> <p>By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF810 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator.</p> <p>The CDR requires the following in order to be properly configured:</p> <ul style="list-style-type: none"> • 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN). • Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF810, 19.</p>
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Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

9.3.10 Differential Driver with FIR Filter

The DS250DF810 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. $C[0]$ can take on values in the range [-31, +31]. $C[-1]$ and $C[+1]$ can take on values in the range [-15, 15].

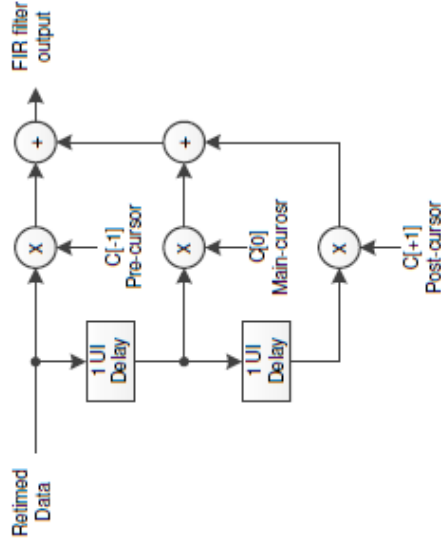


Figure 7. FIR Filter Functional Model

When utilizing the FIR filter, it is important to abide by the following general rules:

- $|C[-1]+C[0]+C[+1]| \leq 31$; the FIR tap coefficients absolute sum must be less or equal to 31)
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect, the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect, the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform in order to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
- $VOD_{low-frequency} = V_2 - V_5$
- $Rpre_{dB} = 20 * \log_{10} (V_3/V_2)$
- $Rpst_{dB} = 20 * \log_{10} (V_1/V_2)$

<p>Claim 1</p>	<p>Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”) DS250DF810, 20.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>1[e] the second DRR device converting between said electrical transit signals and said inbound and outbound multilane data streams for the second host interface port,</p>	<p>DS250DF810 discloses and/or renders obvious this limitation.</p> <p>4 Simplified Schematic</p> <p>(1) SMBus signals need to be pulled up elsewhere in the system.</p>

DS250DF810, 1.

Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

10.1 Application Information

The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

10.2 Typical Application

The DS250DF810 is typically used in the following main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port jitter cleaning / retiming for optical applications

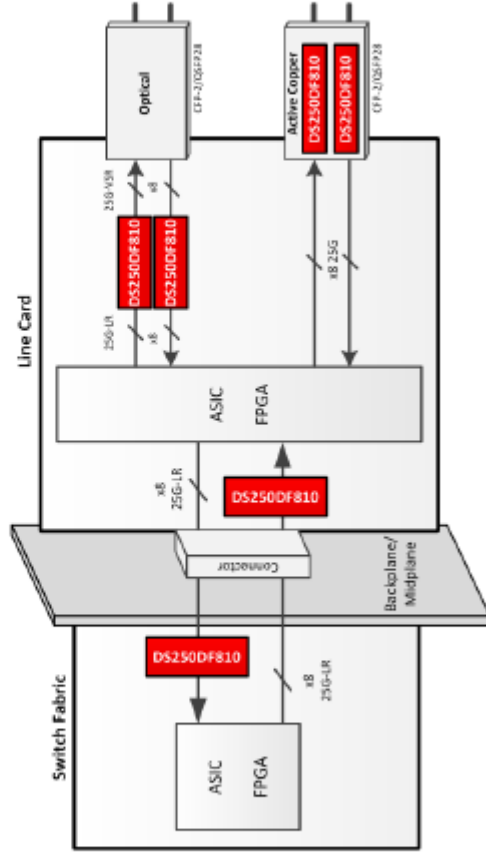


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

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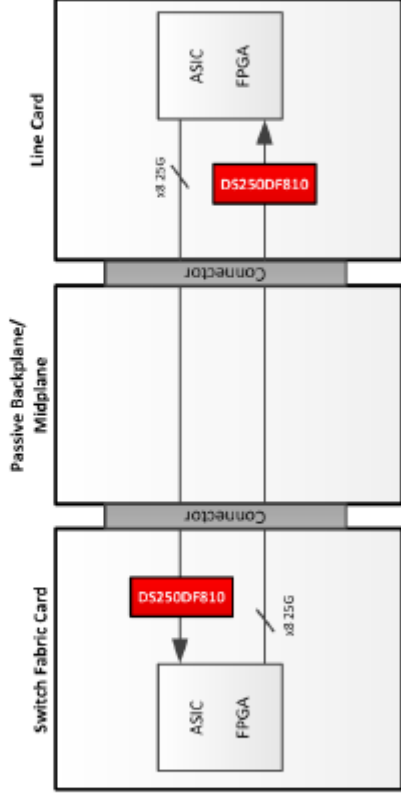
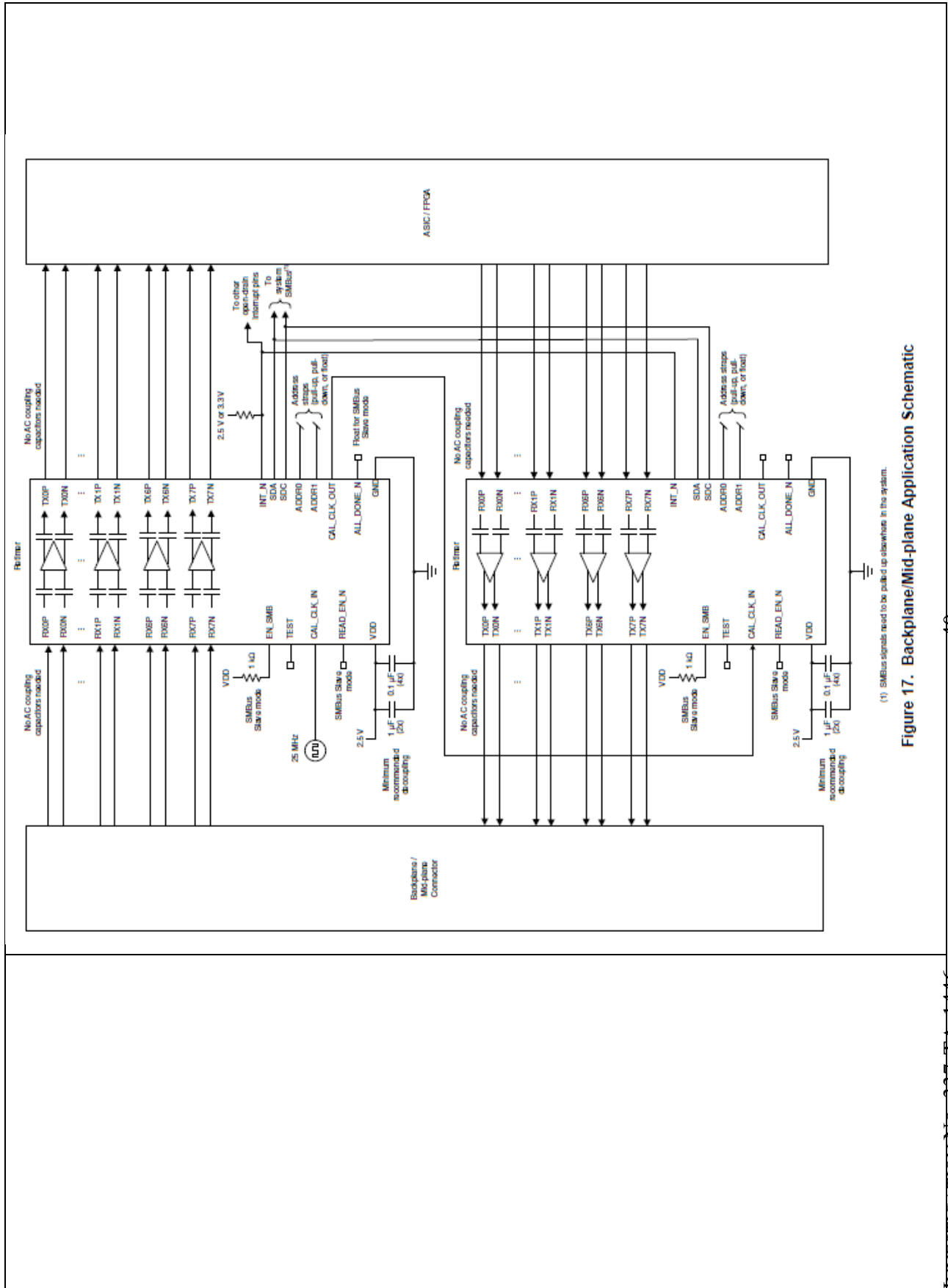


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7



(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Backplane/Mid-plane Application Schematic

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Exhibit A-7

Claim 1	<p>Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)</p> <p>9.3.8 Clock and Data Recovery (CDR)</p> <p>The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes.</p> <p>By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF810 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator.</p> <p>The CDR requires the following in order to be properly configured:</p> <ul style="list-style-type: none"> • 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN). • Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF810, 19.</p>
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Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

9.3.10 Differential Driver with FIR Filter

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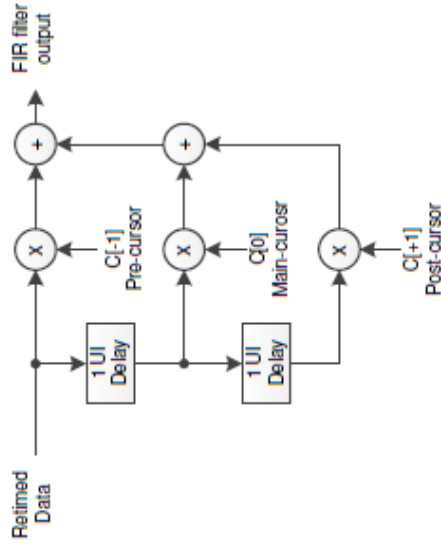


Figure 7. FIR Filter Functional Model

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The FIR filter is used to pre-distort the transmitted waveform in order to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

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Exhibit A-7

Claim 1	Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)
<p>1[f] the first and second DRR devices providing preequalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.</p>	<p>DS250DF810, 20.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>

Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak V_{OD}, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		Peak-to-Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Claim 1

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0a3E[6:0]	FIR SETTINGS		Peak-to-Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0a3D[6:0]	POST-CURSORS: REG_0a3F[6:0]			
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
5		0	RW	Y	RESERVED	RESERVED	
4		0	RW	Y	RESERVED	RESERVED	
3		0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude	
2		0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude	
1		0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude	
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

Claim 1	<p>Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”) DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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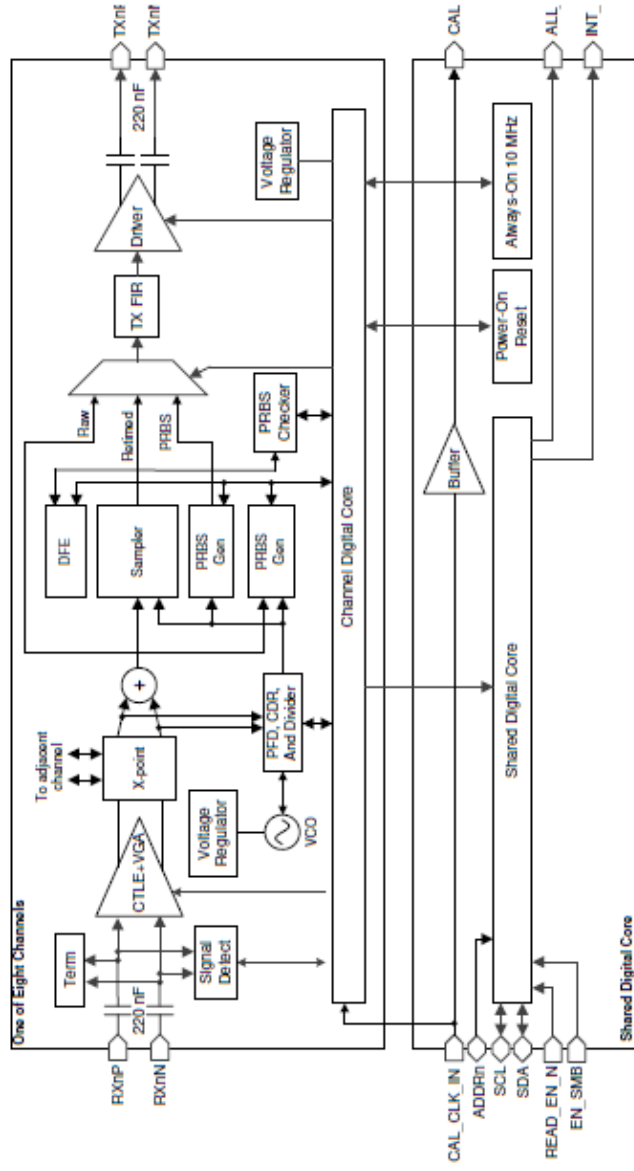
B. DEPENDENT CLAIM 2

Claim 2	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>
<p>2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.</p>	

<p>Claim 2</p>	<p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 2

9.2 Functional Block Diagram



DS250DF810, 17.

<p>Claim 2</p>	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 2</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Exhibit A-7

Claim 2

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	0	0	0	0.205	NA	NA
0	+1	0	0	0.280	NA	NA
0	+2	0	0	0.305	NA	NA
0	+3	0	0	0.355	NA	NA
0	+4	0	0	0.385	NA	NA
0	+5	0	0	0.440	NA	NA
0	+6	0	0	0.490	NA	NA
0	+7	0	0	0.525	NA	NA
0	+8	0	0	0.565	NA	NA
0	+9	0	0	0.610	NA	NA
0	+10	0	0	0.650	NA	NA
0	+11	0	0	0.685	NA	NA
0	+12	0	0	0.720	NA	NA
0	+13	0	0	0.760	NA	NA
0	+14	0	0	0.790	NA	NA
0	+15	0	0	0.825	NA	NA
0	+16	0	0	0.860	NA	NA
0	+17	0	0	0.890	NA	NA
0	+18	0	0	0.925	NA	NA
0	+19	0	0	0.960	NA	NA
0	+20	0	0	0.985	NA	NA
0	+21	0	0	1.010	NA	NA
0	+22	0	0	1.040	NA	NA
0	+23	0	0	1.075	NA	NA
0	+24	0	0	1.095	NA	NA
0	+25	0	0	1.125	NA	NA
0	+26	0	0	1.150	NA	NA
0	+27	0	0	1.165	NA	NA
0	+28	0	0	1.190	NA	NA
0	+29	0	0	1.205	NA	NA
0	+30	0	0	1.220	NA	NA
0	+31	0	0	1.225	NA	NA
0	+18	-1	-1	0.980	NA	2.1
0	+17	-2	-2	0.960	NA	2.5
0	+16	-3	-3	0.960	NA	3.1
0	+15	-4	-4	0.960	NA	3.8
0	+14	-5	-5	0.960	NA	4.7

Claim 2

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13		-6	0.960	NA	5.8
0	+12		-7	0.960	NA	7.2
0	+11		-8	0.960	NA	9.0
0	+10		-9	0.960	NA	11.6
-1	18		0	0.960	1.0	NA
-2	17		0	0.960	1.6	NA
-3	16		0	0.960	2.4	NA
-4	15		0	0.960	3.3	NA
0	26		-1	1.165	NA	1.1
0	25		-2	1.165	NA	1.3
0	24		-3	1.165	NA	1.8
0	23		-4	1.165	NA	2.2
0	22		-5	1.165	NA	2.7
0	21		-6	1.165	NA	3.3
0	20		-7	1.165	NA	3.9
0	19		-8	1.165	NA	4.7
0	18		-9	1.165	NA	5.7
0	17		-10	1.165	NA	6.9
0	16		-11	1.165	NA	8.4
0	15		-12	1.165	NA	10.1
-1	26		0	1.165	0.7	NA
-2	25		0	1.165	1.2	NA
-3	24		0	1.165	1.5	NA
-4	23		0	1.165	2.0	NA
-5	22		0	1.165	2.6	NA
-6	21		0	1.165	3.2	NA
-7	20		0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 2

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

Claim 2	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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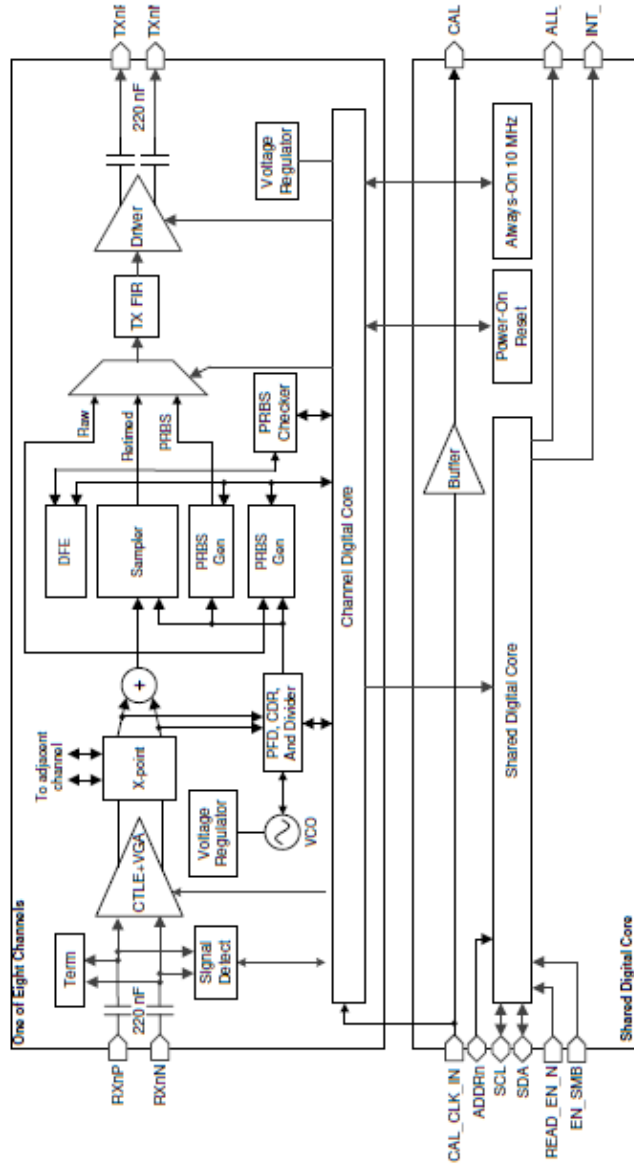
C. DEPENDENT CLAIM 3

Claim 3	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>
<p>3. The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.</p>	

<p>Claim 3</p>	<p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 3

9.2 Functional Block Diagram



DS250DF810, 17.

<p>Claim 3</p>	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 3</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Exhibit A-7

Claim 3

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSORS: REG_0x3E[6:0]	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Claim 3

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 3

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

Claim 3	DS250DF810, 54-55. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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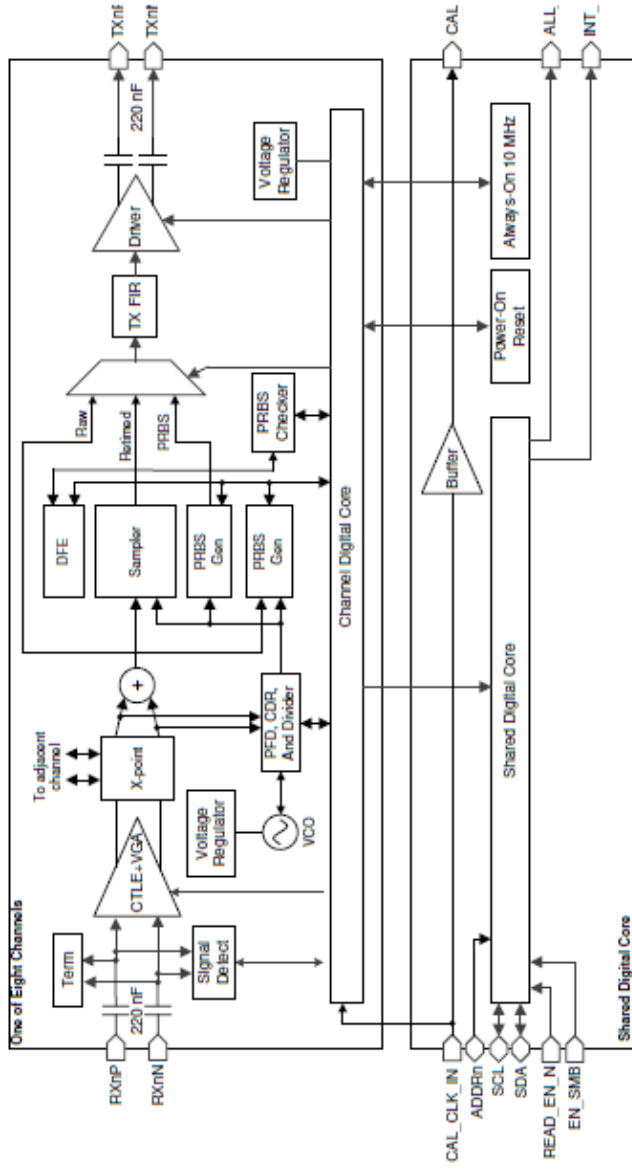
D. DEPENDENT CLAIM 4

Claim 4 4. The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.	DS250DF810 discloses and/or renders obvious this limitation.
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<p>Claim 4</p>	<p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 4

9.2 Functional Block Diagram



DS250DF810, 17.

<p>Claim 4</p>	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 4</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Exhibit A-7

Claim 4

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSORS: REG_0x3E[6:0]	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Claim 4

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 4

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

Claim 4	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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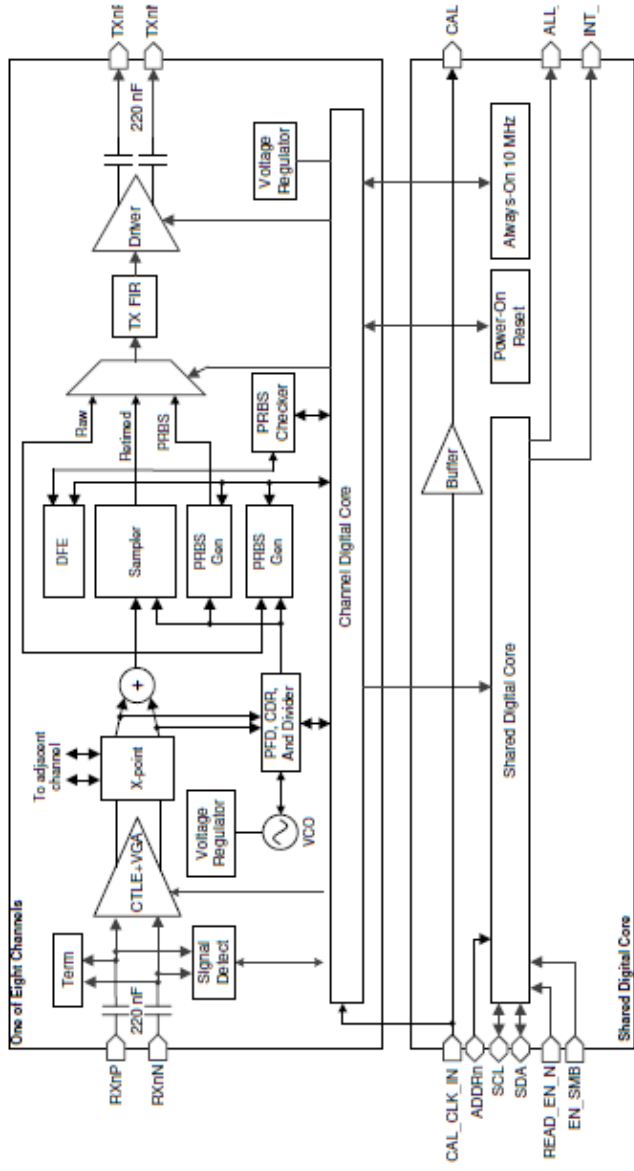
E. DEPENDENT CLAIM 5

Claim 5	<p>5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.</p> <p>DS250DF810 discloses and/or renders obvious this limitation.</p>
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<p>Claim 5</p>	<p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 5

9.2 Functional Block Diagram



DS250DF810, 17.

<p>Claim 5</p>	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 5</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Exhibit A-7

Claim 5

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSORS: REG_0x3E[6:0]	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Claim 5

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 5

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

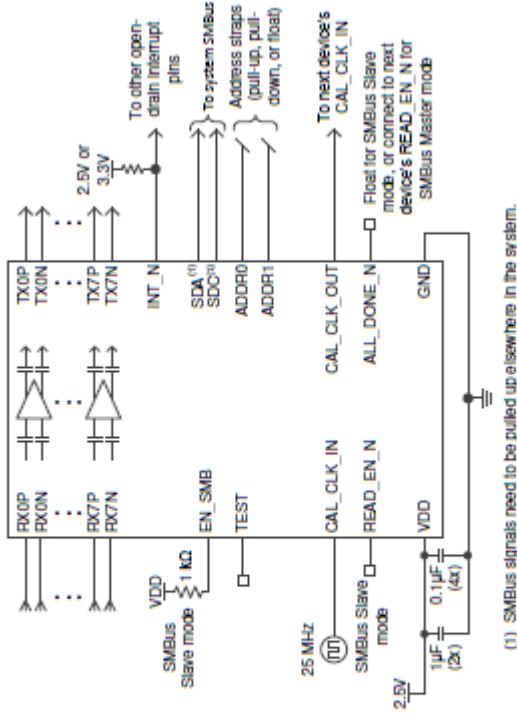
Claim 5	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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F. DEPENDENT CLAIM 6

Claim 6	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>
<p>6. The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.</p>	

Claim 6

4 Simplified Schematic



DS250DF810, 1.

(1) SMBus signals need to be pulled up elsewhere in the system.

Claim 6

10.1 Application Information

The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

10.2 Typical Application

The DS250DF810 is typically used in the following main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port jitter cleaning / retiming for optical applications

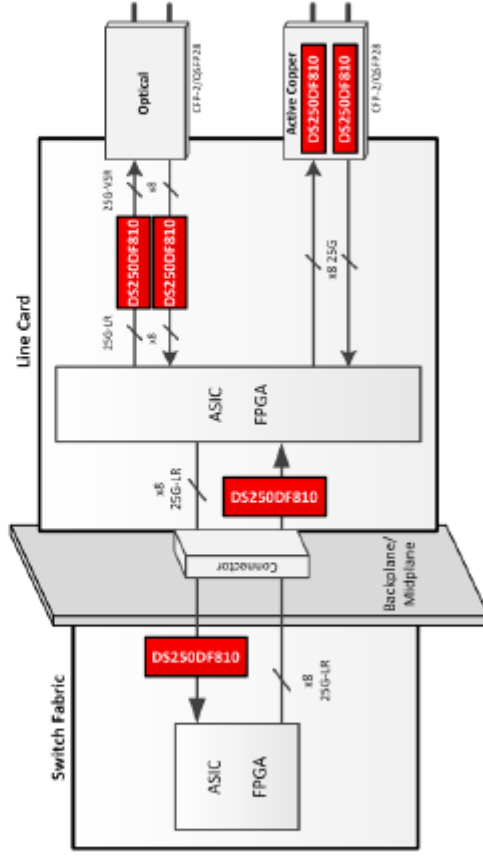


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

Exhibit A-7

Claim 6

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

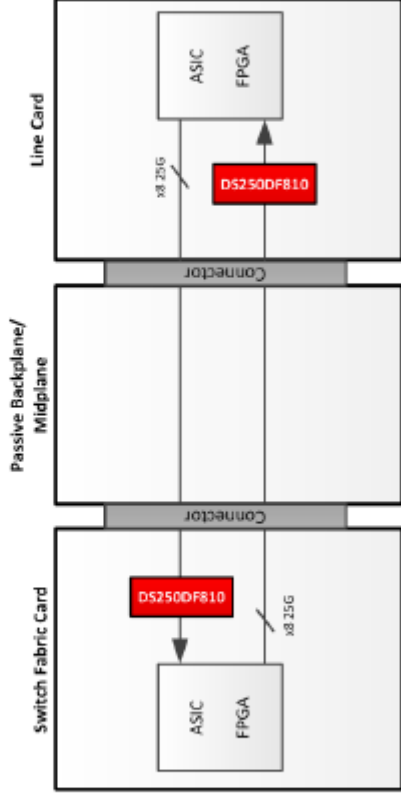
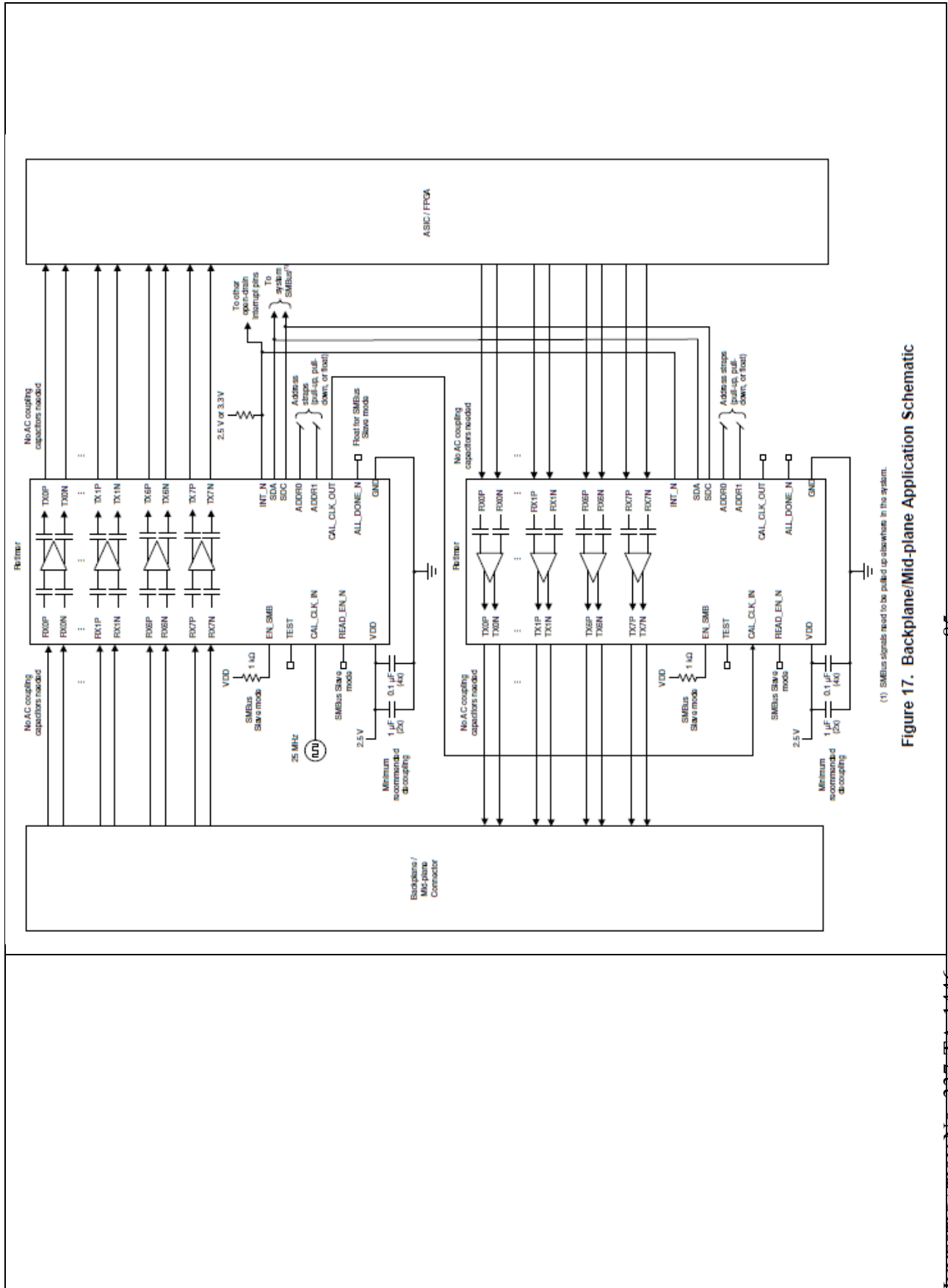


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7



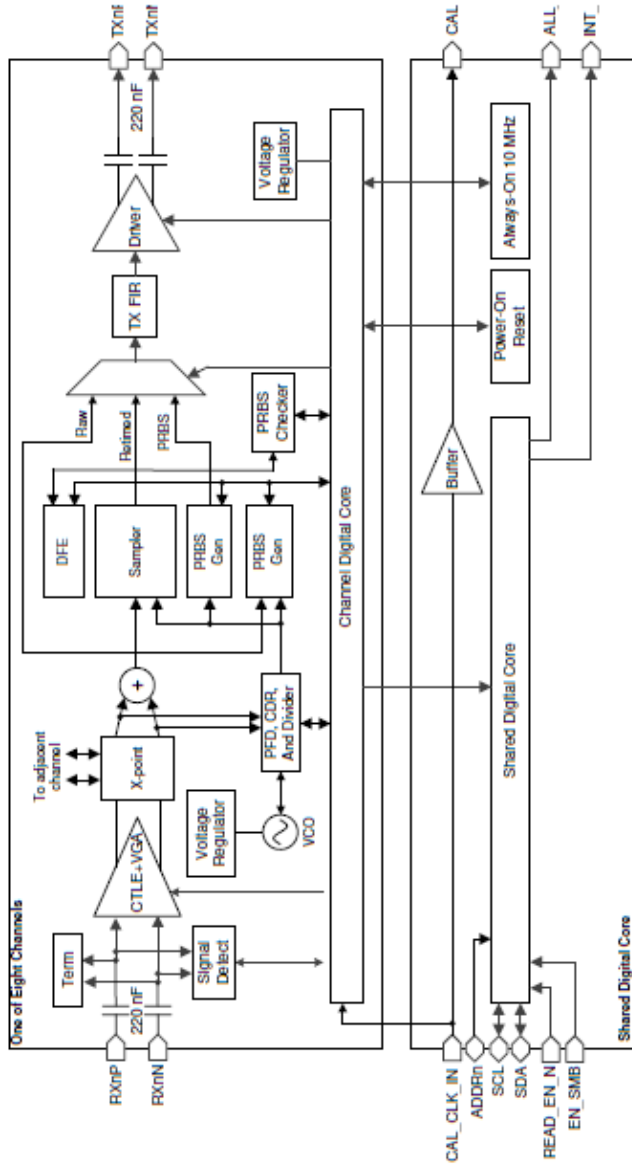
(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Backplane/Mid-plane Application Schematic

<p>Claim 6</p>	<p>DS250DF810, 79.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 6

9.2 Functional Block Diagram



DS250DF810, 17.

To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine in the Cover Pleading and/or other invalidity claim charts. The ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

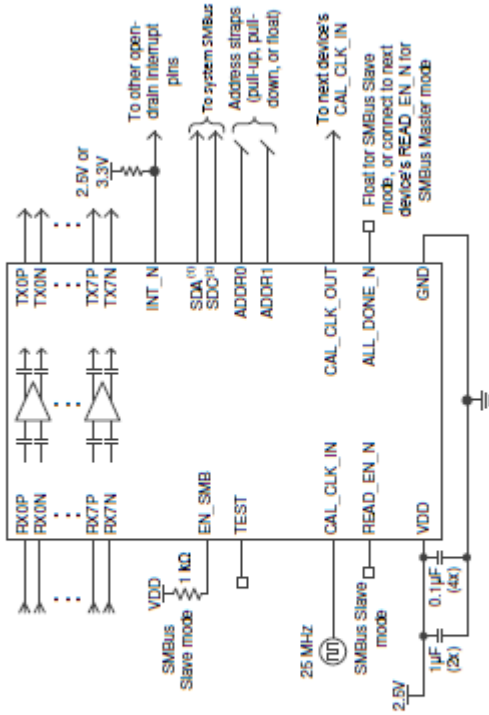
G. DEPENDENT CLAIM 7

Claim 7

7. The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

DS250DF810 discloses and/or renders obvious this limitation.

4 Simplified Schematic



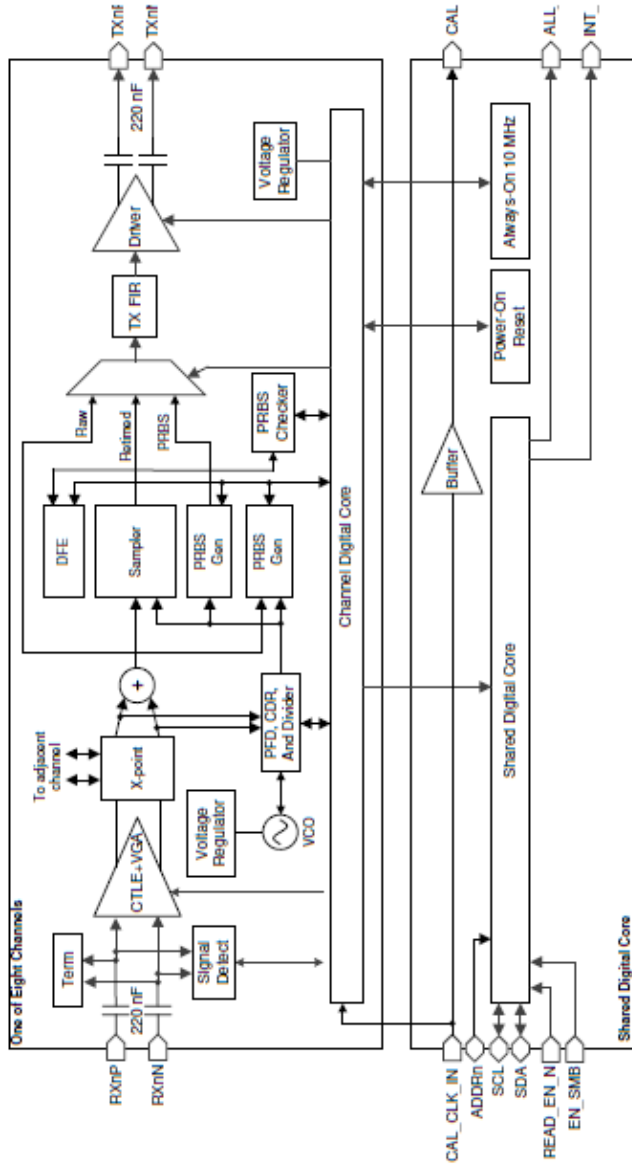
(1) SMBus signals need to be pulled up elsewhere in the system.

DS250DF810, 1.

<p>Claim 7</p>	<p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 7

9.2 Functional Block Diagram



DS250DF810, 17.

<p>Claim 7</p>	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 7</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Exhibit A-7

Claim 7

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	0	0	0	0.205	NA	NA
0	+1	0	0	0.280	NA	NA
0	+2	0	0	0.305	NA	NA
0	+3	0	0	0.355	NA	NA
0	+4	0	0	0.385	NA	NA
0	+5	0	0	0.440	NA	NA
0	+6	0	0	0.490	NA	NA
0	+7	0	0	0.525	NA	NA
0	+8	0	0	0.565	NA	NA
0	+9	0	0	0.610	NA	NA
0	+10	0	0	0.650	NA	NA
0	+11	0	0	0.685	NA	NA
0	+12	0	0	0.720	NA	NA
0	+13	0	0	0.760	NA	NA
0	+14	0	0	0.790	NA	NA
0	+15	0	0	0.825	NA	NA
0	+16	0	0	0.860	NA	NA
0	+17	0	0	0.890	NA	NA
0	+18	0	0	0.925	NA	NA
0	+19	0	0	0.960	NA	NA
0	+20	0	0	0.985	NA	NA
0	+21	0	0	1.010	NA	NA
0	+22	0	0	1.040	NA	NA
0	+23	0	0	1.075	NA	NA
0	+24	0	0	1.095	NA	NA
0	+25	0	0	1.125	NA	NA
0	+26	0	0	1.150	NA	NA
0	+27	0	0	1.165	NA	NA
0	+28	0	0	1.190	NA	NA
0	+29	0	0	1.205	NA	NA
0	+30	0	0	1.220	NA	NA
0	+31	0	0	1.225	NA	NA
0	+18	-1	-1	0.980	NA	2.1
0	+17	-2	-2	0.960	NA	2.5
0	+16	-3	-3	0.960	NA	3.1
0	+15	-4	-4	0.960	NA	3.8
0	+14	-5	-5	0.960	NA	4.7

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 7

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

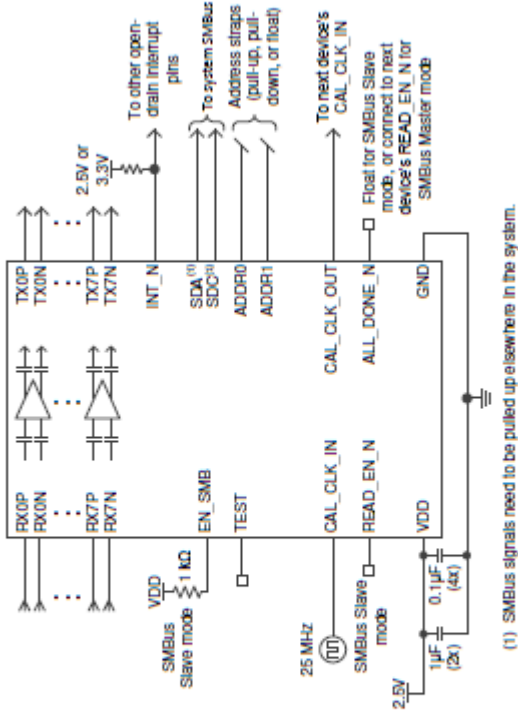
Claim 7	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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H. INDEPENDENT CLAIM 8

Claim 8	<p>To the extent the preamble is limiting, DS250DF810 discloses and/or renders obvious this limitation.</p>
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Claim 8

4 Simplified Schematic



(1) SMBus signals need to be pulled up elsewhere in the system.

DS250DF810, 1.

Claim 8

10.1 Application Information

The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

10.2 Typical Application

The DS250DF810 is typically used in the following main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port jitter cleaning / retiming for optical applications

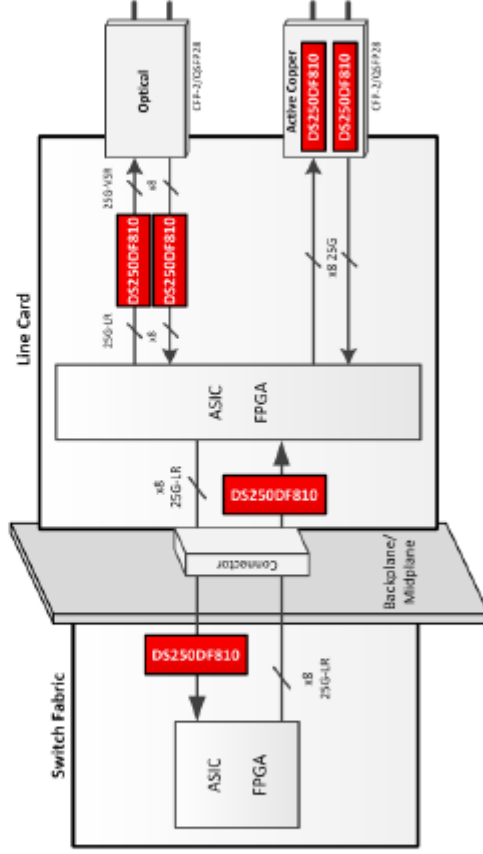


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

Exhibit A-7

Claim 8

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

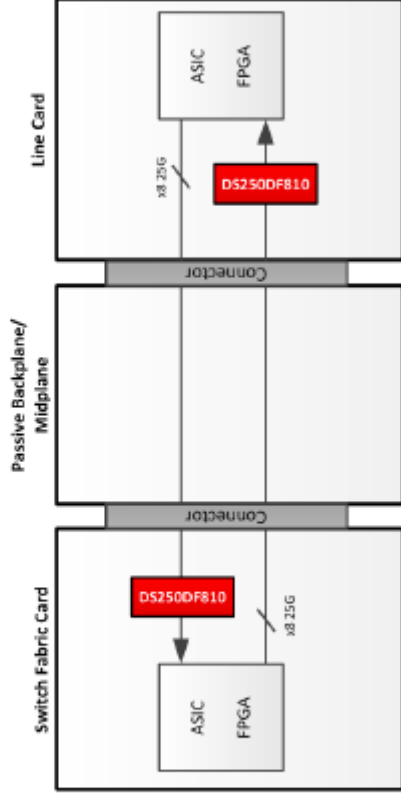
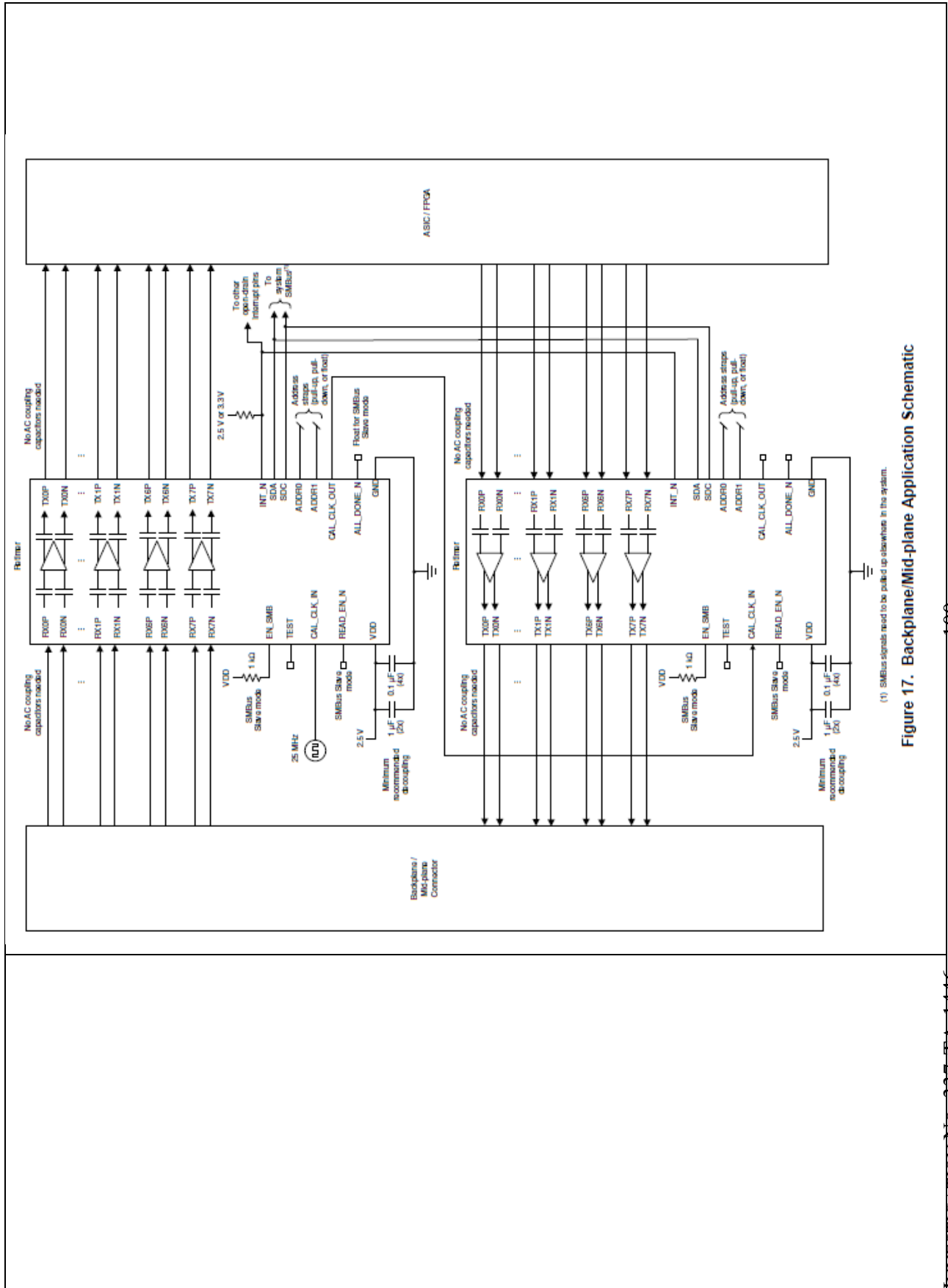


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7



(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Backplane/Mid-plane Application Schematic

<p>Claim 8</p>	<p>DS250DF810, 79.</p> <p>To the extent that this preamble is not disclosed, either explicitly or inherently, by DS250DF810, this preamble is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>8[a] connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges multi-lane data streams with a first host interface port via the first connector plug;</p>	<p>DS250DF810 discloses and/or renders obvious this limitation.</p> <p>4 Simplified Schematic</p> <p>(1) SMBus signals need to be pulled up elsewhere in the system.</p>

DS250DF810, 1.

Claim 8

10.1 Application Information

The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

10.2 Typical Application

The DS250DF810 is typically used in the following main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port jitter cleaning / retiming for optical applications

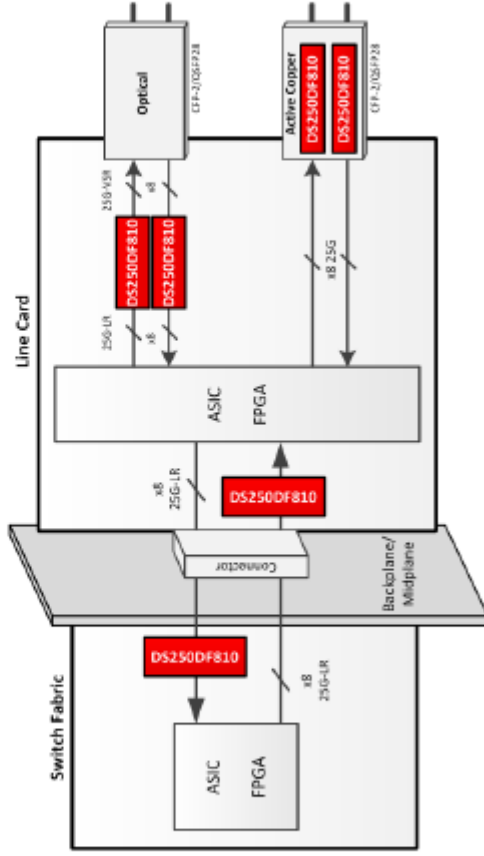


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

Exhibit A-7

Claim 8

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

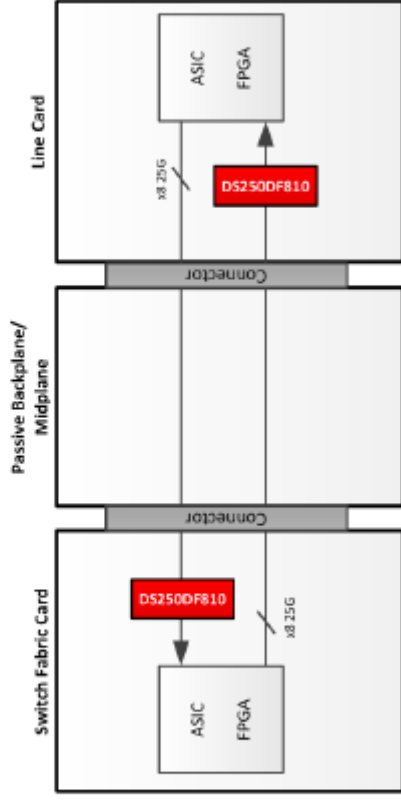


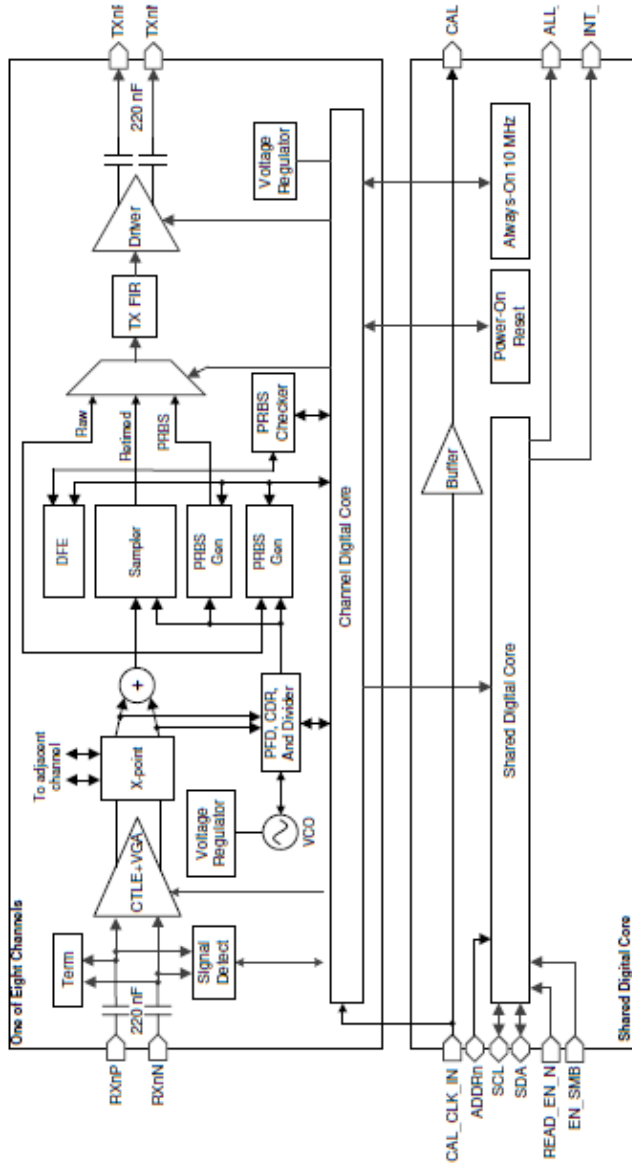
Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

<p>Claim 8</p>	<p>DS250DF810, 79.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 8

9.2 Functional Block Diagram



DS250DF810, 17.

Exhibit A-7

<p>Claim 8</p>	<p>9.3.8 Clock and Data Recovery (CDR) The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes. By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF810 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator. The CDR requires the following in order to be properly configured:</p> <ul style="list-style-type: none">• 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN).• Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF810, 19.</p>
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Claim 8

9.3.10 Differential Driver with FIR Filter

The DS250DF810 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. $C[0]$ can take on values in the range [-31, +31]. $C[-1]$ and $C[+1]$ can take on values in the range [-15, 15].

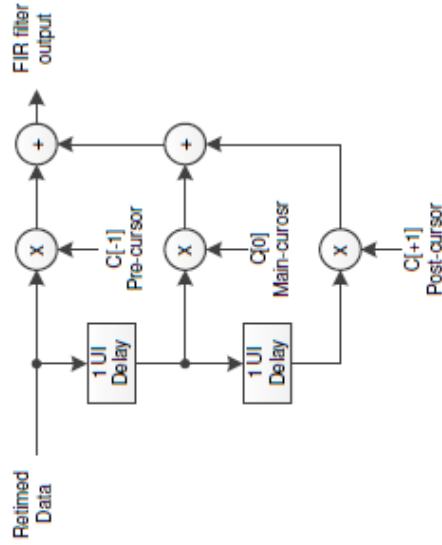


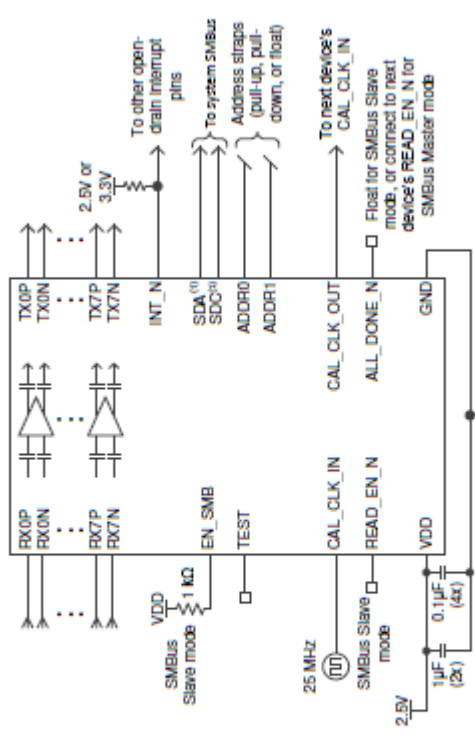
Figure 7. FIR Filter Functional Model

When utilizing the FIR filter, it is important to abide by the following general rules:

- $|C[-1]+C[0]+C[+1]| \leq 31$; the FIR tap coefficients absolute sum must be less or equal to 31)
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform in order to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
- $VOD_{low-frequency} = V_2 - V_5$
- $Rpre_{dB} = 20 * \log_{10} (V_3/V_2)$
- $Rpst_{dB} = 20 * \log_{10} (V_1/V_2)$

<p>Claim 8</p>	<p>DS250DF810, 20.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>8[b] connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;</p>	<p>DS250DF810 discloses and/or renders obvious this limitation.</p> <p>4 Simplified Schematic</p>  <p>The schematic shows a multi-lane data interface with TX0P/TX0N, TX7P/TX7N, RX0P/RX0N, and RX7P/RX7N. Control signals include INT_N, SDA, SDC, ADDR0, and ADDR1. Power and timing signals include VDD, EN_SMB, TEST, CAL_CLK_IN, CAL_CLK_OUT, CAL_CLK_IN, READ_EN_N, and VDD. Timing components include a 25 MHz oscillator, a 1µF capacitor, and a 0.1µF capacitor. A note indicates that SMBus signals need to be pulled up elsewhere in the system.</p>
<p>DS250DF810, 1.</p>	<p>DS250DF810, 1.</p>

Claim 8

10.1 Application Information

The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

10.2 Typical Application

The DS250DF810 is typically used in the following main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port jitter cleaning / retiming for optical applications

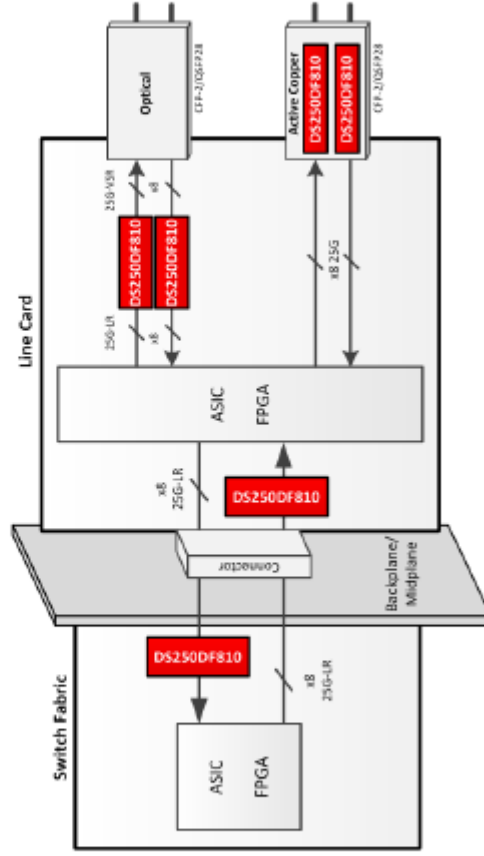


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

Exhibit A-7

Claim 8

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

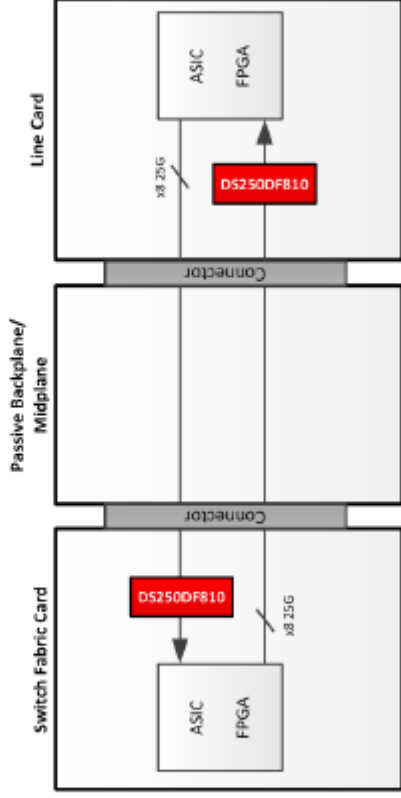
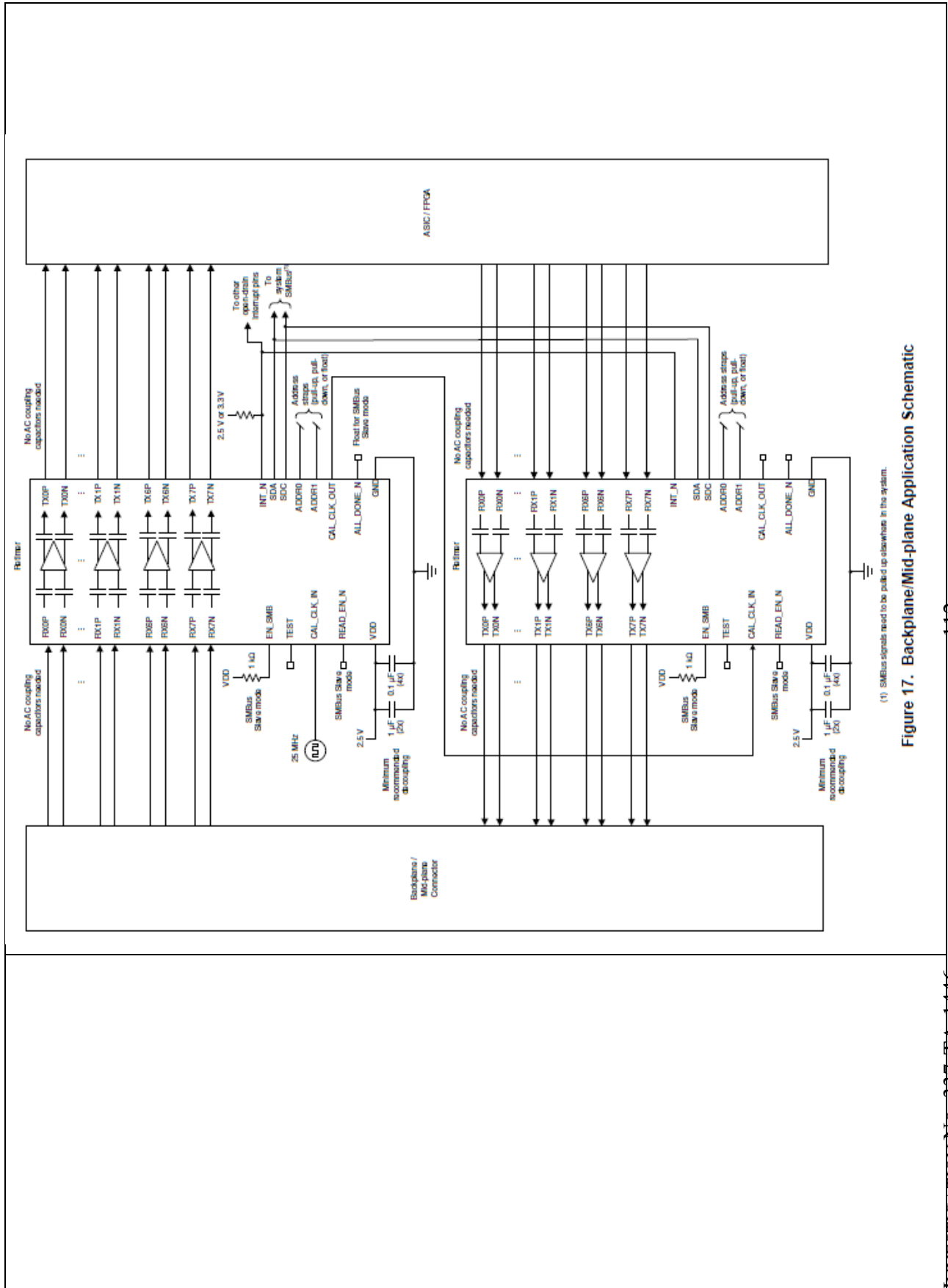


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7



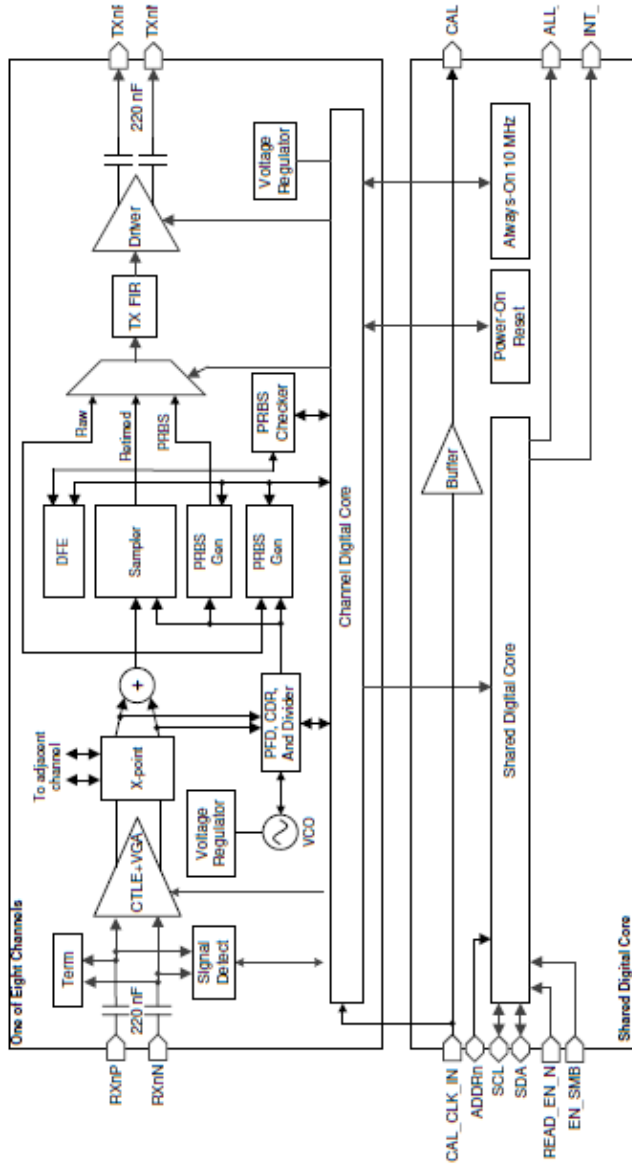
(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Backplane/Mid-plane Application Schematic

<p>Claim 8</p>	<p>DS250DF810, 79.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 8

9.2 Functional Block Diagram



DS250DF810, 17.

Exhibit A-7

<p>Claim 8</p>	<p>9.3.8 Clock and Data Recovery (CDR) The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes. By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF810 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator. The CDR requires the following in order to be properly configured:</p> <ul style="list-style-type: none"> • 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN). • Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF810, 19.</p>
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Claim 8

9.3.10 Differential Driver with FIR Filter

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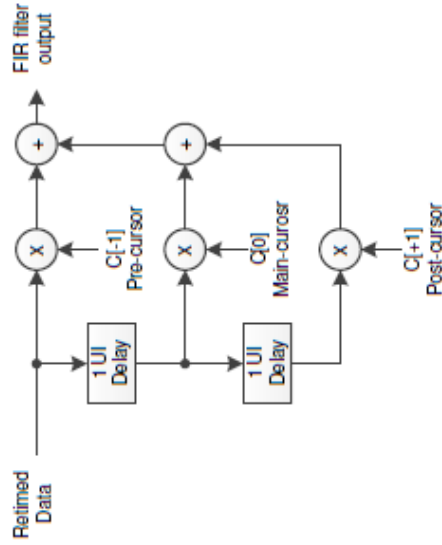


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- $\text{sgn}(C[-1])=\text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform in order to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
- $VOD_{low-frequency} = V_2 - V_5$
- $Rpre_{dB} = 20 * \log_{10} (V_3/V_2)$
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<p>Claim 8</p>	<p>DS250DF810, 20.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>8[c] connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween,</p>	<p>4 Simplified Schematic</p> <p>(1) SMBus signals need to be pulled up elsewhere in the system.</p>
	<p>DS250DF810, 1.</p>

Claim 8

10.1 Application Information

The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

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1. Backplane and mid-plane reach extension
2. Front-port jitter cleaning / retiming for optical applications

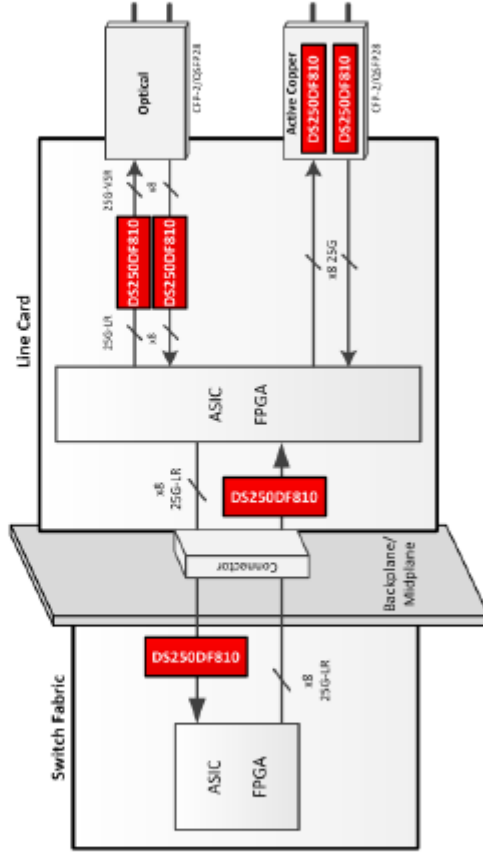


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

Exhibit A-7

Claim 8

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

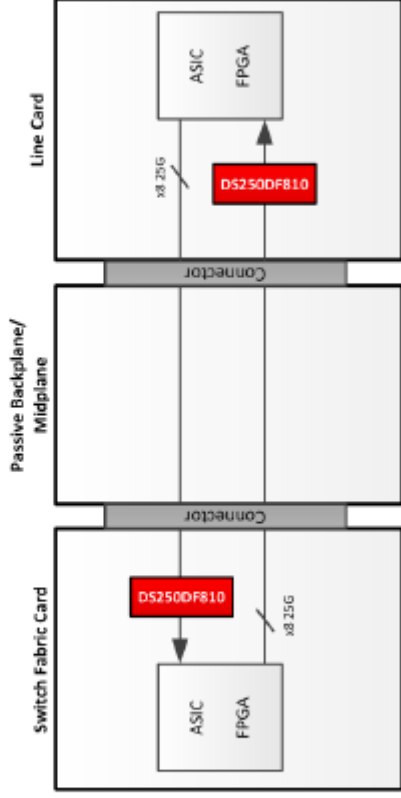
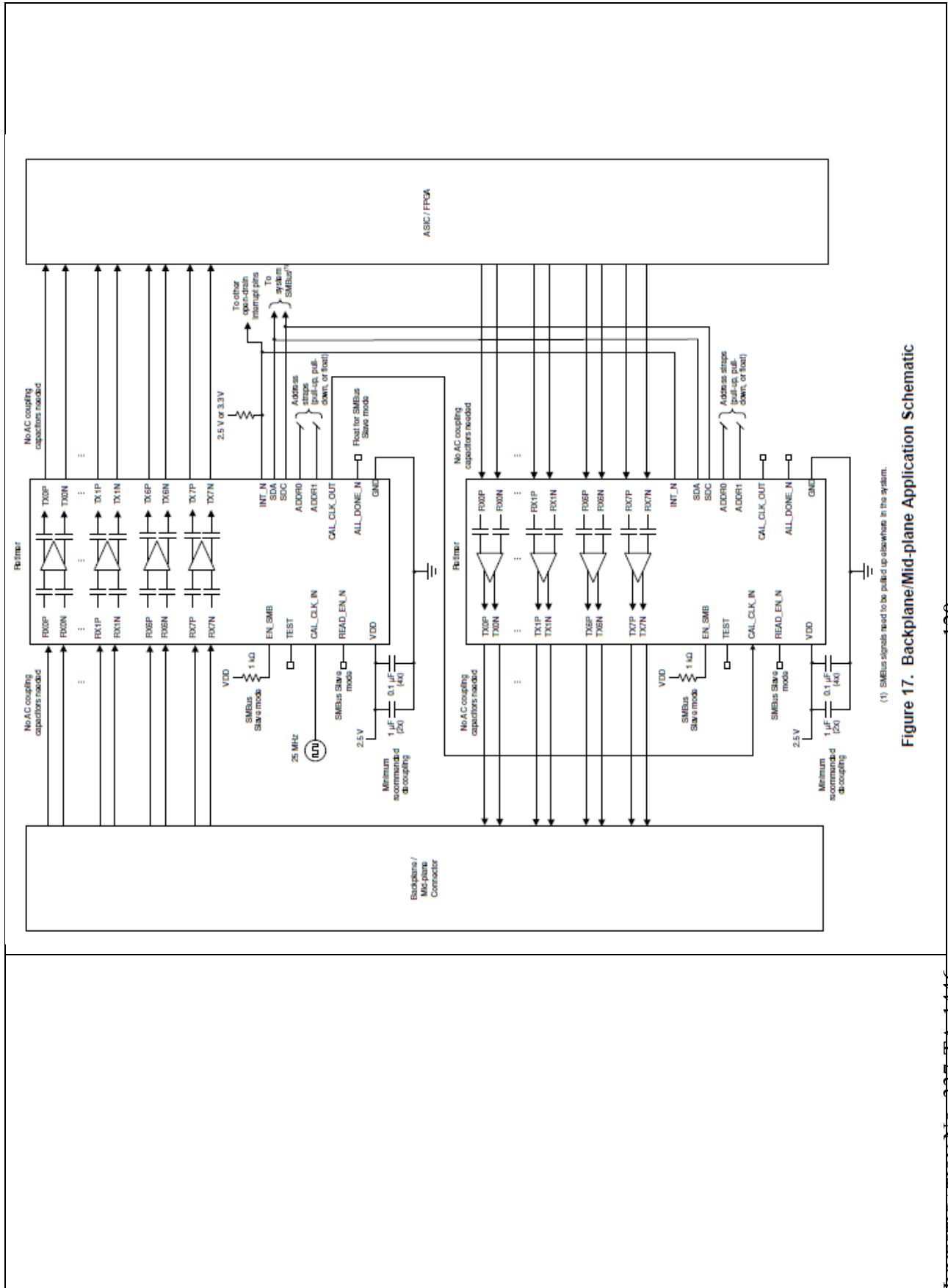


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7



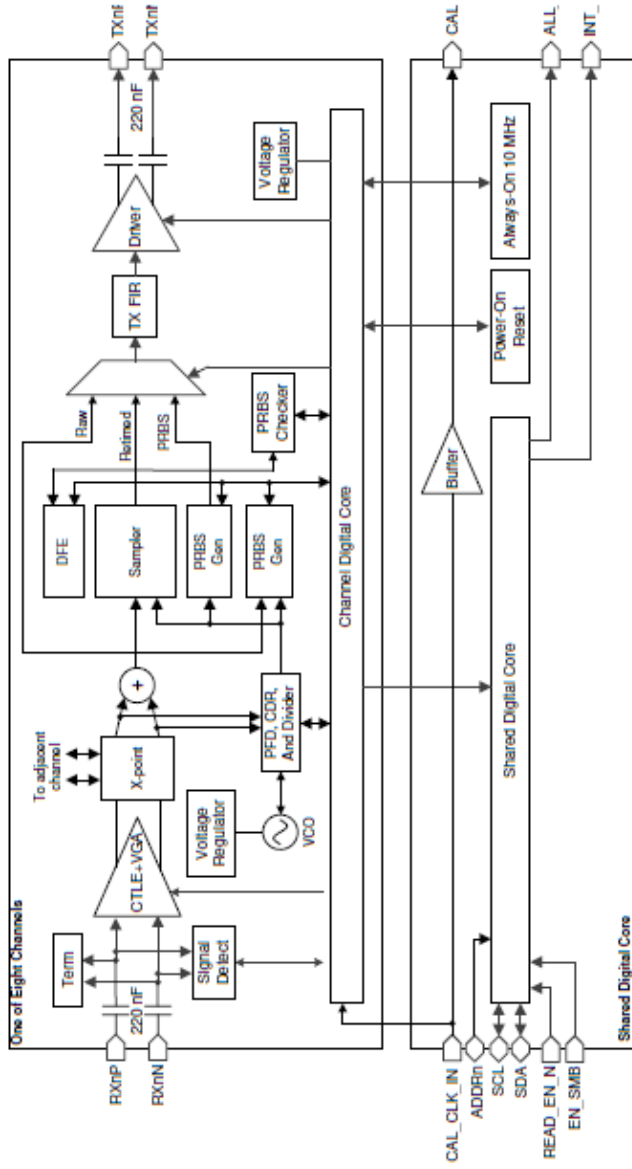
(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Backplane/Mid-plane Application Schematic

<p>Claim 8</p>	<p>DS250DF810, 79.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 8

9.2 Functional Block Diagram



DS250DF810, 17.

To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine in the Cover Pleading and/or other invalidity claim charts. The ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

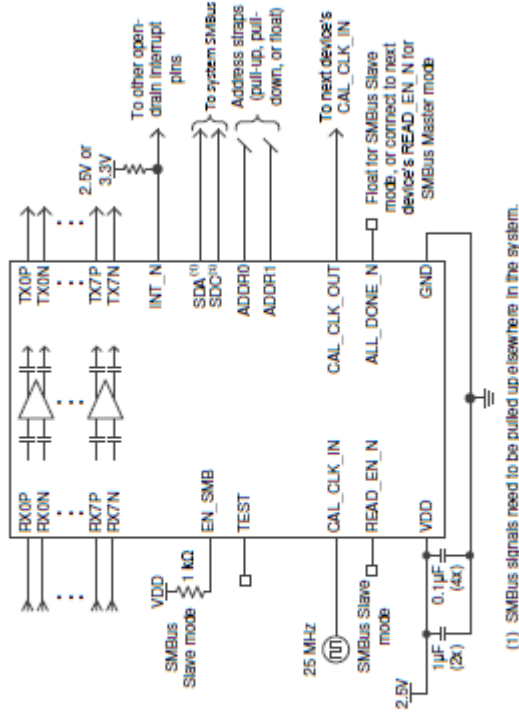
8[d] the first DRR device converting between said

DS250DF810 discloses and/or renders obvious this limitation.

Claim 8

electrical transit signals and said multi-lane data streams for the first host interface port, and

4 Simplified Schematic



(1) SMBus signals need to be pulled up elsewhere in the system.

DS250DF810, 1.

Claim 8

10.1 Application Information

The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

10.2 Typical Application

The DS250DF810 is typically used in the following main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port jitter cleaning / retiming for optical applications

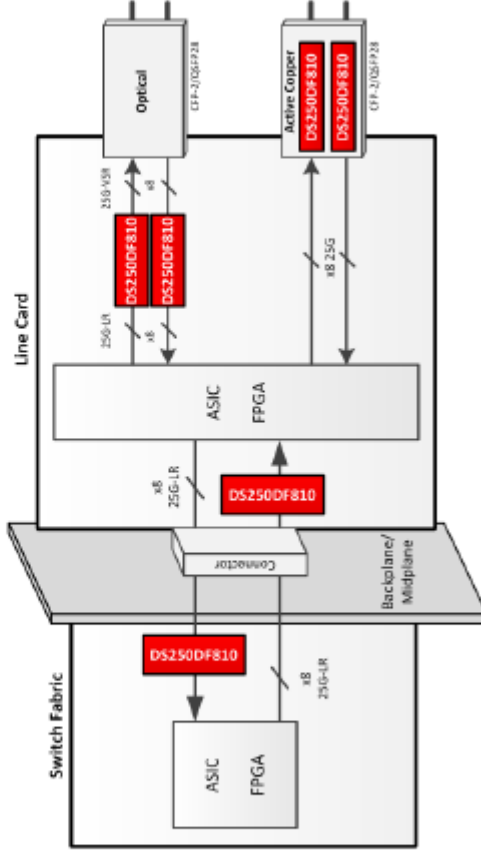


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

Exhibit A-7

Claim 8

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

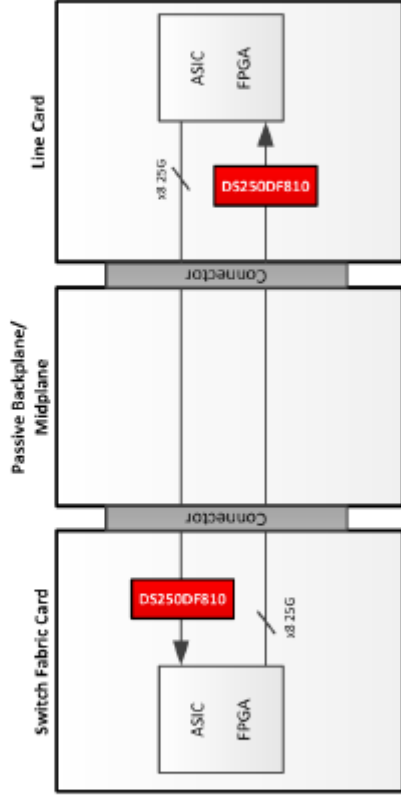
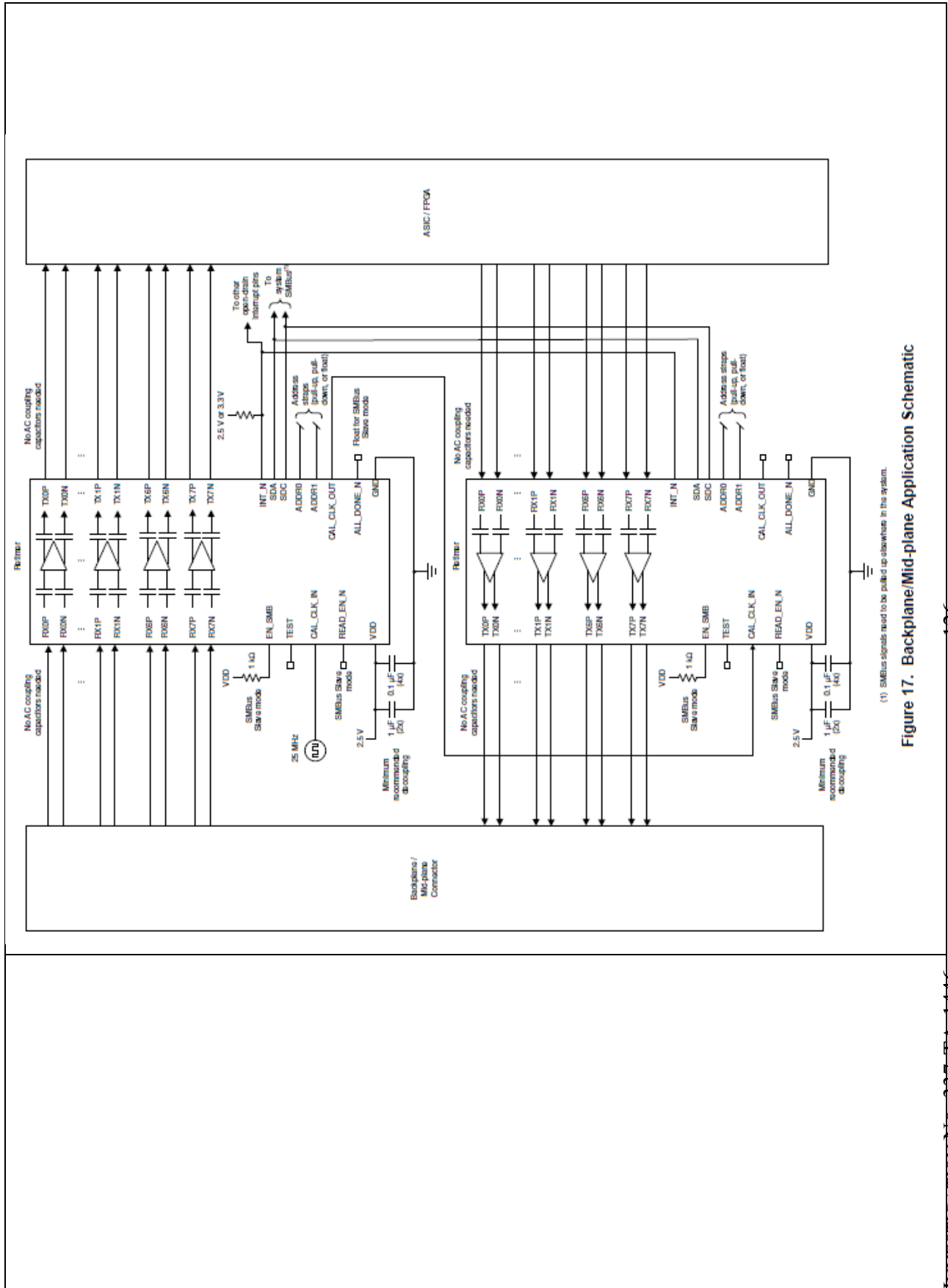


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7



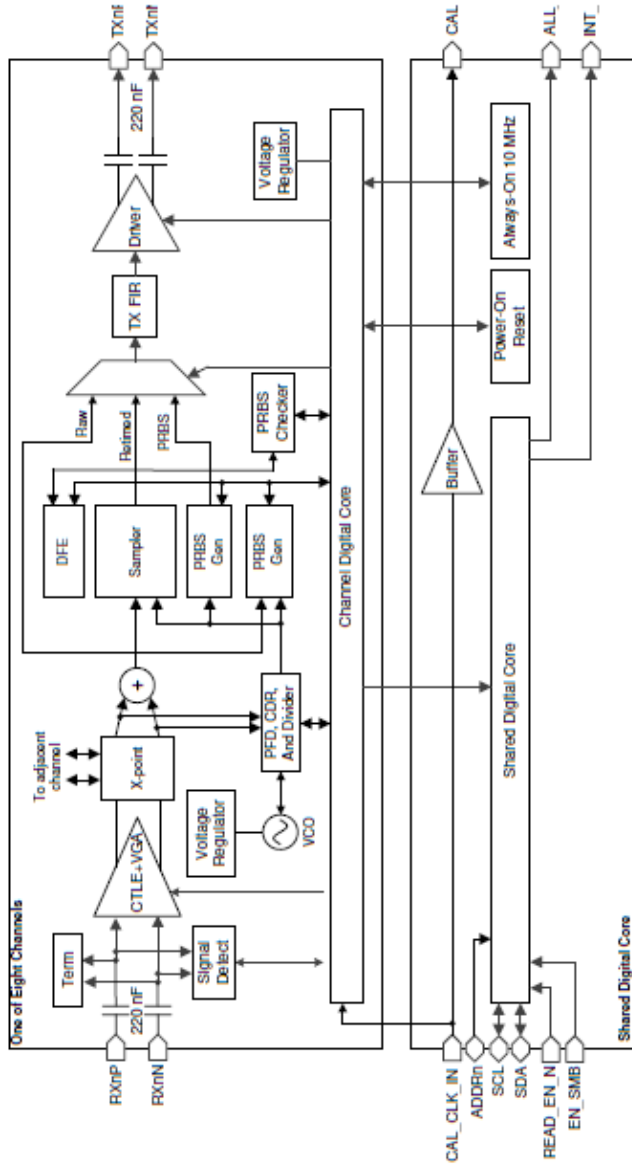
(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Backplane/Mid-plane Application Schematic

<p>Claim 8</p>	<p>DS250DF810, 79.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 8

9.2 Functional Block Diagram



DS250DF810, 17.

Exhibit A-7

<p>Claim 8</p>	<p>9.3.8 Clock and Data Recovery (CDR) The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes. By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF810 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator. The CDR requires the following in order to be properly configured:</p> <ul style="list-style-type: none">• 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN).• Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF810, 19.</p>
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Claim 8

9.3.10 Differential Driver with FIR Filter

The DS250DF810 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. $C[0]$ can take on values in the range [-31, +31]. $C[-1]$ and $C[+1]$ can take on values in the range [-15, 15].

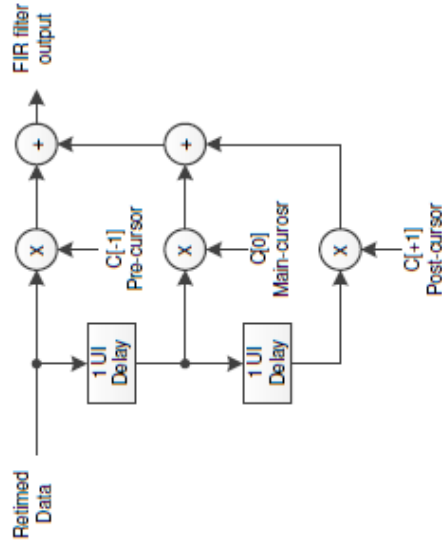


Figure 7. FIR Filter Functional Model

When utilizing the FIR filter, it is important to abide by the following general rules:

- $|C[-1]+C[0]+C[+1]| \leq 31$; the FIR tap coefficients absolute sum must be less or equal to 31)
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform in order to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
- $VOD_{low-frequency} = V_2 - V_5$
- $R_{pre-dB} = 20 * \log_{10} (V_3/V_2)$
- $R_{pst-dB} = 20 * \log_{10} (V_1/V_2)$

<p>Claim 8</p>	<p>DS250DF810, 20.</p> <p>DS250DF810 discloses and/or renders obvious this limitation.</p> <p>4 Simplified Schematic</p> <p>(1) SMBus signals need to be pulled up elsewhere in the system.</p>
<p>8[e] the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port,</p>	<p>DS250DF810, 1.</p>

Claim 8

10.1 Application Information

The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

10.2 Typical Application

The DS250DF810 is typically used in the following main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port jitter cleaning / retiming for optical applications

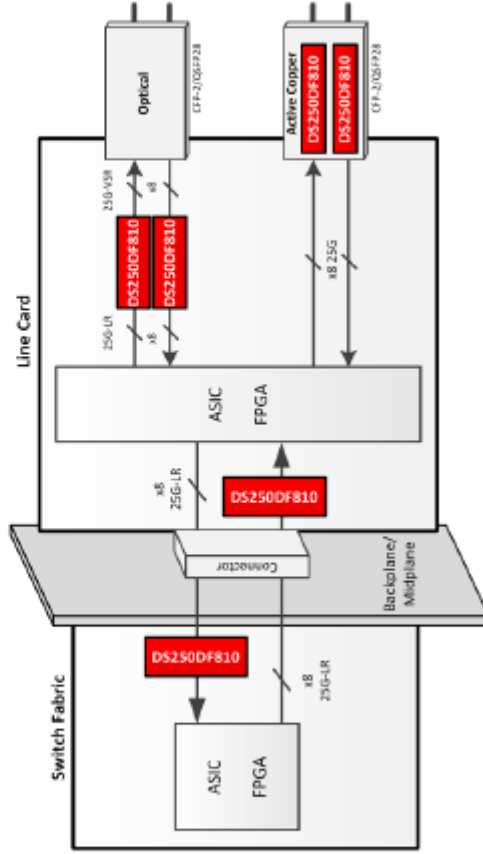


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

Exhibit A-7

Claim 8

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

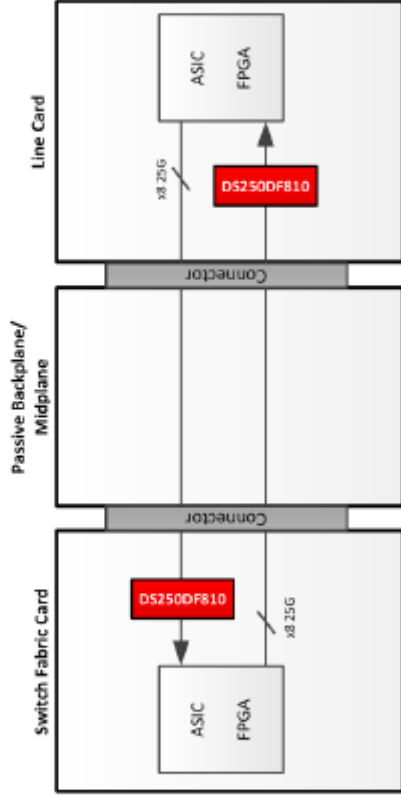
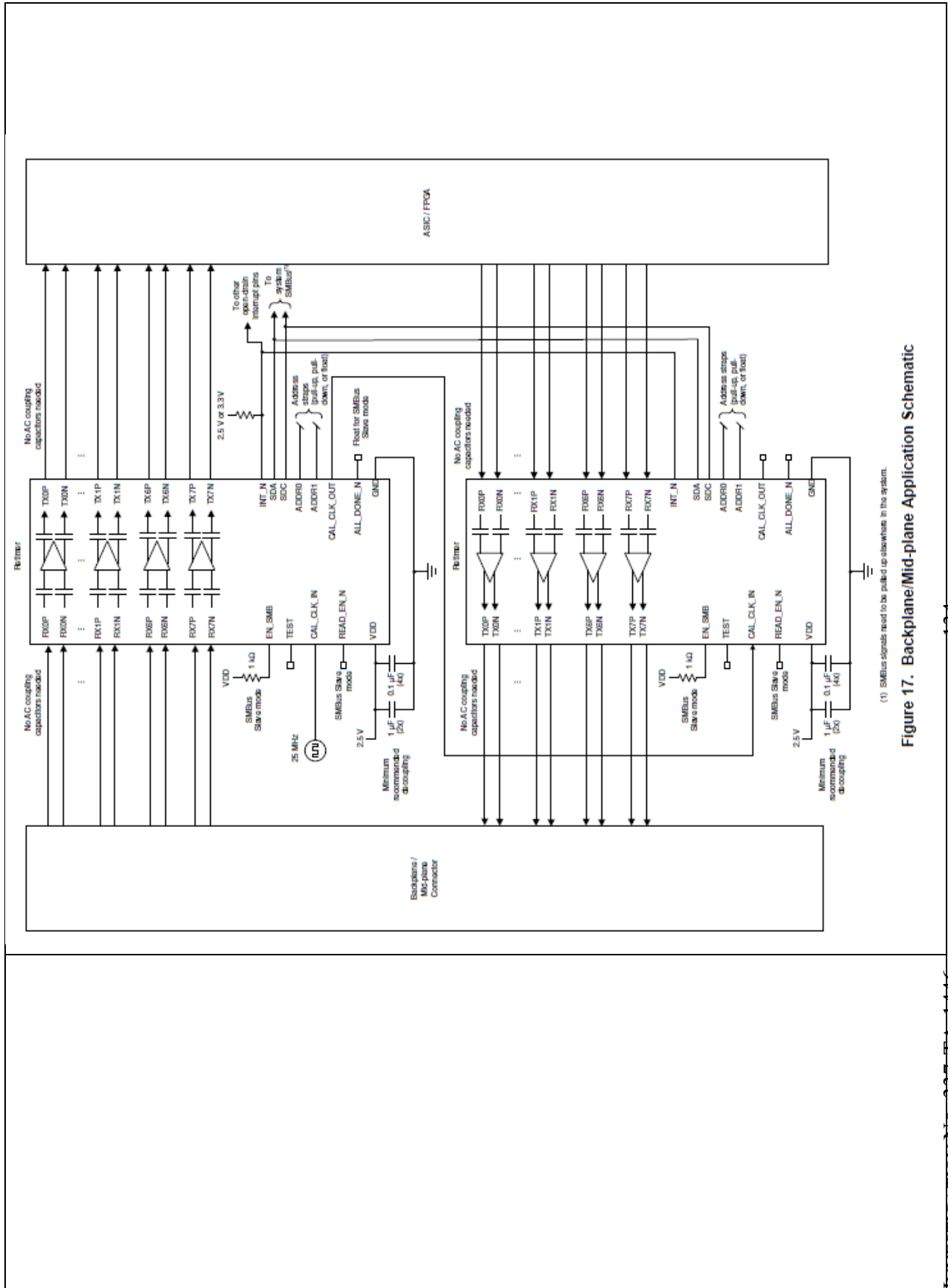


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7



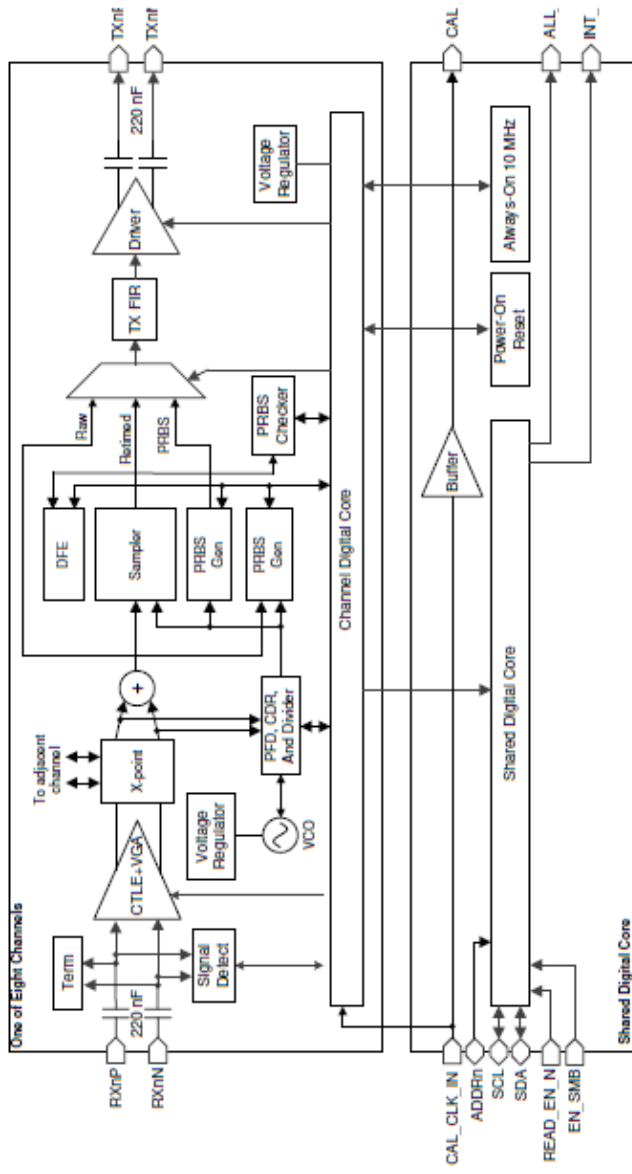
(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Backplane/Mid-plane Application Schematic

<p>Claim 8</p>	<p>DS250DF810, 79.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 8

9.2 Functional Block Diagram



DS250DF810, 17.

Exhibit A-7

<p>Claim 8</p>	<p>9.3.8 Clock and Data Recovery (CDR) The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes. By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF810 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator. The CDR requires the following in order to be properly configured:</p> <ul style="list-style-type: none">• 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN).• Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF810, 19.</p>
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Claim 8

9.3.10 Differential Driver with FIR Filter

The DS250DF810 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. $C[0]$ can take on values in the range [-31, +31]. $C[-1]$ and $C[+1]$ can take on values in the range [-15, 15].

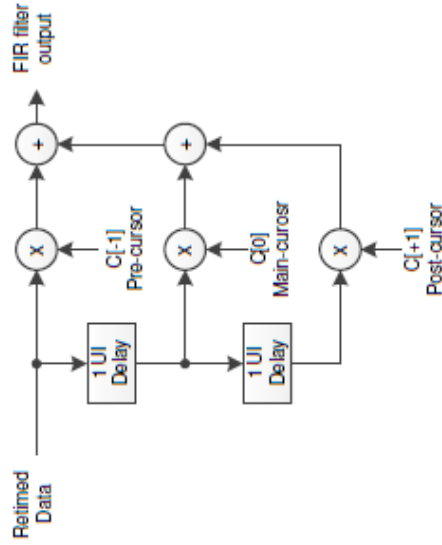


Figure 7. FIR Filter Functional Model

When utilizing the FIR filter, it is important to abide by the following general rules:

- $|C[-1]+C[0]+C[+1]| \leq 31$; the FIR tap coefficients absolute sum must be less or equal to 31)
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform in order to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
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- $R_{pre-dB} = 20 * \log_{10} (V_3/V_2)$
- $R_{pst-dB} = 20 * \log_{10} (V_1/V_2)$

Exhibit A-7

Claim 8	
<p>8[f] the first and second DRR devices providing preequalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.</p>	<p>DS250DF810, 20.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>

Exhibit A-7

Claim 8

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSORS: REG_0x3E[6:0]	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Claim 8

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 8

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

Claim 8	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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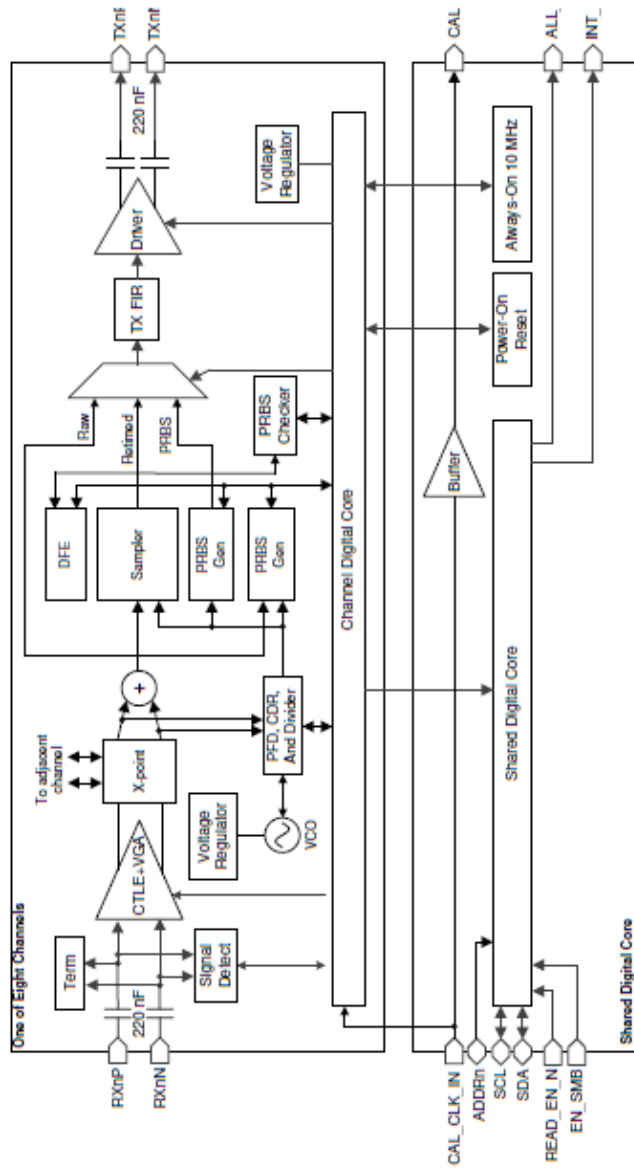
I. DEPENDENT CLAIM 2

Claim 9	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>
<p>9. The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.</p>	

<p>Claim 9</p>	<p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 9

9.2 Functional Block Diagram



DS250DF810, 17.

<p>Claim 9</p>	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 9</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Exhibit A-7

Claim 9

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	0	0	0	0.205	NA	NA
0	+1	0	0	0.280	NA	NA
0	+2	0	0	0.305	NA	NA
0	+3	0	0	0.355	NA	NA
0	+4	0	0	0.385	NA	NA
0	+5	0	0	0.440	NA	NA
0	+6	0	0	0.490	NA	NA
0	+7	0	0	0.525	NA	NA
0	+8	0	0	0.565	NA	NA
0	+9	0	0	0.610	NA	NA
0	+10	0	0	0.650	NA	NA
0	+11	0	0	0.685	NA	NA
0	+12	0	0	0.720	NA	NA
0	+13	0	0	0.760	NA	NA
0	+14	0	0	0.790	NA	NA
0	+15	0	0	0.825	NA	NA
0	+16	0	0	0.860	NA	NA
0	+17	0	0	0.890	NA	NA
0	+18	0	0	0.925	NA	NA
0	+19	0	0	0.960	NA	NA
0	+20	0	0	0.985	NA	NA
0	+21	0	0	1.010	NA	NA
0	+22	0	0	1.040	NA	NA
0	+23	0	0	1.075	NA	NA
0	+24	0	0	1.095	NA	NA
0	+25	0	0	1.125	NA	NA
0	+26	0	0	1.150	NA	NA
0	+27	0	0	1.165	NA	NA
0	+28	0	0	1.190	NA	NA
0	+29	0	0	1.205	NA	NA
0	+30	0	0	1.220	NA	NA
0	+31	0	0	1.225	NA	NA
0	+18	-1	-1	0.980	NA	2.1
0	+17	-2	-2	0.960	NA	2.5
0	+16	-3	-3	0.960	NA	3.1
0	+15	-4	-4	0.960	NA	3.8
0	+14	-5	-5	0.960	NA	4.7

Claim 9

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 9

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

Claim 9	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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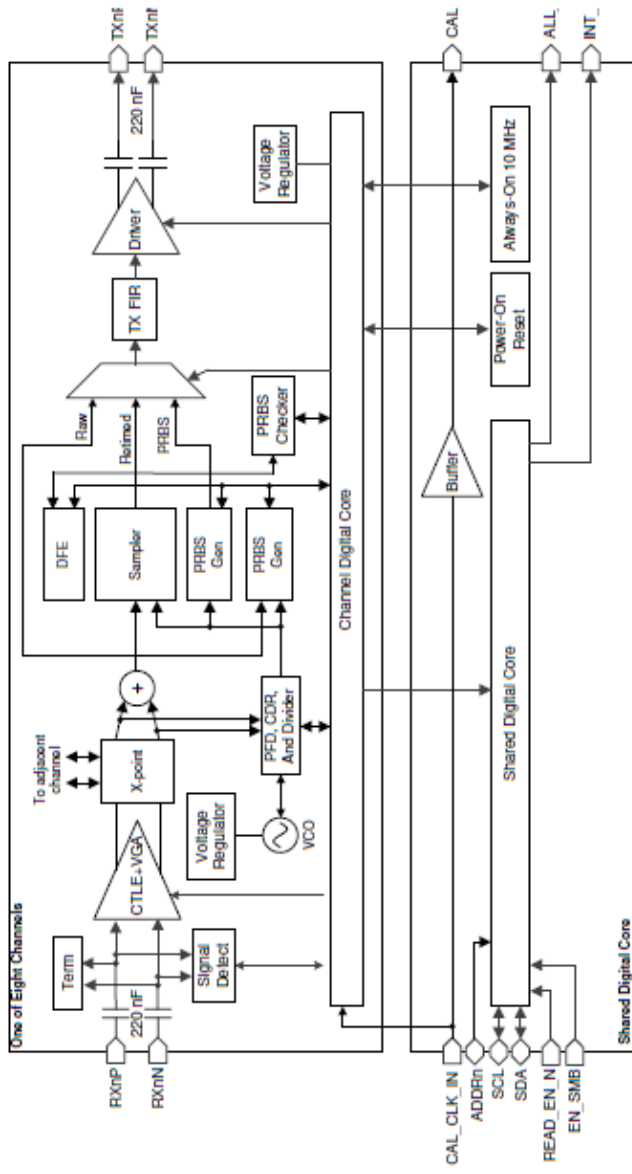
J. DEPENDENT CLAIM 10

Claim 10	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>
<p>10. The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.</p>	

<p>Claim 10</p>	<p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 10

9.2 Functional Block Diagram



DS250DF810, 17.

Claim 10	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 10</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Exhibit A-7

Claim 10

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSORS: REG_0x3E[6:0]	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 10

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

Claim 10	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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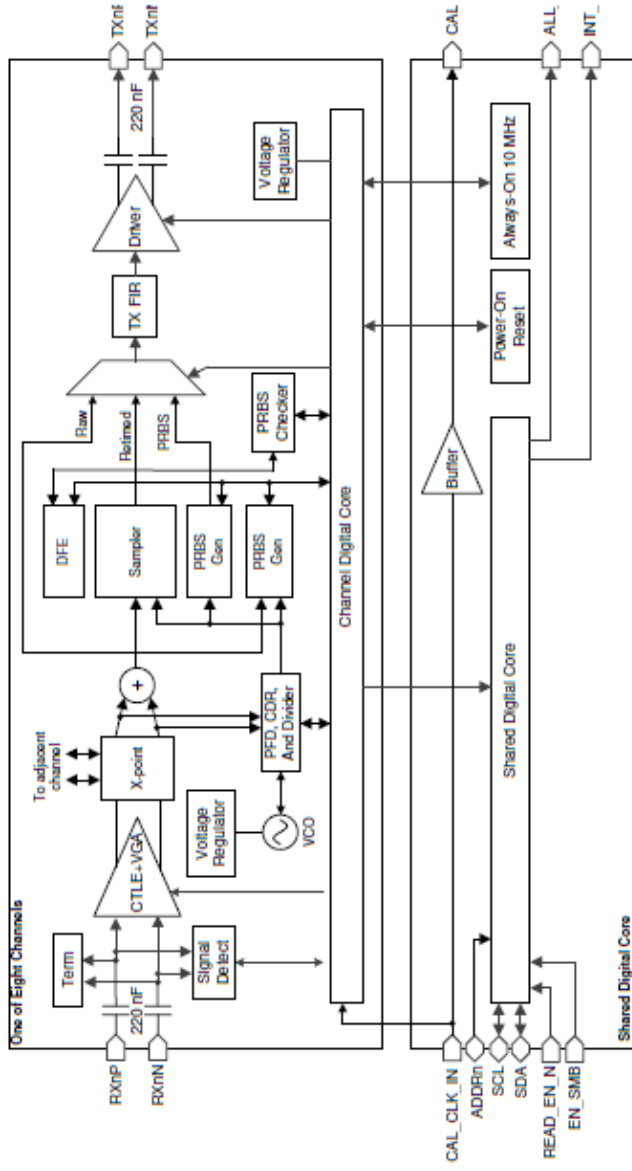
K. DEPENDENT CLAIM 11

Claim 11	<p>11. The method of claim 10, further comprising: after connecting the electrical conductors, characterizing the channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.</p> <p>DS250DF810 discloses and/or renders obvious this limitation.</p>
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<p>Claim 11</p>	<p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 11

9.2 Functional Block Diagram



DS250DF810, 17.

<p>Claim 11</p>	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 11</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Exhibit A-7

Claim 11

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSORS: REG_0x3E[6:0]	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 11

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

	<p>Claim 11</p> <p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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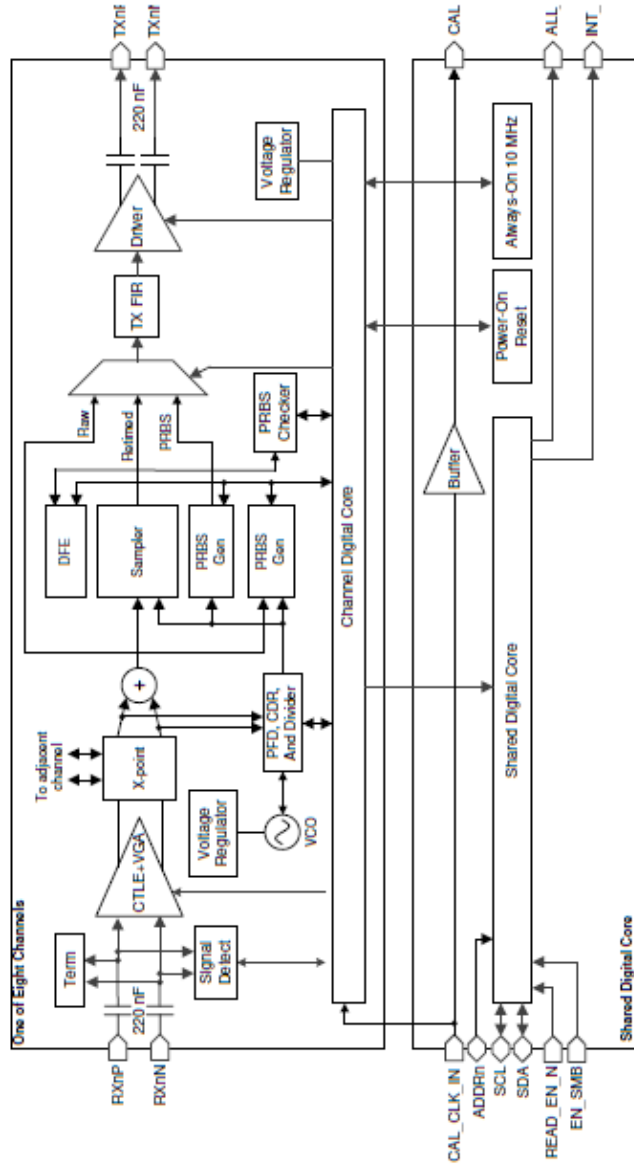
L. DEPENDENT CLAIM 12

<p>Claim 12</p> <p>12. The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.</p>	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>
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<p>Claim 12</p>	<p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 12

9.2 Functional Block Diagram



DS250DF810, 17.

<p>Claim 12</p>	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 12</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Claim 12

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSORS: REG_0x3E[6:0]	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 12

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

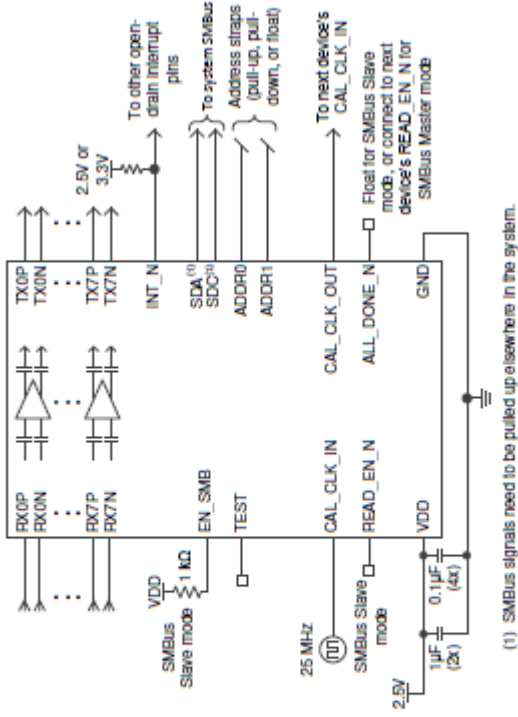
Claim 12	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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M. DEPENDENT CLAIM 13

Claim 13	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>
<p>13. The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.</p>	

Claim 13

4 Simplified Schematic



DS250DF810, 1.

(1) SMBus signals need to be pulled up elsewhere in the system.

Claim 13

10.1 Application Information

The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

10.2 Typical Application

The DS250DF810 is typically used in the following main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port jitter cleaning / retiming for optical applications

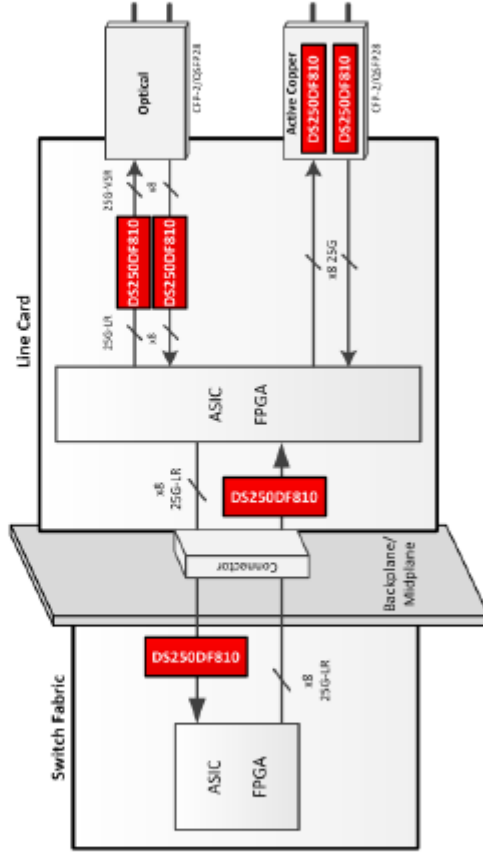


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

Claim 13

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

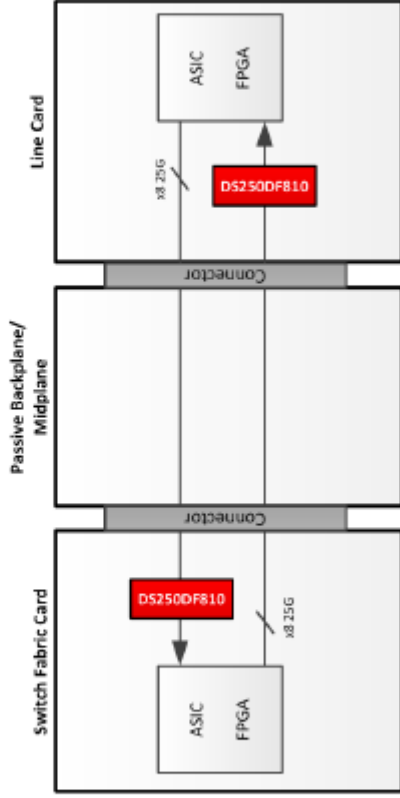


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7

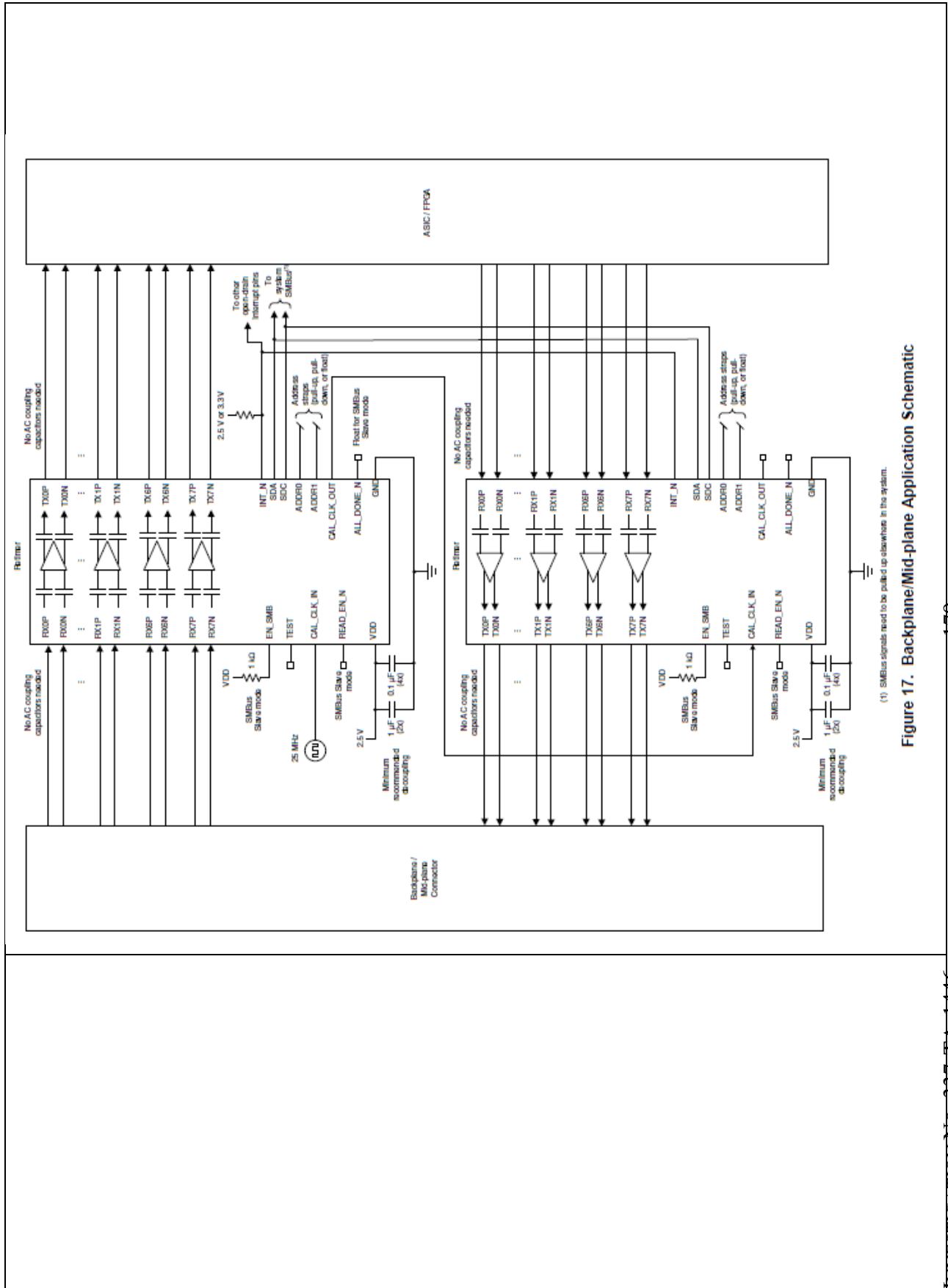


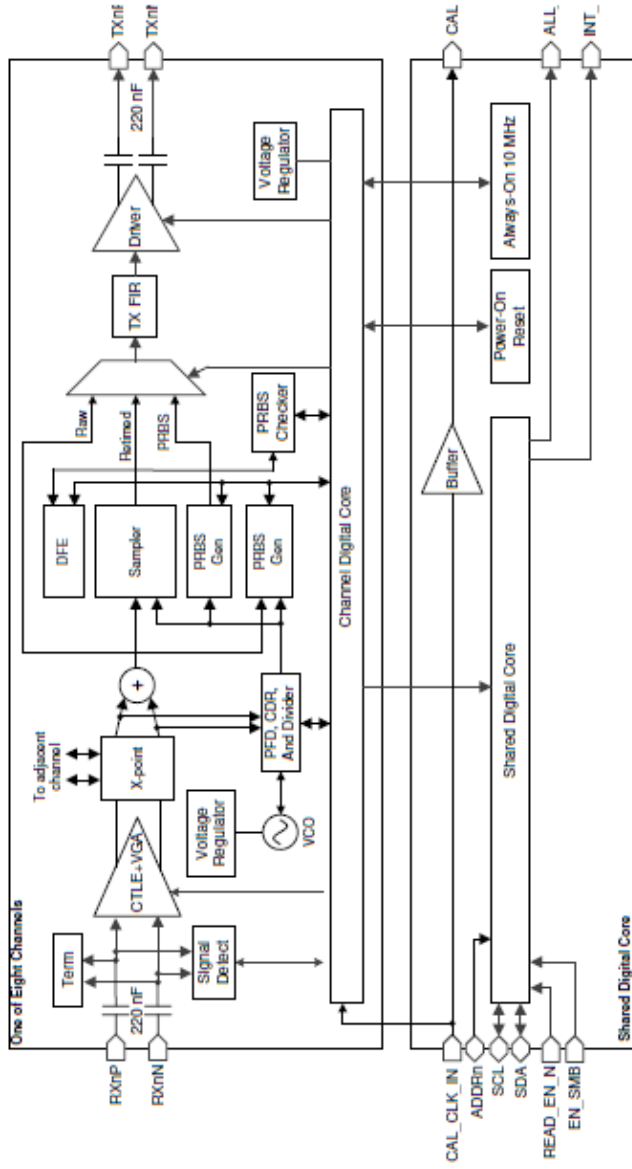
Figure 17. Backplane/Mid-plane Application Schematic

(1) SMBus signals need to be pulled up elsewhere in the system.

<p>Claim 13</p>	<p>DS250DF810, 79.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 13

9.2 Functional Block Diagram



DS250DF810, 17.

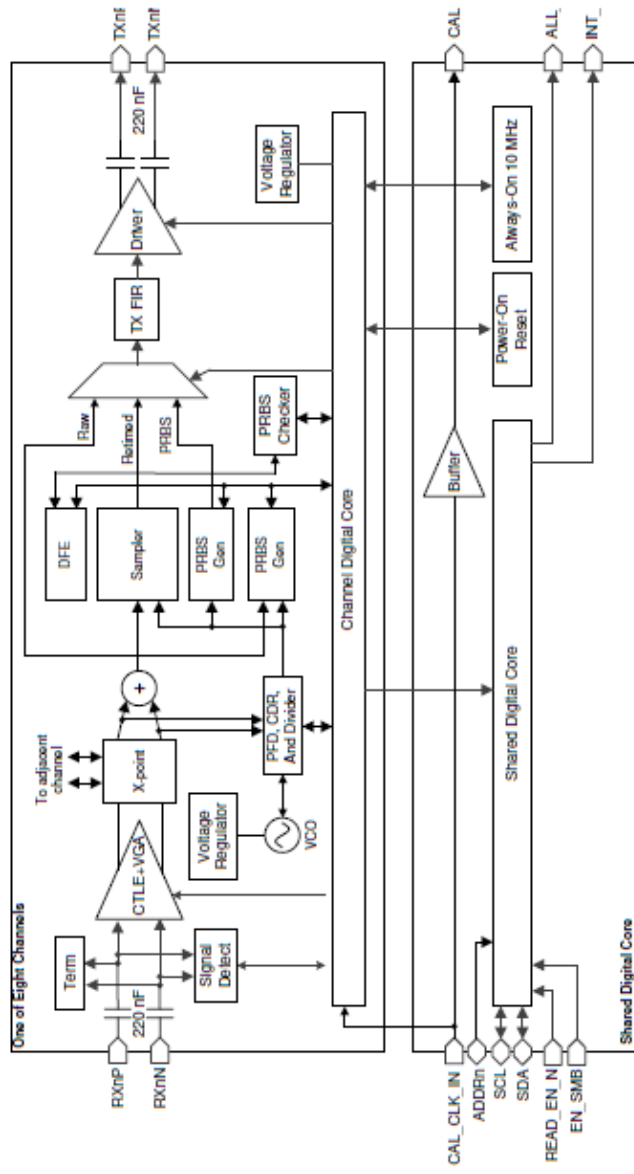
To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine in the Cover Pleading and/or other invalidity claim charts. The ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

N. DEPENDENT CLAIM 14

<p>Claim 14</p> <p>14. The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.</p>	<p>DS250DF810 discloses and/or renders obvious this limitation.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 14

9.2 Functional Block Diagram



DS250DF810, 17.

<p>Claim 14</p>	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 14</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Exhibit A-7

Claim 14

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSORS: REG_0x3E[6:0]	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 14

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

<p>Claim 14</p>	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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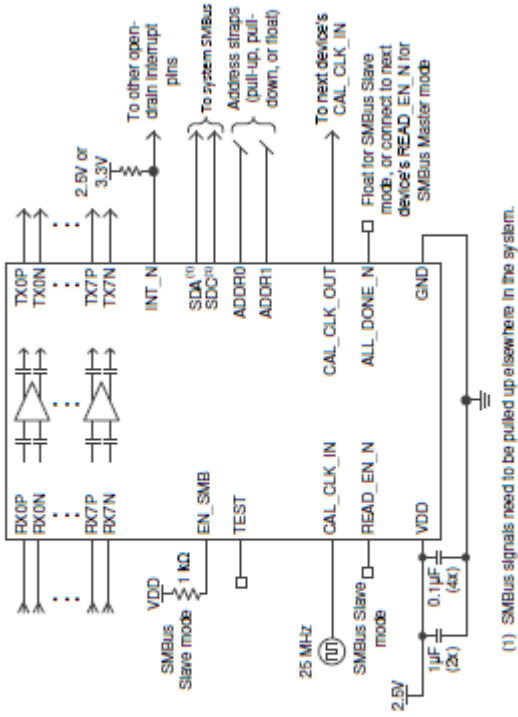
O. INDEPENDENT CLAIM 1

Claim 15

15[pre] A communications method that comprises:

To the extent the preamble is limiting, DS250DF810 discloses and/or renders obvious this limitation.

4 Simplified Schematic



DS250DF810, 1.

Claim 15

10.1 Application Information

The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

10.2 Typical Application

The DS250DF810 is typically used in the following main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port jitter cleaning / retiming for optical applications

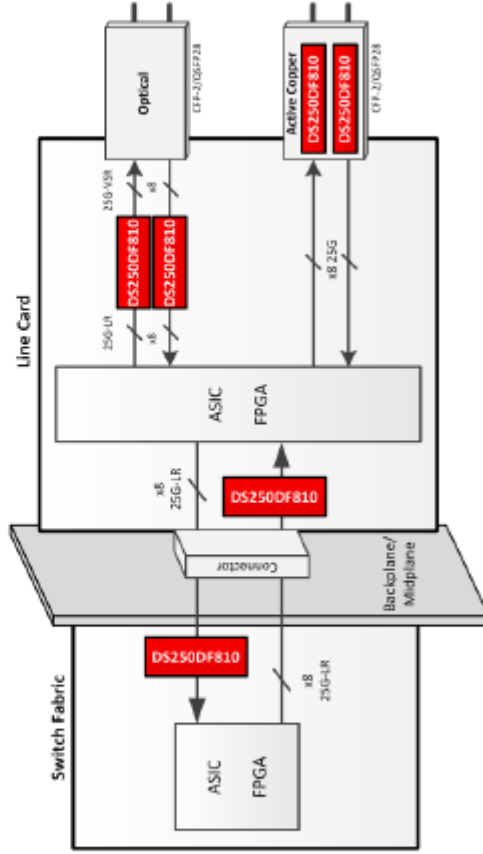


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

Claim 15

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

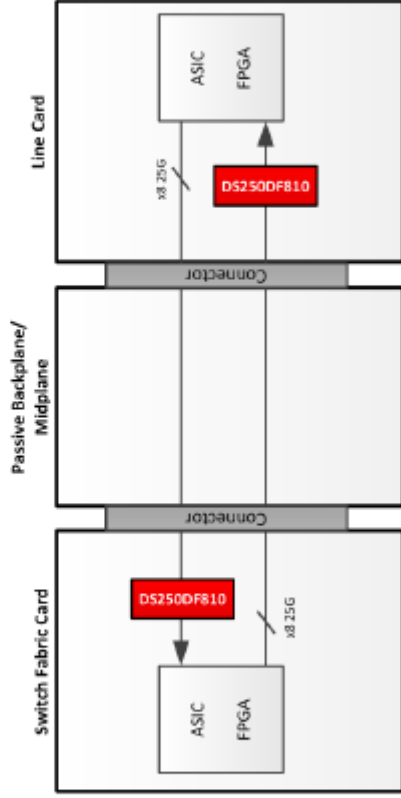


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7

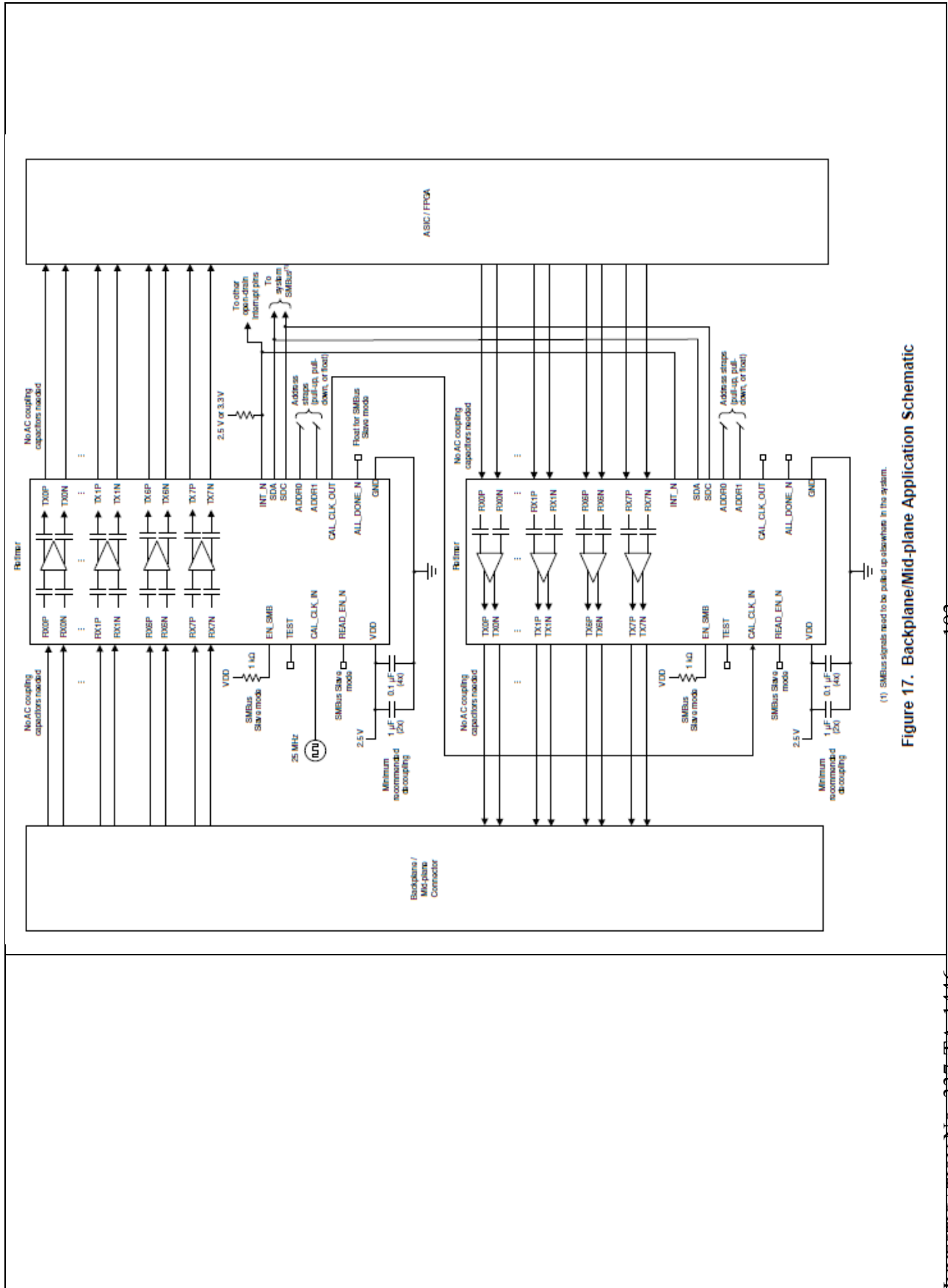


Figure 17. Backplane/Mid-plane Application Schematic

<p>Claim 15</p>	<p>To the extent that this preamble is not disclosed, either explicitly or inherently, by DS250DF810, this preamble is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p> <p>DS250DF810, 79.</p>
<p>15[a] inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and</p>	<p>DS250DF810 discloses and/or renders obvious this limitation.</p> <p>4 Simplified Schematic</p> <p>(1) SMBus signals need to be pulled up elsewhere in the system.</p>

DS250DF810, 1.

Claim 15

10.1 Application Information

The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

10.2 Typical Application

The DS250DF810 is typically used in the following main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port jitter cleaning / retiming for optical applications

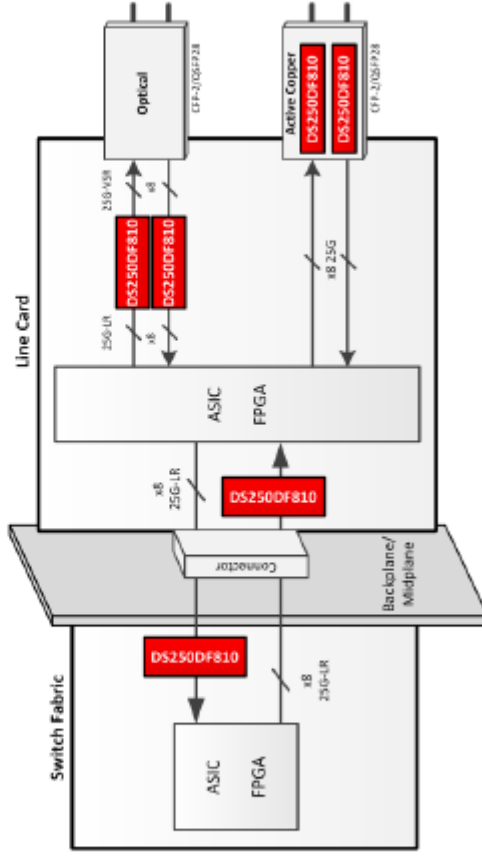


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

Claim 15

10.2.1 Backplane and Mid-Plane Applications

The DS250DF810 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF810 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

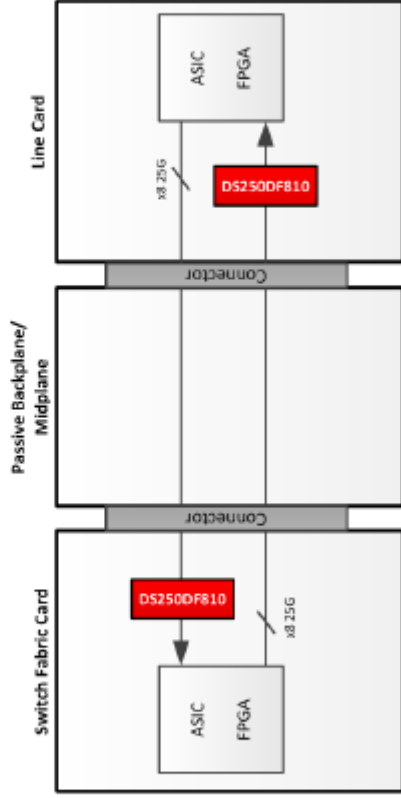


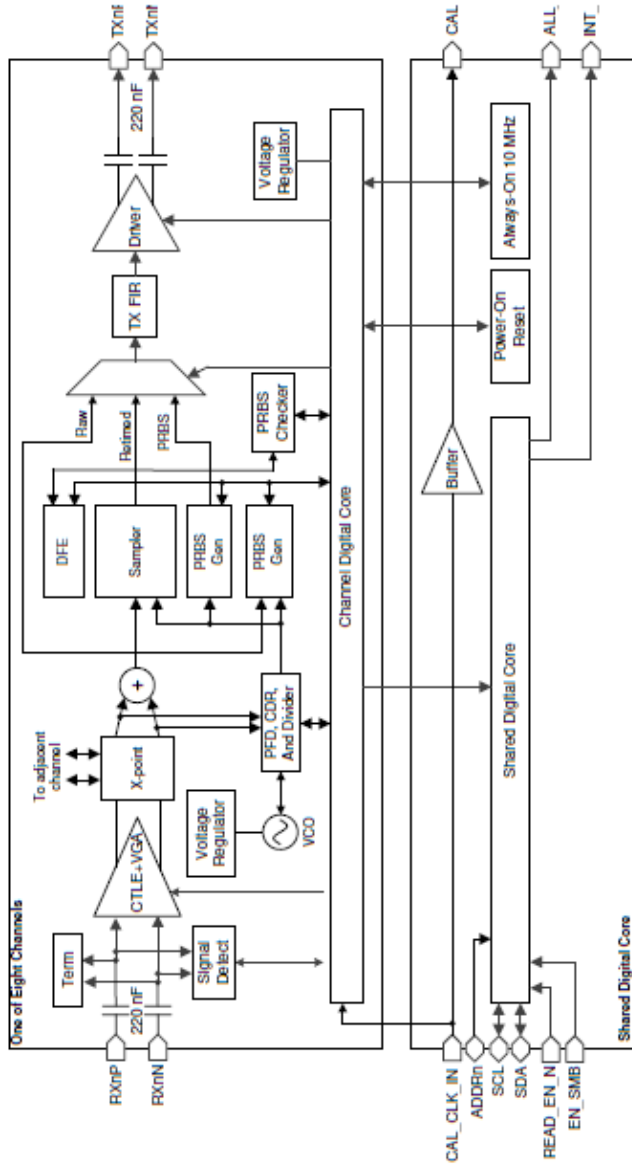
Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

<p>Claim 15</p>	<p>DS250DF810, 79.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 15

9.2 Functional Block Diagram



DS250DF810, 17.

Exhibit A-7

<p>Claim 15</p>	<p>9.3.8 Clock and Data Recovery (CDR) The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes. By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF810 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator. The CDR requires the following in order to be properly configured:</p> <ul style="list-style-type: none">• 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN).• Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF810, 19.</p>
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Claim 15

9.3.10 Differential Driver with FIR Filter

The DS250DF810 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. $C[0]$ can take on values in the range [-31, +31]. $C[-1]$ and $C[+1]$ can take on values in the range [-15, 15].

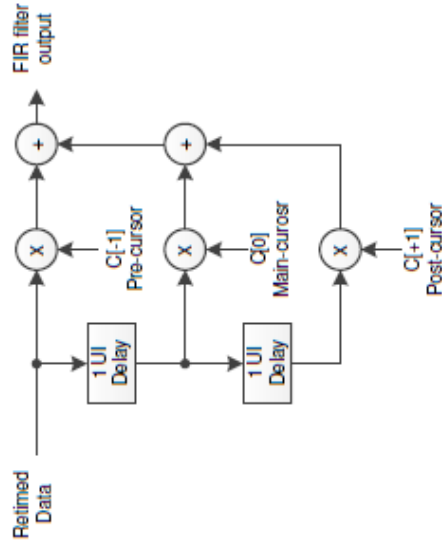


Figure 7. FIR Filter Functional Model

When utilizing the FIR filter, it is important to abide by the following general rules:

- $|C[-1]+C[0]+C[+1]| \leq 31$; the FIR tap coefficients absolute sum must be less or equal to 31)
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform in order to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
- $VOD_{low-frequency} = V_2 - V_5$
- $R_{pre-dB} = 20 * \log_{10} (V_3/V_2)$
- $R_{pst-dB} = 20 * \log_{10} (V_1/V_2)$

<p>Claim 15</p>	<p>DS250DF810, 20.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>15[b] inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,</p>	<p>DS250DF810 discloses and/or renders obvious this limitation.</p> <p>4 Simplified Schematic</p> <p>(1) SMBus signals need to be pulled up elsewhere in the system.</p>

DS250DF810, 1.

Claim 15

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The DS250DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

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2. Front-port jitter cleaning / retiming for optical applications

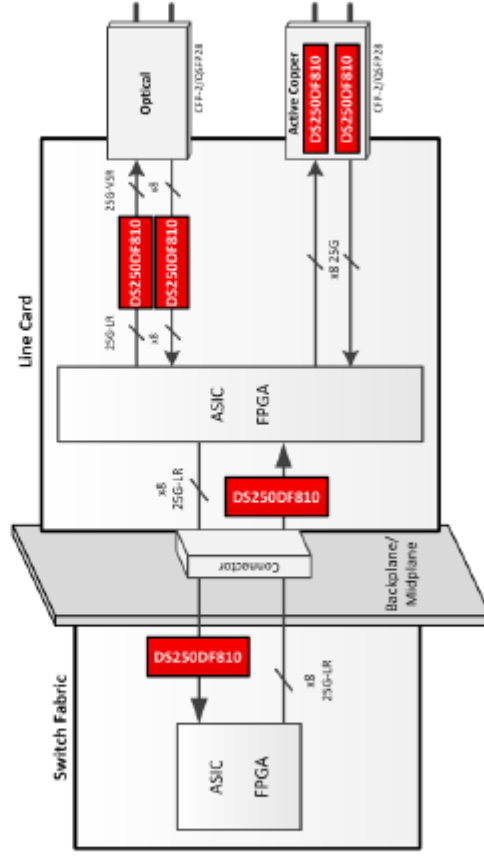


Figure 15. Typical Uses for the DS250DF810 in a System

DS250DF810, 77.

Claim 15

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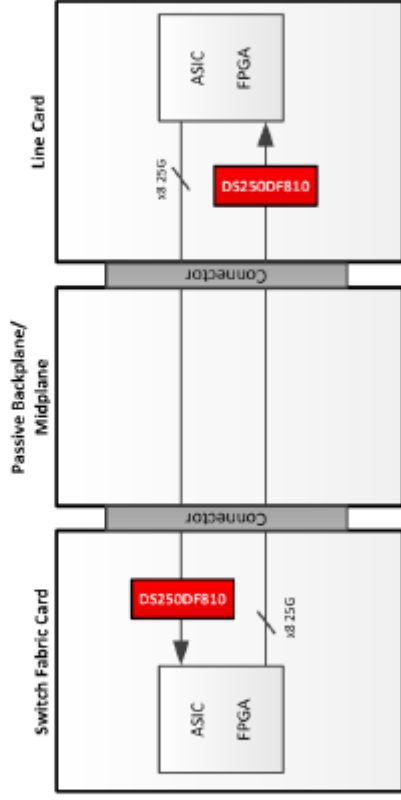
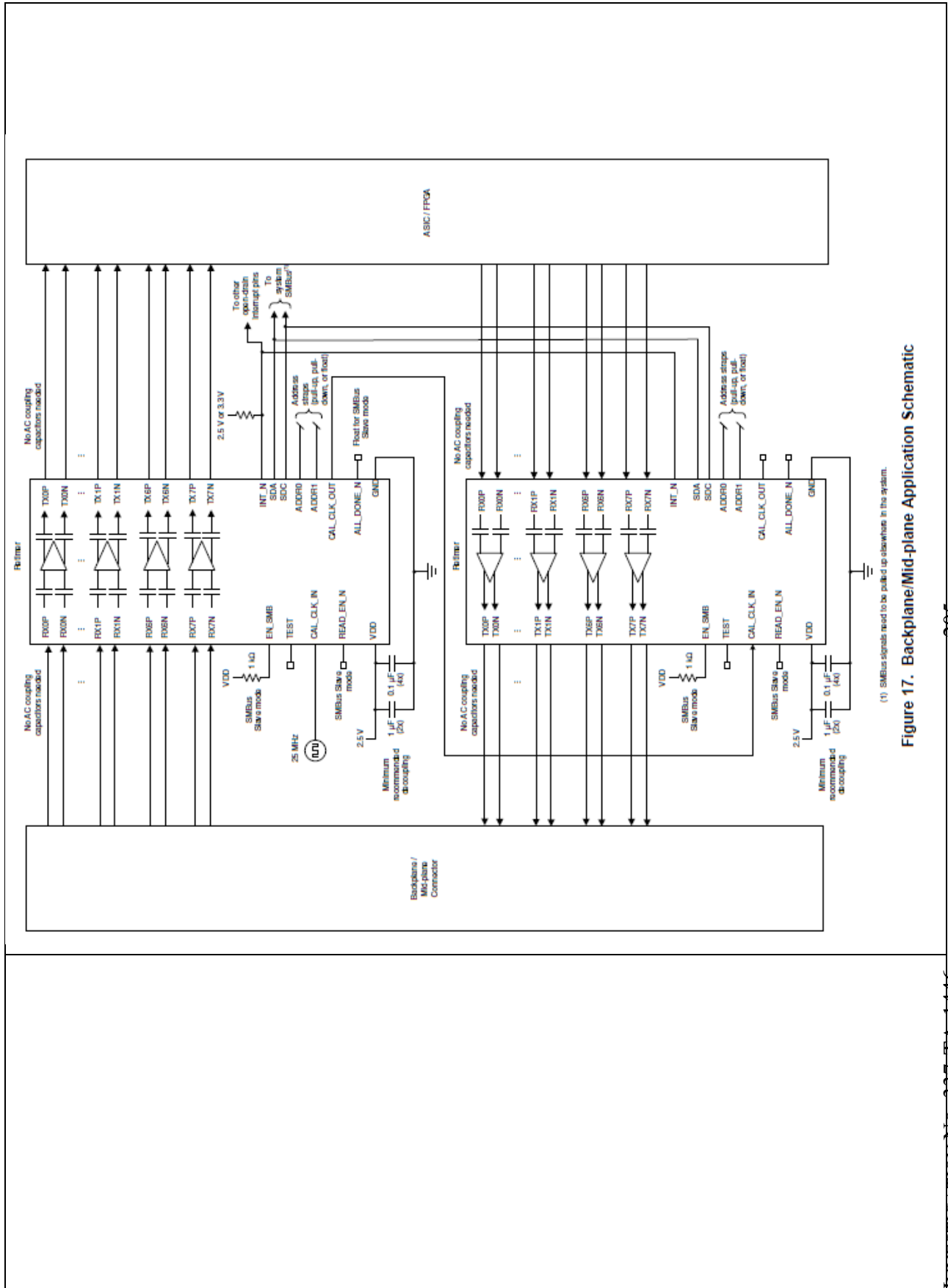


Figure 16. Backplane/Mid-plane Application Block Diagram

DS250DF810, 78.

Exhibit A-7



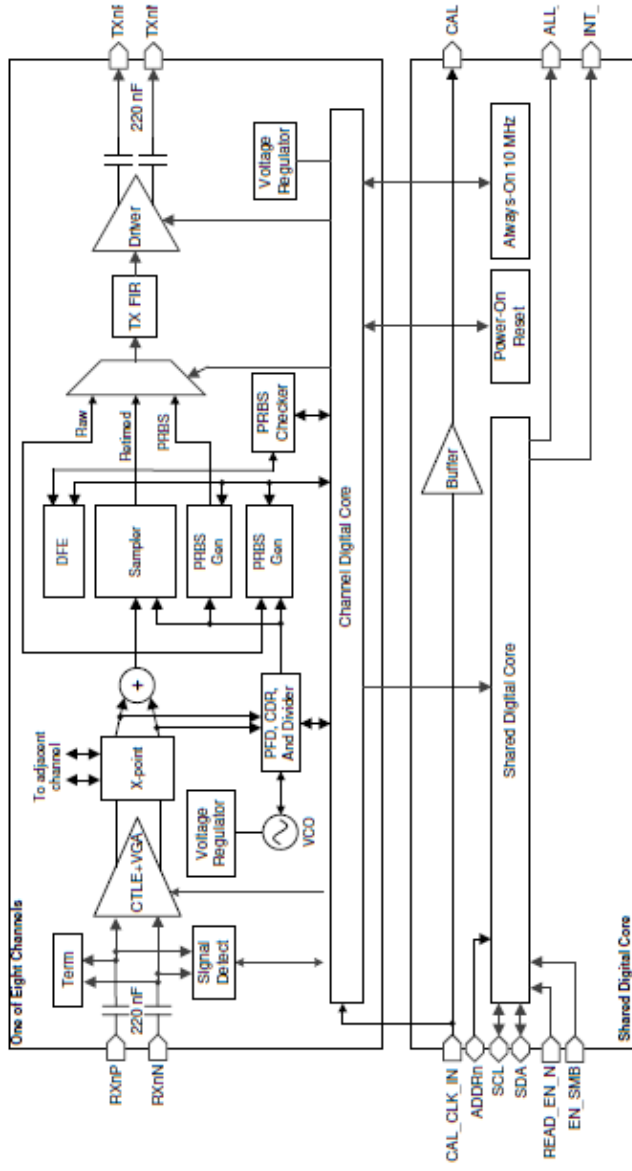
(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Backplane/Mid-plane Application Schematic

<p>Claim 15</p>	<p>DS250DF810, 79.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 15

9.2 Functional Block Diagram



DS250DF810, 17.

Exhibit A-7

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Claim 15

9.3.10 Differential Driver with FIR Filter

The DS250DF810 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. $C[0]$ can take on values in the range [-31, +31]. $C[-1]$ and $C[+1]$ can take on values in the range [-15, 15].

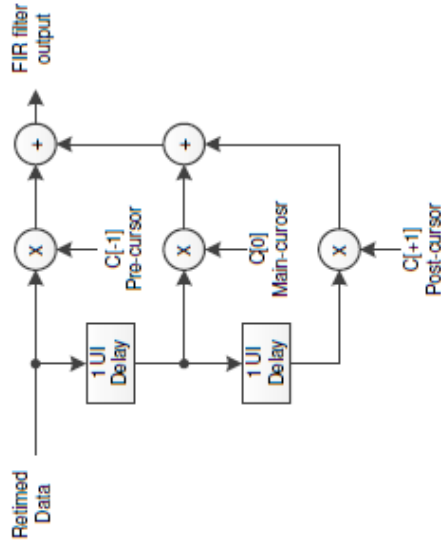


Figure 7. FIR Filter Functional Model

When utilizing the FIR filter, it is important to abide by the following general rules:

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- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform in order to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

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- $Rpre_{dB} = 20 * \log_{10} (V_3/V_2)$
- $Rpst_{dB} = 20 * \log_{10} (V_1/V_2)$

Exhibit A-7

<p>Claim 15</p>	<p>DS250DF810, 20.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>15[c] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.</p>	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>

Exhibit A-7

Claim 15

9.3.11 Setting the Output V_{oo}

The output differential voltage (V_{oo}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSORS: REG_0x3E[6:0]	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Exhibit A-7

Claim 15

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 15

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

Claim 15	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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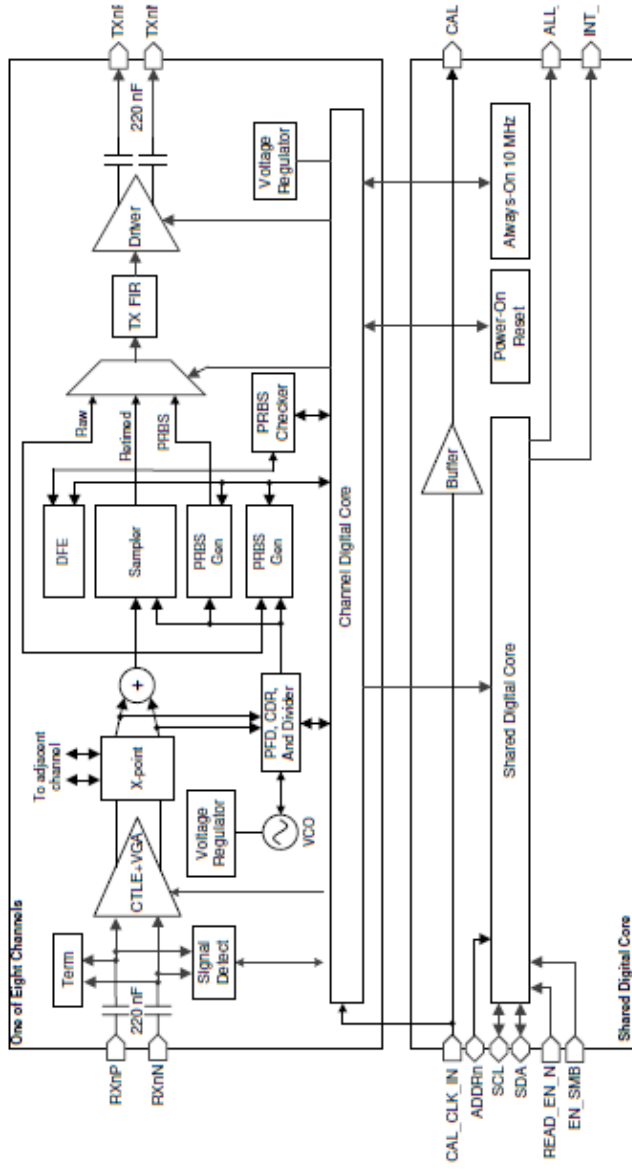
P. DEPENDENT CLAIM 16

Claim 16	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>
<p>16. The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively, each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.</p>	

<p>Claim 16</p>	<p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 16

9.2 Functional Block Diagram



DS250DF810, 17.

Claim 16	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 16</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Exhibit A-7

Claim 16

9.3.11 Setting the Output V_{oo}

The output differential voltage (V_{oo}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSORS: REG_0x3E[6:0]	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 16

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

Claim 16	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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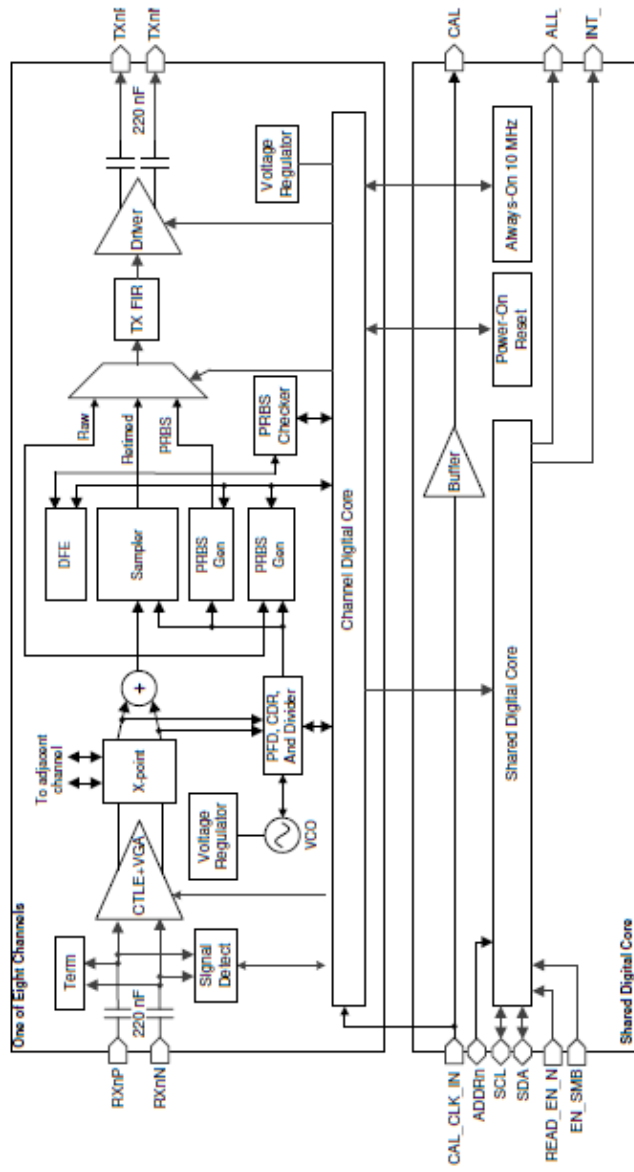
Q. DEPENDENT CLAIM 17

Claim 17	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>
<p>17. The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.</p>	

<p>Claim 17</p>	<p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 17

9.2 Functional Block Diagram



DS250DF810, 17.

<p>Claim 17</p>	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 17</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Exhibit A-7

Claim 17

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSORS: REG_0x3E[6:0]	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 17

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

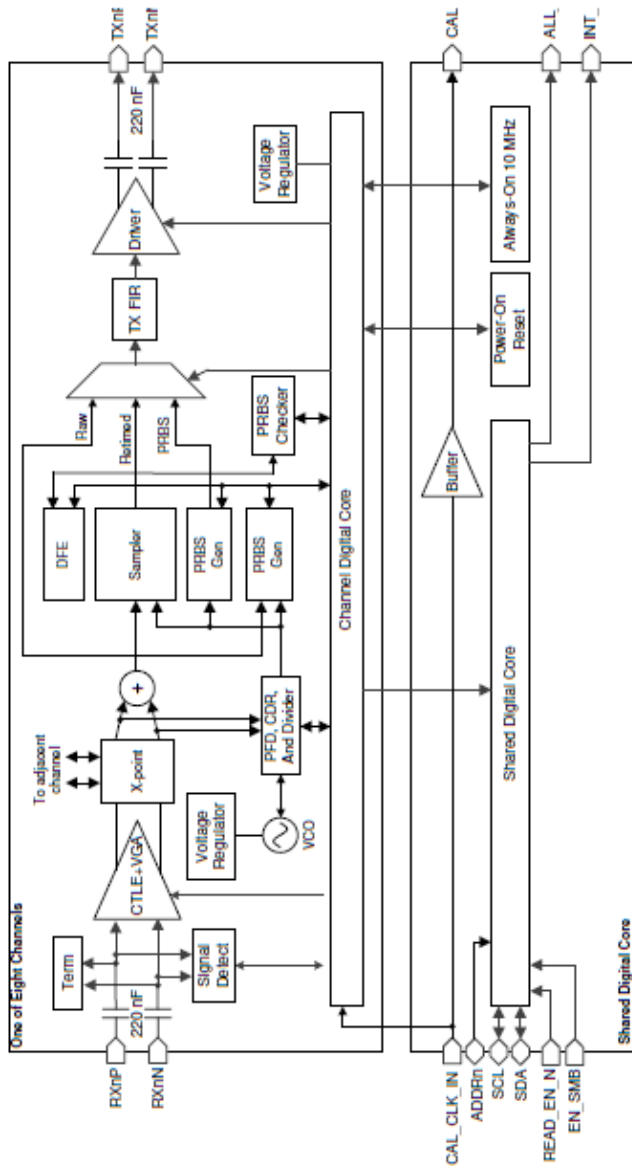
Claim 17	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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R. DEPENDENT CLAIM 18

Claim 18	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>
<p>18. The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.</p>	

<p>Claim 18</p>	<p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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9.2 Functional Block Diagram



DS250DF810, 17.

<p>Claim 18</p>	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 18</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Claim 18

9.3.11 Setting the Output V_{OO}

The output differential voltage (V_{OO}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSORS: REG_0x3E[6:0]	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 18

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

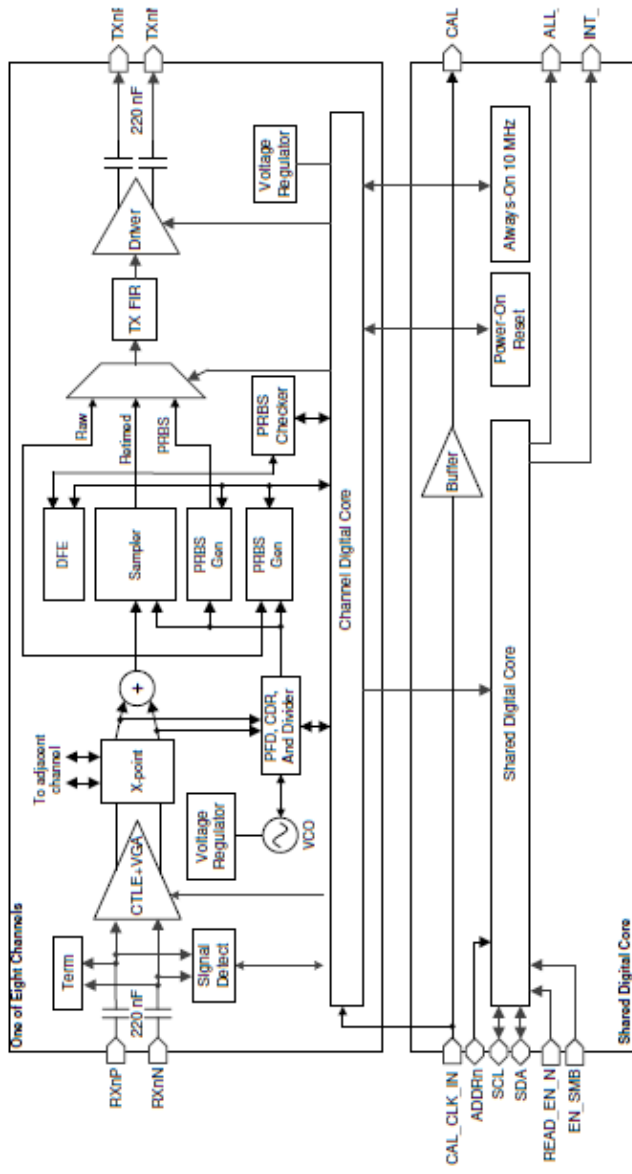
<p>Claim 18</p>	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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S. DEPENDENT CLAIM 19

<p>Claim 19</p> <p>19. The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.</p>	<p>DS250DF810 discloses and/or renders obvious this limitation.</p> <p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 19

9.2 Functional Block Diagram



DS250DF810, 17.

<p>Claim 19</p>	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 19</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Claim 19

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	0	0	0	0.205	NA	NA
0	+1	0	0	0.280	NA	NA
0	+2	0	0	0.305	NA	NA
0	+3	0	0	0.355	NA	NA
0	+4	0	0	0.385	NA	NA
0	+5	0	0	0.440	NA	NA
0	+6	0	0	0.490	NA	NA
0	+7	0	0	0.525	NA	NA
0	+8	0	0	0.565	NA	NA
0	+9	0	0	0.610	NA	NA
0	+10	0	0	0.650	NA	NA
0	+11	0	0	0.685	NA	NA
0	+12	0	0	0.720	NA	NA
0	+13	0	0	0.760	NA	NA
0	+14	0	0	0.790	NA	NA
0	+15	0	0	0.825	NA	NA
0	+16	0	0	0.860	NA	NA
0	+17	0	0	0.890	NA	NA
0	+18	0	0	0.925	NA	NA
0	+19	0	0	0.960	NA	NA
0	+20	0	0	0.985	NA	NA
0	+21	0	0	1.010	NA	NA
0	+22	0	0	1.040	NA	NA
0	+23	0	0	1.075	NA	NA
0	+24	0	0	1.095	NA	NA
0	+25	0	0	1.125	NA	NA
0	+26	0	0	1.150	NA	NA
0	+27	0	0	1.165	NA	NA
0	+28	0	0	1.190	NA	NA
0	+29	0	0	1.205	NA	NA
0	+30	0	0	1.220	NA	NA
0	+31	0	0	1.225	NA	NA
0	+18	-1	-1	0.980	NA	2.1
0	+17	-2	-2	0.960	NA	2.5
0	+16	-3	-3	0.960	NA	3.1
0	+15	-4	-4	0.960	NA	3.8
0	+14	-5	-5	0.960	NA	4.7

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 19

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1	0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude		
0	0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude		

Table 13. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Exhibit A-7

Claim 19	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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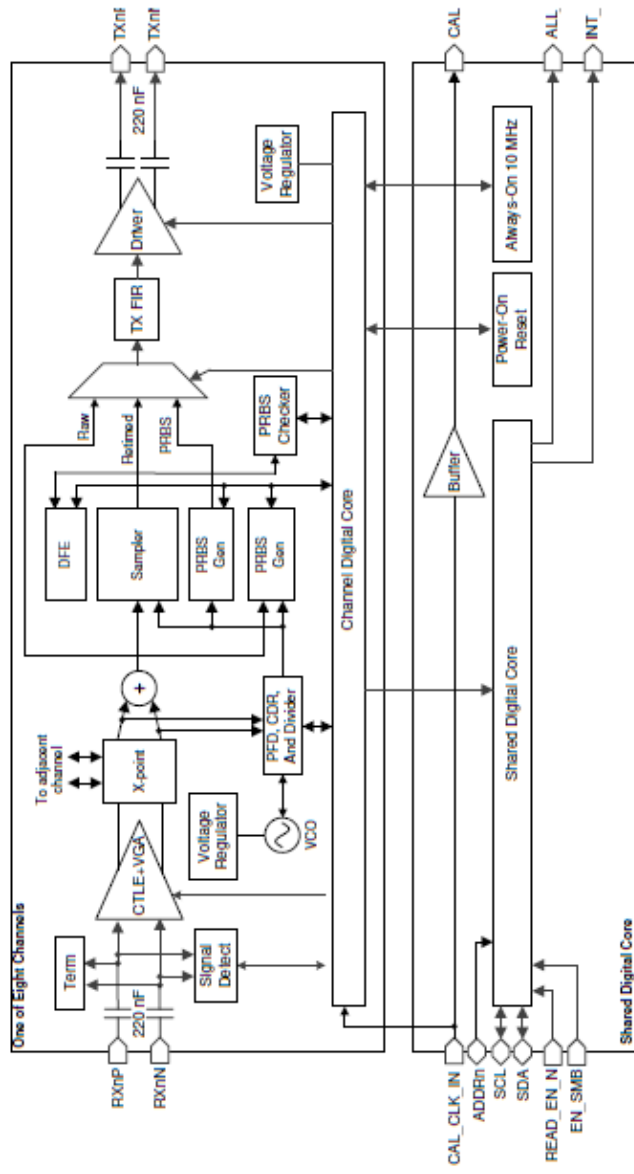
T. DEPENDENT CLAIM 2

Claim 20	<p>DS250DF810 discloses and/or renders obvious this limitation.</p>
<p>20. The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.</p>	

<p>Claim 20</p>	<p>9.1 Overview</p> <p>The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF810 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF810.</p> <p>All transmit and receive channels on the DS250DF810 are AC-coupled with physical AC-coupling capacitors (220 nF +/- 20%) on the package substrate. This ensures common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF810 is configurable through a single SMBus port. The DS250DF810 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF810 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF810. For more information about how to program or operate these features, consult the DS250DF810 Programming Guide.</p> <p>DS250DF810, 16.</p>
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Claim 20

9.2 Functional Block Diagram



DS250DF810, 17.

<p>Claim 20</p>	<p>9.5 Programming</p> <p>9.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing <p>9.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF810 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.
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<p>Claim 20</p>	<p>Programming (continued)</p> <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF1810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFF[5:4] is used to select the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).</p> <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF810.</p> <p>DS250DF810, 30-31.</p>
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Claim 20

9.3.11 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre/post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{op} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Table 2. Typical VOD and FIR Values

FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSORS: REG_0x3E[6:0]	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.280	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.385	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.980	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		POST-CURSORS: REG_0x3F[6:0]	Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]					
0	+13	-6		0.960	NA	5.8
0	+12	-7		0.960	NA	7.2
0	+11	-8		0.960	NA	9.0
0	+10	-9		0.960	NA	11.6
-1	18	0		0.960	1.0	NA
-2	17	0		0.960	1.6	NA
-3	16	0		0.960	2.4	NA
-4	15	0		0.960	3.3	NA
0	26	-1		1.165	NA	1.1
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF810 receiver.

DS250DF810, 22-23.

Exhibit A-7

Claim 20							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	Main-cursor magnitude	
	2	0	RW	Y	FIR_C0[2]	Main-cursor magnitude	
	1	1	RW	Y	FIR_C0[1]	Main-cursor magnitude	
	0	0	RW	Y	FIR_C0[0]	Main-cursor magnitude	
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
		2	0	RW	Y	FIR_CN1[2]	Pre-cursor magnitude
1		0	RW	Y	FIR_CN1[1]	Pre-cursor magnitude	
0		0	RW	Y	FIR_CN1[0]	Pre-cursor magnitude	

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	Post-cursor magnitude
	1	0	RW	Y	FIR_CP1[1]	Post-cursor magnitude
	0	0	RW	Y	FIR_CP1[0]	Post-cursor magnitude

Table 13. Channel Registers, 3A to A9 (continued)

Exhibit A-7

<p>Claim 20</p>	<p>DS250DF810, 54-55.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF810, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF810 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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