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Paper No. ___

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AMPHENOL CORPORATION,
Petitioner,

v.

CREDO TECHNOLOGY GROUP LTD
Patent Owner.

Case No. IPR2025-00835
Patent No. 10,877,233

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq**

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EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent No. 10,877,233 (“the ’233 Patent”)
1002	Prosecution History of U.S. Patent No. 10,877,233
1003	Declaration of Paul S. Min, Ph.D. (“Min”)
1004	Curriculum Vitae of Paul S. Min, Ph.D.
1005	U.S. Patent No. 9,882,706 (“Lugthart-706”)
1006	U.S. Patent No. 7,233,617 (“Gorecki-617”)
1007	IEEE Std. 802.3-2015, Section 1 (“802.3-2015, Section 1”)
1008	IEEE Std. 802.3-2015, Section 2 (“802.3-2015, Section 2”)
1009	IEEE Std. 802.3-2015, Section 3 (“802.3-2015, Section 3”)
1010	IEEE Std. 802.3-2015, Section 4 (“802.3-2015, Section 4”)
1011	IEEE Std. 802.3-2015, Section 5 (“802.3-2015, Section 5”)
1012	IEEE Std. 802.3-2015, Section 6 (“802.3-2015, Section 6”)
1013	U.S. Patent No. 9,172,578 (“Dabiri”)
1014	U.S. Patent No. 6,975,140 (“Hsu-140”)
1015	U.S. Patent No. 8,990,654 (“Bliss”)
1016	U.S. Pub. No. 2013/0195155 (“Pan”)
1017	U.S. Patent No. 9,806,812 (“Schmidt”)
1018	U.S. Patent No. 9,137,063 (“Zerbe-063”)
1019	U.S. Patent No. 9,152,257 (“McCall”)
1020	U.S. Pub. No. 2014/0119425 (“Boccaccio”)
1021	<i>Intentionally left blank</i>
1022	SFP-DD MSA, “SFP-DD Hardware Specification for SFP Double Density 2X Pluggable Transceiver,” SFP-DD Rev 3.0 (April 10, 2019) (“SFP-DD-3.0”)
1023	SFF-8436 Specification for QSFP+ 4X 10 Gb/s Pluggable Transceiver, Rev. 4.9 (Aug. 31, 2018)

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1024	U.S. Patent No. 9,178,542 (“Shimanouchi”)
1025	U.S. Pub. No. 2005/0078758 (“Aziz”)
1026	U.S. Patent No. 7,570,708 (“Laturell”)
1027	Pavan Kumar Hanumolu, et al., “Equalizers for High-Speed Serial Links.” <i>International Journal of High Speed Electronics and Systems</i> , vol. 15, no. 2, 2005, pp. 429-458 (“Hanumolu”)
1028	U.S. Pub. No. 2014/0281068 (“Das Sharma”)
1029	’233 Patent Claim Limitation Comparison Chart
1030	Affidavit of Tanya Zeif including Exhibit B, DS125DF1610 9.8 to 12.5 Gbps 16-Channel Retimer Datasheet, SNLS482B, Texas Instruments Incorporated (January 2017) (“TI-Retimer”)
1031	U.S. Pub. No. 2014/0075076 (“Pillai”)
1032	U.S. Patent No. 8,000,176 (“Bakx”)
1033	Section 337 Statistics: Average Length of Investigations, available at https://www.usitc.gov/intellectual_property/337_statistics_average_length_investigations.htm (visited March 21, 2025).
1034	Federal Court Management Statistic-Profiles for the Eastern District of Texas, available at https://www.uscourts.gov/data-news/reports/statistical-reports/federal-court-management-statistics/federal-court-management-statistics-december-2024 (visited March 21, 2025).
1035	<i>In re Certain Active Electrical Cables and Components Thereof</i> , Inv. No. 337-TA-3814, Complaint (Mar. 13, 2025).
1036	<i>In re Certain Active Electrical Cables and Components Thereof</i> , Inv. No. 337-TA-3814, Amended Complaint (Mar. 18, 2025).
1037	<i>In re Certain Active Electrical Cables and Components Thereof</i> , Inv. No. 337-TA-3814, Amended Exhibit 34 to Amended Complaint (Mar. 18, 2025).
1038	Dkt. 1, Complaint, <i>Credo Semiconductor Inc. et al. v. Amphenol Corp.</i> , No. 2:25-cv-00296 (E.D. Tex. Mar. 13, 2025)

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1039	Dkt. 1-4, Exh. 4 To Complaint, <i>Credo Semiconductor Inc. et al. v. Amphenol Corp.</i> , No. 2:25-cv-00296 (E.D. Tex. Mar. 13, 2025)
1040	Dkt. 1, Complaint, <i>Credo Semiconductor Inc. et al. v. Molex, Inc.</i> , No. 1:25-cv-00316 (D. Del. Mar. 13, 2025)
1041	Dkt. 1, Complaint, <i>Credo Semiconductor Inc. et al. v. TE Connectivity PLC</i> , No. 2:25-cv-00297 (E.D. Tex. Mar. 13, 2025)
1042	Dkt. 1, Complaint, <i>Credo Semiconductor Inc. et al. v. Volex PLC</i> , No. 2:25-cv-00298 (E.D. Tex. Mar. 13, 2025)
1043	Boalick, Chief APJ, “Guidance on USPTO’s rescission of ‘Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation’” (Mar. 24, 2025)
1044	U.S. Patent No. 5,452,333 (“Guo”)
1045	U.S. Patent No. 7,762,727 (“Aronson”)
1046	Proakis, John G., <i>Digital Communication</i> . McGraw-Hill, 4th Edition, 2000, pp. 583-635 (“Proakis”)
1047	U.S. Pub. No. 2005/0013317 (“Lindsay”)
1048	Liu, Jin and Xiaofeng Lin, “Equalization in high-speed communication systems.” <i>IEEE Circuits and Systems Magazine</i> , vol. 4, no. 2, 2004, pp. 4-17 (“Liu”)
1049	Hsieh, Ming-ta and Gerald E. Sobelman, “Architectures for multi-gigabit wire-linked clock and data recovery.” <i>IEEE Circuits and Systems Magazine</i> , vol. 8, no. 4, 2008, pp. 45-57 (“Hsieh”)
1050	U.S. Patent No. 8,787,430 (“Raghavan”)
1051	U.S. Pub. No. 2015/0106536 (“Lauby”)

MANDATORY NOTICES

A. Real Party-In-Interest

Petitioner Amphenol Corporation is a real party-in-interest to this proceeding under 37 C.F.R. §42.8(b)(1).

B. Related Matters

A decision in this proceeding could affect or be affected by the following. The '233 Patent is currently asserted in actions listed in Section B.2, and infringement of the '233 Patent is alleged in the action in Section B.3.

1. United States Patent and Trademark Office

U.S. Patent No. 10,877,233 (“the '233 Patent”) issued from application ser. no. 16/698,935. It purports to claim priority to Chinese application no. CN201910542576.3, filed on July 1, 2019.

2. United States District Court

a. Eastern District of Texas

Credo Semiconductor Inc. et al. v. Amphenol Corp., No. 2:25-cv-00296 (E.D. Tex.), filed March 13, 2025 (“the Texas Litigation”).

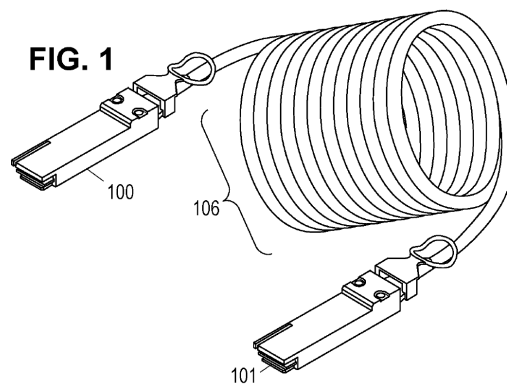
Credo Semiconductor Inc. et al. v. TE Connectivity PLC, No. 2:25-cv-00297 (E.D. Tex.), filed March 13, 2025 (“the TE Connectivity Litigation”).

Credo Semiconductor Inc. et al. v. Volex PLC, No. 2:25-cv-00298 (E.D. Tex.), filed March 13, 2025 (“the Volex Litigation”).

Petitioner Amphenol Corporation (“Petitioner”) requests *inter partes* review and cancellation of claims 1-20 (“Challenged Claims”) of U.S. Patent No. 10,877,233 (EX1001, “the ’233 Patent”).

I. INTRODUCTION

The ’233 Patent concerns active electrical cables. Active electrical cables provide high speed data communication—such as between servers and routers in data centers. The cables have standardized pluggable modules at each end and support standardized Ethernet communications. Figure 1 is exemplary.



The pluggable modules contain electronics, including a transceiver, providing signal conditioning that improves high speed data communication. The signal conditioning includes pre-equalization. Pre-equalization is a process wherein a transmit filter pre-distorts a signal to compensate for distortion that a communication channel—such as an electrical cable—is expected to impart during transmission, so that a digital signal recovered from the received signal closely approximates the transmitted digital signal. Setting the filter coefficient values

controls the filter behavior, and in this way also controls the pre-equalization settings. This was all well-known. The Ethernet standard describes controlling pre-equalization by setting transmit filter coefficients.

The '233 Patent claims recite a cable (and a manufacturing method and communication method) using these well-known components in well-known ways. The specification extensively quotes the Ethernet standard as specifying functionality that the cable provides. The Office, however, allowed claims in a first action. The Office wrongly determined that the prior art failed to describe a transceiver using filter coefficient values that were stored in non-volatile memory—a limitation that appears in every claim, and a functionality that was widely known and practiced in the art.

The Chinese Patent Office however, did identify prior art showing the claimed use of non-volatile memory in an active cable and rejected all claims in the Chinese priority application, which Patent Owner abandoned.

Lugthart-706 is a prior art patent describing active electrical cables, and their electronics, in great detail. Gorecki-617 is a prior art patent describing components and methods for setting transmit filter coefficients for equalization—including pre-equalization—using values stored in non-volatile memory. The Office never considered either reference. **Ground 1** shows that Lugthart-706 in view of Gorecki-617 (“Lugthart+Gorecki”) renders each independent claim—and

fourteen dependent claims—obvious. **Ground 2** shows that Lugthart+Gorecki, further in view of the Ethernet standard (e.g., IEEE Std. 802.3-2015), renders the remaining three dependent claims obvious.

On March 13, 2025, Patent Owner filed a complaint with the ITC alleging that Petitioner and three other industry participants infringe the '233 Patent. This Petition is filed *before* a Section 337 Investigation has been instituted. As explained below the Board would likely issue FWD before any final determination in the ITC. That makes the Board the best forum to resolve the patentability of the Challenged Claims—claims that are now threatening the active electrical cable industry, that should never have issued, and that recite well-known functionality, in a patent whose foreign priority application the Chinese Patent Office squarely rejected.

The Petition demonstrates a reasonable likelihood that at least one Challenged Claim is unpatentable. Accordingly, Petitioner requests that the Board institute IPR and cancel the Challenged Claims.

II. STANDING CERTIFICATION

The '233 Patent is available for IPR. Petitioner is neither barred nor estopped from requesting IPR of the '233 Patent. 37 C.F.R. §42.104(a).

III. UNPATENTABILITY GROUNDS

The Challenged Claims are unpatentable under post-AIA §103 as follows:

Ground	References	Claims
1	Lugthart-706, Gorecki-617	1-6, 8-13, 15-19
2	Lugthart-706, Gorecki-617, IEEE Std. 802.3-2015	7, 14, 20

Post-AIA law applies because the '233 Patent's earliest possible effective-filing date is after March 16, 2013. The '233 Patent issued from an application filed November 27, 2019 (EX1001, code (22)) and purports to claim priority to a Chinese application filed July 1, 2019 (EX1002, 75-76). All references are prior art to each Challenged Claim under post-AIA §102(a) even assuming a July 2019 effective filing-date.

Reference	Published	Priority	Filing
Lugthart-706 (EX1005)	2018-01-30	2013-12-27	2016-12-28
Gorecki-617 (EX1006)	2007-06-19	2002-10-11	2003-04-10
IEEE Std. 802.3-2015 (EX1007-EX1012)	2016-03-04 ¹		

¹ See <https://ieeexplore.ieee.org/servlet/opac?punumber=7428774>.

IV. THE '233 PATENT²

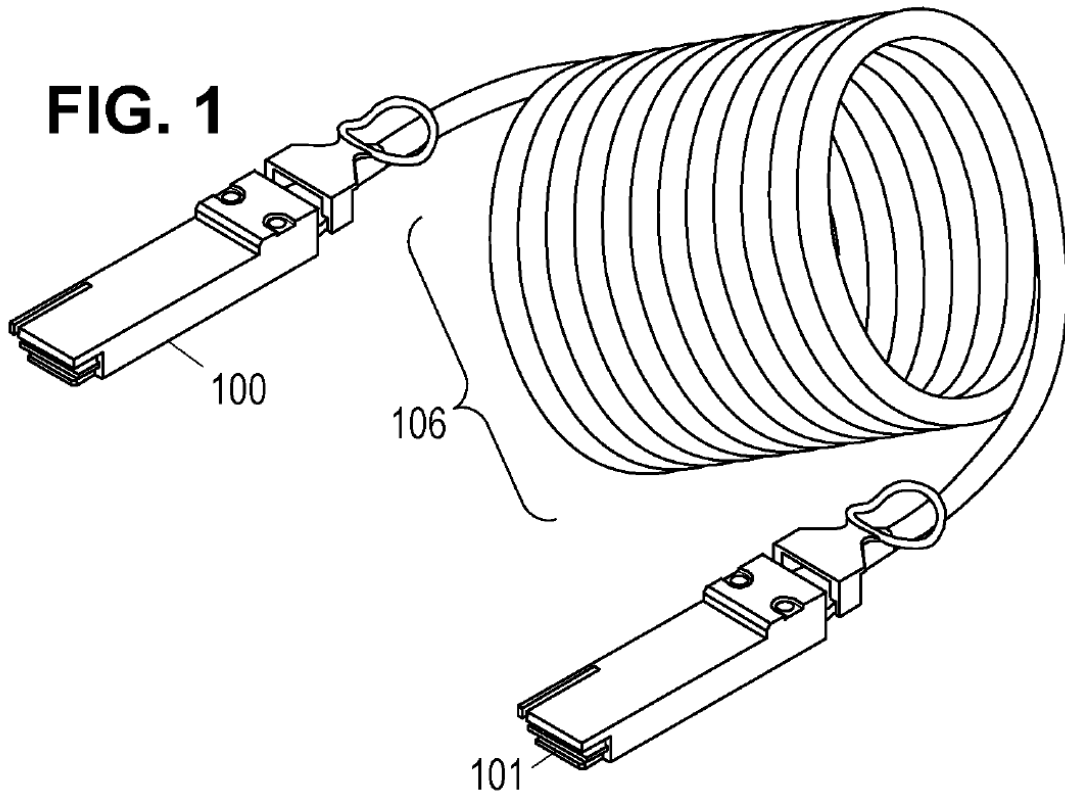
A. Background

The '233 Patent describes an active electrical cable (which it calls an “active Ethernet cable” or “AEC”), a cable manufacturing method, and a communications method using a cable, employing preset transmit-side equalization (e.g., pre-equalization or pre-emphasis). EX1001, Abstract, code (54), 1:32-36, 3:8-9. Pre-equalization was a well-known technique wherein a transmit filter modifies a signal in a way that compensates for the signal distortion that occurs during transmission on a communication path—over a cable, over a backplane—so that on receipt the recovered digital signal closely approximates the digital signal transmitted. EX1003, Declaration of Paul S. Min (“Min”), ¶59. The transmit filter behavior is controlled by setting filter coefficients or “taps.” EX1001, 5:39-48, 9:11-12, 10:40-44; Min, ¶59. The '233 Patent describes storing filter coefficients in non-volatile memory, and setting transmit filter coefficients using those stored values. EX1001, 5:3-5, 5:27-35, 11:3-6; Min, ¶59.

The cable has an industry-standard SFP or QSFP connector at each end, wherein the connector comprises a transceiver that the '233 Patent calls a “data

² Unbolded italics indicate claim language, while all other emphasis in the petition is added unless otherwise indicated.

recovery and re-modulation (DRR) device.” EX1001, Abstract, Fig. 1 (below), 3:49-55 (“[E]ach connector 100, 101 may include a powered transceiver that performs clock and data recovery (CDR) and re-modulation of data streams, hereafter called a data recovery and re-modulation (DRR) device.”), 9:19-22, 10:5-9; Min, ¶60.



Each connector, a pluggable module, mates with a receiving port in a host device, and the AEC provides a communication link between the host devices coupled to each AEC connector according to protocols that “can be found in the current Ethernet standard” and whose implementation details were “well within” the POSA’s ordinary skill. EX1001, 7:14-34. “[T]he transceivers perform CDR

and re-modulation not only of the inbound data streams to the host interface as they exit the cable, but also of the outbound data streams from the host interface entering the cable.” EX1001, 3:55-60. Clock and data recovery (e.g., CDR) was a known process for recovering a data signal from a received signal. Min, ¶¶61, 87-101.

The '233 Patent describes data streams being communicated in lanes, referring to particular signal paths. The '233 Patent describes re-modulating data streams entering or exiting the DRR device (such as the data streams that the transceiver receives from and transmits to a host device) as met by “format conversion” such as converting “1 lane of PAM4 symbols into 2 lanes of NRZ symbols, and vice versa.” EX1001, 4:43-45; Min, ¶62. PAM-4 and NRZ were known coding schemes used with known standards like Ethernet. EX1015 (“Bliss”), 4:5-13; Min, ¶62. PAM-4 is four-level pulse amplitude modulation, which encodes two bits per symbol. Bliss, 4:5-13; Min, ¶62. NRZ is non-return to zero, which encoded one bit per symbol. EX1016 (“Pan”), ¶4; Min, ¶62. Thus, the '233 Patent describes the known concepts of a transceiver converting two received NRZ data streams into one transmitted PAM-4 data stream, and vice versa. EX1031 (“Pillai”), [0006]; Min, ¶62.

B. Challenged Claims

The '233 Patent has 20 claims. Claims 1, 8, and 15 are independent. Appendix A provides a claim list labeling limitations (e.g., “[1.a]”).

Claim 1 recites an electrical cable connecting a “*data recovery and re-modulation (DRR) device*” at each end. Limitations [1.a]-[1.c]. Each *DRR device* “*exchanges inbound and outbound multi-lane data streams*” with a host device coupled to a respective *DRR device*. Limitations [1.a]-[1.b]. Each *DRR device* “*convert[s]*” between signals received over the cable and the “*multi-lane data streams*” received from and transmitted to the host. Limitations [1.d]-[1.e]. Each *DRR device* pre-equalizes signal transmitted over the cable “*using transmit filter coefficient values stored in nonvolatile memories.*” Limitation [1.f].

Claim 8 recites a manufacturing method for claim 1’s cable, while claim 15 recites a communication method over a cable.

C. Prosecution History

The '233 Patent issued from application no. 16/698,935, filed November 27, 2019. EX1001, code (21), (22). The Examiner allowed all claims in a first action. EX1002, 107. The applicant then requested continued examination (RCE) to consider an Information Disclosure Statement citing Office communications in different cases. EX1002, 134-138. The Examiner thereafter repeated the claim allowance without discussing any art cited in the communications from the

unrelated cases. The Examiner stated in the reasons for allowance that the prior art failed to teach limitations [1.f], [8.f], and [15.c], e.g., *the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories*. EX1002, 154.

D. POSA

On July 1, 2019, a person having ordinary skill in the art (“POSA”) would have had a Bachelor of Science in electrical or computer engineering with at least three years of experience in digital communication system design. Min, ¶¶50-57. A higher level of education may substitute for less experience. Min, ¶53.

V. CLAIM INTERPRETATION

The Board construes claim terms using the civil action standard (35 U.S.C. §282(b)) consistent with the ordinary and customary meaning as understood by a POSA. 37 C.F.R. §42.100(b). The Board need only construe terms to the extent necessary to resolve disputes. *Nidec v. Zhongshan*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); 83 Fed. Reg. 51340, 51353. The Board need not reach an exact outer construction for any term because the prior art meets the claims under any reasonable interpretation.

VI. GROUND 1: LUGTHART+GORECKI RENDERS OBVIOUS CLAIMS 1-6, 8-13, AND 15-19

A. Lugthart-706

Lugthart-706 discloses an “active cable” that “includes... first and second transceiver assemblies 105a, 105b positioned at either end of... conductive lines 111.” Lugthart-706, 14:30-34, Fig. 2A (below); Min, ¶111.

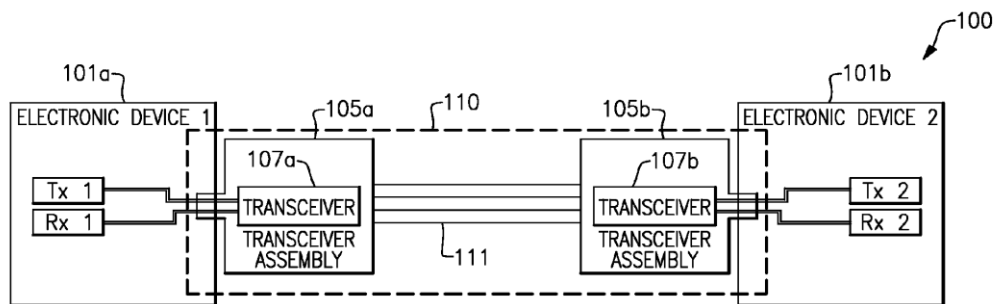
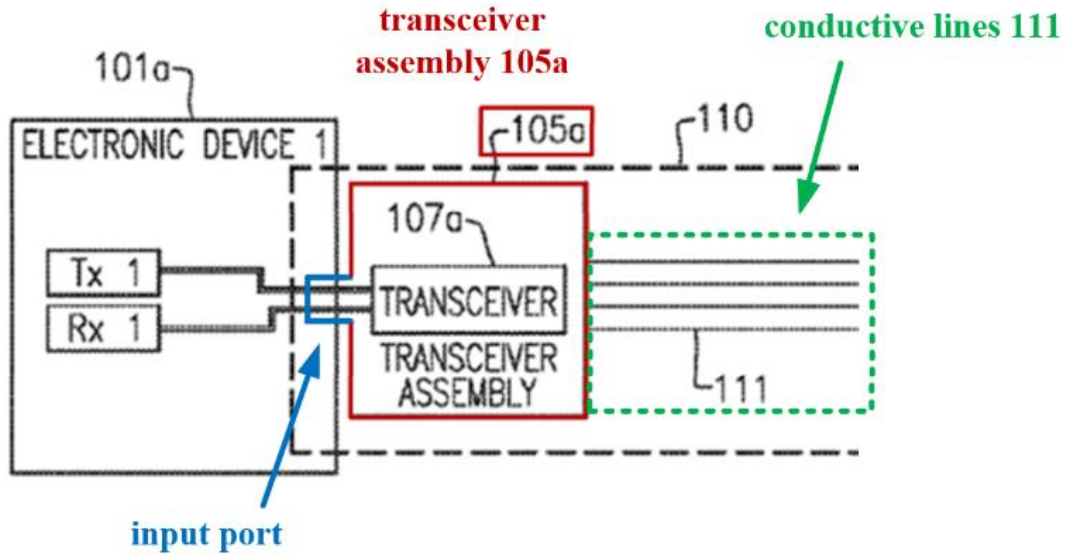


FIG. 2A

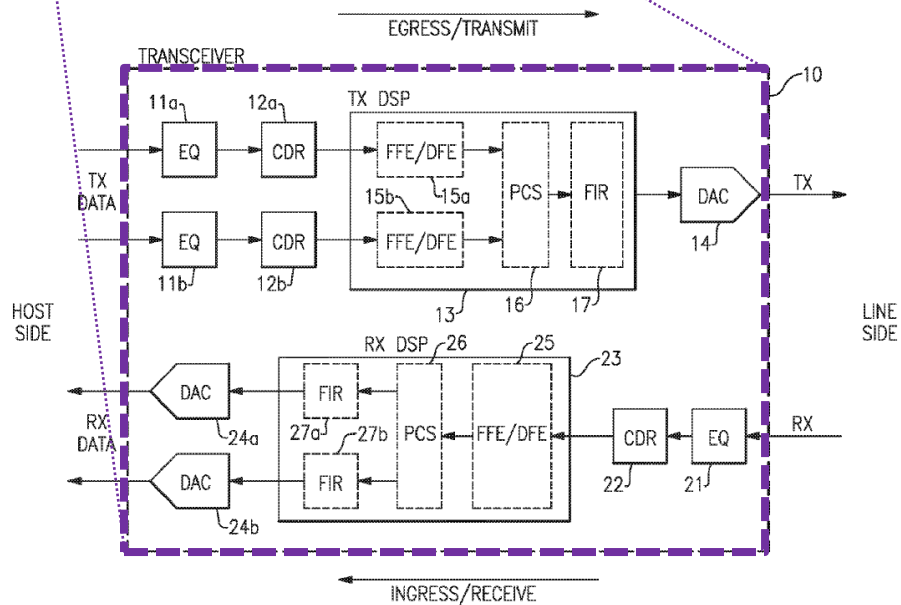
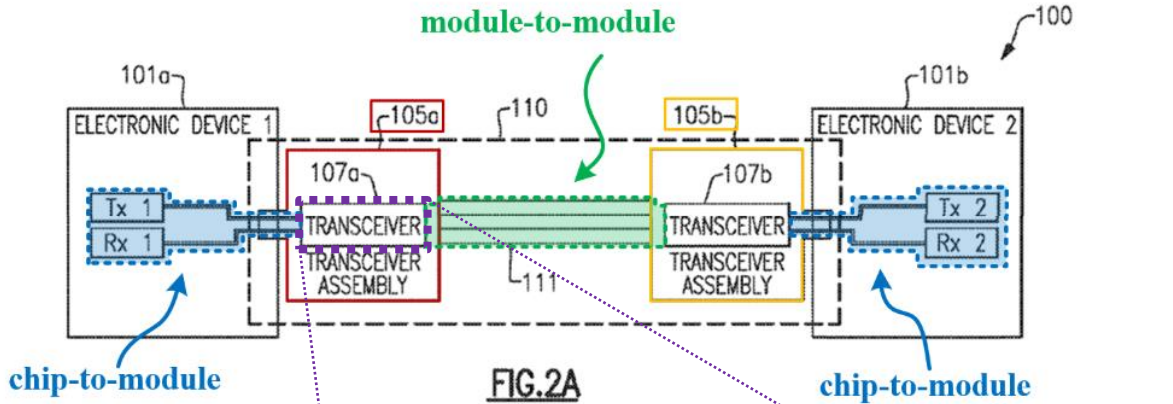
An active cable’s electronic components improve signal quality. Lugthart-706, 14:29-31; Min, ¶¶68-101, 112. The transceiver assemblies 105a, 105b include transceivers 107a, 107b, respectively. Lugthart-706, Fig. 2A, 14:47-53; Min, ¶112. Each transceiver assembly has a “host side” electrically connected to a host (termed an “electronic device”) and a “line side” electrically connected to one end of the cable’s conductive lines 111. Lugthart-706, 14:34-38, Fig. 2A (annotated detail below); Min, ¶112.



Each transceiver assembly’s input port comprises a connector, such as an industry standard SFP or QSFP connector, that “is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b, and an output port that is connected to the cable.” Lugthart-706, 15:42-52, Figs. 2A, 17A, 17B, 18; Min, ¶113.

Lugthart-706’s transceiver 107a/107b can perform pre-equalization (which Lugthart-706 calls pre-emphasis) on signals transmitted over the cable’s conductive lines 111, as well as on signals transmitted to electronic devices 101a/101b. Lugthart-706, 23:62-64, 29:23-28; Min, ¶114.

Figure 1A's transceiver 10 illustrates one embodiment of Figure 2A's pluggable module transceiver 107a/107b. Lugthart-706, 14:47-53; Min, ¶115.



Transceiver 10's "EGRESS/TRANSMIT" path through DSP 13 performs digital signal processing, including retiming, on the multi-lane TX DATA signal before transmitting the TX signal over conductive lines 111. Lugthart-706, Figs. 1A, 2A, 15:64-16:3, 21:35-38; Min, ¶116. Finite impulse response (FIR) filter 17

is a transmit filter that performs pre-emphasis on the re-timed TX signal transmitted over conductive lines 111. Lugthart-706, 16:11-15, 29:23-28; Min, ¶116.

Lugthart-706 configures FIR filters using “tap coefficients,” and the filters “perform emphasis on the signal to compensate for channel losses.” Lugthart-706, 22:13-16, 23:59-64; Min, ¶117. “Pre-emphasis” and “pre-equalization” were used interchangeably in the art. Min, ¶117; EX1050 (“Raghavan”), 2:39-41 (describing a “technique for combating ISI [inter-symbol interference]... known as ‘pre-emphasis’, or pre-equalization”); EX1017 (“Schmidt”), 7:54-55; EX1018 (“Zerbe-063”), 3:24-27; EX1019 (“McCall”), 5:4-8. The pre-equalization compensates for anticipated channel distortion on a transmitted signal. Min, ¶¶86, 117.

On the “INGRESS/RECEIVE” path, DSP 23 performs digital signal processing on signal RX received from the cable before that signal is transmitted to the host (electronic device 101a/101b in Figure 2A). Lugthart-706, 8:26-32, 9:38-51, Fig. 1A; Min, ¶118. DSP 23 includes FIR filters 27a/27b. Lugthart-706, 9:38-46. DSP 23 uses these FIR filters for “adaptive and configurable signal conditioning features such as... output pre-emphasis” on the signal transmitted to the host. Lugthart-706, 9:52-55, 29:23-28; Min, ¶118. In one embodiment, Lugthart-706 describes a five-tap FIR 17 and 27a/27b. Lugthart-706, 22:12-16; Min, ¶118.

B. Gorecki-617

Gorecki-617 describes systems and methods for transmitter equalization (e.g., “pre-emphasis equalization” or pre-equalization) by FIR transmit filters in high-speed digital communication systems, including cables. Gorecki-617, Abstract, 1:15-17, 1:59-2:11, 19:61-66; Min, ¶119. Gorecki-617 explains that it was known to digitally equalize data, thus implementing FIR filters in digital signal processing, before converting the equalized signals to analog. Gorecki-617, 16:40-46; Min, ¶119.

Gorecki-617 describes storing FIR filter tap coefficients in non-volatile memory (“NVM”) including writable NVM (e.g., “ROM, PROM, EPROM, EEPROM or the like”). Gorecki-617, 7:18-43, 10:37-51, 17:41-51. EEPROM is electrically erasable programmable read only memory that is rewritable. Min, ¶120. Flash memory was another well-known rewritable non-volatile memory (e.g., “EEPROM or the like”) conventionally used with transmit FIR filters. E.g., *Id.*; Hsu-140, 3:42-4:2 (“Any type of NVRAM can be used as the rewritable non-volatile storage, so long as [it] is of the type suitable for integration on an integrated circuit.”).

Gorecki’s filter taps are programmable. Gorecki-617, 3:42-45; Min, ¶121. “In this way, the transmitter may access the memory to retrieve the necessary information during start-up/power-up, initialization or re-initialization.” Gorecki-

617, 7:31-33. Gorecki describes a “controller” that adjusts equalizer tap coefficients by distributing filter coefficient values from its non-volatile memory to a transmitter to implement FIR filter taps “within the equalization circuitry.” Gorecki-617, 7:9-17; Min, ¶121.

Gorecki-617 also explains the filter coefficients stored in its non-volatile memory can be “re-programmed.” Gorecki-617, 7:18-26, 20:41-43 (claim 2, “pre-programmed [tap] coefficient... is... re-programmed”); Min, ¶122. The filter coefficients can also be “fine-tuned” using adaptive algorithms. Gorecki-617, 7:50-61, 10:26-51; Min, ¶122.

C. Lugthart+Gorecki

1. Reasons to Combine

While Lugthart-706 describes multi-tap transmit filters (FIR 17), it does not explain how to set the transmit filter coefficients and thus leaves the implementation details to the POSA. E.g., Lugthart-706, Fig. 2A, 22:12-16 (describing five-tap filter); Min, ¶124.

A POSA would have had reasons to configure the transmit filters of Lugthart-706 based on Gorecki-617’s approach of using coefficients stored in non-volatile memory. Min, ¶125. Gorecki-617 is directed to “enhancing the performance of high-speed digital communications through a communications channel.” Gorecki-617, 1:15-17, 6:4-5, 19:61-66. Gorecki-617 explains that “[t]he

extent of equalization introduced by the circuitry, however, may vary between equalization circuitry of each transmitter in the high-speed digital communication system.” Gorecki-617, 8:66-9:2. For each transmitter, “the amount of equalization may be adjusted or controlled by... changing the coefficients of the taps[.]” Gorecki-617, 9:37-40. The equalizers are “configured to introduce compensation that is ideally the inverse of the effects caused by the communications channel.” Gorecki-617, 9:8-10. Gorecki-617 achieves this result by storing and loading equalization parameters, including transmit filter coefficient values, from “ROM, PROM, EPROM, EEPROM or the like” (i.e., *nonvolatile memory*). Gorecki-617, 7:25; Min, ¶125. A POSA, therefore, would have understood that “performance of high-speed digital communications” could be enhanced by *using transmit filter coefficient values stored in nonvolatile memories*. Min, ¶126.

Having a transmitter “access the memory” to retrieve the filter coefficient values and program an equalizer (including setting pre-equalizer filter taps) with those values when Lugthart-706’s transceiver is powered up, initialized, or re-initialized was a conventional and convenient technique for setting filter coefficients while persisting the coefficient values for use as power to the AEC transceiver was cycled. Gorecki-617, 7:18-42; Min, ¶127. A POSA would have understood that the controller that Gorecki-617 describes distributing filter tap coefficients to a transmitter to set taps by user programming would also have been

a conventional way to implement that transmitter's memory access and setting programmable FIR filter taps. Gorecki-617, 7:1-17; EX1014 ("Hsu-140"), 4:25-38, 9:54-62; EX1020 ("Boccaccio," cited by the Chinese Patent Office in rejecting all claims of the priority application), Fig. 6 (micro-controller 68, EEPROM 70), [0049]-[0050] (programmable equalizer 56 includes on-board microcontroller 68 that sets equalizer parameters after power-up using values stored in non-volatile memory 70); Min, ¶128.

Providing Lugthart-706's transceiver with pre-set filter coefficient values in non-volatile memory would have allowed setting the AEC with initial coefficient values determined at manufacture and/or default pre-set coefficient values for various chip-to-module channel models for host devices that could be used with the AEC. Min, ¶129.

The resulting Lugthart+Gorecki combination would have combined familiar elements (Lugthart-706's equalizer and FIR filters with Gorecki's controller, EEPROM or the like, and techniques for programming filter coefficient values from such memory) according to known methods (as demonstrated by Gorecki-617) yielding no more than predictable results. *KSR Int'l v. Teleflex*, 550 U.S. 398, 416 (2007); Min, ¶130. Lugthart+Gorecki would have arranged known elements with each performing the same function it had been known to perform. *KSR*, 550 U.S. at 417; Min, ¶131. A POSA would have recognized that Gorecki's coefficient

storage and filter programming techniques could improve Lugthart-706's equalization circuitry in the same way that they improved Gorecki-617's equalization circuitry. *KSR*, 550 U.S. at 417; Min, ¶131.

2. Reasonable Expectation of Success

A POSA would have had a reasonable expectation of success achieving Lugthart+Gorecki because the combination used known components with known filter programming and non-volatile coefficient value storage techniques that were within the POSA's ordinary skill and conventionally used for pre-equalization. Gorecki-617, 16:40-46 (describing digital pre-equalization); Lugthart-706, 8:33-39, 15:30-52, 22:12-16, 29:6-20; Gorecki, 6:39-67; 7:18-49; Min, ¶132. As Hsu explains, for example, "[f]lash memory is a non-volatile random access memory (NVRAM) suitable for use as the rewriteable non-volatile storage to store updated control information for operating the FIR transmitter. ... Any type of NVRAM can be used as the rewriteable non-volatile storage, so long as such NVRAM is of the type suitable for integration on an integrated circuit chip." Hsu-140, 3:42-4:3; Min, ¶133.

D. Lugthart+Gorecki Renders Obvious Claims 1-6, 8-13, and 15-19

1. Claim 1

a. Preamble

1.PRE	A cable that comprises:
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Lugthart+Gorecki meets [1.PRE] because Lugthart-706 describes “an electrical cable including one or more pairs of differential micro coaxial cables or conductors” to implement a “high-speed communication link between first and second electronic devices.” Lugthart-706, Fig. 2A (cable 110), 6:65-7:20, 14:7-31, 15:42-47; Min, ¶134.

b. Limitations [1.a]/[1.b]

1.a	a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;
1.b	a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and

Lugthart+Gorecki meets [1.a] and [1.b] as shown below. Min, ¶¶135-154.

i. *DRR device*

The '233 Patent defines “a data recovery and re-modulation (DRR) device” as “a powered transceiver that performs clock and data recovery (CDR) and re-

modulation of data streams.” EX1001, 3:51-55; Min, ¶¶135-136. The transceivers of Lugthart-706 have these characteristics and are *DRR devices*. Min, ¶¶136-154.

Lugthart-706 discloses *a first DRR device and a second DRR device* because its active cable includes “a pair of *transceivers* provided at respective ends of the cable.” Lugthart-706, 6:65-67; *id.*, Figs. 1A (transceiver 10), 1B-1C, 2A (annotated below showing transceivers 107a/107b), 8:8-60 (describing transceiver 10); Min, ¶137. These transceivers are *powered*. Lugthart-706, 14:7-53 (“cable 110... includ[es] actively powered componentry for improving performance of the cable 110”); Min, ¶137.

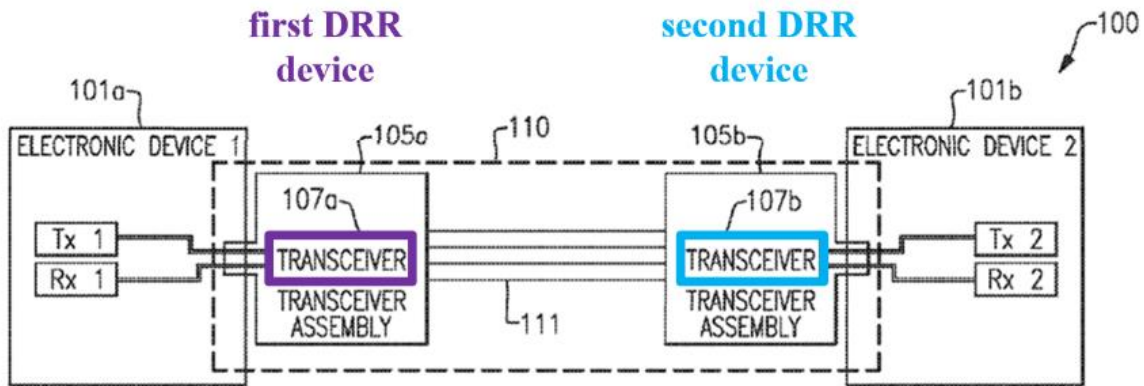


FIG.2A

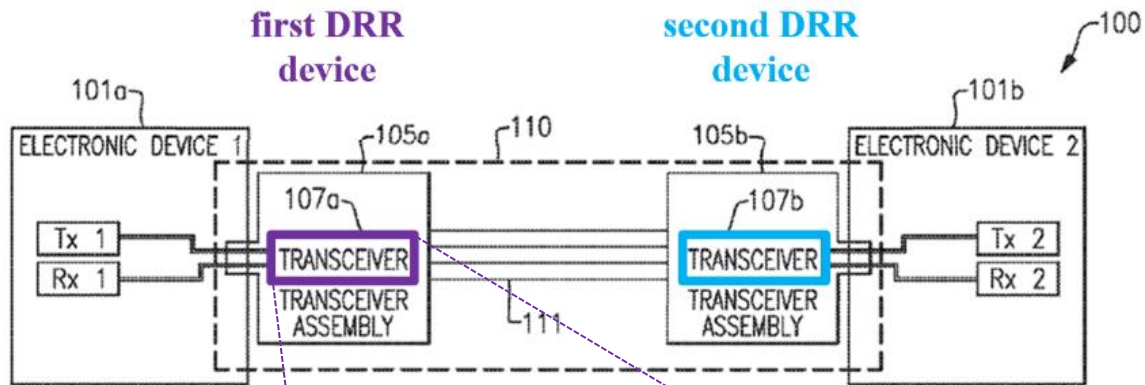


FIG. 2A

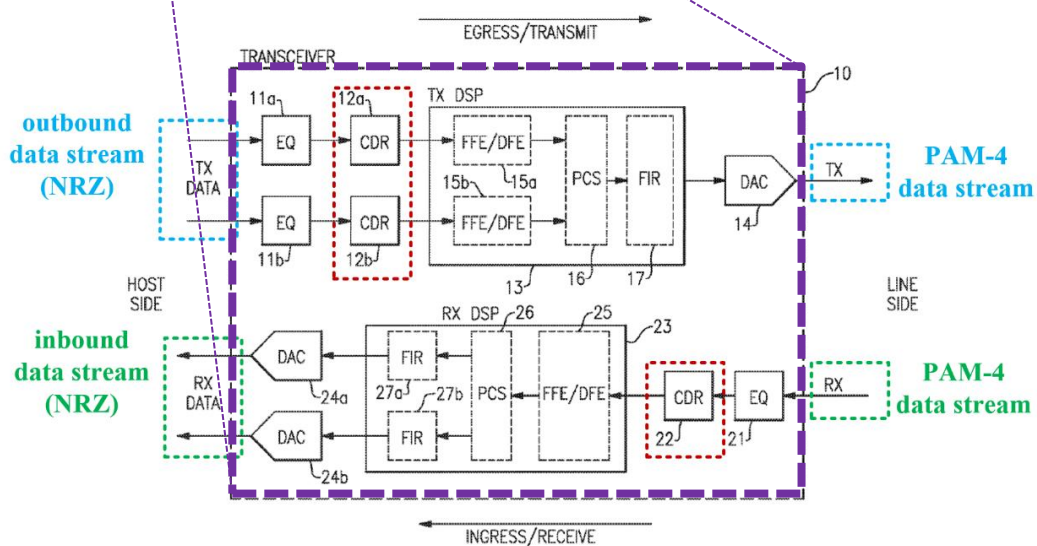


FIG. 1A

Lugthart-706's transceiver 10 is an embodiment of transceivers 107a/107b. Lugthart-706, Fig. 1A (annotated above), 8:8-12; Min, ¶138. CDR 12a/12b and 22 “perform clock and data recovery operations” on respective signals—“TX Data” (*outbound data stream*) from the host (CDR 12a/12b) and “RX” from the line (CDR 22). Lugthart-706, Figs. 1A (above), 2A, 9:26-37, 33:3-8; Min, ¶138.

As explained below transceiver 10 *remodulates* host-side non-return-to-zero (NRZ) “TX Data” (*outbound data stream*) to a four-level pulse amplitude

modulation (PAM-4) “TX” data stream for transmission over the cable, and vice-versa. Lugthart-706, 7:8-22, 8:40-60; 13:25-27; Min, ¶139. Transceivers 107a and 107b are a *first* and *second DRR device*, respectively. Min, ¶139.

ii. *inbound and outbound multi-lane data streams*

The ’233 Patent defines *inbound* and *outbound* from a *host’s* viewpoint, e.g., “*inbound* data streams *to the host interface*” and “*outbound* data streams *from the host interface.*” EX1001, 3:57-60, 4:47-52; Min, ¶140. Like the claims, Lugthart-706 defines data streams and communication paths from the *host’s* perspective. Min, ¶140.

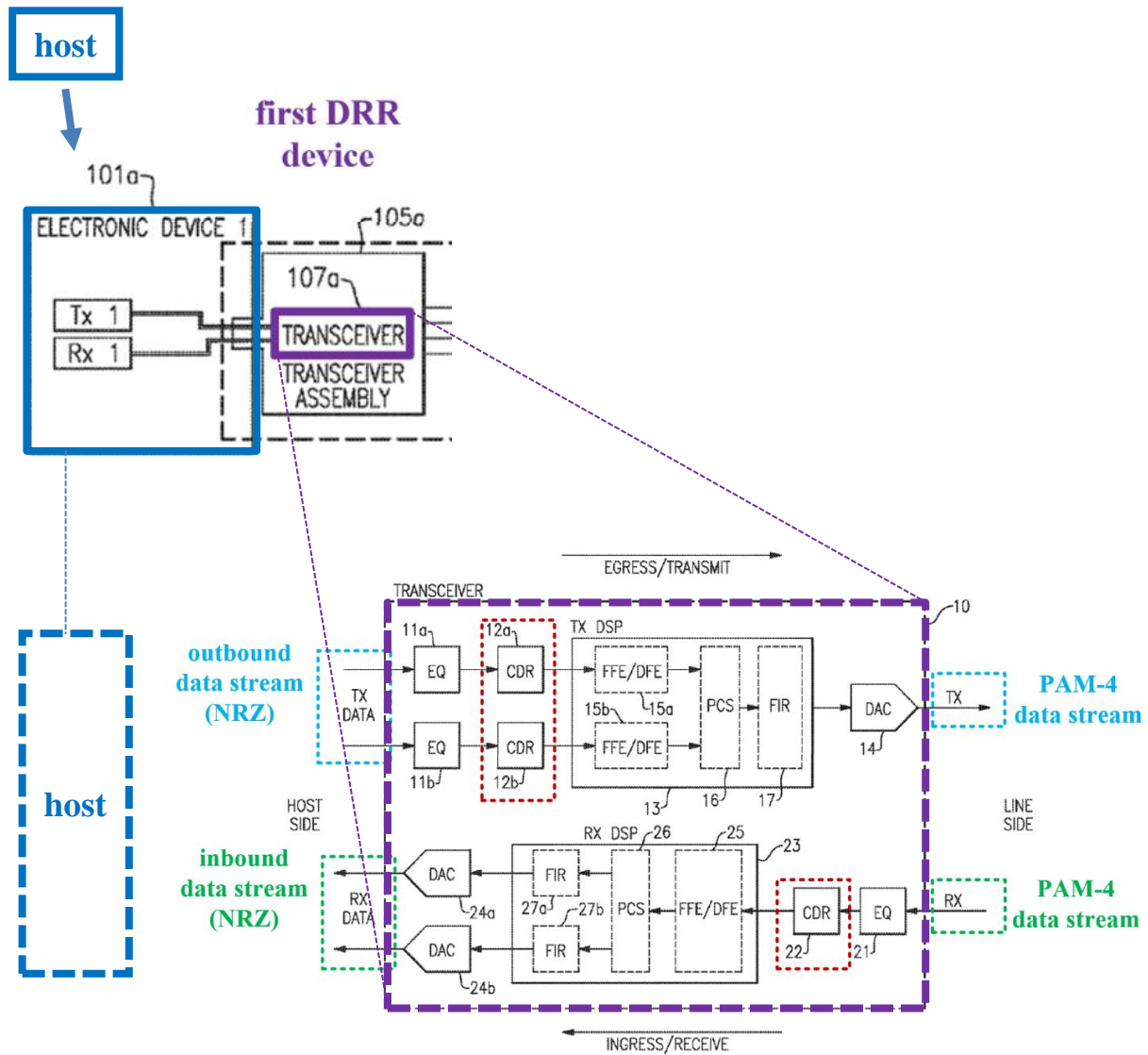


FIG.1A

The RX and TX DATA indicated on the host (left) side of Figure 1A are *inbound* and *outbound data streams*. Min, ¶141.

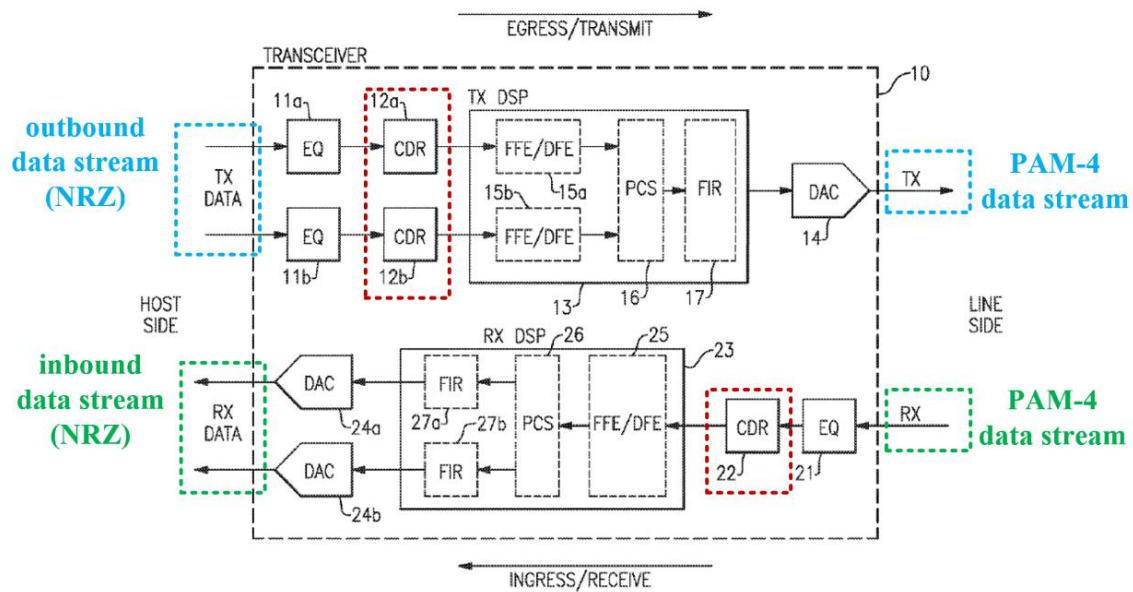


FIG. 1A

A POSA would have understood the multiple arrows for each data stream to represent multiple lanes. Min, ¶142. Lughart-706 uses the term “lane” in a way that makes clear that the multiple arrows in Fig. 1A indicate multiple lanes. E.g., Lughart-706, 13:52-57 (“each of the transceivers described above as implementing a multiplexing function in the egress/transmit direction will be capable of performing a corresponding demultiplexing function in the ingress/receive direction to generate the *appropriate number of host-side lanes.*”), Figs. 1A-1D, 13:13-48 (describing configurations with different numbers of lanes at the host-side and/or line-side); Min, ¶142.

This usage is consistent with the Ethernet standard in which a “lane” is a “bundle of signals” that “communicate a quantum of data and/or control

information between two end-points.” EX1007, IEEE Std. 802.3-2015, 86 (§1.4.246); Min, ¶143.

This usage is also consistent with the ’233 specification, which describes “converting 1 lane of PAM4 symbols into 2 lanes of NRZ symbols, and vice versa,” as is depicted in FIG. 1A of Lugthart-706. *Compare* EX1001, 4:44-45; Lugthart-706, 8:50-60; Min, ¶144.

The ’233 specification also refers to a “unidirectional connection” and defines a “*bidirectional* lane” as “formed by two unidirectional connections” wherein one is for transmit (TX) and the other for receive (RX). EX1001, Fig. 3A, 5:16-24 (bidirectional lanes LN0-LN3); Min, ¶145. Accordingly, one of the arrows for the TX DATA and one for the RX DATA in Lugthart-706 Fig. 1A represents a bidirectional *lane* as that term is used in the specification. Min, ¶145.

The specification uses a *multi-lane data stream* to describe multiple lanes that each carry a portion of a data stream, as is shown in Lugthart-706 Figure 1A. E.g., EX1001, 2:18-20 (describing “[a DRR] device... converts *a multi-lane data stream* from the first host interface port”); Min, ¶146.

Lugthart-706 discloses *inbound and outbound multi-lane data streams* because its transceiver receives TX DATA (*outbound data stream*) *from a host* in multiple lanes on the “EGRESS/TRANSMIT” path. E.g., Lugthart-706, Figs. 1A (TX data on two lanes), 1C-1D (showing multiple host-side differential TX lanes),

Fig. 2A, 7:24-27, 8:13-32, 13:25-27; Min, ¶147. Transceiver 10 transmits RX DATA (*inbound data stream*) **to a host**—on the “INGRESS/RECEIVE” path—in multiple lanes. Lugthart-706, Figs. 1A (RX DATA on two lanes), 1C-1D (showing multiple host-side differential RX lanes), 2A, 7:24-27, 8:13-32, 13:25-27; Min, ¶147.

iii. end connector plug

The “end connector plug” is capable of being inserted in a “host interface port.” Limitation [15.a]; EX1001, 2:16-17; Min, ¶148. The ’233 specification describes a connector terminating an end of a cable as including a “plug” (e.g., *end connector plug*) adapted to mate with a host device’s Ethernet port (e.g., *host interface port*). EX1001, Figs. 2 (connector 100), Fig. 3B (connector 100/101, plug 200/201, host device 302/304), 4:47-54 (“Connector 100 includes a plug 200 adapted to fit a standard-compliant Ethernet port in a first host device 302[.]”), 7:14-15 (“The connectors 100, 101, have plugs 200, 201 that mate with the receptacles 336 of the two host devices 302, 304.”); Min, ¶148.

Lugthart-706’s cable has transceiver assemblies 105a/105b at respective ends of cable 110. Lugthart-706, 6:65-67, 15:42-47, Fig. 2A (annotated below); Min, ¶149. “Each of the transceiver assemblies 105a and 105b **has an input port** that is **configured to mechanically and electrically connect**, e.g., in a releasable

fashion, *to a corresponding port... on the respective electronic device 101a, 101b[.]*” Lugthart-706, 15:42-47; Min, ¶149.

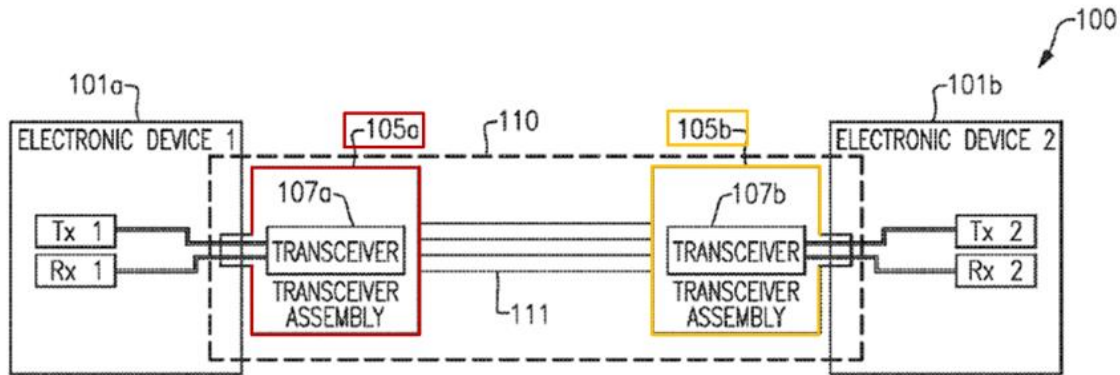


FIG. 2A

Lugthart-706’s input port for each transceiver assembly 105a/105b is a *first/second end connector plug*, respectively, because it mechanically and electrically mates with the corresponding port on an electronic device (e.g., host device) just like plug 200 in the ’233 Patent. Min, ¶150. POSAs also understood that the corresponding port in each electronic device was conventionally a “standard-complaint Ethernet port” (EX1001, 4:47-54) because Lugthart-706 describes the input port as comprising standardized connectors including SFP and QSFP that were typically used for Ethernet-complaint connections and had *plugs* for mating with an electronic device’s interface port. Lugthart-706, 15:47-52, 15:59-63; EX1022, 26-27; EX1023, 24; Min, ¶150.

iv. *host interface port*

The '233 Patent describes “inserting [an] end connector plug of a cable into a... host interface port[.]” Limitation [15.a]; EX1001, 2:16-17; Min, ¶151.

Lugthart-706’s electronic device is a *host* device. Lugthart-706, 14:14-15 (“first and second electronic devices 101a, 101b, which can also be referred to herein as host devices.”); Min, ¶152. The electronic device interface is a *host interface*. Lugthart-706, 3:31-34 (“a communication device includes a host interface”); Min, ¶152. The transceiver assembly 107a/107b input port “***mechanically and electrically connect[s]***, e.g., in a releasable fashion, ***to a corresponding port... on the respective electronic device*** 101a, 101b[.]” Lugthart-706, 15:42-47; Min, ¶152. The “corresponding port” on electronic device 101a/101b is the *first/second host interface port*, respectively, because it receives and electrically and mechanically connects the transceiver assembly 107a/107b input port (e.g., *first/second end connector plug*). Min, ¶152.

When used Lugthart-706’s transceiver 107a *exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug* because as explained above, e.g., Figure 1A, when connected to a host device the transceiver electrically receives two lanes of TX data (*outbound multi-lane data stream*) from, and transmits two lanes of RX data (*inbound multi-lane data stream*) to, electronic device 101a (host device) through the

“corresponding port” (*first host interface port*) that electrically connects the transceiver assembly 107a’s input port (*first end connector plug*), meeting [1.a]. Lugthart-706, 8:8-32 (transceiver “receive[s] host side transmit data,” DAC 24a/24b “generate host side receive data”), 8:33-39 (“transceiver 10 can be used to support data transfer between various electronic devices”) Min, ¶153. Transceiver 107b in transceiver assembly 105b provides the same functionality with electronic device 101b, meeting [1.b]. Min, ¶153.

c. Limitation [1.c]

1.c	electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,
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Lugthart+Gorecki meets [1.c] because Lugthart-706 describes cable 110 comprising conductive lines 111 (*electrical conductors*) connecting transceivers 107a/107b. Lugthart-706, Fig. 2A (annotated below), 14:29-42, 16:11-20 (copper conducting lines 111); 19:2-6 (lines 111 can be twinaxial cable providing differential signaling); Min, ¶155.

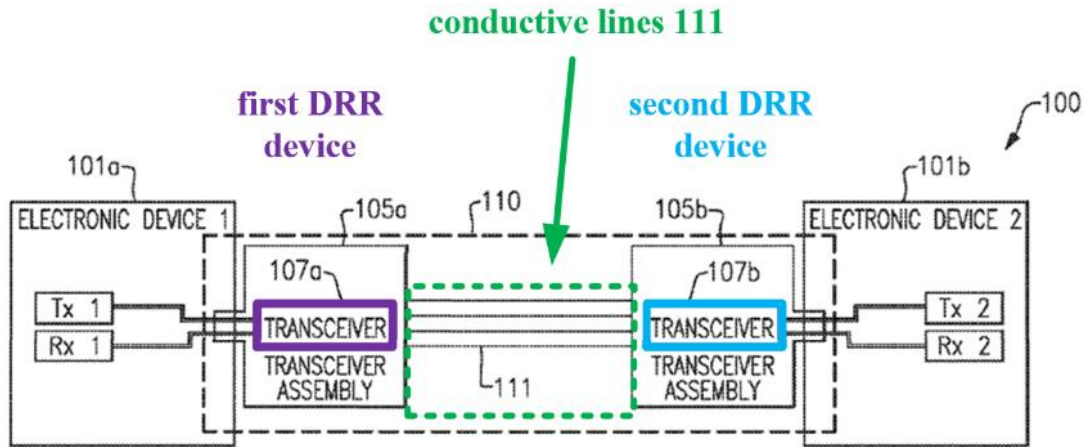


FIG. 2A

The '233 Patent describes electrical signals “transiting the cable conductors” as “electrical transit signals.” EX1001, 2:5-7, 4:17-18; Min, ¶156. Lugthart-706’s conducting lines 111 conduct electrical signals between transceivers 107a and 107b. E.g., Lugthart-706, 14:7-42, 16:11-15 (“electrical conducting lines 111... can transport electrical signals” between electronic devices 101a/b), 19:2-6 (twinax lines 111 support differential signaling); Min, ¶¶156-157.

d. Limitations [1.d]/[1.e]

1.d	the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and
1.e	the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,

As explained *supra* §VI.D.1.b ([1.a]), Lugthart-706 converts multiple NRZ data streams from a host to, e.g., re-timed NRZ or PAM-4 data stream(s) over the cable, and the reverse for RX signal from the cable to RX DATA transmitted to the host device. E.g., Lugthart-706, 8:40-60, 13:13-48; Min, ¶158. This matches an example of *converting* in the specification. EX1001, 4:44-45; Min, ¶158.

Lugthart+Gorecki meets [1.d] because—when used—Lugthart-706’s transceiver 107a receives multiple signals from a host device comprising “host side transmit data (TX DATA),” e.g., *outbound multi-lane data streams*. Lugthart-706, Figs. 1A (annotated below), 6A, 8:13-17, 30:23-25; *supra* §VI.D.1.b ([1.a]); Min, ¶159.

Transceiver 107a “converts between” the TX DATA from the *first* host (electronic device 101a)—received over the *first host interface port* (*supra* §VI.D.1.b ([1.a]))—and the TX signal (e.g., *electrical transit signal*, (*supra* §VI.D.1.c ([1.c])) transmitted over the cable by equalizing the TX DATA signal

received (equalizers 11a/11b), performing a CDR function (CDR 12a/12b), conditioning and recovering the TX DATA (DSP 13), and multiplexing and remodulating the TX DATA into the TX signal (DSP 13, DAC 14). Lugthart-706, Figs. 1A (annotated below), 2A, 6A, 8:19-22, 9:52-55, 16:11-15, 30:25-55, generally 7:66-10:27 (describing transceiver); Min, ¶160.

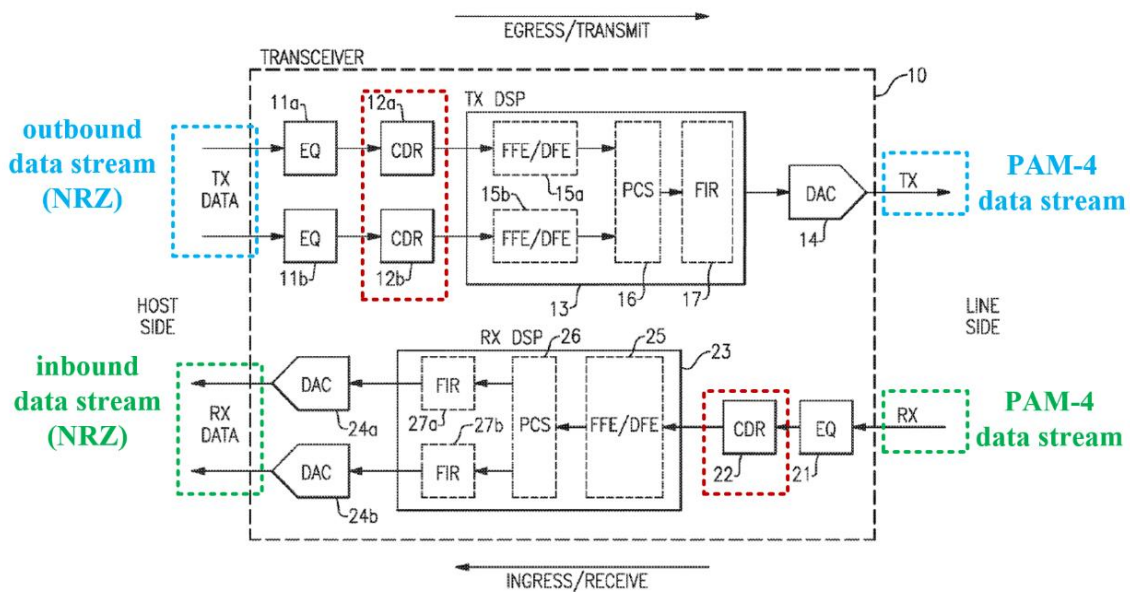


FIG.1A

The receive path electronics perform the same operations—in a reverse order—to convert between the RX signal from the cable to the RX DATA signal transmitted to the host device. Min, ¶161. The transceiver signal conversion is *for the first host interface port* because as explained above transceiver 107a receives TX DATA from, and transmits RX DATA to, electronic device 101a via the *first host interface port*. Lugthart-706, Figs. 1A (“INGRESS/RECEIVE”), 2A, 6A, 9:10-51, generally 7:66-10:27 (describing transceiver); Min, ¶161.

Lugthart-706 transceiver 107b provides the same functionality for electronic device 101b, meeting [1.e]. Min, ¶¶162-163.

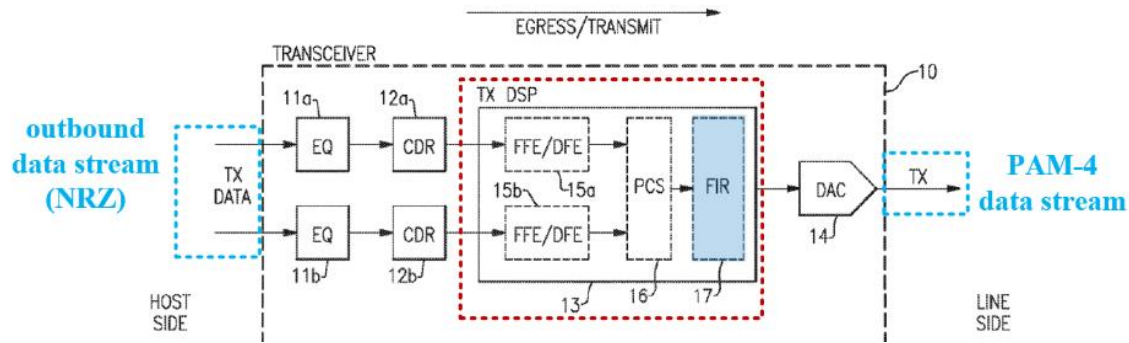
e. Limitation [1.f]

1.f	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.
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i. pre-equalization

Lugthart+Gorecki meets [1.f] because Lugthart-706’s transceivers 107a/b provide “adaptive and configurable signal conditioning features such as... *output pre-emphasis*” on the TX signals transported by conductive lines 111 (e.g., *electrical transit signals, supra* §VI.D.1.c ([1.c])). Lugthart-706, Figs. 1A, 2A, 16:11-15, 23:59-24:2, 29:23-28; Min, ¶164. POSAs understood that “pre-emphasis” and “pre-equalization” have the same meaning. Min, ¶164; Raghavan, 2:39-41 (describing a “technique for combating ISI... known as ‘pre-emphasis’, or pre-equalization”); Schmidt, 7:54-55; Zerbe-063, 3:24-27; McCall, 5:4-8.

Transceivers 107a/107b provide pre-equalization in DSP 13 using finite impulse response (FIR) filter 17. FIR filter 17 is a *transmit filter* because DAC 14 converts the FIR 17 output to an analog signal that is transmitted on the line side. Lugthart-706, Fig. 1A (annotated detail below), 23:13-17, 23:59-24:2; Min, ¶165.



FIR filter 17 “perform[s] emphasis on the signal to compensate for channel losses,” e.g., it *pre-equaliz[es] the electrical transit signal*. Lugthart-706, 23:62-64; Min, ¶166. FIR filter 17 forwards conditioned signals to DAC 14 for transmission over cable 110 and conductive lines 111. Lugthart-706, Figs. 1A, 2A, 8:19-22, 16:11-15, 23:59-24:2; Min, ¶166. The TX signals transmitted on the cable’s conductive lines are *electrical transit signals*. Min, ¶166.

The filter 17 tap coefficients are *transmit filter coefficient values*. Min, ¶167. The '233 Patent states that “equalization parameters may include filter coefficient values for pre-equalizer filters[.]” EX1001, 5:45-48, 8:15-26 (during training adaptation adjusts filter coefficient values); Min, ¶167. Lugthart-706 explains that FIR filter 17 can be “a five tap FIR filter with tap coefficients S5.3, S7.3, S8.3, S7.3, S5.3,” Lugthart-706, 22:12-16, while Gorecki-617 provides that “tap weights or coefficients (values) may be determined or controlled[.]” Gorecki-617, 6:56-57; Min, ¶167.

ii. non-volatile memory

Lugthart+Gorecki uses Gorecki-617's teaching to store filter coefficient values in EEPROM, and use those values to set filter coefficients to provide pre-equalization. Gorecki-617, 7:18-33 (“[I]nformation representative of... *the coefficients of the tap(s)*... may be *stored... in... for example... ROM or EEPROM*. In this way, the transmitter *may access the memory to retrieve the necessary information* during start-up/power-up, initialization or re-initialization.”); Min, ¶168. An EEPROM [electrically erasable programmable read-only memory] is non-volatile memory. EX1051 (“Lauby”), [0081] (“nonvolatile memory can include... electrically erasable PROM (EEPROM)”); EX1032 (“Bakx”), 2:53-54 (“EEPROM is a non-volatile memory”); EX1047 (“Lindsay”), [0012] (“non-volatile memory may include... an EEPROM”); Min, ¶¶120, 168. Lugthart+Gorecki uses Gorecki-617's teaching to program filter 17 coefficients using the values stored in non-volatile EEPROM to pre-equalize the TX signal in transceiver 107a and 107b, thus meeting [1.f]. *Supra* §VI.C (combination); Min, ¶¶168-169.

2. Claim 2

2	The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.
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Lugthart+Gorecki meets claim 2 because Gorecki-617 teaches “[I]nformation representative of... *the coefficients of the tap(s)*... may be stored... in... for example... ROM or EEPROM. In this way, the transmitter *may access the memory to retrieve the necessary information* during start up/power-up,” which is a *power-on event*. Gorecki-617, 7:18-33, 16:47-53; *supra* §VI.C (combination); Min, ¶170. Gorecki-617 describes a “controller” that “distribute[s] to the transmitter” the filter coefficients thereby configuring FIR filter 17 for pre-emphasis at this power-on event. Gorecki-617, 7:4-17; 7:26-33; Min, ¶170. For transceiver 107a this is a *first controller*, so that Lugthart+Gorecki meets claim 2. Min, ¶¶170-171.

3. Claim 3

3	The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.
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The analysis treats “*transmit coefficient values*” as referring to [1.f] “*transmit filter coefficient values*,” as the term otherwise has no antecedent basis.

Lugthart+Gorecki meets claim 3 because Lugthart-706's FIR 17 in transceivers 107a and 107b use *transmit filter coefficient values* that have been stored in memory. *Supra* §§VI.C (combination), VI.D.2 (claim 1); Min, ¶¶172-173. Like the '233 Patent's specification, Gorecki-617 refers to storing of values in memory as programming. Gorecki-617, 7:1-33 ("the adjustment or control of the taps of the equalization circuitry may be by the user via *programming*... coefficients of the tap(s), and/or the pulse durations of the tap(s) may be *pre-programmed*"), Min, ¶174; EX1001, 11:3-6 ("the automated tester equipment 'burns' the flash memory or otherwise *programs* the initial default values of the filter coefficients[.]").

Gorecki-617 teaches that the programmed memory "may reside on the integrated circuit containing the transmitter, receiver or transceiver." Gorecki-617, 7:43-49. A POSA would have found such an implementation of Lugthart+Gorecki obvious, as Lugthart-706 already includes programmable circuitry. Lugthart-706, 30:42-44 ("Programmable chip sets, physical coding sublayer (PCS) blocks, FPGAs, FIR filters can be used to condition and multiplex the digital data signal."); Min, ¶175. As the *first and second DRR devices* include the transceivers, a POSA would have understood that Lugthart+Gorecki meets "*the first and second DRR devices are programmed.*" Min, ¶175.

This programming is done *to use the transmit coefficient values when power is supplied to the first and second end connector plugs*. In Lugthart+Gorecki, stored FIR filter coefficients are retrieved from the non-volatile memory at start-up/power-up as taught in Gorecki-617. Gorecki-617, 7:18-33, *supra* §§VI.C (combination), VI.D.2 (claim 2); Min, ¶176.

Power-up in Lugthart+Gorecki indicates that *power is supplied to the first and second end connector plugs*. POSAs would have understood that power is supplied from a host device when the enclosing connector's connector plug was electrically connected to the host interface port in a corresponding electronic device 101a/b as described *supra* §VI.D.1.b ([1.a]) because this was conventionally how standardized connectors like QSFP or SFP worked. *E.g.*, Lugthart-706, 15:36-52 (describing connector formats); EX1023, 21 (“A host board together with the QSFP+ module(s) forms an integrated power system. ***The host supplies stable power to the module.***”), 22 Fig. 4 (“Recommended Host Board Power Supply Filtering”); Min, ¶177. Regardless, a POSA would have found it conventional and obvious to implement Lugthart+Gorecki with QSFP connectors powered by a connected host device. Min, ¶177.

A POSA would have understood that Lugthart+Gorecki uses the transmit coefficient values stored in memory *each time* power is supplied to the first and second end connector plugs. Gorecki-617 teaches that the programmed values can

be stored “permanently, semi-permanently or temporarily[.]” Gorecki-617, 7:21. When stored permanently, a POSA would have understood them to be used *each time power is supplied to the first and second end connector plugs*. Min, ¶¶178-179.

4. Claim 4

4	The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.
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A POSA would have had reasons to implement Lugthart+Gorecki by *determin[ing]* and then storing the transmit filter coefficient values in the non-volatile memories *after assembly of the cable*. Min, ¶180. As Gorecki-617 teaches, the values should be selected to offset effects of a communication channel. Gorecki-617, 9:8-10 (The equalizers are “configured to introduce compensation that is ideally the inverse of the effects caused by the communications channel.”); *supra* §VI.D.1.b; Min, ¶180. In Lugthart+Gorecki the communications channel includes the electrical conductors as connected to the *first and second DRR devices*. Min, ¶181. That communication channel does not exist until the cable is assembled by attaching the first and second DRR devices to the electrical conductors. Min, ¶181. Accordingly, a POSA would have found it obvious to determine and then store filter coefficients, such as by measuring the effects in that

communication channel *after assembly*. Min, ¶182. Such an approach was known in the art. Boccaccio, [0033] (“The programming is preferably performed with the cable installed between the actual source and actual sink it will be connecting.”); Min, ¶182.

Additionally, Lugthart+Gorecki meets claim 4 because Gorecki-617 describes “the coefficients of the tap(s)... are adjusted or controlled *during operation* of the transmitter, for example using an adaptive algorithm.” Gorecki-617, 10:27-51, 6:50-53, 17:41-51; Min, ¶183. Determining values “during operation” happens after cable assembly. Min, ¶183. Gorecki-617 teaches that the adaptive algorithm—which *determin[es] transmit filter coefficient values*—is performed “after (or during) the performance of an initialization or re-initialization process.” Gorecki-617, 7:50-61; Min, ¶183.

Gorecki-617 describes stored coefficient values can be “fine-tuned to enhance the system performance” (Gorecki-617, 7:51-53), and that the values can be “re-programmed” and, for that reason, are stored in writable non-volatile memory. Gorecki-617, 7:18-33, 10:37-51; Min, ¶184.

A POSA would have had reasons to implement Lugthart+Gorecki with writable non-volatile memory, as Gorecki-617 describes NVM including writable NVM (“*EEPROM or the like*”). Gorecki-617, 7:24-25, 10:46-47; Min, ¶185. EEPROM is electrically erasable programmable read only memory, e.g., rewritable

NVM. *Supra* §VI.B; Min, ¶185. A POSA would have known that flash memory was another well-known rewritable non-volatile memory (e.g., “EEPROM or the like”) conventionally used with transmit FIR filters. E.g., Hsu-140, 3:42-4:2 (“Any type of NVRAM can be used as the rewritable non-volatile storage, so long as [it] is of the type suitable for integration on an integrated circuit.”); Min, ¶186. A POSA would have understood such memories would be used when the content of those memories is both re-programmed and preserved through “startup/power-up, initialization or re-initialization,” as described in Gorecki-617, 7:18-33; Min, ¶186.

Thus, Lugthart+Gorecki would have included rewritable non-volatile memory that could be updated with new coefficient values that fine-tuned pre-equalization or equalization with new coefficient values learned through training at manufacture or during usage with a particular device in a particular environment. Lugthart-706, 48:64-49:12, 49:20-34; Gorecki, 7:50-61, 10:37-51; Hsu-140, 3:42-4:2, 9:21-28; Min, ¶187. Preserving such adapted pre-equalization filter coefficients in rewritable non-volatile memory like an EEPROM would have ensured that the fine-tuned coefficients remained available after an AEC transceiver—or the host powering it—was power cycled, initialized, or re-initialized. Gorecki-617, 7:31-33 (“In this way, the transmitter may access the

memory to retrieve the necessary information during start up/power-up, initialization or re-initialization.”); Min, ¶188.

Regardless, POSAs would have known that storing updated filter coefficients in Lugthart+Gorecki’s non-volatile memory was conventional and desirable so that the adapted coefficient values would be available after power cycling the AEC transceiver by unplugging it from a host device powering it, or power cycling the host device powering the AEC transceiver. E.g., Hsu-140, Abstract (“[D]ata transmitter includes a rewriteable non-volatile storage, operable to be rewritten with control information representing the values of coefficients updated during operation off the FIR driver.”), 2:46-49 (same), 3:45-52 (“Updated values of the coefficients used in the taps of the FIR transmitter 30 are determined and stored to the flash memory 20 during the operation of the FIR transmitter. *When the FIR transmitter is powered off and back on again, the coefficient values as last updated are available to be retrieved from the flash memory 20 and applied to the taps of the FIR transmitter again.*”); Min, ¶¶189-190.

5. Claim 5

5	The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.
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The '233 specification parrots the “receiver-based equalization” claim language but does not give examples or explain what it is. E.g., EX1001, 2:42-45, 2:61-63. Regardless, “receiver-based equalization” is met by equalizing a received signal to compensate for distortion incurred during transmission. EX1024 (“Shimanouchi”), 10:22-35; EX1025 (“Aziz”), ¶4; EX1026 (“Laturell”), 2:17-21; EX1027 (“Hanumolu”), p.185 (describing “receive-side equalization” suppressing channel loss); Min, ¶191.

A POSA would have had a reason to implement Lugthart+Gorecki in a way that meets claim 5. Lugthart-706’s transceiver equalizes signals received over conductive lines 111 (e.g., *electrical transit signals*) using receive path equalizer 21 to improve signal fidelity. Lugthart-706, Fig. 1A, 9:10-25 (“receive path equalizer 21 can be used to provide signal equalization to compensate for transmission line losses on the line side” such as “to compensate for high-frequency signal loss by boosting high frequency components of a signal relative to low frequency components of the signal, thereby improving signal fidelity.”), Min, ¶192. As part of the transceivers, receive path equalizers 21 in transceivers

107a and 107b would be in *the first and second DRR devices*, respectively. *Supra* §§VI.C (combination), VI.D.1.e ([1.a]/[1.b]); Min, ¶193.

Receive path equalizers 21 are performing an equalization function analogous to that performed by transmit filters 17. For the reasons explained *supra* §§VI.C (combination), VI.D.1.e ([1.f]) that it would have been obvious to implement transmit filters 17 in Lugthart+Gorecki using coefficient values stored in non-volatile memories, it would have been obvious to implement equalizers 21 with *coefficient values stored in the nonvolatile memories*.

Both Lugthart-706 and Gorecki-617 suggest that equalizers 21 are, like filters 17, configured to compensate for signal distortion over the cable. Lugthart-706, 22:43-48 (“The equalizer 21 can be configured to compensate for losses occurring during transmission over the cable...”); Gorecki-617, 1:59-67 (“[C]onventional high speed digital baseband communications systems often employ circuitry, for example, a finite impulse response filter (‘FIR filter’), *in the receiver*.... Such circuitry typically includes [sic] one or more taps having fixed or pre-programmed ‘positions’ and coefficients.”), 2:17-21 (“**Regardless of where the equalization circuitry is implemented**, the duration of the equalization signal and the relative position or placement of the tap(s) of the equalization circuitry are selected or designed to avoid interference with the signal representative of the transmitted information.”); Min, ¶195.

Equalizer 21's equalization functionality depends on filter coefficient settings like transmit filter 17. Hanumolu, pp. 185-198 (describing different receive-side equalization architectures configured with coefficients $[C_{-1}, C_0, C_1]$); EX1028 ("Das Sharma"), ¶69 (describing applying coefficients to a receiver's settings to minimize communication data loss); Min, ¶196.

Though Gorecki-617 describes implementing its equalization structure and techniques at a transmitter "may have an advantage," Gorecki-617, 18:47-53, a POSA would have recognized from this statement that implementation in the receiver was also an option, particularly as Gorecki-617 explains implementation more generally in connection with equalization circuitry more generally. Min, ¶197; Gorecki-617, 2:17-21, 6:14-23 ("The circuitry and techniques include leading and/or trailing taps to reduce, minimize, mitigate or effectively eliminate precursor and/or post-cursor intersymbol interference due to, for example, bandwidth limitations and reflections in high-speed digital communication systems. In this way, the equalization circuitry and techniques may reduce, minimize or eliminate non optimum (e.g., over-equalization) at the boundaries of the data signal (i.e., the symbol)."). A POSA would have considered such an approach would have been applicable to equalizers 21 as they provide equalization in the same way as transmit filter 17. Min, ¶197.

Additionally, a POSA would have understood that the equalization performed at both transmit filter 17 and receive path equalizer 21 should collectively compensate for the effects introduced the communication channel and would have had a reason to set equalization parameters for both in the same way. Min, ¶198.

As explained *supra* §§VI.C (combination), VI.D.1.e ([1.f]), in Lugthart+Gorecki, transmit filter 17 uses coefficient values stored in non-volatile memory. Min, ¶¶199-200.

6. Claim 6

6	The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.
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Lugthart+Gorecki meets claim 6 because Lugthart-706’s active cable includes at least one twin-axial cable, which includes at least two inner conductors that provide differential signaling. Lugthart-706, 19:2-6 (“a cable can include twinaxial cables (‘Twinax’), where each Twinax cable includes two inner conductors... [and] the two inner conductors can be configured to implement differential signaling.”); Min, ¶¶201-202. The twin-axial cable’s inner conductors are *twin-axial conductors*. EX1013 (“Dabiri”), 3:41-45 (“twinaxial (or ‘twinax’) cables... can each comprise a full-duplex twinax pair of conductors”); Min, ¶201.

The Twinax conductors transport signals (e.g., *electrical transit signals*) between the ends of the cable. Min, ¶¶201.

7. Claim 8

Claim 8 recites a *cable manufacturing method* for the cable in claim 1, comprising three “connecting” steps (Limitations [8.a], [8.b], [8.c]), while limitations [8.d]-[8.f] repeat cable component capabilities recited in Limitations [1.d]-[1.f].

a. Preamble

8.PRE	A cable manufacturing method that comprises:
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Lugthart+Gorecki renders obvious claim 1. *Supra* §VI.D.1. As shown *infra* §VI.D.7.b ([8.a]-[8.c]), POSAs would have found it obvious to manufacture claim 1’s cable by “connecting” Lugthart-706’s transceiver, at each end of a cable, to standard connectors and conductive lines 111, meeting [8.PRE]. Min, ¶¶203-204.

b. Limitations [8.a]-[8.c]

Limitations [8.a]/[8.b] recite *connecting a first/second connector plug* to the *first/second DRR device* recited in [1.a]/[1.b]. EX1029, 1; Min, ¶205.

POSAs would have had reasons to “connect” a “connector plug” to Lugthart-706’s transceivers 107a/107b (*first/second DRR device*, respectively) because as explained *supra* §VI.D.1.b ([1.a]/[1.b]) Lugthart-706 describes each

transceiver having “an input port” comprising the *connector plug*. Min, ¶206. A POSA would have understood that the input port required electrical connection to a transceiver before it could transport signals between a host transceiver and transceiver 107a/107b, to provide the functionality described in Lugthart-706. *Supra* §VI.D.1.b ([1.a]/[1.b]); Lugthart-706, Fig. 2A (below); Min, ¶207.

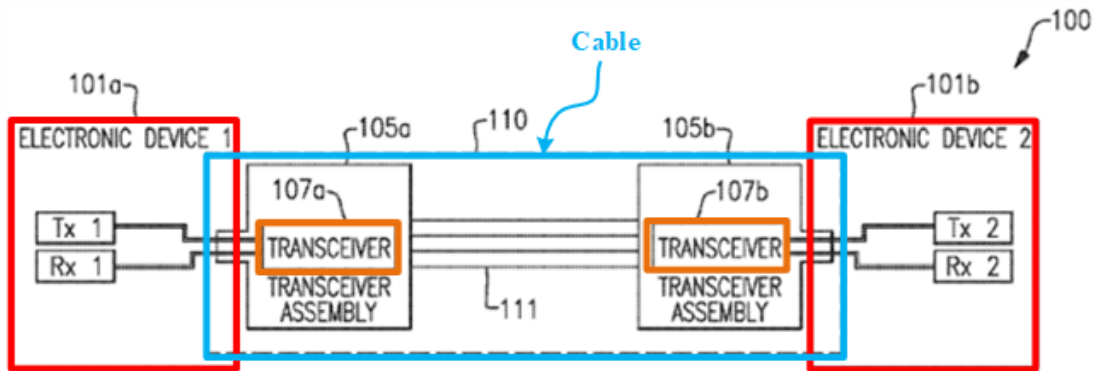


FIG. 2A

A POSA would have had reasons to “connect” conductive lines 111 to Lugthart-706 transceiver 107a/107b, meeting [8.c], in order to achieve the cable that Lugthart-706 describes wherein lines 111 electrically connect transceivers 107a/107b as explained *supra* §VI.D.1.c ([1.c]). Lugthart-706, 16:11-15; EX1029, 1; Min, ¶¶208-209.

c. Limitations [8.d]-[8.f]

Limitations [8.d]-[8.f] substantively recite the same subject matter as limitations [1.d]-[1.f] in device claim 1. EX1029, 1-2; Min, ¶210. The [8.d] *multi-lane data streams* are the [1.d] *inbound and outbound multi-lane data streams*.

Min, ¶210. Lugthart+Gorecki meets limitations [8.d]-[8.f] for the same reasons it meets the corresponding limitations below. Min, ¶¶210-211.

Limitation	Corresponding Limitation	Discussion (<i>supra</i>)
[8.d]	[1.d]	§VI.D.1.d
[8.e]	[1.e]	§VI.D.1.d
[8.f]	[1.f]	§VI.D.1.e

8. Claim 9

9	The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.
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Lugthart+Gorecki meets claim 9 for the reasons it meets claim 2. EX1029, 4; *supra* §VI.D.2 (claim 2); Min, ¶¶212-213. POSAs would have had reasons to “provide” the *first controller* because Gorecki-617 describes a controller that comprises part of Lugthart+Gorecki’s cable. Gorecki-617, 7:4-17; 7:26-33; *supra* §VI.D.2; Min, ¶212.

9. Claim 10

10	The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.
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Lugthart+Gorecki meets claim 10 for the reasons it meets claim 3 *supra* §VI.D.3. EX1029, p.4; Min, ¶¶214-215.

10. Claim 11

11	The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.
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Lugthart+Gorecki meets claim 11 for the reasons it meets claim 4 *supra* §VI.D.4. EX1029, 4; Min, ¶216. POSAs would have had reasons to determine transmit filter 17 coefficient values by training as part of the cable manufacture after connecting transceivers 107a/107b in order to provide the initial pre-set coefficient values that Gorecki-617 describes. Lugthart-706, 4:31-63, 49:3-12, 20-37 (describing training); Gorecki-617, 7:18-33 (describing storing pre-set coefficients); *supra* §VI.D.1.e ([1.f]); Min, ¶216.

As explained *supra* §VI.D.1.e ([1.f]), Lugthart+Gorecki stores preset coefficient values in EEPROM. Min, ¶217. This renders obvious claim 11. Min, ¶218.

11. Claims 12-13

Claims 12-13 recite the same additional limitations as claims 5-6, respectively, and Lugthart+Gorecki meets claims 12-13 for the same reasons. EX1029, 5; *supra* §§VI.D.5 (claim 5), VI.D.6 (claim 6); Min, ¶¶219-220.

12. Claim 15

a. Preamble

15.PRE	A communications method that comprises:
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Lugthart+Gorecki meets [15.PRE] because Lugthart-706 describes “methods for high speed communications.” Lugthart-706, Abstract, 1:36-37; *see also* Gorecki-617, 1:12-14 (“[T]he invention relates to a system and *method for providing high-speed digital communications* through a communications channel”).; Min, ¶221.

b. Limitation [15.a]

15.a	inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and
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Lugthart+Gorecki meets [15.a] for the reasons it meets [1.a], [1.c], and [1.d] *supra* §§VI.D.1.b ([1.a]), VI.D.1.c ([1.c]), VI.D.1.d (1.d)). EX1029, 6; Min, ¶¶222-223. Lugthart-706 describes “Each of the transceiver assemblies 105a and 105b *has an input port* that is *configured to mechanically and electrically connect*, e.g., in a releasable fashion, *to a corresponding port... on the respective electronic device* 101a, 101b[.]” Lugthart-706, 15:42-47; Min, ¶222. POSAs would have had reasons to insert each input port in a corresponding electronic device’s port (*host interface port*) to use the Lugthart+Gorecki cable as shown in Lugthart-706 Figure 2A. Min, ¶222.

c. Limitation [15.b]

15.b	inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,
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Lugthart+Gorecki meets [15.b] for the reasons it meets [1.b], [1.c], and [1.e] *supra* §VI.D.1.b-VI.D.1.c ([1.b]-[1.c]), VI.D.1.d ([1.e]); EX1029, 6-7; Min, ¶¶224-

225. POSAs had reasons to insert transceiver assembly 105b's input port in electronic device 101b's corresponding port (*second host interface port*) for the same reasons described for assembly 105a / electronic device 101a *supra* §VI.D.12.b ([15.a]); Min, ¶224.

d. Limitation [15.c]

15.c	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.
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Lugthart+Gorecki meets [15.c] for the reasons discussed *supra* §VI.D.1.e ([1.f]); EX1029, 7; Min, ¶¶226-227.

13. Claim 16

a. Limitation [16.a]

16.a	The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively,
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Lugthart+Gorecki meets [16.a] for the reasons it meets claim 3 *supra* §VI.D.3. Min, ¶¶228-229. Each transceiver assembly input port (*connector plug*) is supplied power from the host device that electrically connects to the cable when the input port is coupled to the host device's corresponding receiving port. *Supra* §§VI.D.2-VI.D.3 (claims 2-3); Min, ¶228. Each transceiver assembly input port

(*connector plug*) is connected to the Lugthart+Gorecki controller because as explained for claim 2 *supra* §VI.D.2 the controller comprises part of the transceiver assembly, which is electrically connected to the input port. Min, ¶228.

b. Limitation [16.b]

16.b	each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.
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Lugthart+Gorecki meets [16.b]—for the *first and second controller devices*—for the reasons it meets claim 2 *supra* §VI.D.2 for the *first controller device*. Min, ¶¶230-231.

14. Claims 17-19

Claims 17-19 substantively recite the same subject matter as claims 3-5, respectively. EX1029, 8; Min, ¶¶232-233. Lugthart+Gorecki meets claims 17-19 for the same reasons it meets the corresponding claims below. Min, ¶232.

Claim	Corresponding Claim	Discussion (<i>supra</i>)
17	3	§VI.D.3
18	4	§VI.D.4
19	5	§VI.D.5

VII. GROUND 2: LUGTHART+GORECKI+802.3 RENDERS OBVIOUS CLAIMS 7, 14, AND 20

A. IEEE Std. 802.3-2015

IEEE Std. 802.3-2015 (“802.3”) is the 2015 IEEE Standard for Ethernet and is applicant admitted prior art.³ EX1001, 1:6-24, 6:33-45; EX1007, 21 (Introduction), 54 (“This standard defines Ethernet local area, access and metropolitan area networks.”); EX1001, 1:6-24; Min, ¶234. IEEE Std. 802.3-2015 was adopted on September 3, 2015 and published March 4, 2016.⁴ EX1007. The standard defines a three-tap transmit filter for pre-equalization in electrical backplanes (e.g., 10GBASE-KR).⁵ EX1011 Fig. 72-11 (“Transmit equalizer example” with taps $c(-1)$, $c(0)$, and $c(1)$), 490; Min, ¶235. The same three-tap transmit filter is used for pre-equalization in a chip-to-module link. EX1012, Fig. 85-3 (“Transmit equalizer functional model” below), 225 (“The 40GBASE-CR4 and 100GBASE-CR10 transmit function includes programmable equalization to

³ 802.3-2015 comprises six sections provided as EX1007-EX1012, respectively. EX1007, 21-22 (identifying sections).

⁴ See <https://ieeexplore.ieee.org/servlet/opac?punumber=7428774>.

⁵ 10GBASE-KR is the “IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-R encoding over an electrical backplane.” EX1007, 71 (Definitions §1.4.34). Min, ¶235.

compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. ... The requirements for the 40GBASE-CR4 and 100GBASE-CR10 transmit equalizer are intended to be similar to the requirements for 10GBASE-KR specified in 72.7.1.10.”); *see also* Fig. 92-7, 416 (same transmit filter model for 100GBASE-CR4);⁶ Min, ¶¶236-239.

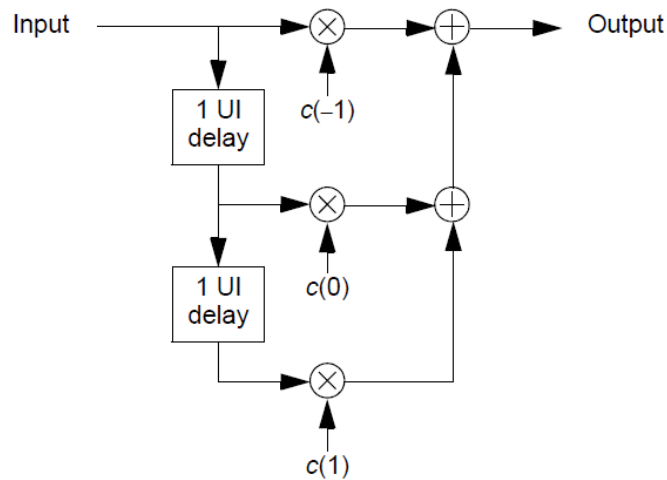


Figure 85-3—Transmit equalizer functional model

⁶ 40GBASE-CR4 is the IEEE 802.3 Physical Layer specification for 40 Gb/s using 40GBASE-R encoding over four lanes of shielded balanced copper cabling. EX1007, 73 (Definitions §1.4.67); Min, ¶¶237-238. 100GBASE-CR4 and 100GBASE-CR10 are the specifications for 100 Gb/s using 100GBASE-R encoding over four (CR4) and ten (CR10) lanes, respectively, of shielded balanced copper cabling (EX1007, 72 (Definitions “§1.4.53 100GBASE-CR4,” “§1.4.54 100GBASE-CR10”). Min, ¶239.

Setting the first and third tap coefficient values (e.g., $c(-1)$ and $c(1)$) to 0, and the second tap coefficient value (e.g., $c(0)$) to “maximum,” passes the input signal without equalization. EX1011, 480 (“If preset is TRUE then the function returns *the coefficient value equivalent to no equalization* [$c(-1)$ and $c(1)$ coefficients are set to zero, $c(0)$ set to maximum].”); Min, ¶240. In other words, 802.3 specifically defines transmit filter tap settings that disable pre-equalization. Min, ¶240.

B. Lugthart+Gorecki+802.3

A POSA would have had reasons to use 802.3’s teaching to disable transmit equalization in Lugthart+Gorecki (*supra* §VI.C) because it was known that disabling filter taps could minimize transceiver power consumption where signal quality was achievable without transmit pre-equalization. Min, ¶¶241-243. A POSA would have known that disabling a filter tap would have the same effect as setting a filter tap coefficient value to zero as taught in 802.3. Min, ¶244. For example, Zerbe-063 describes transmit pre-equalization and explains that “the FIRs of the transmitter... can be modified to support modes in which... *taps can be disabled if not needed* to consume minimum power while satisfying the performance or margin objective.... Through a combination of enabling or disabling Tx and Rx DFE taps... the overall system power can be minimized while maintaining adequate margins.” Zerbe-063, 27:15-43; Min, ¶244. A POSA would

have known that disabling transmit pre-equalization was a conventional functionality for a transceiver. EX1030, Ex. B (“TI-Retimer”), 37, Table 14 (describing hexadecimal channel register 1E setting for “Raw Data” in which “FIR filter will not function”); Gorecki-617, 18:3-17 (explaining “the leading and/or trailing taps may be ‘turned off’ or disabled”); Min, ¶245. And a POSA would have known that Lugthart-706’s five-tap transmit filter pre-equalization functionality could be disabled through choice of tap coefficient values in the same manner as the Ethernet Standard taught for its three-tap transmit filter (e.g., by setting certain taps to zero while maximizing the central tap). Min, ¶245.

The resulting Lugthart+Gorecki+802.3 combination provides a mechanism for disabling transmit pre-equalization in FIR 17 and 27a/27b. Min, ¶246. A POSA would have disabled Lugthart+Gorecki+802.3 pre-equalization in FIR 17 and/or FIR 27a/27b in order to reduce power consumption where pre-equalization was not needed to meet signal quality requirements. Min, ¶246.

Lugthart+Gorecki+802.3 thus would have combined familiar elements according to known methods yielding no more than predictable results. *KSR*, 550 U.S., 416. The combination would have used known methods (disabling FIR filters when pre-equalization was unnecessary) to solve a known problem (reducing power consumption), and would have improved the Lugthart+Gorecki

transceivers and system power consumption in the same way that it improved power consumption in Zerbe-063. *KSR*, 550 U.S. at 417; Min, ¶246.

A POSA would have had a reasonable expectation of success in achieving Lugthart+Gorecki+802.3 because setting filter coefficient values that disabled pre-equalization in transmit filters was known and described in the Ethernet Standard and other prior art discussed above, and—as those same references demonstrate—implementing this functionality was within the POSA’s ordinary skill. Min, ¶247. Disabling pre-equalization was conventional for providing lower power mode in transceiver components. Min, ¶247.

C. Claims 7, 14, and 20

Although claim 7 concerns claim 1’s *cable*, claim 14 concerns claim 14’s *manufacturing method*, and claim 20 concerns claim 15’s “*communications method*”, claims 7, 14, and 20 recite the same negative limitation “*wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.*” EX1029, 3; Min, ¶248.

Lugthart+Gorecki+802.3 uses the 802.3 teaching to set transmit filter coefficients to disable pre-equalization. As was known in the art, a POSA would have disabled pre-equalization “if not needed to consume minimum power while satisfying the performance or margin objective” for a system. Zerbe-063, 27:24-

37; Min, ¶249. Thus, for use-cases where signal transmission between host devices using the active cable meets performance objectives *without* FIR filters 27a/27b pre-equalizing the RX DATA signal transmitted into electronic device 101a/101b, a user would disable the pre-equalization at filters 27a/27b in Lugthart+Gorecki+802.3. *Supra* §VII.B (combination); Min, ¶249.

This renders obvious claims 7, 14, and 20. Min, ¶250.

VIII. NO BASIS FOR DISCRETIONARY DENIAL

A. Section 314(a) Denial is Unwarranted

The *General Plastic* analysis does not apply because the '233 Patent has not previously been challenged in IPR.

The *Fintiv*⁷ factors favor institution. Patent Owner (“PO”) filed a complaint in EDTX and the ITC on March 13, 2025. Petitioner expeditiously filed this Petition within four weeks of the complaints. The ITC has not initiated a Section 337 Investigation—let alone set a trial date—and Petitioner has not even answered the EDTX complaint. *If* the ITC initiates an Investigation, FWD will likely issue *before* the ITC’s investigation concludes.

1. *Fintiv* factor one favors institution.

The complaints were filed four weeks ago and the ITC has not initiated an Investigation. If it does, Petitioner will seek automatic stay of the Texas Litigation

⁷ *Apple v. Fintiv*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential).

under 28 U.S.C. §1659. *Fintiv* states that “an *earlier* ITC trial date *may* favor denial... *if* the ITC is going to decide the same or substantially similar issues to those presented in the petition. *Fintiv*, Paper 15, 8-9 (May 13, 2020) (informative); EX1043, 2 (“[T]he Board is less likely to deny institution under *Fintiv* where the ITC projected final determination date is *after* the Board's deadline to issue [FWD].”). There will be no “earlier ITC trial” here because FWD will likely issue before an ITC investigation—*if* ordered—is completed. Because the Petition was expeditiously filed, neither the Texas Litigation nor an ITC Investigation—which has not even been instituted—is sufficiently developed to determine that the same or similar issues will be presented in those proceedings.

1. *Fintiv* factor two favors institution.

The ITC has not initiated an Investigation. If it does, the ITC’s average time to completion is 18 months (EX1033), followed by a presidential review period of 60 days. If the Texas Litigation is not stayed, the average time to trial in EDTX is 23 months (EX1034). Given the mandate to issue FWD within 18 months, an FWD will likely issue before final decision/trial in the ITC/district court proceedings, which favors institution. *Fintiv*, Paper 11, 9; EX1043, 2.

2. *Fintiv* factor three favors institution.

Petitioner filed “expeditiously”—only four weeks after PO’s ITC and district court complaints and before any response deadline for either. *Fintiv*, Paper 11, 11

(“If the evidence shows that the petitioner filed the petition expeditiously, such as promptly after becoming aware of the claims being asserted, this fact has weighed *against* exercising the authority to deny institution[.]”); *Mobileye Global v. Facet Tech.*, IPR2024-01110, Paper 16, 13 (Mar. 5, 2025); *Apple v. Alivacor*, IPR2021-00972, Paper 10, 12-13 (Dec. 8, 2021) (weighing factor three against denial where Petitioner filed IPR before response deadlines in ITC and district court).

3. *Fintiv* factor four favors institution.

This Petition challenges all claims. Although PO’s ITC complaint asserts all claims, at any ITC trial the asserted claims will likely be narrowed; PO identifies a single asserted claim in the Texas Litigation. EX1038, ¶17; EX1039, 1-24. The dependent claims challenged in the Petition raise numerous issues that will not overlap with either a hypothetical ITC proceeding or the Texas Litigation. This favors institution. *Fintiv*, Paper 11, at 12-13; *Volkswagen Group of Am. v. Arigna Tech.*, IPR2021-01531, Paper 7, 10 (Mar. 16, 2022); *3Shape A/S v. Align Tech., Inc.*, IPR2020-00223, Paper 12, at 34 (May 26, 2020).

Moreover, because Petitioner promptly filed this Petition, neither the Texas Litigation nor the ITC Investigation (which has not even been instituted) is sufficiently developed to determine whether, and to what extent, any issues will overlap, making factor four neutral at worst. *Cast Lighting v. Wangs Alliance*, PGR2021-00012, Paper 12, 34-35 (Jun. 7, 2021).

4. *Fintiv* factor five is neutral.

Despite Petitioner being an ITC “proposed Respondent” and Texas Litigation defendant, factor five is neutral because—given Petitioner’s expeditious filing—neither proceeding is developed sufficiently to warrant denying institution. *Google v. Parus*, IPR2020-00846, Paper 9, 20-21 (Oct. 21, 2020) (factor five is neutral when it is speculative which tribunal will decide invalidity first).

5. *Fintiv* factor six favors institution.

Factor six favors institution because the Petition’s merits are strong.

Moreover, PO filed complaints against multiple potential parties in multiple venues. *See* EX1036 (ITC); EX1038 (Amphenol); EX1040 (Molex); EX1041 (TE Connectivity); EX1042 (Volex). The Board is the most efficient venue to resolve the ’233 Patent validity disputes and avoid piecemeal resolution in multiple proceedings. Since FWD will likely issue before validity determinations in any parallel proceeding the Board’s decision will preclude needlessly duplicating efforts in those forums.

* * *

Factors 1-4 and 6 favor instituting IPR while factor 5 is neutral.

Discretionary denial under *Fintiv* and Section 314(a) is unwarranted.

B. Section 325(d) Denial is Unwarranted

There is no basis for discretionary denial under Section 325(d) because both Grounds fail each step of *Advanced Bionics, LLC v. Med-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (Feb. 13, 2020) (precedential).

The Office allowed claims in a first action. The Office never considered Lugthart-706 or Gorecki-617 (Ground 1), which are not of record.⁸ EX1001, code (56); *Advanced Bionics*, 7 (“Under §325(d), the art and arguments must have been

⁸ After a first Notice of Allowance (EX1002, 107), PO filed an IDS listing a “Non Final Office Action” in a different patent application (EX1002, 138 (item 4)), wherein a different Examiner rejected different claims over U.S. Patent No. 9,337,993 (“Lugthart-993”). Neither PO nor the Office made Lugthart-993 of-record. EX1001, code (56); 37 C.F.R. §1.98(a)(1) (IDS must separately list patent reference for it to be considered); MPEP 609.05(a), form paragraph 6.49.06 (“[U]nless the references have been cited by the examiner on form PTO-892, they have not been considered.”). In a second Notice of Allowance (after repeating earlier reasons for allowance) the Examiner specifically stated that “[*n*]o new art is cited” (EX1002, 155). Lugthart-993 was therefore never presented to the Office. Because it was never presented in the ’233 Patent prosecution nothing in Lugthart-993 is relevant to the *Advanced Bionics* analysis.

previously presented to the Office during proceedings pertaining to the challenged patent.”). By allowing claims in a first action, the Office never identified a single reference that provided a substantially similar disclosure as Lugthart-706 or Gorecki-617. *Id.*, 7-8.

The Office also never considered admitted prior art IEEE Std. 802.3-2015, a secondary reference in Ground 2, in combination with Lugthart-706 or Gorecki-617 (Ground 2). *Advanced Bionics*, 7-8.

Gorecki-617 expressly teaches storing equalization filter coefficients in non-volatile memory, and setting transmit filter coefficients using those stored values to provide pre-equalization. *Supra* §§VI.B (Gorecki-617), VI.C (combination), VI.D.1.e ([1.f]). The fact that Gorecki-617 teaches the very functionality that the Examiner cited as reasons for allowing the challenged claims confirms that the Examiner never considered Gorecki-617 or any substantially similar prior art. EX1002, 113, 154. This means that the prior art in Grounds 1 and 2, which rely on combinations using Gorecki-617’s teachings, was never presented to the Office and fails *Advanced Bionics* step one. *Advanced Bionics*, 7-8.

Thus, the Office has never considered the Petition’s arguments, or any similar argument, showing that the Challenged Claims are not patentable. The Section 325(d) analysis fails *Advanced Bionics* step one and there is no basis for discretionary denial under Section 325(d).

To the extent the Board disagrees, then Grounds 1 and 2 each fail *Advanced Bionics* step two because the Examiner materially erred in allowing the Challenged Claims at least because as explained *supra* §§IV.C, VI.D.1.e ([1.f]), VI.D.7.c ([8.f]), and VI.D.12.d ([15.c]), Gorecki-617 teaches the subject matter in Limitations [1.f], [8.f], and [15.c] that the Examiner identified as missing in the prior art and a reason for allowance (EX1002, 113, 154-155). *Advanced Bionics*, 8-9. Thus, as shown above independent claims 1, 8, and 15 would have been obvious over Lugthart+Gorecki as explained *supra* §§VI.D.1 (claim 1), VI.D.7 (claim 8), and VI.D.12 (claim 15).

IX. CONCLUSION

The Board should institute review and cancel claims 1-20.

Respectfully submitted,
Amphenol Corporation

Dated: April 10, 2025

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APPENDIX A: U.S. PATENT NO. 10,877,233 CLAIM LIST

Ref	Limitation
1.PRE	A cable that comprises:
1.a	a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;
1.b	a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and
1.c	electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,
1.d	the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and
1.e	the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,
1.f	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.
2	The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.
3	The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

Ref	Limitation
4	The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.
5	The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.
6	The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.
7	The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.
8.PRE	A cable manufacturing method that comprises:
8.a	connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges multi-lane data streams with a first host interface port via the first connector plug;
8.b	connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;
8.c	connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween,
8.d	the first DRR device converting between said electrical transit signals and said multi-lane data streams for the first host interface port, and
8.e	the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port,

Ref	Limitation
8.f	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.
9	The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.
10	The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.
11	The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.
12	The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.
13	The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.
14	The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.
15.PRE	A communications method that comprises:

Ref	Limitation
15.a	inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and
15.b	inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,
15.c	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.
16.a	The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively,
16.b	each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.
17	The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.
18	The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.
19	The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

Ref	Limitation
20	The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

CERTIFICATE OF SERVICE UNDER 37 C.F.R. §42.6(e)(4)

I certify that on April 10, 2025, a copy of the foregoing document, including any exhibits or appendices filed therewith, is being served via *Overnight FedEx* at the following correspondence address of record for the patent:

Ramey LLP
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Date: April 10, 2025

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, the undersigned certifies that the foregoing Petition for *Inter Partes* Review contains 10,837 words excluding a table of contents, a table of authorities, Mandatory Notices under § 42.8, a certificate of service or word count, or appendix of exhibits or claim listing. Petitioner has relied on the word count feature of the word processing system used to create this paper in making this certification.

Date: April 10, 2025

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