

Exhibit A-2

Invalidity of U.S. Patent No. 10,877,233 (the “’233 Patent”) in View of U.S. Patent Publication No. 2017/0302431 (“Lugthart 431”)

Lugthart 431 was filed on June 30, 2017, published October 19, 2017, and claims priority to U.S. Provisional Application No. 61/982,233, filed on April 21, 2014. Lugthart 431 qualifies as prior art under at least 35 U.S.C. § 102(a) (AIA).

The Administrative Law Judge has not yet construed the claims and therefore the meaning of the terms in the claims has yet to be resolved. The support identified here for limitations of the Asserted Claims of the ’233 Patent is responsive to Complainant’s apparent infringement contentions in its Complaint, which Respondents disagree with. As such, nothing in Respondents’ claim charts should be construed as an admission regarding infringement, either literally or under the doctrine of equivalents, or as an admission regarding Respondents’ understanding of the proper scope of the Asserted Claims of the ’233 Patent.

All cross-references should be understood to include material that is cross-referenced within the cross-reference. Where a particular Figure is cited, the citation should be understood to encompass the caption and description of the Figure as well as any text relating to or describing the Figure. Conversely, where particular text referring to a Figure is cited, the citation should be understood to include the Figure as well. Respondents reserve the right to rely on additional citations or sources of evidence that also may be applicable, or that may become applicable in light of claim construction, changes in Complainant’s infringement and/or domestic industry contentions, and/or information obtained during discovery as the Investigation progresses.

To the extent Complainant alleges that Lugthart 431 does not disclose any particular limitation of the Asserted Claims of the ’233 Patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the ’233 Patent to modify Lugthart 431 and/or to combine the teachings of Lugthart 431 with other prior art references, including but not limited to the prior art references cited in the Cover Pleading and the relevant section(s) of claim charts for other prior art references for the ’233 Patent in a manner that would have rendered the Asserted Claims invalid as obvious.

Because Complainant has yet to identify any limitation of the Asserted Claims of the ’233 Patent that it contends is not fully disclosed by Lugthart 431, either alone or in combination with other prior art cited by Respondents, Respondents expressly reserve the right to rebut any such contention, including by identifying additional obviousness combinations, if any such contention is made by Complainant. Respondents further reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the Cover Pleading.

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A. INDEPENDENT CLAIM 1

Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
1[pre] A cable that comprises:	To the extent the preamble is limiting, Lugthart 431 discloses and/or renders obvious this limitation.
	<p>[0014] In a further aspect, a method of electronic communication includes receiving a first plurality of host-side signals from a host device, wherein each of the first plurality of host-side signals has a first data rate. The method can further include converting the first plurality of host-side signals into a plurality of digitized egress signals using host-side analog-to-digital converter (ADC) circuitry. The method may also include processing the plurality of digitized egress signals to generate one or more multiplexed signals using a first digital signal processor. The step of processing the plurality of digitized egress signals can include digitally conditioning the plurality of digitized egress signals and encoding the one or more multiplexed signals with a multi-level encoding. The method can additionally include converting the one or more multiplexed signals into one or more differential output signals using line-side digital-to-analog converter (DAC) circuitry. Each of the one or more differential output signals can have a second data rate greater than the first data rate. In addition, the method can include transmitting the one or more differential output signals over one or more paired differential conductors of a cable at a data rate of at least 40 Gbit/s.</p>
	Lugthart 431, ¶14.

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Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0015] According to yet another aspect, an active cable comprises a first cable comprising a first pair of conductors including a first pluggable module. The first pluggable module can include a first transceiver including host-side analog-to-digital converter (ADC) circuitry configured to receive a first plurality of host-side signals and to generate a plurality of digitized egress signals. A first host-side signal of the first plurality of host-side signals can have a first data rate. The first transceiver can further include a first digital signal processor (DSP) configured to generate one or more multiplexed signals based on multiplexing the plurality of digitized egress signals. The one or more multiplexed signals can have a multi-level encoding. The transceiver can further include line-side digital-to-analog converter (DAC) circuitry configured to convert the one or more multiplexed signals into one or more differential output signals including a first differential output signal. The line-side DAC circuitry can be configured to transmit the first differential output signal over the first pair of conductors at a second data rate that is greater than the first data rate.</p>
	<p>Lugthart 431, ¶15.</p>
	<p>[0057] A high-speed communication link can include a cable and a pair of transceivers provided at respective ends of the cable. The cable can be implemented in a wide variety of ways. For example, in certain configurations, the cable can correspond to an electrical cable including one or more pairs of differential micro coaxial cables or conductors. However, other configurations are possible, such as implementations in which the cable is implemented as an optical cable.</p>
	<p>Lugthart 431, ¶57.</p>

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Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 111 as well as first and second transceiver assemblies 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.</p>
	<p>Lugthart 431, ¶107.</p>
	<p>[0109] The first and second transceiver assemblies 105a, 105b can be implemented in a variety of ways. For example, the first and second transceiver assemblies include first and second transceivers 107a, 107b, respectively, which can be implemented using, for example, any of the embodiments of transceivers described earlier with respect to FIGS. 1A-1D.</p>
	<p>Lugthart 431, ¶109.</p>

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Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0113] Integrating transceivers into a cable can achieve a wide variety of advantages. For example, at a given bit rate, an active cable can permit communication over longer distance and/or with a thinner cable relative to a passive cable. Additionally, using an active cable can decrease jitter, noise, and/or ISI relative to a configuration using a passive cable. However, certain applications can use passive cables, for instance, to lower cable cost. For example, some passive cable configurations can be used in backplane applications.</p>
	<p>Lugthart 431, ¶113.</p>
	<p>[0121] The conducting lines 111 can include metal (e.g., copper) conductors, for example. In some implementations, the conducting lines 111 can alternatively or additionally include one or more other types of conductors, such as one or more optical fibers that can transport optical signals. As indicated, the conducting lines 111 in alternative embodiments are not housed within a cable, and can instead reside on a PCB or other substrate.</p>
	<p>Lugthart 431, ¶121.</p>
	<p>[0122] The conducting lines 111 can include one or more sets of paired lines configured for differential signaling, which in some implementations include one or more sets of paired micro coaxial cables. However, other types of conducting lines 111 are possible. For example, shielded or unshielded twisted pair cables can be used in addition to any other appropriate type of cables, such as those that can support different data and video protocols (e.g., Serial ATA, Infiniband, PCI Express, DisplayPort I/O protocols, gigabit Ethernet, etc.).</p>
	<p>Lugthart 431, ¶122.</p>

Claim 1

U.S. 2017/0302431 (“Lugthart 431”)

[0125] In various implementations, the cable **110** of FIG. 2A and/or the cable **115** of FIG. 2B can be configured to transport data rates greater than 10 Gbit/s (e.g., 20 Gbit/s, 25 Gbit/s, 28 Gbit/s, 32 Gbit/s, 40 Gbit/s, 50 Gbit/s, 56 Gbit/s, 64 Gbit/s, 100 Gbit/s, 112 Gbit/s, 128 Gbit/s, 200 Gbit/s, 224 Gbit/s, 256 Gbit/s, 400 Gbit/s, and 448 Gbit/s or greater than any of these amounts, or rates between any of the foregoing values, etc.). In various implementations, the cable can have a length between about 0.5 m to about 10 m, for example, a length of about 2 m, about 3 m, about 4 m, about 5 m, about 6 m, about 7 m, about 9 m, or a length between the foregoing values, etc. In other implementations, the cable has a length greater than 10 m, for example, a length of about 10-15 m, about 15-20 m, about 20-30 m, about 30-50 m, about 50-100 m, or lengths between the foregoing, etc. In some embodiments, the cable **110** has a length of greater than 100 m. Thus, the length of the cable **110** of FIG. 2A and/or the cable **115** of FIG. 2B can depend on a variety of factors, including, for example, application, communication speed, signaling protocols, and/or operating environment.

Lugthart 431, ¶125.

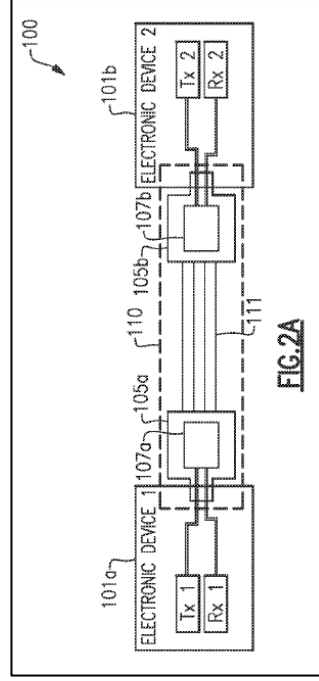


FIG. 2A

Lugthart 431, Figure 2A.

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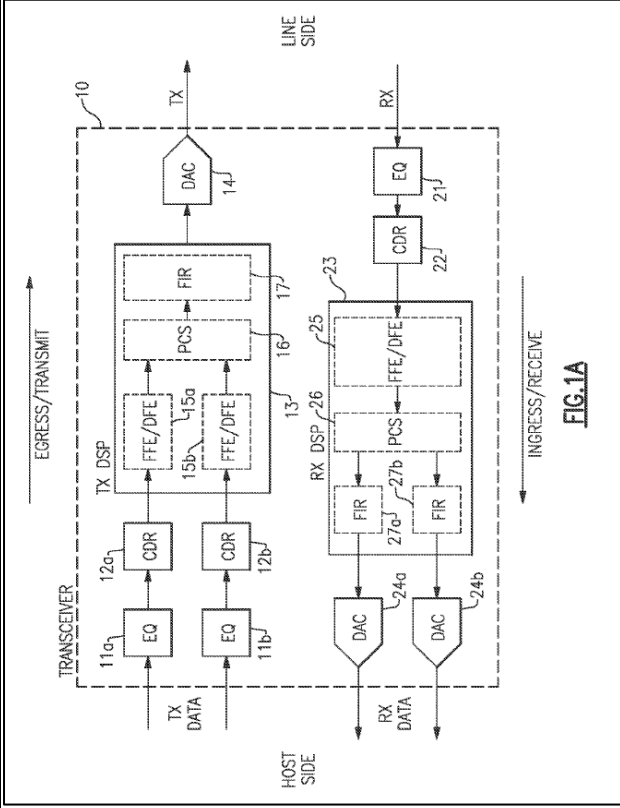
Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
<p>1 [a] a first data recovery and remodulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;</p>	<p>To the extent that this preamble is not disclosed, either explicitly or inherently, by Lugthart 431, this preamble is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>1 [a] a first data recovery and remodulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="638 789 1094 1465" style="border: 1px solid black; padding: 5px;"> <p>[0058] In certain configurations, the transceivers can implement a serializer/deserializer (SerDes) function. For example, in certain implementations each transceiver can be a full duplex multiplexer and re-timer capable of receiving multiple (e.g., 2, 4, or more) signals from a host via a host-side interface. The transceiver multiplexes the received signals for transmission via a line-side interface over the cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved via multi-level modulation encoding, for example. In one non-limiting embodiment, each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable.</p> </div> <p>Lugthart 431, ¶58.</p>

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Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0059] The transceiver can also be configurable in different operational modes. For instance, depending on the mode, the transceiver can handle different numbers of host-side data streams having variable data rates. In one embodiment, the transceiver operates in a first operational mode to translate two host-side 20 Gbit/s NRZ data streams into a single PAM-4 40 Gbit/s stream on the line side, and vice versa. In a second operational mode, the transceiver translates four host-side 10 Gbps NRZ data streams into a single PAM-4 40 Gbit/s stream on the line-side, and vice versa. Such flexibility allows the transceiver to be employed in a variety of different contexts, such as in both consumer and data center contexts.</p>
	<p>Lugthart 431, ¶59.</p>
	<p>[0060] The transceiver in some embodiments includes a timing recovery circuit including a digital clock recovery path having a dedicated, relatively low latency and/or low power analog-to-digital converter (ADC). The data path can include a separate ADC having more bits than the ADC included in the clock recovery path. Different filtering can be used in the clock and data paths. Moreover, the digital output from the clock recovery path can be used to drive a digitally controlled oscillator (DCO) rather than implementing an analog phase-locked loop (PLL), further reducing latency.</p>
	<p>Lugthart 431, ¶60.</p>

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Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0063] FIG. 1A is a schematic diagram of one example of a transceiver 10. The transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b.</p> <p>Lugthart 431, ¶63.</p>
	<p>[0065] As shown in FIG. 1A, the first and second transmit path equalizers 11a, 11b include inputs that receive host side transmit data (TX DATA) and outputs electrically connected to inputs of the first and second transmit path CDR circuits 12a, 12b, respectively. The first and second transmit path CDR circuits 12a, 12b further include outputs electrically connected to inputs of the transmit path DSP 13. The transmit path DAC 14 includes an input electrically connected to an output of the transmit path DSP 13 and an output that generates a line side transmit signal (TX). The receive path equalizer 21 includes an input that receives a line side receive signal (RX), and an output electrically connected to an input of the receive path CDR circuit 22. The receive path CDR circuit 22 further includes an output electrically connected to an input of the receive path DSP 23. The receive path DSP 23 further includes outputs electrically connected to inputs of the first and second receive path DACs 24a, 24b. The first and second receive path DACs 24a, 24b further include outputs that generate host side receive data (RX DATA).</p> <p>Lugthart 431, ¶65.</p>



Lugthart 431, Figure 1A.

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Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0067] In certain configurations, the transceiver 10 can implement a serializer/deserializer (SerDes) function or operation. For example, in one embodiment, the transceiver 10 can operate as a full duplex multiplexer and re-timer capable of receiving multiple (for example, 2, 4, or more) signals from a host via a host-side interface. Additionally, the transceiver 10 can multiplex the received host-side transmit signals for transmission via a line-side interface over a cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved, for example, via multi-level modulation encoding. In one non-limiting example, an egress/transmit path of the transceiver 10 is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals on the host side and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission to the line side over the cable. Conversely, an ingress/receive path of the transceiver in such an example is capable of receiving a single 40 Gbit/s PAM-4 signal on the line side and de-multiplexing this signal into dual 20 Gbit/s NRZ signals for communication to the host side.</p>
	<p>Lugthart 431, ¶67.</p>

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Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0068] FIG. 1A illustrates the host side transmit data as including two signals and the line side transmit data as including one signal (e.g., via a multiplexing operation), and illustrates the line side receive data as including one signal and the host side receive data as including two signals (via a de-multiplexing operation). However, other configurations are possible, including configurations with additional signals on the host side and/or line side. For example, the first and second receive path DACs 24a, 24b can be replicated in parallel to include, for instance, 10, 20, or 40 or more DACs to provide wider RX DATA bandwidth. Similarly, the first and second transmit path equalizers 11a, 11b and the first and second transmit path CDR circuits 12a, 12b can be replicated in provide wider TX DATA bandwidth. In such configurations, different multiplexing, de-multiplexing, and/or modulation formats can be employed, as appropriate.</p> <p>Lugthart 431, ¶68.</p>

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Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.</p> <p>Lugthart 431, ¶72.</p>

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Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0116] In various implementations, the packaging can have a design and a form factor similar to the packaging defined by an existing interface standard (e.g., Thunderbolt Gen1/Gen2 or USB 2.0/3.0), although the packaging can have some other form factor. The packaging can comprise materials suitable for electronic and computer interfaces, such as plastic, metal or a composite material. Each of the transceiver assemblies 105a and 105b has an input port that is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b, and an output port that is connected to the cable. The input port can include a connector similar to connectors of existing interface standards, including, but not limited to, Thunderbolt, USB 2.0/3.0, small form-factor pluggable (SFP), enhanced small form-factor pluggable (SFP+), and/or quad small form-factor pluggable (QSFP).</p> <p>Lugthart 431, ¶116.</p> <p>[0118] In certain embodiments, the transceiver assemblies 105a and 105b implement an egress path by: (a) receiving at least two differential signals from a host device; (b) digitally re-timing, conditioning, and multiplexing the received differential signals; and (c) transmitting the multiplexed signal as a multi-level modulated signal (e.g., PAM-4) over the cable.</p> <p>Lugthart 431, ¶118.</p>

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Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0119] In certain embodiments, the transceiver assemblies are further configured to implement an ingress path by: (a) receiving a multi-level modulated signal (e.g., PAM-4) from the cable; (b) digitally conditioning and de-multiplexing the received multi-level modulated signal; and (c) transmitting the de-multiplexed signals as an analog signal to the host device.</p> <p>Lugthart 431, ¶119.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>1[b] a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p>

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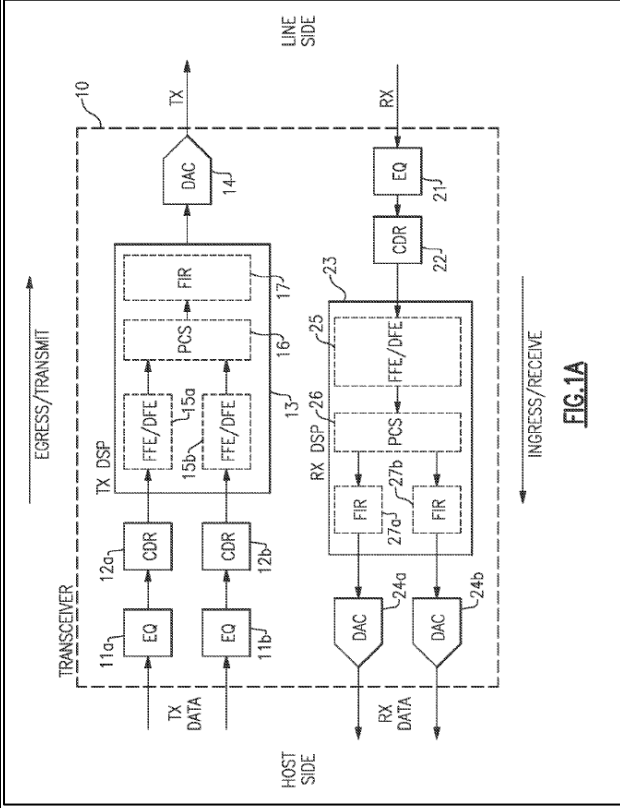
Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0058] In certain configurations, the transceivers can implement a serializer/deserializer (SerDes) function. For example, in certain implementations each transceiver can be a full duplex multiplexer and re-timer capable of receiving multiple (e.g., 2, 4, or more) signals from a host via a host-side interface. The transceiver multiplexes the received signals for transmission via a line-side interface over the cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved via multi-level modulation encoding, for example. In one non-limiting embodiment, each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable.</p>
	<p>Lugthart 431, ¶58.</p>
	<p>[0059] The transceiver can also be configurable in different operational modes. For instance, depending on the mode, the transceiver can handle different numbers of host-side data streams having variable data rates. In one embodiment, the transceiver operates in a first operational mode to translate two host-side 20 Gbit/s NRZ data streams into a single PAM-4 40 Gbit/s stream on the line side, and vice versa. In a second operational mode, the transceiver translates four host-side 10 Gbps NRZ data streams into a single PAM-4 40 Gbit/s stream on the line-side, and vice versa. Such flexibility allows the transceiver to be employed in a variety of different contexts, such as in both consumer and data center contexts.</p>
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	<p>[0060] The transceiver in some embodiments includes a timing recovery circuit including a digital clock recovery path having a dedicated, relatively low latency and/or low power analog-to-digital converter (ADC). The data path can include a separate ADC having more bits than the ADC included in the clock recovery path. Different filtering can be used in the clock and data paths. Moreover, the digital output from the clock recovery path can be used to drive a digitally controlled oscillator (DCO) rather than implementing an analog phase-locked loop (PLL), further reducing latency.</p>
	<p>Lugthart 431, ¶60.</p>
	<p>[0063] FIG. 1A is a schematic diagram of one example of a transceiver 10. The transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b.</p>
	<p>Lugthart 431, ¶63.</p>

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	<p>[0065] As shown in FIG. 1A, the first and second transmit path equalizers 11a, 11b include inputs that receive host side transmit data (TX DATA) and outputs electrically connected to inputs of the first and second transmit path CDR circuits 12a, 12b, respectively. The first and second transmit path CDR circuits 12a, 12b further include outputs electrically connected to inputs of the transmit path DSP 13. The transmit path DAC 14 includes an input electrically connected to an output of the transmit path DSP 13 and an output that generates a line side transmit signal (TX). The receive path equalizer 21 includes an input that receives a line side receive signal (RX), and an output electrically connected to an input of the receive path CDR circuit 22. The receive path CDR circuit 22 further includes an output electrically connected to an input of the receive path DSP 23. The receive path DSP 23 further includes outputs electrically connected to inputs of the first and second receive path DACs 24a, 24b. The first and second receive path DACs 24a, 24b further include outputs that generate host side receive data (RX DATA).</p> <p>Lugthart 431, ¶65.</p>



Lugthart 431, Figure 1A.

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	<p>Lugthart 431, ¶67.</p>

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	<p>[0068] FIG. 1A illustrates the host side transmit data as including two signals and the line side transmit data as including one signal (e.g., via a multiplexing operation), and illustrates the line side receive data as including one signal and the host side receive data as including two signals (via a de-multiplexing operation). However, other configurations are possible, including configurations with additional signals on the host side and/or line side. For example, the first and second receive path DACs 24a, 24b can be replicated in parallel to include, for instance, 10, 20, or 40 or more DACs to provide wider RX DATA bandwidth. Similarly, the first and second transmit path equalizers 11a, 11b and the first and second transmit path CDR circuits 12a, 12b can be replicated in provide wider TX DATA bandwidth. In such configurations, different multiplexing, de-multiplexing, and/or modulation formats can be employed, as appropriate.</p> <p>Lugthart 431, ¶68.</p>

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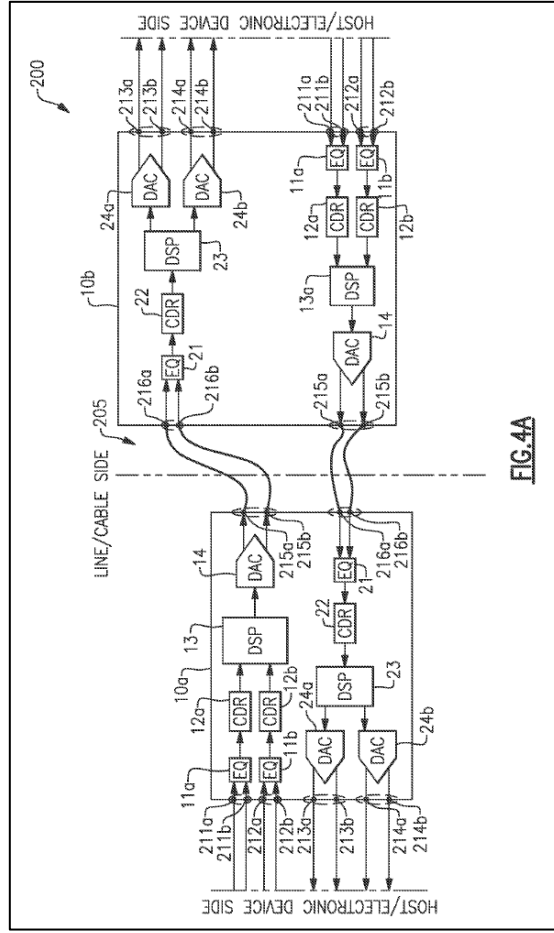
Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0116] In various implementations, the packaging can have a design and a form factor similar to the packaging defined by an existing interface standard (e.g., Thunderbolt Gen1/Gen2 or USB 2.0/3.0), although the packaging can have some other form factor. The packaging can comprise materials suitable for electronic and computer interfaces, such as plastic, metal or a composite material. Each of the transceiver assemblies 105a and 105b has an input port that is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b, and an output port that is connected to the cable. The input port can include a connector similar to connectors of existing interface standards, including, but not limited to, Thunderbolt, USB 2.0/3.0, small form-factor pluggable (SFP), enhanced small form-factor pluggable (SFP+), and/or quad small form-factor pluggable (QSFP).</p> <p>Lugthart 431, ¶116.</p> <p>[0118] In certain embodiments, the transceiver assemblies 105a and 105b implement an egress path by: (a) receiving at least two differential signals from a host device; (b) digitally re-timing, conditioning, and multiplexing the received differential signals; and (c) transmitting the multiplexed signal as a multi-level modulated signal (e.g., PAM-4) over the cable.</p> <p>Lugthart 431, ¶118.</p>

Claim 1

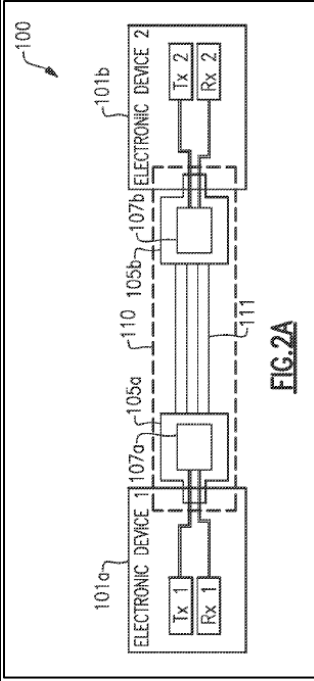
U.S. 2017/0302431 (“Lugthart 431”)

[0119] In certain embodiments, the transceiver assemblies are further configured to implement an ingress path by: (a) receiving a multi-level modulated signal (e.g., PAM-4) from the cable; (b) digitally conditioning and de-multiplexing the received multi-level modulated signal; and (c) transmitting the de-multiplexed signals as an analog signal to the host device.

Lugthart 431, ¶119.



Lugthart 431, Figure 4A.



Lugthart 431, Figure 2A.

[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 111 as well as first and second transceiver assemblies 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.

Lugthart 431, ¶107.

Exhibit A-2

Claim 1

U.S. 2017/0302431 (“Lugthart 431”)

[0143] FIG. 4A illustrates an example of a communication system 200 including a first transceiver 10a connected to another similar transceiver 10b by a cable 205. The first and second transceivers 10a, 10b are implemented in a manner similar to that of the transceiver 10 of FIG. 1A, with differential signaling used on the host and line sides of the transceivers.

Lugthart 431, ¶143.

[0144] Although the communication system 200 of FIG. 2A is shown as including transceivers similar to the transceiver 10 of FIG. 1A, other configurations are possible. For example, any of the transceivers shown in FIGS. 1A-1D can communicate with one another over a cable.

Lugthart 431, ¶144.

[0145] As shown in FIG. 4A, the first and second transceivers 10a, 10b have a host side for facing an electronic device and a line side for facing the cable 205. For example, with reference back to FIG. 2A, the first transceiver 10a can communicate with a first electronic device 101a and the second transceiver 10b can communicate with a second electronic device 101b. Thus, the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable 205 and an ingress path configured to transport signals from the cable 205 to the electronic device. For example, the first transceiver 10a includes an egress path for transmitting signals from a first electronic device to the cable 205 and an ingress path for providing signals received over the cable 205 to the first electronic device. Similarly, the second transceiver 10b includes an egress path for transmitting signals from a

Lugthart 431, ¶145.

Exhibit A-2

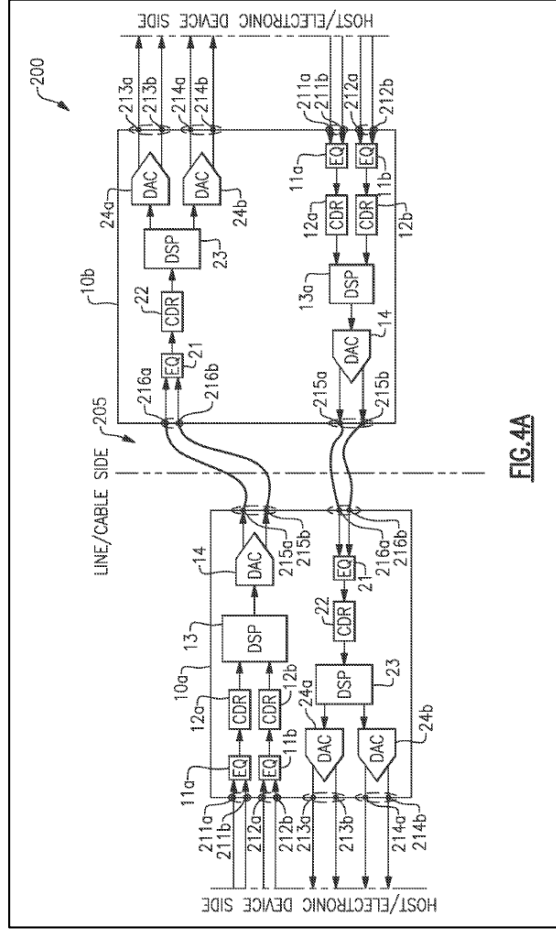
Claim 1

U.S. 2017/0302431 (“Lugthart 431”)

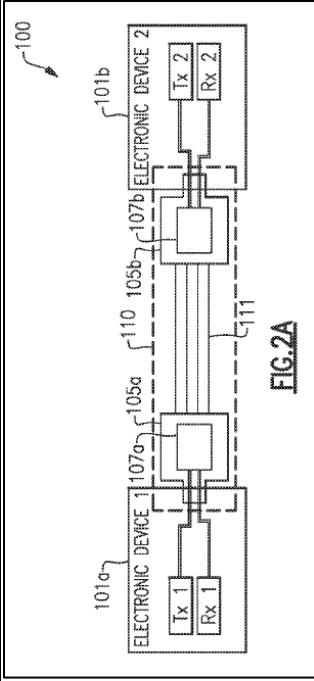
To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

1[c] electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,

Lugthart 431 discloses and/or renders obvious this limitation.



Lugthart 431, Figure 4A.



Lugthart 431, Figure 2A.

[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 105b. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.

Lugthart 431, ¶107.

Exhibit A-2

Claim 1

U.S. 2017/0302431 (“Lugthart 431”)

[0143] FIG. 4A illustrates an example of a communication system 200 including a first transceiver 10a connected to another similar transceiver 10b by a cable 205. The first and second transceivers 10a, 10b are implemented in a manner similar to that of the transceiver 10 of FIG. 1A, with differential signaling used on the host and line sides of the transceivers.

Lugthart 431, ¶143.

[0144] Although the communication system 200 of FIG. 2A is shown as including transceivers similar to the transceiver 10 of FIG. 1A, other configurations are possible. For example, any of the transceivers shown in FIGS. 1A-1D can communicate with one another over a cable.

Lugthart 431, ¶144.

[0145] As shown in FIG. 4A, the first and second transceivers 10a, 10b have a host side for facing an electronic device and a line side for facing the cable 205. For example, with reference back to FIG. 2A, the first transceiver 10a can communicate with a first electronic device 101a and the second transceiver 10b can communicate with a second electronic device 101b. Thus, the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable 205 and an ingress path configured to transport signals from the cable 205 to the electronic device. For example, the first transceiver 10a includes an egress path for transmitting signals from a first electronic device to the cable 205 and an ingress path for providing signals received over the cable 205 to the first electronic device. Similarly, the second transceiver 10b includes an egress path for transmitting signals from a

Lugthart 431, ¶145.

Exhibit A-2

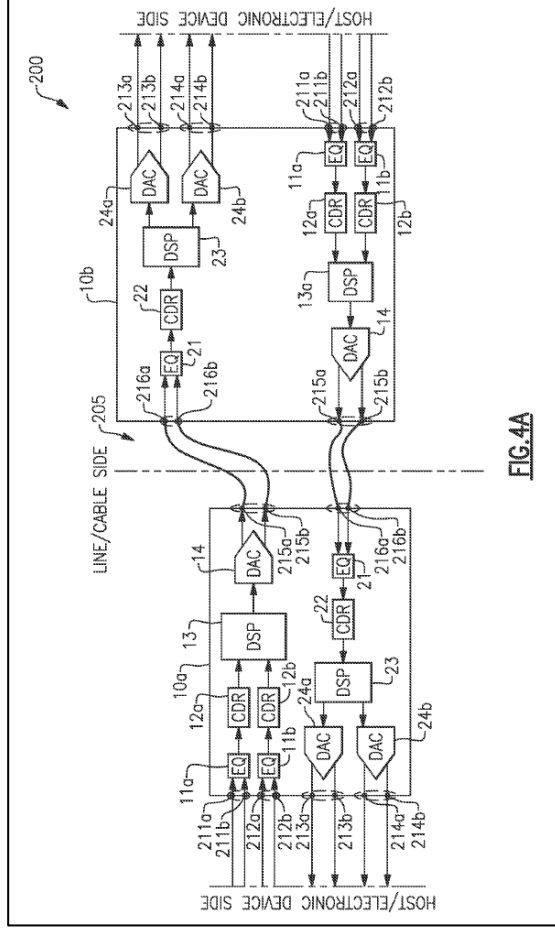
Claim 1

U.S. 2017/0302431 (“Lugthart 431”)

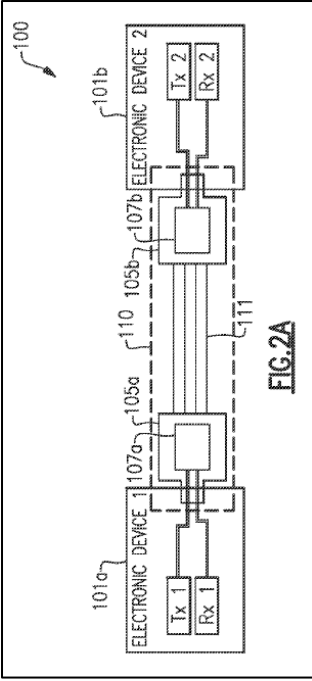
To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

1[d] the first DRR device converting between said electrical transit signals and said inbound and outbound multilane data streams for the first host interface port, and

Lugthart 431 discloses and/or renders obvious this limitation.



Lugthart 431, Figure 4A.



Lugthart 431, Figure 2A.

[0065] As shown in FIG. 1A, the first and second transmit path equalizers 11a, 11b include inputs that receive host side transmit data (TX DATA) and outputs electrically connected to inputs of the first and second transmit path CDR circuits 12a, 12b, respectively. The first and second transmit path CDR circuits 12a, 12b further include outputs electrically connected to inputs of the transmit path DSP 13. The transmit path DAC 14 includes an input electrically connected to an output of the transmit path DSP 13 and an output that generates a line side transmit signal (TX). The receive path equalizer 21 includes an input that receives a line side receive signal (RX), and an output electrically connected to an input of the receive path CDR circuit 22. The receive path CDR circuit 22 further includes an output electrically connected to an input of the receive path DSP 23. The receive path DSP 23 further includes outputs electrically connected to inputs of the first and second receive path DACs 24a, 24b. The first and second receive path DACs 24a, 24b further include outputs that generate host side receive data (RX DATA).

Lugthart 431, ¶65.

Exhibit A-2

Claim 1

U.S. 2017/0302431 (“Lugthart 431”)

[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 111 as well as first and second transceiver assemblies 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.

Lugthart 431, ¶107.

[0143] FIG. 4A illustrates an example of a communication system 200 including a first transceiver 10a connected to another similar transceiver 10b by a cable 205. The first and second transceivers 10a, 10b are implemented in a manner similar to that of the transceiver 10 of FIG. 1A, with differential signaling used on the host and line sides of the transceivers.

Lugthart 431, ¶143.

[0144] Although the communication system 200 of FIG. 2A is shown as including transceivers similar to the transceiver 10 of FIG. 1A, other configurations are possible. For example, any of the transceivers shown in FIGS. 1A-1D can communicate with one another over a cable.

Lugthart 431, ¶144.

Exhibit A-2

U.S. 2017/0302431 (“Lugthart 431”)	
Claim 1	<p>[0145] As shown in FIG. 4A, the first and second transceivers 10a, 10b have a host side for facing an electronic device and a line side for facing the cable 205. For example, with reference back to FIG. 2A, the first transceiver 10a can communicate with a first electronic device 101a and the second transceiver 10b can communicate with a second electronic device 101b. Thus, the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable 205 and an ingress path configured to transport signals from the cable 205 to the electronic device. For example, the first transceiver 10a includes an egress path for transmitting signals from a first electronic device to the cable 205 and an ingress path for providing signals received over the cable 205 to the first electronic device. Similarly, the second transceiver 10b includes an egress path for transmitting signals from a</p> <p>Lugthart 431, ¶145.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
1[e] the second DRR device converting between said electrical transit signals and said inbound and outbound multilane data streams for the second host interface port,	Lugthart 431 discloses and/or renders obvious this limitation.

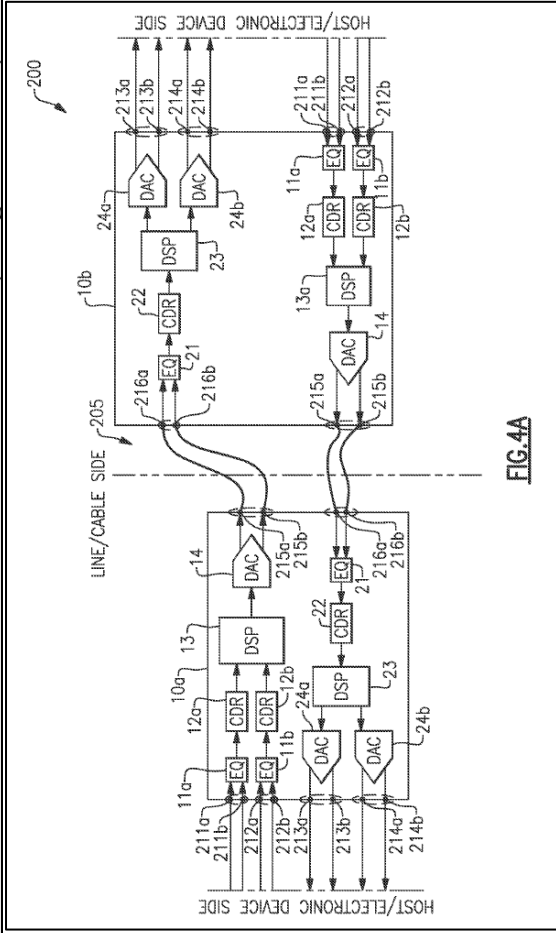


FIG. 4A

Lugthart 431, Figure 4A.

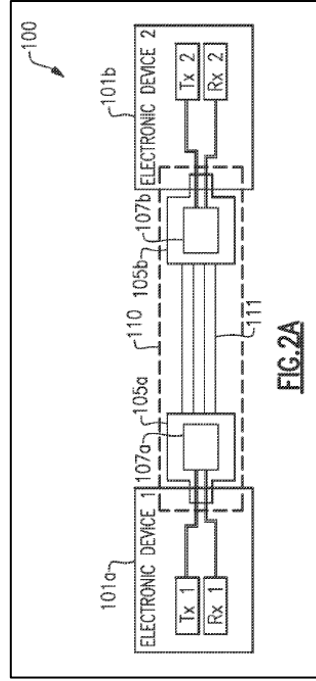


FIG. 2A

Lugthart 431, Figure 2A.

Exhibit A-2

Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0065] As shown in FIG. 1A, the first and second transmit path equalizers 11a, 11b include inputs that receive host side transmit data (TX DATA) and outputs electrically connected to inputs of the first and second transmit path CDR circuits 12a, 12b, respectively. The first and second transmit path CDR circuits 12a, 12b further include outputs electrically connected to inputs of the transmit path DSP 13. The transmit path DAC 14 includes an input electrically connected to an output of the transmit path DSP 13 and an output that generates a line side transmit signal (TX). The receive path equalizer 21 includes an input that receives a line side receive signal (RX), and an output electrically connected to an input of the receive path CDR circuit 22. The receive path CDR circuit 22 further includes an output electrically connected to an input of the receive path DSP 23. The receive path DSP 23 further includes outputs electrically connected to inputs of the first and second receive path DACs 24a, 24b. The first and second receive path DACs 24a, 24b further include outputs that generate host side receive data (RX DATA).</p> <p>Lugthart 431, ¶65.</p>

Exhibit A-2

Claim 1

U.S. 2017/0302431 (“Lugthart 431”)

[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 111 as well as first and second transceiver assemblies 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.

Lugthart 431, ¶107.

[0143] FIG. 4A illustrates an example of a communication system 200 including a first transceiver 10a connected to another similar transceiver 10b by a cable 205. The first and second transceivers 10a, 10b are implemented in a manner similar to that of the transceiver 10 of FIG. 1A, with differential signaling used on the host and line sides of the transceivers.

Lugthart 431, ¶143.

[0144] Although the communication system 200 of FIG. 2A is shown as including transceivers similar to the transceiver 10 of FIG. 1A, other configurations are possible. For example, any of the transceivers shown in FIGS. 1A-1D can communicate with one another over a cable.

Lugthart 431, ¶144.

Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>[0145] As shown in FIG. 4A, the first and second transceivers 10a, 10b have a host side for facing an electronic device and a line side for facing the cable 205. For example, with reference back to FIG. 2A, the first transceiver 10a can communicate with a first electronic device 101a and the second transceiver 10b can communicate with a second electronic device 101b. Thus, the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable 205 and an ingress path configured to transport signals from the cable 205 to the electronic device. For example, the first transceiver 10a includes an egress path for transmitting signals from a first electronic device to the cable 205 and an ingress path for providing signals received over the cable 205 to the first electronic device. Similarly, the second transceiver 10b includes an egress path for transmitting signals from a</p> <p>Lugthart 431, ¶145.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>1[f] the first and second DRR devices providing preequalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p>

Exhibit A-2

Claim 1

U.S. 2017/0302431 (“Lugthart 431”)

[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.

Lugthart 431, ¶71.

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Exhibit A-2

Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	<p>Lugthart 431, ¶72.</p> <p>[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.</p> <p>Lugthart 431, ¶172.</p> <p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>

Exhibit A-2

<p>Claim 1</p>	<p>U.S. 2017/0302431 (“Lugthart 431”)</p>
<p>[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.</p> <p>Lugthart 431, ¶344.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of</p>	

Exhibit A-2

Claim 1	U.S. 2017/0302431 (“Lugthart 431”)
	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

B. DEPENDENT CLAIM 2

<p>Claim 2</p> <p>2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="418 764 850 1436" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>
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Exhibit A-2

Claim 2

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

Exhibit A-2

Claim 2	
	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>

Exhibit A-2

Claim 2

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

Exhibit A-2

Claim 2	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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C. DEPENDENT CLAIM 3

<p>Claim 3</p> <p>3. The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div style="border: 1px solid black; padding: 5px; margin: 10px 0;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>
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Exhibit A-2

Claim 3

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

Exhibit A-2

Claim 3	
	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>

Exhibit A-2

Claim 3

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

Exhibit A-2

Claim 3	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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D. DEPENDENT CLAIM 4

<p>Claim 4</p> <p>4. The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="418 764 850 1436" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>
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Exhibit A-2

Claim 4

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

Exhibit A-2

Claim 4	
	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>

Exhibit A-2

Claim 4

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

Exhibit A-2

Claim 4	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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DEPENDENT CLAIM 5

Claim 5	<p>5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.</p>
	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p>
	<div style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>

Exhibit A-2

Claim 5

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

Exhibit A-2

Claim 5	
	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>

Exhibit A-2

Claim 5

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

Exhibit A-2

Claim 5	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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Exhibit A-2

E. DEPENDENT CLAIM 6

Claim 6

6. The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.

Lugthart 431 discloses and/or renders obvious this limitation.

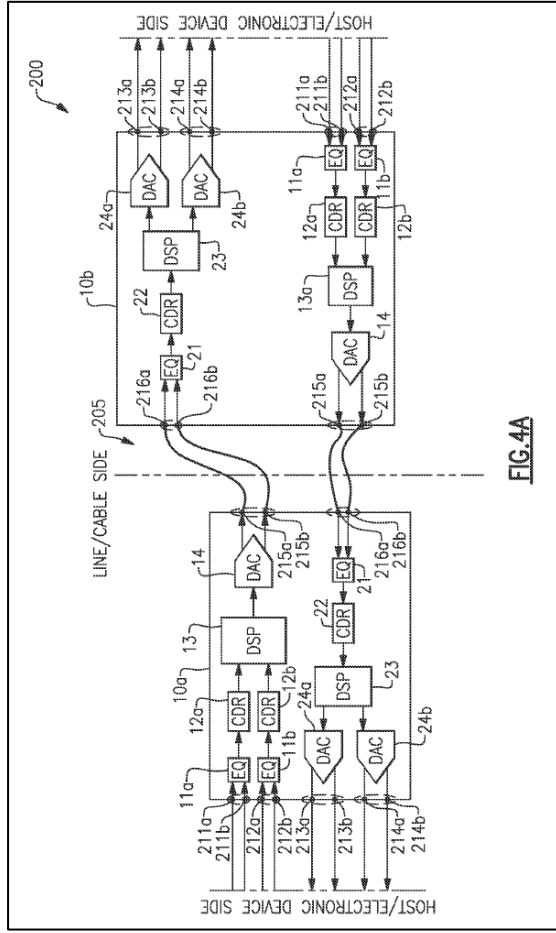


FIG. 4A

Lugthart 431, Figure 4A.

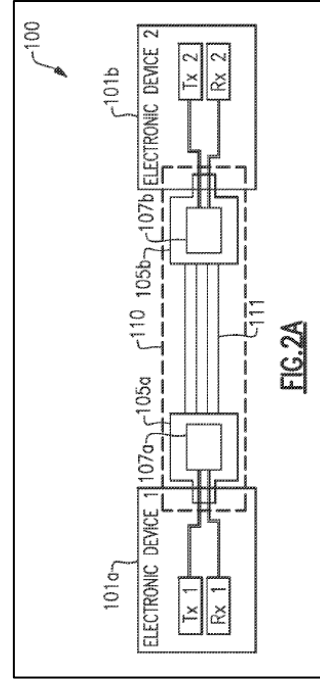


FIG. 2A

<p>Claim 6</p>	<p>Lugthart 431, Figure 2A.</p> <p>[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 111 as well as first and second transceiver assemblies 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.</p> <p>Lugthart 431, ¶107.</p> <p>[0143] FIG. 4A illustrates an example of a communication system 200 including a first transceiver 10a connected to another similar transceiver 10b by a cable 205. The first and second transceivers 10a, 10b are implemented in a manner similar to that of the transceiver 10 of FIG. 1A, with differential signaling used on the host and line sides of the transceivers.</p> <p>Lugthart 431, ¶143.</p> <p>[0144] Although the communication system 200 of FIG. 2A is shown as including transceivers similar to the transceiver 10 of FIG. 1A, other configurations are possible. For example, any of the transceivers shown in FIGS. 1A-1D can communicate with one another over a cable.</p>
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<p>Claim 6</p>	<p>Lugthart 431, ¶144.</p> <div style="border: 1px solid black; padding: 5px;"> <p>[0145] As shown in FIG. 4A, the first and second transceivers 10a, 10b have a host side for facing an electronic device and a line side for facing the cable 205. For example, with reference back to FIG. 2A, the first transceiver 10a can communicate with a first electronic device 101a and the second transceiver 10b can communicate with a second electronic device 101b. Thus, the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable 205 and an ingress path configured to transport signals from the cable 205 to the electronic device. For example, the first transceiver 10a includes an egress path for transmitting signals from a first electronic device to the cable 205 and an ingress path for providing signals received over the cable 205 to the first electronic device. Similarly, the second transceiver 10b includes an egress path for transmitting signals from a</p> </div> <p>Lugthart 431, ¶145.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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F. DEPENDENT CLAIM 7

<p>Claim 7</p> <p>7. The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="418 764 850 1436" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>
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Exhibit A-2

Claim 7

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

Exhibit A-2

Claim 7	
	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>

Exhibit A-2

Claim 7

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

Exhibit A-2

Claim 7	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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G. INDEPENDENT CLAIM 8

Claim 8

8[pre] A cable manufacturing method that comprises:

To the extent the preamble is limiting, Lugthart 431 discloses and/or renders obvious this limitation.

[0014] In a further aspect, a method of electronic communication includes receiving a first plurality of host-side signals from a host device, wherein each of the first plurality of host-side signals has a first data rate. The method can further include converting the first plurality of host-side signals into a plurality of digitized egress signals using host-side analog-to-digital converter (ADC) circuitry. The method may also include processing the plurality of digitized egress signals to generate one or more multiplexed signals using a first digital signal processor. The step of processing the plurality of digitized egress signals can include digitally conditioning the plurality of digitized egress signals and encoding the one or more multiplexed signals with a multi-level encoding. The method can additionally include converting the one or more multiplexed signals into one or more differential output signals using line-side digital-to-analog converter (DAC) circuitry. Each of the one or more differential output signals can have a second data rate greater than the first data rate. In addition, the method can include transmitting the one or more differential output signals over one or more paired differential conductors of a cable at a data rate of at least 40 Gbit/s.

Lugthart 431, ¶14.

Exhibit A-2

Claim 8

[0015] According to yet another aspect, an active cable comprises a first cable comprising a first pair of conductors including a first pluggable module. The first pluggable module can include a first transceiver including host-side analog-to-digital converter (ADC) circuitry configured to receive a first plurality of host-side signals and to generate a plurality of digitized egress signals. A first host-side signal of the first plurality of host-side signals can have a first data rate. The first transceiver can further include a first digital signal processor (DSP) configured to generate one or more multiplexed signals based on multiplexing the plurality of digitized egress signals. The one or more multiplexed signals can have a multi-level encoding. The transceiver can further include line-side digital-to-analog converter (DAC) circuitry configured to convert the one or more multiplexed signals into one or more differential output signals including a first differential output signal. The line-side DAC circuitry can be configured to transmit the first differential output signal over the first pair of conductors at a second data rate that is greater than the first data rate.

Lugthart 431, ¶15.

[0057] A high-speed communication link can include a cable and a pair of transceivers provided at respective ends of the cable. The cable can be implemented in a wide variety of ways. For example, in certain configurations, the cable can correspond to an electrical cable including one or more pairs of differential micro coaxial cables or conductors. However, other configurations are possible, such as implementations in which the cable is implemented as an optical cable.

Lugthart 431, ¶57.

Exhibit A-2

<p>Claim 8</p>	<p>[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 111 as well as first and second transceiver assemblies 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.</p> <p>Lugthart 431, ¶107.</p> <p>[0109] The first and second transceiver assemblies 105a, 105b can be implemented in a variety of ways. For example, the first and second transceiver assemblies include first and second transceivers 107a, 107b, respectively, which can be implemented using, for example, any of the embodiments of transceivers described earlier with respect to FIGS. 1A-1D.</p> <p>Lugthart 431, ¶109.</p>
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Exhibit A-2

Claim 8	
	<p>[0113] Integrating transceivers into a cable can achieve a wide variety of advantages. For example, at a given bit rate, an active cable can permit communication over longer distance and/or with a thinner cable relative to a passive cable. Additionally, using an active cable can decrease jitter, noise, and/or ISI relative to a configuration using a passive cable. However, certain applications can use passive cables, for instance, to lower cable cost. For example, some passive cable configurations can be used in backplane applications.</p> <p>Lugthart 431, ¶113.</p>
	<p>[0121] The conducting lines 111 can include metal (e.g., copper) conductors, for example. In some implementations, the conducting lines 111 can alternatively or additionally include one or more other types of conductors, such as one or more optical fibers that can transport optical signals. As indicated, the conducting lines 111 in alternative embodiments are not housed within a cable, and can instead reside on a PCB or other substrate.</p> <p>Lugthart 431, ¶121.</p>
	<p>[0122] The conducting lines 111 can include one or more sets of paired lines configured for differential signaling, which in some implementations include one or more sets of paired micro coaxial cables. However, other types of conducting lines 111 are possible. For example, shielded or unshielded twisted pair cables can be used in addition to any other appropriate type of cables, such as those that can support different data and video protocols (e.g., Serial ATA, Infiniband, PCI Express, DisplayPort I/O protocols, gigabit Ethernet, etc.).</p> <p>Lugthart 431, ¶122.</p>

Exhibit A-2

Claim 8

[0125] In various implementations, the cable **110** of FIG. 2A and/or the cable **115** of FIG. 2B can be configured to transport data rates greater than 10 Gbit/s (e.g., 20 Gbit/s, 25 Gbit/s, 28 Gbit/s, 32 Gbit/s, 40 Gbit/s, 50 Gbit/s, 56 Gbit/s, 64 Gbit/s, 100 Gbit/s, 112 Gbit/s, 128 Gbit/s, 200 Gbit/s, 224 Gbit/s, 256 Gbit/s, 400 Gbit/s, and 448 Gbit/s or greater than any of these amounts, or rates between any of the foregoing values, etc.). In various implementations, the cable can have a length between about 0.5 m to about 10 m, for example, a length of about 2 m, about 3 m, about 4 m, about 5 m, about 6 m, about 7 m, about 9 m, or a length between the foregoing values, etc. In other implementations, the cable has a length greater than 10 m, for example, a length of about 10-15 m, about 15-20 m, about 20-30 m, about 30-50 m, about 50-100 m, or lengths between the foregoing, etc. In some embodiments, the cable **110** has a length of greater than 100 m. Thus, the length of the cable **110** of FIG. 2A and/or the cable **115** of FIG. 2B can depend on a variety of factors, including, for example, application, communication speed, signaling protocols, and/or operating environment.

Lugthart 431, ¶125.

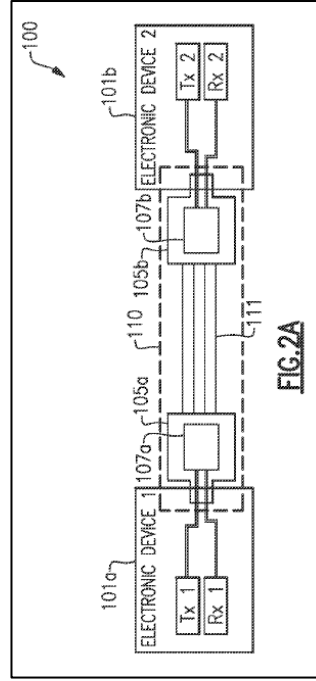


FIG. 2A

Lugthart 431, Figure 2A.

Exhibit A-2

<p>Claim 8</p>	<p>To the extent that this preamble is not disclosed, either explicitly or inherently, by Lughart 431, this preamble is obvious to a person of ordinary skill in the art based on (1) Lughart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>8[a] connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges multi-lane data streams with a first host interface port via the first connector plug;</p>	<p>Lughart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="638 789 1094 1467" style="border: 1px solid black; padding: 5px;"> <p>[0058] In certain configurations, the transceivers can implement a serializer/deserializer (SerDes) function. For example, in certain implementations each transceiver can be a full duplex multiplexer and re-timer capable of receiving multiple (e.g., 2, 4, or more) signals from a host via a host-side interface. The transceiver multiplexes the received signals for transmission via a line-side interface over the cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved via multi-level modulation encoding, for example. In one non-limiting embodiment, each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable.</p> </div> <p>Lughart 431, ¶58.</p>

Exhibit A-2

Claim 8

[0059] The transceiver can also be configurable in different operational modes. For instance, depending on the mode, the transceiver can handle different numbers of host-side data streams having variable data rates. In one embodiment, the transceiver operates in a first operational mode to translate two host-side 20 Gbit/s NRZ data streams into a single PAM-4 40 Gbit/s stream on the line side, and vice versa. In a second operational mode, the transceiver translates four host-side 10 Gbps NRZ data streams into a single PAM-4 40 Gbit/s stream on the line-side, and vice versa. Such flexibility allows the transceiver to be employed in a variety of different contexts, such as in both consumer and data center contexts.

Lugthart 431, ¶59.

[0060] The transceiver in some embodiments includes a timing recovery circuit including a digital clock recovery path having a dedicated, relatively low latency and/or low power analog-to-digital converter (ADC). The data path can include a separate ADC having more bits than the ADC included in the clock recovery path. Different filtering can be used in the clock and data paths. Moreover, the digital output from the clock recovery path can be used to drive a digitally controlled oscillator (DCO) rather than implementing an analog phase-locked loop (PLL), further reducing latency.

Lugthart 431, ¶60.

Exhibit A-2

Claim 8

[0063] FIG. 1A is a schematic diagram of one example of a transceiver 10. The transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b.

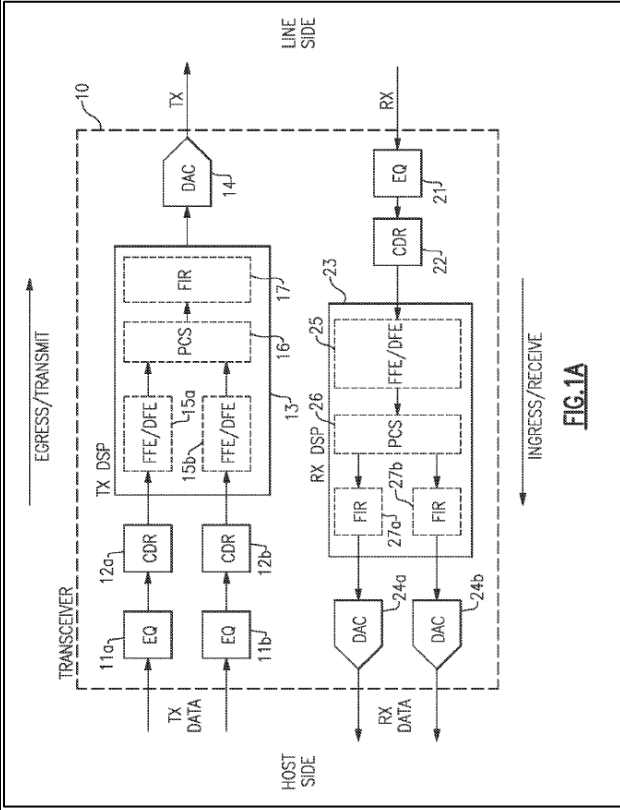
Lugthart 431, ¶63.

[0065] As shown in FIG. 1A, the first and second transmit path equalizers 11a, 11b include inputs that receive host side transmit data (TX DATA) and outputs electrically connected to inputs of the first and second transmit path CDR circuits 12a, 12b, respectively. The first and second transmit path CDR circuits 12a, 12b further include outputs electrically connected to inputs of the transmit path DSP 13. The transmit path DAC 14 includes an input electrically connected to an output of the transmit path DSP 13 and an output that generates a line side transmit signal (TX). The receive path equalizer 21 includes an input that receives a line side receive signal (RX), and an output electrically connected to an input of the receive path CDR circuit 22. The receive path CDR circuit 22 further includes an output electrically connected to an input of the receive path DSP 23. The receive path DSP 23 further includes outputs electrically connected to inputs of the first and second receive path DACs 24a, 24b. The first and second receive path DACs 24a, 24b further include outputs that generate host side receive data (RX DATA).

Lugthart 431, ¶65.

Exhibit A-2

Claim 8



Lugthart 431, Figure 1A.

Exhibit A-2

<p>Claim 8</p>	<p>[0067] In certain configurations, the transceiver 10 can implement a serializer/deserializer (SerDes) function or operation. For example, in one embodiment, the transceiver 10 can operate as a full duplex multiplexer and re-timer capable of receiving multiple (for example, 2, 4, or more) signals from a host via a host-side interface. Additionally, the transceiver 10 can multiplex the received host-side transmit signals for transmission via a line-side interface over a cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved, for example, via multi-level modulation encoding. In one non-limiting example, an egress/transmit path of the transceiver 10 is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals on the host side and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission to the line side over the cable. Conversely, an ingress/receive path of the transceiver in such an example is capable of receiving a single 40 Gbit/s PAM-4 signal on the line side and de-multiplexing this signal into dual 20 Gbit/s NRZ signals for communication to the host side.</p> <p>Lugthart 431, ¶67.</p>
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Exhibit A-2

<p>Claim 8</p>	<p>[0068] FIG. 1A illustrates the host side transmit data as including two signals and the line side transmit data as including one signal (e.g., via a multiplexing operation), and illustrates the line side receive data as including one signal and the host side receive data as including two signals (via a de-multiplexing operation). However, other configurations are possible, including configurations with additional signals on the host side and/or line side. For example, the first and second receive path DACs 24a, 24b can be replicated in parallel to include, for instance, 10, 20, or 40 or more DACs to provide wider RX DATA bandwidth. Similarly, the first and second transmit path equalizers 11a, 11b and the first and second transmit path CDR circuits 12a, 12b can be replicated in provide wider TX DATA bandwidth. In such configurations, different multiplexing, de-multiplexing, and/or modulation formats can be employed, as appropriate.</p> <p>Lugthart 431, ¶68.</p>
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Exhibit A-2

<p>Claim 8</p>	<p>[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.</p> <p>Lugthart 431, ¶72.</p>
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Exhibit A-2

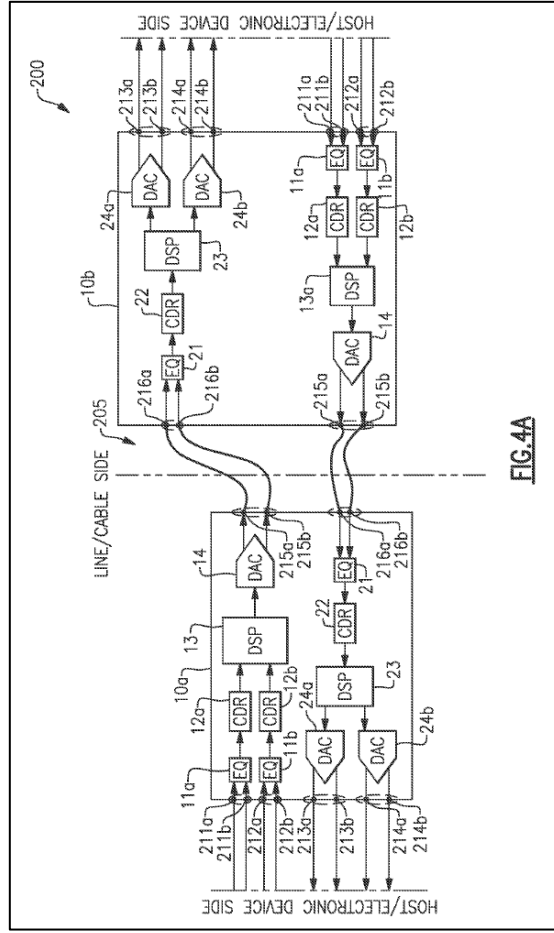
<p>Claim 8</p>	<p>[0116] In various implementations, the packaging can have a design and a form factor similar to the packaging defined by an existing interface standard (e.g., Thunderbolt Gen1/Gen2 or USB 2.0/3.0), although the packaging can have some other form factor. The packaging can comprise materials suitable for electronic and computer interfaces, such as plastic, metal or a composite material. Each of the transceiver assemblies 105a and 105b has an input port that is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b, and an output port that is connected to the cable. The input port can include a connector similar to connectors of existing interface standards, including, but not limited to, Thunderbolt, USB 2.0/3.0, small form-factor pluggable (SFP), enhanced small form-factor pluggable (SFP+), and/or quad small form-factor pluggable (QSFP).</p> <p>Lugthart 431, ¶116.</p> <p>[0118] In certain embodiments, the transceiver assemblies 105a and 105b implement an egress path by: (a) receiving at least two differential signals from a host device; (b) digitally re-timing, conditioning, and multiplexing the received differential signals; and (c) transmitting the multiplexed signal as a multi-level modulated signal (e.g., PAM-4) over the cable.</p> <p>Lugthart 431, ¶118.</p>
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Exhibit A-2

Claim 8

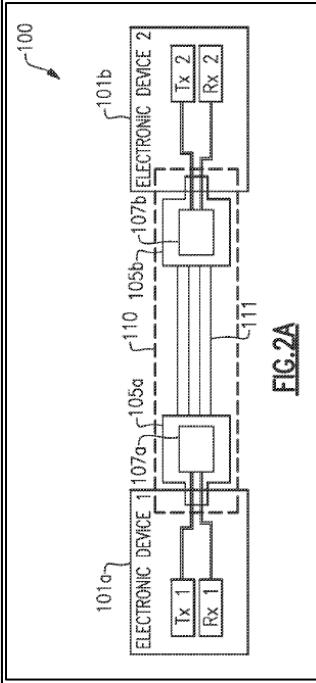
[0119] In certain embodiments, the transceiver assemblies are further configured to implement an ingress path by: (a) receiving a multi-level modulated signal (e.g., PAM-4) from the cable; (b) digitally conditioning and de-multiplexing the received multi-level modulated signal; and (c) transmitting the de-multiplexed signals as an analog signal to the host device.

Lugthart 431, ¶119.



Lugthart 431, Figure 4A.

Claim 8



Lugthart 431, Figure 2A.

[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 105b. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.

Lugthart 431, ¶107.

Exhibit A-2

Claim 8

[0143] FIG. 4A illustrates an example of a communication system 200 including a first transceiver 10a connected to another similar transceiver 10b by a cable 205. The first and second transceivers 10a, 10b are implemented in a manner similar to that of the transceiver 10 of FIG. 1A, with differential signaling used on the host and line sides of the transceivers.

Lugthart 431, ¶143.

[0144] Although the communication system 200 of FIG. 2A is shown as including transceivers similar to the transceiver 10 of FIG. 1A, other configurations are possible. For example, any of the transceivers shown in FIGS. 1A-1D can communicate with one another over a cable.

Lugthart 431, ¶144.

[0145] As shown in FIG. 4A, the first and second transceivers 10a, 10b have a host side for facing an electronic device and a line side for facing the cable 205. For example, with reference back to FIG. 2A, the first transceiver 10a can communicate with a first electronic device 101a and the second transceiver 10b can communicate with a second electronic device 101b. Thus, the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable 205 and an ingress path configured to transport signals from the cable 205 to the electronic device. For example, the first transceiver 10a includes an egress path for transmitting signals from a first electronic device to the cable 205 and an ingress path for providing signals received over the cable 205 to the first electronic device. Similarly, the second transceiver 10b includes an egress path for transmitting signals from a

Lugthart 431, ¶145.

Exhibit A-2

<p>Claim 8</p>	<p>To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>8[b] connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="638 789 1094 1465" style="border: 1px solid black; padding: 5px;"> <p>[0058] In certain configurations, the transceivers can implement a serializer/deserializer (SerDes) function. For example, in certain implementations each transceiver can be a full duplex multiplexer and re-timer capable of receiving multiple (e.g., 2, 4, or more) signals from a host via a host-side interface. The transceiver multiplexes the received signals for transmission via a line-side interface over the cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved via multi-level modulation encoding, for example. In one non-limiting embodiment, each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable.</p> </div> <p>Lugthart 431, ¶58.</p>

Exhibit A-2

Claim 8

[0059] The transceiver can also be configurable in different operational modes. For instance, depending on the mode, the transceiver can handle different numbers of host-side data streams having variable data rates. In one embodiment, the transceiver operates in a first operational mode to translate two host-side 20 Gbit/s NRZ data streams into a single PAM-4 40 Gbit/s stream on the line side, and vice versa. In a second operational mode, the transceiver translates four host-side 10 Gbps NRZ data streams into a single PAM-4 40 Gbit/s stream on the line-side, and vice versa. Such flexibility allows the transceiver to be employed in a variety of different contexts, such as in both consumer and data center contexts.

Lugthart 431, ¶59.

[0060] The transceiver in some embodiments includes a timing recovery circuit including a digital clock recovery path having a dedicated, relatively low latency and/or low power analog-to-digital converter (ADC). The data path can include a separate ADC having more bits than the ADC included in the clock recovery path. Different filtering can be used in the clock and data paths. Moreover, the digital output from the clock recovery path can be used to drive a digitally controlled oscillator (DCO) rather than implementing an analog phase-locked loop (PLL), further reducing latency.

Lugthart 431, ¶60.

Exhibit A-2

Claim 8

[0063] FIG. 1A is a schematic diagram of one example of a transceiver 10. The transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b.

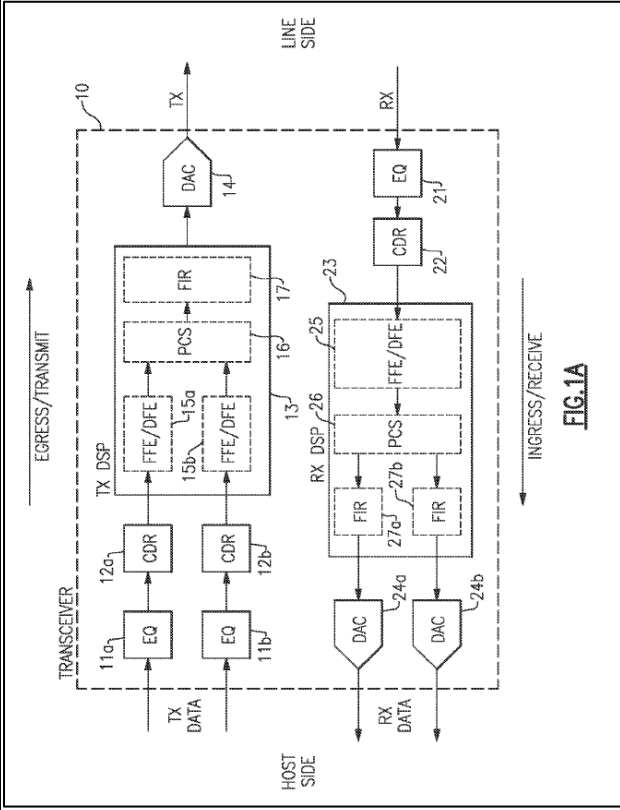
Lugthart 431, ¶63.

[0065] As shown in FIG. 1A, the first and second transmit path equalizers 11a, 11b include inputs that receive host side transmit data (TX DATA) and outputs electrically connected to inputs of the first and second transmit path CDR circuits 12a, 12b, respectively. The first and second transmit path CDR circuits 12a, 12b further include outputs electrically connected to inputs of the transmit path DSP 13. The transmit path DAC 14 includes an input electrically connected to an output of the transmit path DSP 13 and an output that generates a line side transmit signal (TX). The receive path equalizer 21 includes an input that receives a line side receive signal (RX), and an output electrically connected to an input of the receive path CDR circuit 22. The receive path CDR circuit 22 further includes an output electrically connected to an input of the receive path DSP 23. The receive path DSP 23 further includes outputs electrically connected to inputs of the first and second receive path DACs 24a, 24b. The first and second receive path DACs 24a, 24b further include outputs that generate host side receive data (RX DATA).

Lugthart 431, ¶65.

Exhibit A-2

Claim 8



Lugthart 431, Figure 1A.

Exhibit A-2

<p>Claim 8</p>	<p>[0067] In certain configurations, the transceiver 10 can implement a serializer/deserializer (SerDes) function or operation. For example, in one embodiment, the transceiver 10 can operate as a full duplex multiplexer and re-timer capable of receiving multiple (for example, 2, 4, or more) signals from a host via a host-side interface. Additionally, the transceiver 10 can multiplex the received host-side transmit signals for transmission via a line-side interface over a cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved, for example, via multi-level modulation encoding. In one non-limiting example, an egress/transmit path of the transceiver 10 is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals on the host side and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission to the line side over the cable. Conversely, an ingress/receive path of the transceiver in such an example is capable of receiving a single 40 Gbit/s PAM-4 signal on the line side and de-multiplexing this signal into dual 20 Gbit/s NRZ signals for communication to the host side.</p> <p>Lugthart 431, ¶67.</p>
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Exhibit A-2

<p>Claim 8</p>	<p>[0068] FIG. 1A illustrates the host side transmit data as including two signals and the line side transmit data as including one signal (e.g., via a multiplexing operation), and illustrates the line side receive data as including one signal and the host side receive data as including two signals (via a de-multiplexing operation). However, other configurations are possible, including configurations with additional signals on the host side and/or line side. For example, the first and second receive path DACs 24a, 24b can be replicated in parallel to include, for instance, 10, 20, or 40 or more DACs to provide wider RX DATA bandwidth. Similarly, the first and second transmit path equalizers 11a, 11b and the first and second transmit path CDR circuits 12a, 12b can be replicated in provide wider TX DATA bandwidth. In such configurations, different multiplexing, de-multiplexing, and/or modulation formats can be employed, as appropriate.</p> <p>Lugthart 431, ¶68.</p>
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Exhibit A-2

<p>Claim 8</p>	<p>[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.</p> <p>Lugthart 431, ¶72.</p>
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Exhibit A-2

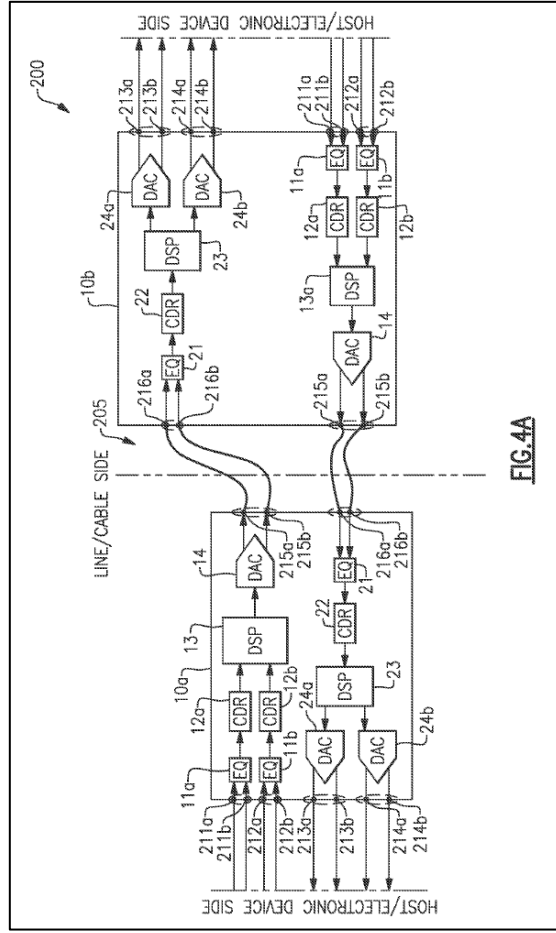
<p>Claim 8</p>	<p>[0116] In various implementations, the packaging can have a design and a form factor similar to the packaging defined by an existing interface standard (e.g., Thunderbolt Gen1/Gen2 or USB 2.0/3.0), although the packaging can have some other form factor. The packaging can comprise materials suitable for electronic and computer interfaces, such as plastic, metal or a composite material. Each of the transceiver assemblies 105a and 105b has an input port that is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b, and an output port that is connected to the cable. The input port can include a connector similar to connectors of existing interface standards, including, but not limited to, Thunderbolt, USB 2.0/3.0, small form-factor pluggable (SFP), enhanced small form-factor pluggable (SFP+), and/or quad small form-factor pluggable (QSFP).</p> <p>Lugthart 431, ¶116.</p> <p>[0118] In certain embodiments, the transceiver assemblies 105a and 105b implement an egress path by: (a) receiving at least two differential signals from a host device; (b) digitally re-timing, conditioning, and multiplexing the received differential signals; and (c) transmitting the multiplexed signal as a multi-level modulated signal (e.g., PAM-4) over the cable.</p> <p>Lugthart 431, ¶118.</p>
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Exhibit A-2

Claim 8

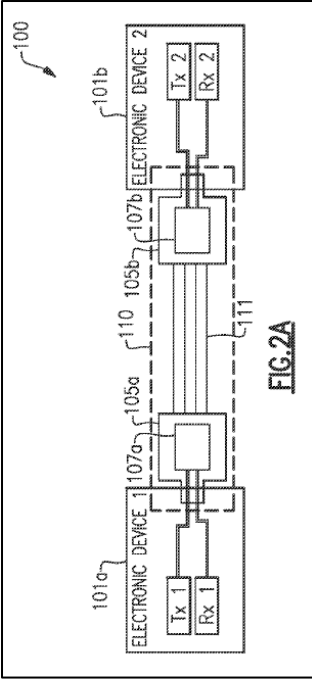
[0119] In certain embodiments, the transceiver assemblies are further configured to implement an ingress path by: (a) receiving a multi-level modulated signal (e.g., PAM-4) from the cable; (b) digitally conditioning and de-multiplexing the received multi-level modulated signal; and (c) transmitting the de-multiplexed signals as an analog signal to the host device.

Lugthart 431, ¶119.



Lugthart 431, Figure 4A.

Claim 8



Lugthart 431, Figure 2A.

[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 105b. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.

Lugthart 431, ¶107.

Exhibit A-2

Claim 8

[0143] FIG. 4A illustrates an example of a communication system 200 including a first transceiver 10a connected to another similar transceiver 10b by a cable 205. The first and second transceivers 10a, 10b are implemented in a manner similar to that of the transceiver 10 of FIG. 1A, with differential signaling used on the host and line sides of the transceivers.

Lugthart 431, ¶143.

[0144] Although the communication system 200 of FIG. 2A is shown as including transceivers similar to the transceiver 10 of FIG. 1A, other configurations are possible. For example, any of the transceivers shown in FIGS. 1A-1D can communicate with one another over a cable.

Lugthart 431, ¶144.

[0145] As shown in FIG. 4A, the first and second transceivers 10a, 10b have a host side for facing an electronic device and a line side for facing the cable 205. For example, with reference back to FIG. 2A, the first transceiver 10a can communicate with a first electronic device 101a and the second transceiver 10b can communicate with a second electronic device 101b. Thus, the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable 205 and an ingress path configured to transport signals from the cable 205 to the electronic device. For example, the first transceiver 10a includes an egress path for transmitting signals from a first electronic device to the cable 205 and an ingress path for providing signals received over the cable 205 to the first electronic device. Similarly, the second transceiver 10b includes an egress path for transmitting signals from a

Lugthart 431, ¶145.

Exhibit A-2

Claim 8

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lughart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lughart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

8[c] connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween,

Lughart 431 discloses and/or renders obvious this limitation.

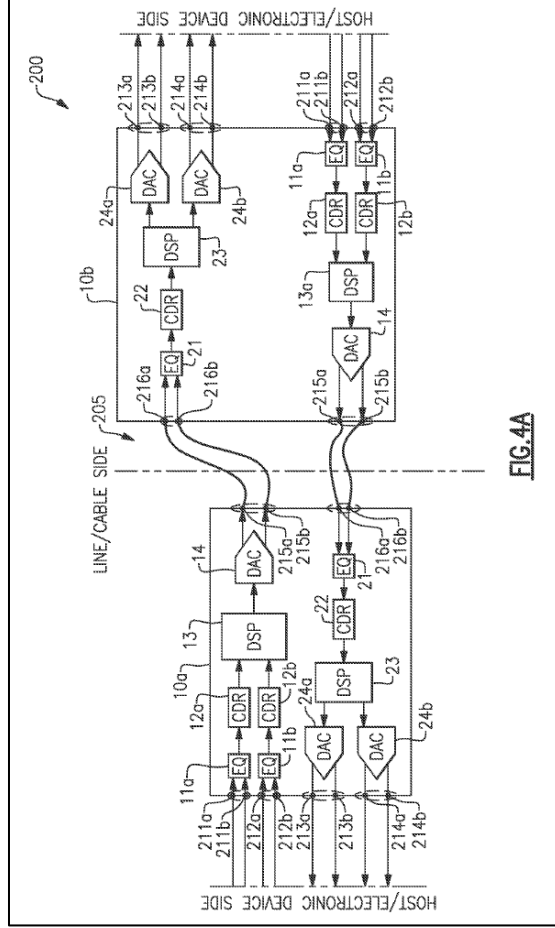
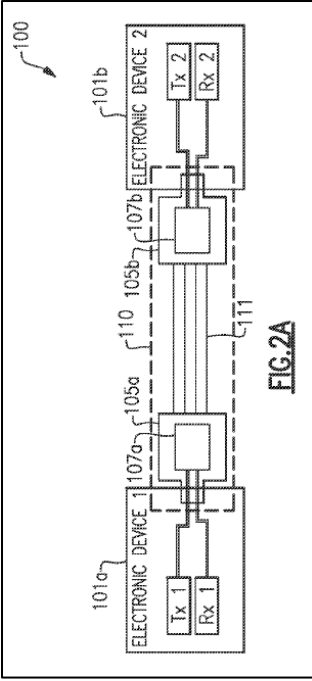


FIG. 4A

Lughart 431, Figure 4A.

Claim 8



Lugthart 431, Figure 2A.

[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 105b. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.

Lugthart 431, ¶107.

Exhibit A-2

Claim 8

[0143] FIG. 4A illustrates an example of a communication system 200 including a first transceiver 10a connected to another similar transceiver 10b by a cable 205. The first and second transceivers 10a, 10b are implemented in a manner similar to that of the transceiver 10 of FIG. 1A, with differential signaling used on the host and line sides of the transceivers.

Lugthart 431, ¶143.

[0144] Although the communication system 200 of FIG. 2A is shown as including transceivers similar to the transceiver 10 of FIG. 1A, other configurations are possible. For example, any of the transceivers shown in FIGS. 1A-1D can communicate with one another over a cable.

Lugthart 431, ¶144.

[0145] As shown in FIG. 4A, the first and second transceivers 10a, 10b have a host side for facing an electronic device and a line side for facing the cable 205. For example, with reference back to FIG. 2A, the first transceiver 10a can communicate with a first electronic device 101a and the second transceiver 10b can communicate with a second electronic device 101b. Thus, the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable 205 and an ingress path configured to transport signals from the cable 205 to the electronic device. For example, the first transceiver 10a includes an egress path for transmitting signals from a first electronic device to the cable 205 and an ingress path for providing signals received over the cable 205 to the first electronic device. Similarly, the second transceiver 10b includes an egress path for transmitting signals from a

Lugthart 431, ¶145.

Exhibit A-2

<p align="center">Claim 8</p>	<p>To the extent that this limitation is not disclosed, either explicitly or inherently, by Lughart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lughart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>8[d] the first DRR device converting between said electrical transit signals and said multi-lane data streams for the first host interface port, and</p>	<p>Lughart 431 discloses and/or renders obvious this limitation.</p> <div style="border: 1px solid black; padding: 5px; margin: 10px 0;"> <p>[0058] In certain configurations, the transceivers can implement a serializer/deserializer (SerDes) function. For example, in certain implementations each transceiver can be a full duplex multiplexer and re-timer capable of receiving multiple (e.g., 2, 4, or more) signals from a host via a host-side interface. The transceiver multiplexes the received signals for transmission via a line-side interface over the cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved via multi-level modulation encoding, for example. In one non-limiting embodiment, each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable.</p> </div> <p>Lughart 431, ¶58.</p>

Exhibit A-2

Claim 8

[0059] The transceiver can also be configurable in different operational modes. For instance, depending on the mode, the transceiver can handle different numbers of host-side data streams having variable data rates. In one embodiment, the transceiver operates in a first operational mode to translate two host-side 20 Gbit/s NRZ data streams into a single PAM-4 40 Gbit/s stream on the line side, and vice versa. In a second operational mode, the transceiver translates four host-side 10 Gbps NRZ data streams into a single PAM-4 40 Gbit/s stream on the line-side, and vice versa. Such flexibility allows the transceiver to be employed in a variety of different contexts, such as in both consumer and data center contexts.

Lugthart 431, ¶59.

[0060] The transceiver in some embodiments includes a timing recovery circuit including a digital clock recovery path having a dedicated, relatively low latency and/or low power analog-to-digital converter (ADC). The data path can include a separate ADC having more bits than the ADC included in the clock recovery path. Different filtering can be used in the clock and data paths. Moreover, the digital output from the clock recovery path can be used to drive a digitally controlled oscillator (DCO) rather than implementing an analog phase-locked loop (PLL), further reducing latency.

Lugthart 431, ¶60.

Exhibit A-2

Claim 8

[0063] FIG. 1A is a schematic diagram of one example of a transceiver 10. The transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b.

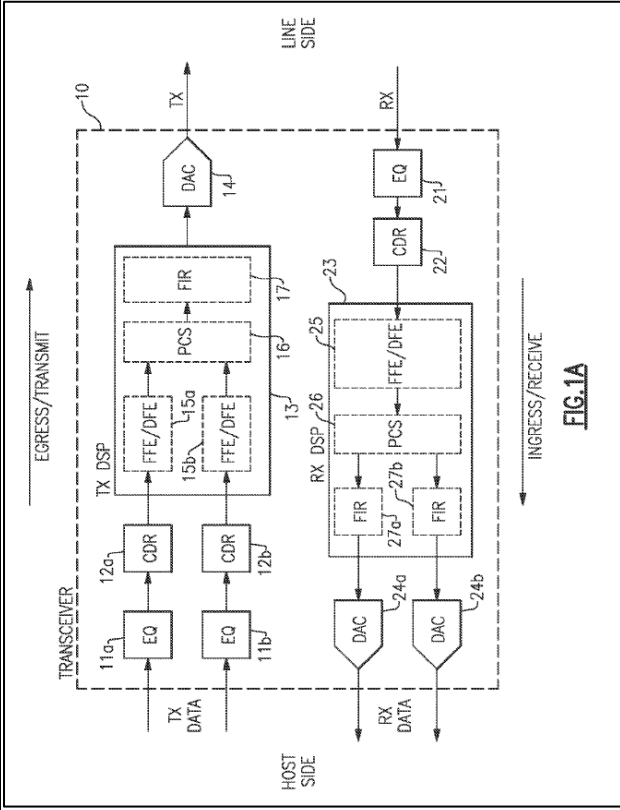
Lugthart 431, ¶63.

[0065] As shown in FIG. 1A, the first and second transmit path equalizers 11a, 11b include inputs that receive host side transmit data (TX DATA) and outputs electrically connected to inputs of the first and second transmit path CDR circuits 12a, 12b, respectively. The first and second transmit path CDR circuits 12a, 12b further include outputs electrically connected to inputs of the transmit path DSP 13. The transmit path DAC 14 includes an input electrically connected to an output of the transmit path DSP 13 and an output that generates a line side transmit signal (TX). The receive path equalizer 21 includes an input that receives a line side receive signal (RX), and an output electrically connected to an input of the receive path CDR circuit 22. The receive path CDR circuit 22 further includes an output electrically connected to an input of the receive path DSP 23. The receive path DSP 23 further includes outputs electrically connected to inputs of the first and second receive path DACs 24a, 24b. The first and second receive path DACs 24a, 24b further include outputs that generate host side receive data (RX DATA).

Lugthart 431, ¶65.

Exhibit A-2

Claim 8



Lugthart 431, Figure 1A.

Exhibit A-2

<p>Claim 8</p>	<p>[0067] In certain configurations, the transceiver 10 can implement a serializer/deserializer (SerDes) function or operation. For example, in one embodiment, the transceiver 10 can operate as a full duplex multiplexer and re-timer capable of receiving multiple (for example, 2, 4, or more) signals from a host via a host-side interface. Additionally, the transceiver 10 can multiplex the received host-side transmit signals for transmission via a line-side interface over a cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved, for example, via multi-level modulation encoding. In one non-limiting example, an egress/transmit path of the transceiver 10 is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals on the host side and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission to the line side over the cable. Conversely, an ingress/receive path of the transceiver in such an example is capable of receiving a single 40 Gbit/s PAM-4 signal on the line side and de-multiplexing this signal into dual 20 Gbit/s NRZ signals for communication to the host side.</p> <p>Lugthart 431, ¶67.</p>
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Exhibit A-2

<p>Claim 8</p>	<p>[0068] FIG. 1A illustrates the host side transmit data as including two signals and the line side transmit data as including one signal (e.g., via a multiplexing operation), and illustrates the line side receive data as including one signal and the host side receive data as including two signals (via a de-multiplexing operation). However, other configurations are possible, including configurations with additional signals on the host side and/or line side. For example, the first and second receive path DACs 24a, 24b can be replicated in parallel to include, for instance, 10, 20, or 40 or more DACs to provide wider RX DATA bandwidth. Similarly, the first and second transmit path equalizers 11a, 11b and the first and second transmit path CDR circuits 12a, 12b can be replicated in provide wider TX DATA bandwidth. In such configurations, different multiplexing, de-multiplexing, and/or modulation formats can be employed, as appropriate.</p> <p>Lugthart 431, ¶68.</p>
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Exhibit A-2

<p>Claim 8</p>	<p>[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.</p> <p>Lugthart 431, ¶72.</p>
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Exhibit A-2

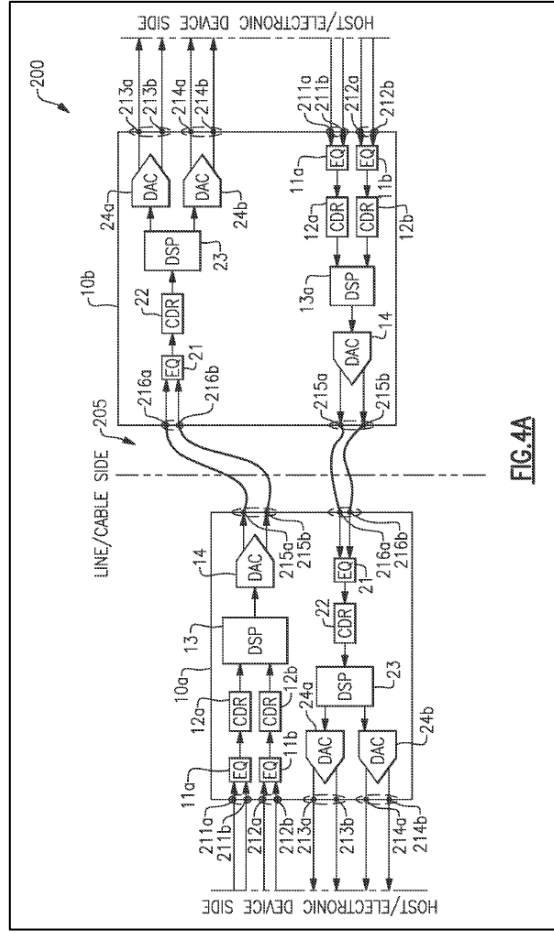
<p>Claim 8</p>	<p>[0116] In various implementations, the packaging can have a design and a form factor similar to the packaging defined by an existing interface standard (e.g., Thunderbolt Gen1/Gen2 or USB 2.0/3.0), although the packaging can have some other form factor. The packaging can comprise materials suitable for electronic and computer interfaces, such as plastic, metal or a composite material. Each of the transceiver assemblies 105a and 105b has an input port that is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b, and an output port that is connected to the cable. The input port can include a connector similar to connectors of existing interface standards, including, but not limited to, Thunderbolt, USB 2.0/3.0, small form-factor pluggable (SFP), enhanced small form-factor pluggable (SFP+), and/or quad small form-factor pluggable (QSFP).</p> <p>Lugthart 431, ¶116.</p> <p>[0118] In certain embodiments, the transceiver assemblies 105a and 105b implement an egress path by: (a) receiving at least two differential signals from a host device; (b) digitally re-timing, conditioning, and multiplexing the received differential signals; and (c) transmitting the multiplexed signal as a multi-level modulated signal (e.g., PAM-4) over the cable.</p> <p>Lugthart 431, ¶118.</p>
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Exhibit A-2

Claim 8

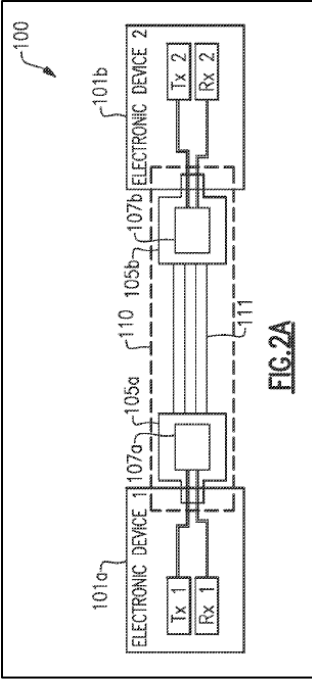
[0119] In certain embodiments, the transceiver assemblies are further configured to implement an ingress path by: (a) receiving a multi-level modulated signal (e.g., PAM-4) from the cable; (b) digitally conditioning and de-multiplexing the received multi-level modulated signal; and (c) transmitting the de-multiplexed signals as an analog signal to the host device.

Lugthart 431, ¶119.



Lugthart 431, Figure 4A.

Claim 8



Lugthart 431, Figure 2A.

[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 105b. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.

Lugthart 431, ¶107.

Exhibit A-2

Claim 8

[0143] FIG. 4A illustrates an example of a communication system 200 including a first transceiver 10a connected to another similar transceiver 10b by a cable 205. The first and second transceivers 10a, 10b are implemented in a manner similar to that of the transceiver 10 of FIG. 1A, with differential signaling used on the host and line sides of the transceivers.

Lugthart 431, ¶143.

[0144] Although the communication system 200 of FIG. 2A is shown as including transceivers similar to the transceiver 10 of FIG. 1A, other configurations are possible. For example, any of the transceivers shown in FIGS. 1A-1D can communicate with one another over a cable.

Lugthart 431, ¶144.

[0145] As shown in FIG. 4A, the first and second transceivers 10a, 10b have a host side for facing an electronic device and a line side for facing the cable 205. For example, with reference back to FIG. 2A, the first transceiver 10a can communicate with a first electronic device 101a and the second transceiver 10b can communicate with a second electronic device 101b. Thus, the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable 205 and an ingress path configured to transport signals from the cable 205 to the electronic device. For example, the first transceiver 10a includes an egress path for transmitting signals from a first electronic device to the cable 205 and an ingress path for providing signals received over the cable 205 to the first electronic device. Similarly, the second transceiver 10b includes an egress path for transmitting signals from a

Lugthart 431, ¶145.

Exhibit A-2

<p>Claim 8</p>	<p>To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>8[e] the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port,</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="634 789 1094 1465" style="border: 1px solid black; padding: 5px;"> <p>[0058] In certain configurations, the transceivers can implement a serializer/deserializer (SerDes) function. For example, in certain implementations each transceiver can be a full duplex multiplexer and re-timer capable of receiving multiple (e.g., 2, 4, or more) signals from a host via a host-side interface. The transceiver multiplexes the received signals for transmission via a line-side interface over the cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved via multi-level modulation encoding, for example. In one non-limiting embodiment, each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable.</p> </div> <p>Lugthart 431, ¶58.</p>

Exhibit A-2

<p>Claim 8</p>	<p>[0059] The transceiver can also be configurable in different operational modes. For instance, depending on the mode, the transceiver can handle different numbers of host-side data streams having variable data rates. In one embodiment, the transceiver operates in a first operational mode to translate two host-side 20 Gbit/s NRZ data streams into a single PAM-4 40 Gbit/s stream on the line side, and vice versa. In a second operational mode, the transceiver translates four host-side 10 Gbps NRZ data streams into a single PAM-4 40 Gbit/s stream on the line-side, and vice versa. Such flexibility allows the transceiver to be employed in a variety of different contexts, such as in both consumer and data center contexts.</p> <p>Lugthart 431, ¶59.</p> <p>[0060] The transceiver in some embodiments includes a timing recovery circuit including a digital clock recovery path having a dedicated, relatively low latency and/or low power analog-to-digital converter (ADC). The data path can include a separate ADC having more bits than the ADC included in the clock recovery path. Different filtering can be used in the clock and data paths. Moreover, the digital output from the clock recovery path can be used to drive a digitally controlled oscillator (DCO) rather than implementing an analog phase-locked loop (PLL), further reducing latency.</p> <p>Lugthart 431, ¶60.</p>
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Exhibit A-2

Claim 8

[0063] FIG. 1A is a schematic diagram of one example of a transceiver 10. The transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b.

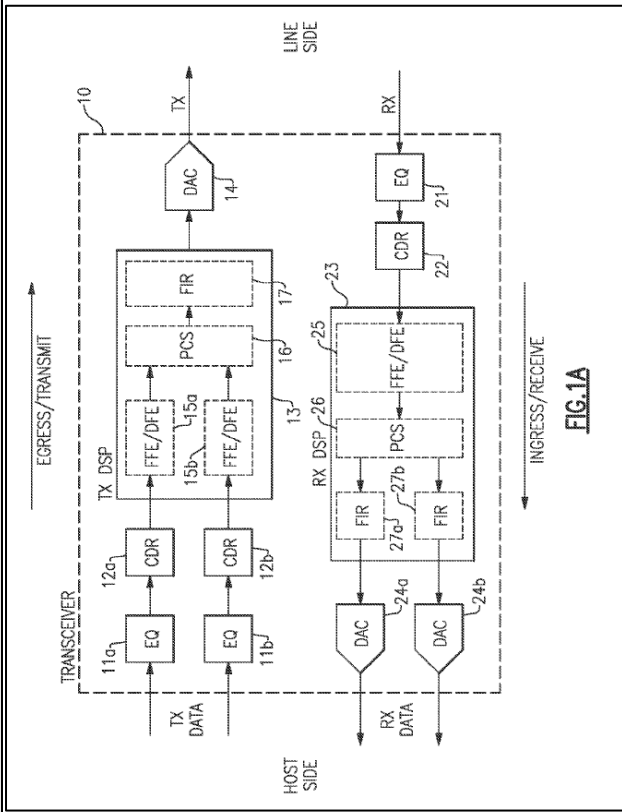
Lugthart 431, ¶63.

[0065] As shown in FIG. 1A, the first and second transmit path equalizers 11a, 11b include inputs that receive host side transmit data (TX DATA) and outputs electrically connected to inputs of the first and second transmit path CDR circuits 12a, 12b, respectively. The first and second transmit path CDR circuits 12a, 12b further include outputs electrically connected to inputs of the transmit path DSP 13. The transmit path DAC 14 includes an input electrically connected to an output of the transmit path DSP 13 and an output that generates a line side transmit signal (TX). The receive path equalizer 21 includes an input that receives a line side receive signal (RX), and an output electrically connected to an input of the receive path CDR circuit 22. The receive path CDR circuit 22 further includes an output electrically connected to an input of the receive path DSP 23. The receive path DSP 23 further includes outputs electrically connected to inputs of the first and second receive path DACs 24a, 24b. The first and second receive path DACs 24a, 24b further include outputs that generate host side receive data (RX DATA).

Lugthart 431, ¶65.

Exhibit A-2

Claim 8



Lugthart 431, Figure 1A.

Exhibit A-2

<p>Claim 8</p>	<p>[0067] In certain configurations, the transceiver 10 can implement a serializer/deserializer (SerDes) function or operation. For example, in one embodiment, the transceiver 10 can operate as a full duplex multiplexer and re-timer capable of receiving multiple (for example, 2, 4, or more) signals from a host via a host-side interface. Additionally, the transceiver 10 can multiplex the received host-side transmit signals for transmission via a line-side interface over a cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved, for example, via multi-level modulation encoding. In one non-limiting example, an egress/transmit path of the transceiver 10 is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals on the host side and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission to the line side over the cable. Conversely, an ingress/receive path of the transceiver in such an example is capable of receiving a single 40 Gbit/s PAM-4 signal on the line side and de-multiplexing this signal into dual 20 Gbit/s NRZ signals for communication to the host side.</p> <p>Lugthart 431, ¶67.</p>
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Exhibit A-2

<p>Claim 8</p>	<p>[0068] FIG. 1A illustrates the host side transmit data as including two signals and the line side transmit data as including one signal (e.g., via a multiplexing operation), and illustrates the line side receive data as including one signal and the host side receive data as including two signals (via a de-multiplexing operation). However, other configurations are possible, including configurations with additional signals on the host side and/or line side. For example, the first and second receive path DACs 24a, 24b can be replicated in parallel to include, for instance, 10, 20, or 40 or more DACs to provide wider RX DATA bandwidth. Similarly, the first and second transmit path equalizers 11a, 11b and the first and second transmit path CDR circuits 12a, 12b can be replicated in provide wider TX DATA bandwidth. In such configurations, different multiplexing, de-multiplexing, and/or modulation formats can be employed, as appropriate.</p> <p>Lugthart 431, ¶68.</p>
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Exhibit A-2

<p>Claim 8</p>	<p>[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.</p> <p>Lugthart 431, ¶72.</p>
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Exhibit A-2

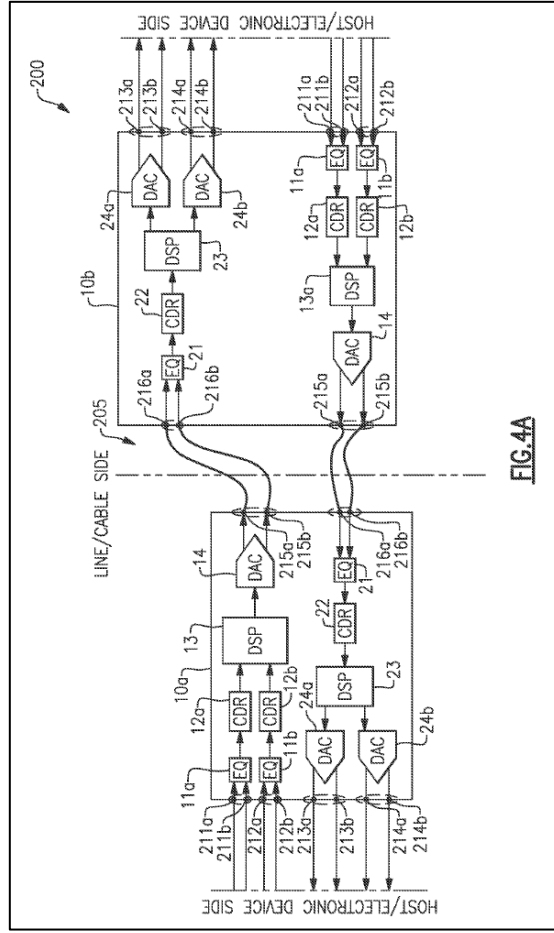
<p>Claim 8</p>	<p>[0116] In various implementations, the packaging can have a design and a form factor similar to the packaging defined by an existing interface standard (e.g., Thunderbolt Gen1/Gen2 or USB 2.0/3.0), although the packaging can have some other form factor. The packaging can comprise materials suitable for electronic and computer interfaces, such as plastic, metal or a composite material. Each of the transceiver assemblies 105a and 105b has an input port that is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b, and an output port that is connected to the cable. The input port can include a connector similar to connectors of existing interface standards, including, but not limited to, Thunderbolt, USB 2.0/3.0, small form-factor pluggable (SFP), enhanced small form-factor pluggable (SFP+), and/or quad small form-factor pluggable (QSFP).</p> <p>Lugthart 431, ¶116.</p> <p>[0118] In certain embodiments, the transceiver assemblies 105a and 105b implement an egress path by: (a) receiving at least two differential signals from a host device; (b) digitally re-timing, conditioning, and multiplexing the received differential signals; and (c) transmitting the multiplexed signal as a multi-level modulated signal (e.g., PAM-4) over the cable.</p> <p>Lugthart 431, ¶118.</p>
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Exhibit A-2

Claim 8

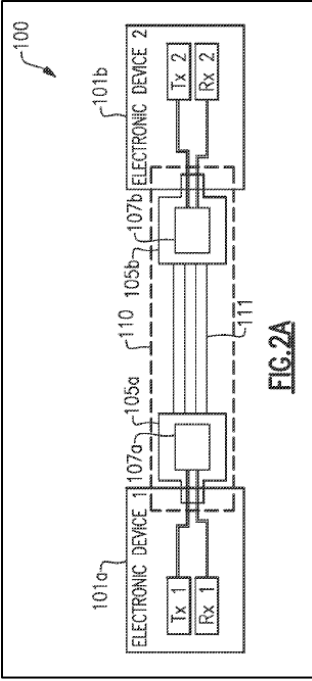
[0119] In certain embodiments, the transceiver assemblies are further configured to implement an ingress path by: (a) receiving a multi-level modulated signal (e.g., PAM-4) from the cable; (b) digitally conditioning and de-multiplexing the received multi-level modulated signal; and (c) transmitting the de-multiplexed signals as an analog signal to the host device.

Lugthart 431, ¶119.



Lugthart 431, Figure 4A.

Claim 8



Lugthart 431, Figure 2A.

[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 105b. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.

Lugthart 431, ¶107.

Exhibit A-2

Claim 8

[0143] FIG. 4A illustrates an example of a communication system 200 including a first transceiver 10a connected to another similar transceiver 10b by a cable 205. The first and second transceivers 10a, 10b are implemented in a manner similar to that of the transceiver 10 of FIG. 1A, with differential signaling used on the host and line sides of the transceivers.

Lugthart 431, ¶143.

[0144] Although the communication system 200 of FIG. 2A is shown as including transceivers similar to the transceiver 10 of FIG. 1A, other configurations are possible. For example, any of the transceivers shown in FIGS. 1A-1D can communicate with one another over a cable.

Lugthart 431, ¶144.

[0145] As shown in FIG. 4A, the first and second transceivers 10a, 10b have a host side for facing an electronic device and a line side for facing the cable 205. For example, with reference back to FIG. 2A, the first transceiver 10a can communicate with a first electronic device 101a and the second transceiver 10b can communicate with a second electronic device 101b. Thus, the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable 205 and an ingress path configured to transport signals from the cable 205 to the electronic device. For example, the first transceiver 10a includes an egress path for transmitting signals from a first electronic device to the cable 205 and an ingress path for providing signals received over the cable 205 to the first electronic device. Similarly, the second transceiver 10b includes an egress path for transmitting signals from a

Lugthart 431, ¶145.

Exhibit A-2

<p>Claim 8</p>	<p>To the extent that this limitation is not disclosed, either explicitly or inherently, by Lughart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lughart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>8[f] the first and second DRR devices providing preequalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.</p>	<p>Lughart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="636 789 1070 1465" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lughart 431, ¶71.</p>

Exhibit A-2

Claim 8

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

Exhibit A-2

Claim 8	
	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>

Exhibit A-2

Claim 8

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

Exhibit A-2

Claim 8	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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H. DEPENDENT CLAIM 9

<p>Claim 9</p> <p>9. The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div style="border: 1px solid black; padding: 5px; margin: 10px 0;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>
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Exhibit A-2

Claim 9

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

Exhibit A-2

Claim 9	
	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>

Exhibit A-2

Claim 9

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

Exhibit A-2

Claim 9	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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I. DEPENDENT CLAIM 10

<p>Claim 10</p> <p>10. The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="415 762 850 1438" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>
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Exhibit A-2

Claim 10

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

Exhibit A-2

<p>Claim 10</p>	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>
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Exhibit A-2

Claim 10

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

Exhibit A-2

Claim 10	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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J. DEPENDENT CLAIM 11

<p>Claim 11</p> <p>11. The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="415 762 850 1444" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>
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Exhibit A-2

Claim 11

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

Exhibit A-2

<p>Claim 11</p>	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>
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Exhibit A-2

Claim 11

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

Exhibit A-2

Claim 11	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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K. DEPENDENT CLAIM 12

<p>Claim 12</p> <p>12. The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="415 762 850 1436" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>
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Exhibit A-2

Claim 12

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

Exhibit A-2

<p>Claim 12</p>	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>
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Exhibit A-2

Claim 12

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

Exhibit A-2

Claim 12	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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L. DEPENDENT CLAIM 13

Claim 13

13. The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.

Lugthart 431 discloses and/or renders obvious this limitation.

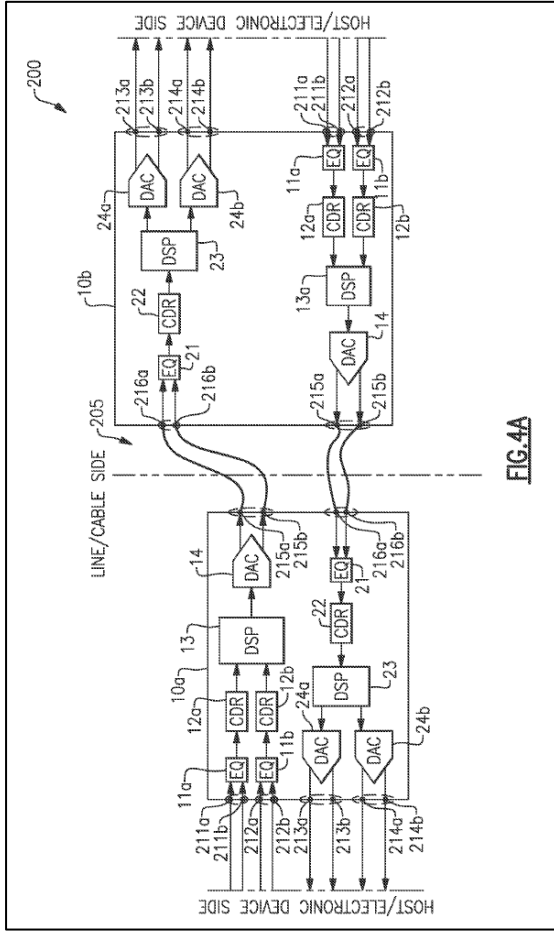


FIG. 4A

Lugthart 431, Figure 4A.

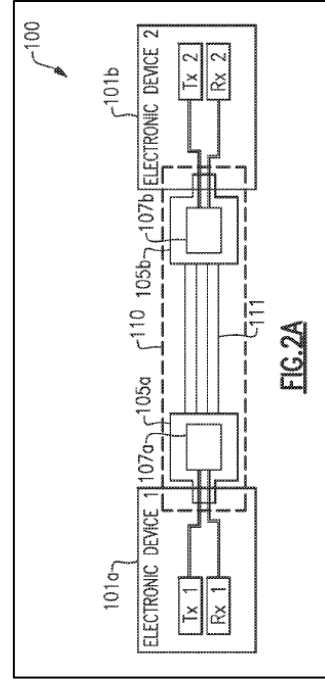


FIG. 2A

Claim 13

Lugthart 431, Figure 2A.

[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 111 as well as first and second transceiver assemblies 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.

Lugthart 431, ¶107.

[0143] FIG. 4A illustrates an example of a communication system 200 including a first transceiver 10a connected to another similar transceiver 10b by a cable 205. The first and second transceivers 10a, 10b are implemented in a manner similar to that of the transceiver 10 of FIG. 1A, with differential signaling used on the host and line sides of the transceivers.

Lugthart 431, ¶143.

[0144] Although the communication system 200 of FIG. 2A is shown as including transceivers similar to the transceiver 10 of FIG. 1A, other configurations are possible. For example, any of the transceivers shown in FIGS. 1A-1D can communicate with one another over a cable.

<p>Claim 13</p>	<p>Lugthart 431, ¶144.</p> <div style="border: 1px solid black; padding: 5px;"> <p>[0145] As shown in FIG. 4A, the first and second transceivers 10a, 10b have a host side for facing an electronic device and a line side for facing the cable 205. For example, with reference back to FIG. 2A, the first transceiver 10a can communicate with a first electronic device 101a and the second transceiver 10b can communicate with a second electronic device 101b. Thus, the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable 205 and an ingress path configured to transport signals from the cable 205 to the electronic device. For example, the first transceiver 10a includes an egress path for transmitting signals from a first electronic device to the cable 205 and an ingress path for providing signals received over the cable 205 to the first electronic device. Similarly, the second transceiver 10b includes an egress path for transmitting signals from a</p> </div> <p>Lugthart 431, ¶145.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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M. DEPENDENT CLAIM 14

<p>Claim 14</p> <p>14. The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="415 762 850 1436" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>
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Exhibit A-2

Claim 14

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

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<p>Claim 14</p>	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>
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Exhibit A-2

Claim 14

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

Exhibit A-2

Claim 14	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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N. INDEPENDENT CLAIM 15

<p>Claim 15</p> <p>15[pre] A communications method that comprises:</p>	<p>To the extent the preamble is limiting, Lugthart 431 discloses and/or renders obvious this limitation.</p> <div style="border: 1px solid black; padding: 5px; margin: 10px 0;"> <p>[0014] In a further aspect, a method of electronic communication includes receiving a first plurality of host-side signals from a host device, wherein each of the first plurality of host-side signals has a first data rate. The method can further include converting the first plurality of host-side signals into a plurality of digitized egress signals using host-side analog-to-digital converter (ADC) circuitry. The method may also include processing the plurality of digitized egress signals to generate one or more multiplexed signals using a first digital signal processor. The step of processing the plurality of digitized egress signals can include digitally conditioning the plurality of digitized egress signals and encoding the one or more multiplexed signals with a multi-level encoding. The method can additionally include converting the one or more multiplexed signals into one or more differential output signals using line-side digital-to-analog converter (DAC) circuitry. Each of the one or more differential output signals can have a second data rate greater than the first data rate. In addition, the method can include transmitting the one or more differential output signals over one or more paired differential conductors of a cable at a data rate of at least 40 Gbit/s.</p> </div> <p>Lugthart 431, ¶14.</p>
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Exhibit A-2

Claim 15

[0015] According to yet another aspect, an active cable comprises a first cable comprising a first pair of conductors including a first pluggable module. The first pluggable module can include a first transceiver including host-side analog-to-digital converter (ADC) circuitry configured to receive a first plurality of host-side signals and to generate a plurality of digitized egress signals. A first host-side signal of the first plurality of host-side signals can have a first data rate. The first transceiver can further include a first digital signal processor (DSP) configured to generate one or more multiplexed signals based on multiplexing the plurality of digitized egress signals. The one or more multiplexed signals can have a multi-level encoding. The transceiver can further include line-side digital-to-analog converter (DAC) circuitry configured to convert the one or more multiplexed signals into one or more differential output signals including a first differential output signal. The line-side DAC circuitry can be configured to transmit the first differential output signal over the first pair of conductors at a second data rate that is greater than the first data rate.

Lugthart 431, ¶15.

[0057] A high-speed communication link can include a cable and a pair of transceivers provided at respective ends of the cable. The cable can be implemented in a wide variety of ways. For example, in certain configurations, the cable can correspond to an electrical cable including one or more pairs of differential micro coaxial cables or conductors. However, other configurations are possible, such as implementations in which the cable is implemented as an optical cable.

Lugthart 431, ¶57.

Exhibit A-2

Claim 15

[10107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 111 as well as first and second transceiver assemblies 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.

Lugthart 431, ¶107.

[10109] The first and second transceiver assemblies 105a, 105b can be implemented in a variety of ways. For example, the first and second transceiver assemblies include first and second transceivers 107a, 107b, respectively, which can be implemented using, for example, any of the embodiments of transceivers described earlier with respect to FIGS. 1A-1D.

Lugthart 431, ¶109.

Exhibit A-2

Claim 15

[0113] Integrating transceivers into a cable can achieve a wide variety of advantages. For example, at a given bit rate, an active cable can permit communication over longer distance and/or with a thinner cable relative to a passive cable. Additionally, using an active cable can decrease jitter, noise, and/or ISI relative to a configuration using a passive cable. However, certain applications can use passive cables, for instance, to lower cable cost. For example, some passive cable configurations can be used in backplane applications.

Lugthart 431, ¶113.

[0121] The conducting lines 111 can include metal (e.g., copper) conductors, for example. In some implementations, the conducting lines 111 can alternatively or additionally include one or more other types of conductors, such as one or more optical fibers that can transport optical signals. As indicated, the conducting lines 111 in alternative embodiments are not housed within a cable, and can instead reside on a PCB or other substrate.

Lugthart 431, ¶121.

[0122] The conducting lines 111 can include one or more sets of paired lines configured for differential signaling, which in some implementations include one or more sets of paired micro coaxial cables. However, other types of conducting lines 111 are possible. For example, shielded or unshielded twisted pair cables can be used in addition to any other appropriate type of cables, such as those that can support different data and video protocols (e.g., Serial ATA, Infiniband, PCI Express, DisplayPort I/O protocols, gigabit Ethernet, etc.).

Lugthart 431, ¶122.

Exhibit A-2

Claim 15

[10125] In various implementations, the cable 110 of FIG. 2A and/or the cable 115 of FIG. 2B can be configured to transport data rates greater than 10 Gbit/s (e.g., 20 Gbit/s, 25 Gbit/s, 28 Gbit/s, 32 Gbit/s, 40 Gbit/s, 50 Gbit/s, 56 Gbit/s, 64 Gbit/s, 100 Gbit/s, 112 Gbit/s, 128 Gbit/s, 200 Gbit/s, 224 Gbit/s, 256 Gbit/s, 400 Gbit/s, and 448 Gbit/s or greater than any of these amounts, or rates between any of the foregoing values, etc.). In various implementations, the cable can have a length between about 0.5 m to about 10 m, for example, a length of about 2 m, about 3 m, about 4 m, about 5 m, about 6 m, about 7 m, about 9 m, or a length between the foregoing values, etc. In other implementations, the cable has a length greater than 10 m, for example, a length of about 10-15 m, about 15-20 m, about 20-30 m, about 30-50 m, about 50-100 m, or lengths between the foregoing, etc. In some embodiments, the cable 110 has a length of greater than 100 m. Thus, the length of the cable 110 of FIG. 2A and/or the cable 115 of FIG. 2B can depend on a variety of factors, including, for example, application, communication speed, signaling protocols, and/or operating environment.

Lugthart 431, ¶125.

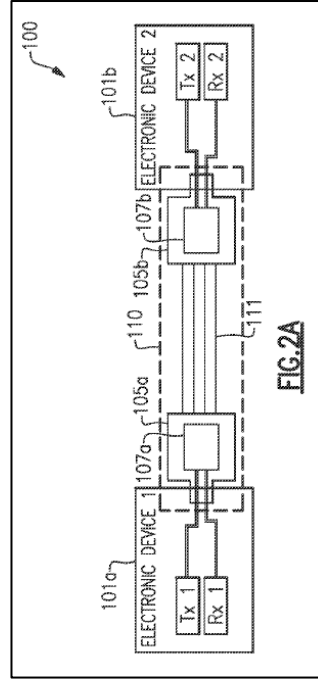


FIG. 2A

Lugthart 431, Figure 2A.

Exhibit A-2

<p>Claim 15</p>	<p>To the extent that this preamble is not disclosed, either explicitly or inherently, by Lugthart 431, this preamble is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>15[a] inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="638 789 1094 1465" style="border: 1px solid black; padding: 5px;"> <p>[0058] In certain configurations, the transceivers can implement a serializer/deserializer (SerDes) function. For example, in certain implementations each transceiver can be a full duplex multiplexer and re-timer capable of receiving multiple (e.g., 2, 4, or more) signals from a host via a host-side interface. The transceiver multiplexes the received signals for transmission via a line-side interface over the cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved via multi-level modulation encoding, for example. In one non-limiting embodiment, each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable.</p> </div> <p>Lugthart 431, ¶58.</p>

Exhibit A-2

Claim 15

[0059] The transceiver can also be configurable in different operational modes. For instance, depending on the mode, the transceiver can handle different numbers of host-side data streams having variable data rates. In one embodiment, the transceiver operates in a first operational mode to translate two host-side 20 Gbit/s NRZ data streams into a single PAM-4 40 Gbit/s stream on the line side, and vice versa. In a second operational mode, the transceiver translates four host-side 10 Gbps NRZ data streams into a single PAM-4 40 Gbit/s stream on the line-side, and vice versa. Such flexibility allows the transceiver to be employed in a variety of different contexts, such as in both consumer and data center contexts.

Lugthart 431, ¶59.

[0060] The transceiver in some embodiments includes a timing recovery circuit including a digital clock recovery path having a dedicated, relatively low latency and/or low power analog-to-digital converter (ADC). The data path can include a separate ADC having more bits than the ADC included in the clock recovery path. Different filtering can be used in the clock and data paths. Moreover, the digital output from the clock recovery path can be used to drive a digitally controlled oscillator (DCO) rather than implementing an analog phase-locked loop (PLL), further reducing latency.

Lugthart 431, ¶60.

Exhibit A-2

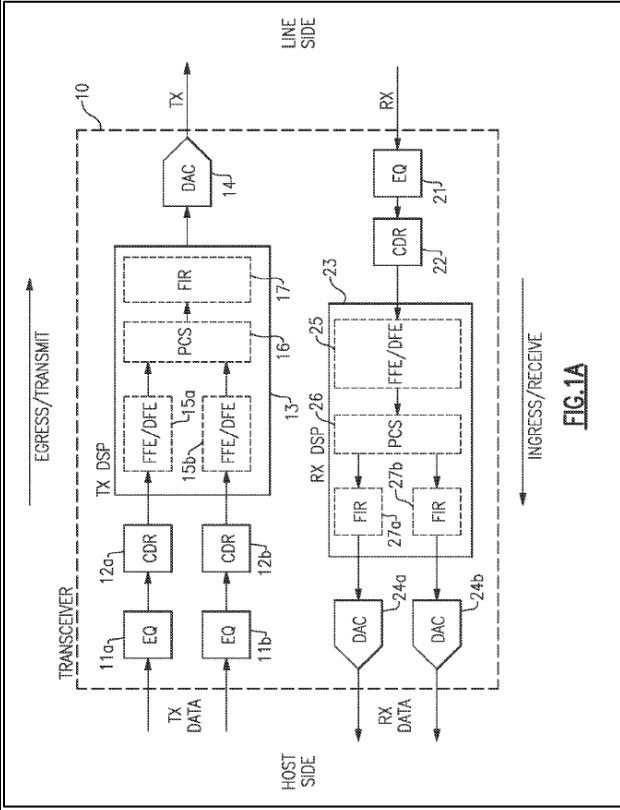
Claim 15

[0063] FIG. 1A is a schematic diagram of one example of a transceiver 10. The transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b.

Lugthart 431, ¶63.

[0065] As shown in FIG. 1A, the first and second transmit path equalizers 11a, 11b include inputs that receive host side transmit data (TX DATA) and outputs electrically connected to inputs of the first and second transmit path CDR circuits 12a, 12b, respectively. The first and second transmit path CDR circuits 12a, 12b further include outputs electrically connected to inputs of the transmit path DSP 13. The transmit path DAC 14 includes an input electrically connected to an output of the transmit path DSP 13 and an output that generates a line side transmit signal (TX). The receive path equalizer 21 includes an input that receives a line side receive signal (RX), and an output electrically connected to an input of the receive path CDR circuit 22. The receive path CDR circuit 22 further includes an output electrically connected to an input of the receive path DSP 23. The receive path DSP 23 further includes outputs electrically connected to inputs of the first and second receive path DACs 24a, 24b. The first and second receive path DACs 24a, 24b further include outputs that generate host side receive data (RX DATA).

Lugthart 431, ¶65.



Lugthart 431, Figure 1A.

Exhibit A-2

Claim 15

[0067] In certain configurations, the transceiver 10 can implement a serializer/deserializer (SerDes) function or operation. For example, in one embodiment, the transceiver 10 can operate as a full duplex multiplexer and re-timer capable of receiving multiple (for example, 2, 4, or more) signals from a host via a host-side interface. Additionally, the transceiver 10 can multiplex the received host-side transmit signals for transmission via a line-side interface over a cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved, for example, via multi-level modulation encoding. In one non-limiting example, an egress/transmit path of the transceiver 10 is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals on the host side and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission to the line side over the cable. Conversely, an ingress/receive path of the transceiver in such an example is capable of receiving a single 40 Gbit/s PAM-4 signal on the line side and de-multiplexing this signal into dual 20 Gbit/s NRZ signals for communication to the host side.

Lugthart 431, ¶67.

Exhibit A-2

<p>Claim 15</p>	<p>[0068] FIG. 1A illustrates the host side transmit data as including two signals and the line side transmit data as including one signal (e.g., via a multiplexing operation), and illustrates the line side receive data as including one signal and the host side receive data as including two signals (via a de-multiplexing operation). However, other configurations are possible, including configurations with additional signals on the host side and/or line side. For example, the first and second receive path DACs 24a, 24b can be replicated in parallel to include, for instance, 10, 20, or 40 or more DACs to provide wider RX DATA bandwidth. Similarly, the first and second transmit path equalizers 11a, 11b and the first and second transmit path CDR circuits 12a, 12b can be replicated in provide wider TX DATA bandwidth. In such configurations, different multiplexing, de-multiplexing, and/or modulation formats can be employed, as appropriate.</p> <p>Lugthart 431, ¶68.</p>
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Exhibit A-2

<p>Claim 15</p>	<p>[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.</p> <p>Lugthart 431, ¶72.</p>
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Exhibit A-2

Claim 15

[0116] In various implementations, the packaging can have a design and a form factor similar to the packaging defined by an existing interface standard (e.g., Thunderbolt Gen1/Gen2 or USB 2.0/3.0), although the packaging can have some other form factor. The packaging can comprise materials suitable for electronic and computer interfaces, such as plastic, metal or a composite material. Each of the transceiver assemblies **105a** and **105b** has an input port that is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device **101a**, **101b**, and an output port that is connected to the cable. The input port can include a connector similar to connectors of existing interface standards, including, but not limited to, Thunderbolt, USB 2.0/3.0, small form-factor pluggable (SFP), enhanced small form-factor pluggable (SFP+), and/or quad small form-factor pluggable (QSFP).

Lugthart 431, ¶116.

[0118] In certain embodiments, the transceiver assemblies **105a** and **105b** implement an egress path by: (a) receiving at least two differential signals from a host device; (b) digitally re-timing, conditioning, and multiplexing the received differential signals; and (c) transmitting the multiplexed signal as a multi-level modulated signal (e.g., PAM-4) over the cable.

Lugthart 431, ¶118.

Exhibit A-2

Claim 15

[0119] In certain embodiments, the transceiver assemblies are further configured to implement an ingress path by: (a) receiving a multi-level modulated signal (e.g., PAM-4) from the cable; (b) digitally conditioning and de-multiplexing the received multi-level modulated signal; and (c) transmitting the de-multiplexed signals as an analog signal to the host device.

Lugthart 431, ¶119.

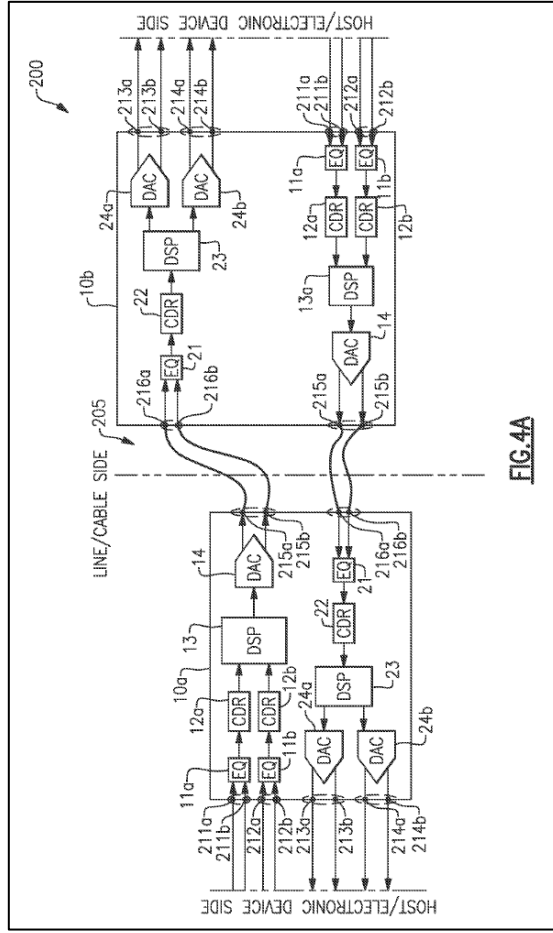
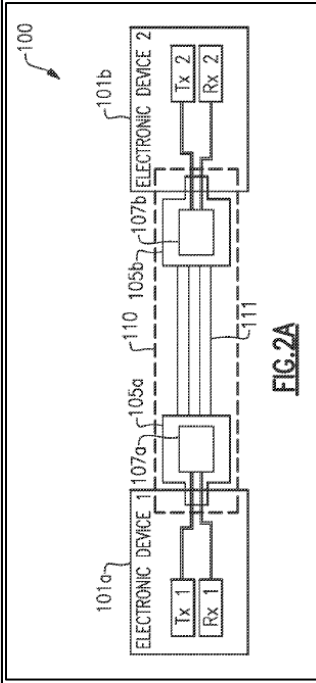


FIG. 4A

Lugthart 431, Figure 4A.

Claim 15



Lugthart 431, Figure 2A.

[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 105b. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.

Lugthart 431, ¶107.

Exhibit A-2

Claim 15

[0143] FIG. 4A illustrates an example of a communication system 200 including a first transceiver 10a connected to another similar transceiver 10b by a cable 205. The first and second transceivers 10a, 10b are implemented in a manner similar to that of the transceiver 10 of FIG. 1A, with differential signaling used on the host and line sides of the transceivers.

Lugthart 431, ¶143.

[0144] Although the communication system 200 of FIG. 2A is shown as including transceivers similar to the transceiver 10 of FIG. 1A, other configurations are possible. For example, any of the transceivers shown in FIGS. 1A-1D can communicate with one another over a cable.

Lugthart 431, ¶144.

[0145] As shown in FIG. 4A, the first and second transceivers 10a, 10b have a host side for facing an electronic device and a line side for facing the cable 205. For example, with reference back to FIG. 2A, the first transceiver 10a can communicate with a first electronic device 101a and the second transceiver 10b can communicate with a second electronic device 101b. Thus, the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable 205 and an ingress path configured to transport signals from the cable 205 to the electronic device. For example, the first transceiver 10a includes an egress path for transmitting signals from a first electronic device to the cable 205 and an ingress path for providing signals received over the cable 205 to the first electronic device. Similarly, the second transceiver 10b includes an egress path for transmitting signals from a

Lugthart 431, ¶145.

Exhibit A-2

<p>Claim 15</p>	<p>To the extent that this limitation is not disclosed, either explicitly or inherently, by Lughart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lughart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>15[b] inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,</p>	<p>Lughart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="636 787 1094 1465" style="border: 1px solid black; padding: 5px;"> <p>[0058] In certain configurations, the transceivers can implement a serializer/deserializer (SerDes) function. For example, in certain implementations each transceiver can be a full duplex multiplexer and re-timer capable of receiving multiple (e.g., 2, 4, or more) signals from a host via a host-side interface. The transceiver multiplexes the received signals for transmission via a line-side interface over the cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved via multi-level modulation encoding, for example. In one non-limiting embodiment, each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable.</p> </div> <p>Lughart 431, ¶58.</p>

Exhibit A-2

Claim 15

[0059] The transceiver can also be configurable in different operational modes. For instance, depending on the mode, the transceiver can handle different numbers of host-side data streams having variable data rates. In one embodiment, the transceiver operates in a first operational mode to translate two host-side 20 Gbit/s NRZ data streams into a single PAM-4 40 Gbit/s stream on the line side, and vice versa. In a second operational mode, the transceiver translates four host-side 10 Gbps NRZ data streams into a single PAM-4 40 Gbit/s stream on the line-side, and vice versa. Such flexibility allows the transceiver to be employed in a variety of different contexts, such as in both consumer and data center contexts.

Lugthart 431, ¶59.

[0060] The transceiver in some embodiments includes a timing recovery circuit including a digital clock recovery path having a dedicated, relatively low latency and/or low power analog-to-digital converter (ADC). The data path can include a separate ADC having more bits than the ADC included in the clock recovery path. Different filtering can be used in the clock and data paths. Moreover, the digital output from the clock recovery path can be used to drive a digitally controlled oscillator (DCO) rather than implementing an analog phase-locked loop (PLL), further reducing latency.

Lugthart 431, ¶60.

Exhibit A-2

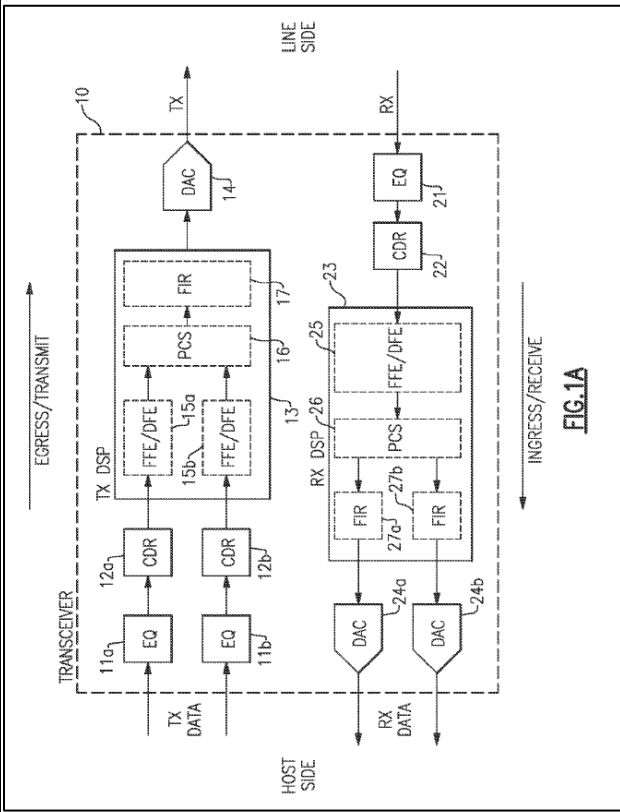
Claim 15

[0063] FIG. 1A is a schematic diagram of one example of a transceiver 10. The transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b.

Lugthart 431, ¶63.

[0065] As shown in FIG. 1A, the first and second transmit path equalizers 11a, 11b include inputs that receive host side transmit data (TX DATA) and outputs electrically connected to inputs of the first and second transmit path CDR circuits 12a, 12b, respectively. The first and second transmit path CDR circuits 12a, 12b further include outputs electrically connected to inputs of the transmit path DSP 13. The transmit path DAC 14 includes an input electrically connected to an output of the transmit path DSP 13 and an output that generates a line side transmit signal (TX). The receive path equalizer 21 includes an input that receives a line side receive signal (RX), and an output electrically connected to an input of the receive path CDR circuit 22. The receive path CDR circuit 22 further includes an output electrically connected to an input of the receive path DSP 23. The receive path DSP 23 further includes outputs electrically connected to inputs of the first and second receive path DACs 24a, 24b. The first and second receive path DACs 24a, 24b further include outputs that generate host side receive data (RX DATA).

Lugthart 431, ¶65.



Lugthart 431, Figure 1A.

Exhibit A-2

Claim 15

[0067] In certain configurations, the transceiver 10 can implement a serializer/deserializer (SerDes) function or operation. For example, in one embodiment, the transceiver 10 can operate as a full duplex multiplexer and re-timer capable of receiving multiple (for example, 2, 4, or more) signals from a host via a host-side interface. Additionally, the transceiver 10 can multiplex the received host-side transmit signals for transmission via a line-side interface over a cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved, for example, via multi-level modulation encoding. In one non-limiting example, an egress/transmit path of the transceiver 10 is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals on the host side and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission to the line side over the cable. Conversely, an ingress/receive path of the transceiver in such an example is capable of receiving a single 40 Gbit/s PAM-4 signal on the line side and de-multiplexing this signal into dual 20 Gbit/s NRZ signals for communication to the host side.

Lugthart 431, ¶67.

Exhibit A-2

<p>Claim 15</p>	<p>[0068] FIG. 1A illustrates the host side transmit data as including two signals and the line side transmit data as including one signal (e.g., via a multiplexing operation), and illustrates the line side receive data as including one signal and the host side receive data as including two signals (via a de-multiplexing operation). However, other configurations are possible, including configurations with additional signals on the host side and/or line side. For example, the first and second receive path DACs 24a, 24b can be replicated in parallel to include, for instance, 10, 20, or 40 or more DACs to provide wider RX DATA bandwidth. Similarly, the first and second transmit path equalizers 11a, 11b and the first and second transmit path CDR circuits 12a, 12b can be replicated in provide wider TX DATA bandwidth. In such configurations, different multiplexing, de-multiplexing, and/or modulation formats can be employed, as appropriate.</p> <p>Lugthart 431, ¶68.</p>
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Exhibit A-2

<p>Claim 15</p>	<p>[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.</p> <p>Lugthart 431, ¶72.</p>
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Exhibit A-2

Claim 15

[0116] In various implementations, the packaging can have a design and a form factor similar to the packaging defined by an existing interface standard (e.g., Thunderbolt Gen1/Gen2 or USB 2.0/3.0), although the packaging can have some other form factor. The packaging can comprise materials suitable for electronic and computer interfaces, such as plastic, metal or a composite material. Each of the transceiver assemblies **105a** and **105b** has an input port that is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device **101a**, **101b**, and an output port that is connected to the cable. The input port can include a connector similar to connectors of existing interface standards, including, but not limited to, Thunderbolt, USB 2.0/3.0, small form-factor pluggable (SFP), enhanced small form-factor pluggable (SFP+), and/or quad small form-factor pluggable (QSFP).

Lugthart 431, ¶116.

[0118] In certain embodiments, the transceiver assemblies **105a** and **105b** implement an egress path by: (a) receiving at least two differential signals from a host device; (b) digitally re-timing, conditioning, and multiplexing the received differential signals; and (c) transmitting the multiplexed signal as a multi-level modulated signal (e.g., PAM-4) over the cable.

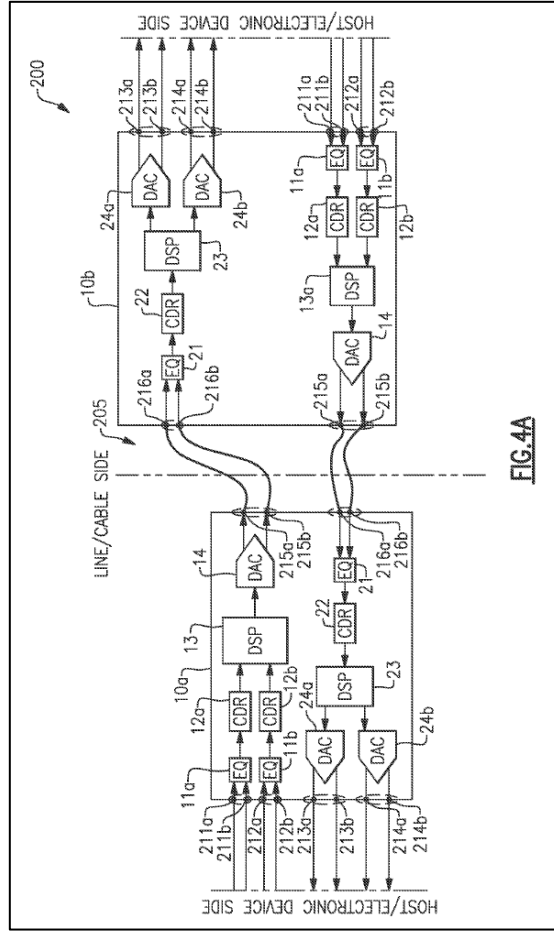
Lugthart 431, ¶118.

Exhibit A-2

Claim 15

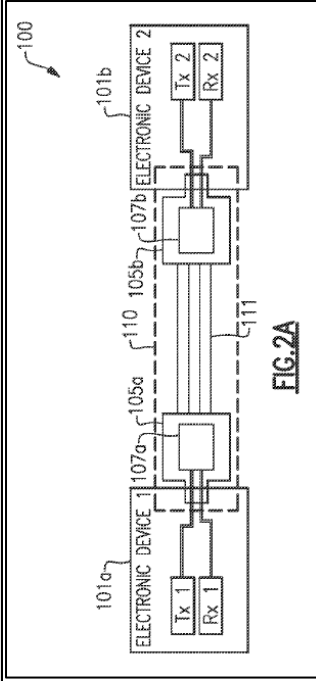
[0119] In certain embodiments, the transceiver assemblies are further configured to implement an ingress path by: (a) receiving a multi-level modulated signal (e.g., PAM-4) from the cable; (b) digitally conditioning and de-multiplexing the received multi-level modulated signal; and (c) transmitting the de-multiplexed signals as an analog signal to the host device.

Lugthart 431, ¶119.



Lugthart 431, Figure 4A.

Claim 15



Lugthart 431, Figure 2A.

[0107] FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 105b. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111.

Lugthart 431, ¶107.

Exhibit A-2

Claim 15

[0143] FIG. 4A illustrates an example of a communication system 200 including a first transceiver 10a connected to another similar transceiver 10b by a cable 205. The first and second transceivers 10a, 10b are implemented in a manner similar to that of the transceiver 10 of FIG. 1A, with differential signaling used on the host and line sides of the transceivers.

Lugthart 431, ¶143.

[0144] Although the communication system 200 of FIG. 2A is shown as including transceivers similar to the transceiver 10 of FIG. 1A, other configurations are possible. For example, any of the transceivers shown in FIGS. 1A-1D can communicate with one another over a cable.

Lugthart 431, ¶144.

[0145] As shown in FIG. 4A, the first and second transceivers 10a, 10b have a host side for facing an electronic device and a line side for facing the cable 205. For example, with reference back to FIG. 2A, the first transceiver 10a can communicate with a first electronic device 101a and the second transceiver 10b can communicate with a second electronic device 101b. Thus, the transceivers 10a, 10b each include an egress path configured to transport signals from an electronic device towards the cable 205 and an ingress path configured to transport signals from the cable 205 to the electronic device. For example, the first transceiver 10a includes an egress path for transmitting signals from a first electronic device to the cable 205 and an ingress path for providing signals received over the cable 205 to the first electronic device. Similarly, the second transceiver 10b includes an egress path for transmitting signals from a

Lugthart 431, ¶145.

Exhibit A-2

<p>Claim 15</p>	<p>To the extent that this limitation is not disclosed, either explicitly or inherently, by Lughart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lughart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>15[c] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.</p>	<p>Lughart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="636 789 1070 1465" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lughart 431, ¶71.</p>

Exhibit A-2

Claim 15

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

Exhibit A-2

<p>Claim 15</p>	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>
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Exhibit A-2

Claim 15

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

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Claim 15	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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O. DEPENDENT CLAIM 16

<p>Claim 16</p>	
<p>16. The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively, each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="415 762 850 1436" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>

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Claim 16

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

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<p>Claim 16</p>	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>
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Claim 16

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

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Claim 16	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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P. DEPENDENT CLAIM 17

<p>Claim 17</p> <p>17. The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="418 764 850 1436" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>
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Claim 17

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

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<p>Claim 17</p>	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>
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Claim 17

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

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Claim 17	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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Q. DEPENDENT CLAIM 18

<p>Claim 18</p> <p>18. The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="418 764 850 1436" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>
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Claim 18

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

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<p>Claim 18</p>	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>
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Claim 18

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

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Claim 18	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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Claim 19

<p>Claim 19</p> <p>19. The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="415 762 850 1436" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>
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Claim 19

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

Lugthart 431, ¶172.

[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

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<p>Claim 19</p>	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>
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Claim 19

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

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Claim 19	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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Claim 20

<p>Claim 20</p> <p>20. The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.</p>	<p>Lugthart 431 discloses and/or renders obvious this limitation.</p> <div data-bbox="415 762 850 1436" style="border: 1px solid black; padding: 5px;"> <p>[0071] The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.</p> </div> <p>Lugthart 431, ¶71.</p>
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Claim 20

[0072] The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.

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[0172] The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.

Lugthart 431, ¶172.

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<p>Claim 20</p>	<p>[0206] Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).</p> <p>Lugthart 431, ¶206.</p>
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Claim 20

[0344] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The steps of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above also may be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

Lugthart 431, ¶344.

To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart 431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart 431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of

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Claim 20	ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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