

Exhibit A-6

Invalidity of U.S. Patent No. 10,877,233 (the “’233 Patent”) in View of Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Refimer (“DS250DF410”)

DS250DF410 was published in October 2019. DS250DF410 qualifies as prior art under at least 35 U.S.C. § 102(a) (AIA).

The Administrative Law Judge has not yet construed the claims and therefore the meaning of the terms in the claims has yet to be resolved. The support identified here for limitations of the Asserted Claims of the ’233 Patent is responsive to Complainant’s apparent infringement contentions in its Complaint, which Respondents disagree with. As such, nothing in Respondents’ claim charts should be construed as an admission regarding infringement, either literally or under the doctrine of equivalents, or as an admission regarding Respondents’ understanding of the proper scope of the Asserted Claims of the ’233 Patent.

All cross-references should be understood to include material that is cross-referenced within the cross-reference. Where a particular Figure is cited, the citation should be understood to encompass the caption and description of the Figure as well as any text relating to or describing the Figure. Conversely, where particular text referring to a Figure is cited, the citation should be understood to include the Figure as well. Respondents reserve the right to rely on additional citations or sources of evidence that also may be applicable, or that may become applicable in light of claim construction, changes in Complainant’s infringement and/or domestic industry contentions, and/or information obtained during discovery as the Investigation progresses.

To the extent Complainant alleges that DS250DF410 does not disclose any particular limitation of the Asserted Claims of the ’233 Patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the ’233 Patent to modify DS250DF410 and/or to combine the teachings of DS250DF410 with other prior art references, including but not limited to the prior art references cited in the Cover Pleading and the relevant section(s) of claim charts for other prior art references for the ’233 Patent in a manner that would have rendered the Asserted Claims invalid as obvious.

Because Complainant has yet to identify any limitation of the Asserted Claims of the ’233 Patent that it contends is not fully disclosed by DS250DF410, either alone or in combination with other prior art cited by Respondents, Respondents expressly reserve the right to rebut any such contention, including by identifying additional obviousness combinations, if any such contention is made by Complainant. Respondents further reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the Cover Pleading.

A. INDEPENDENT CLAIM 1

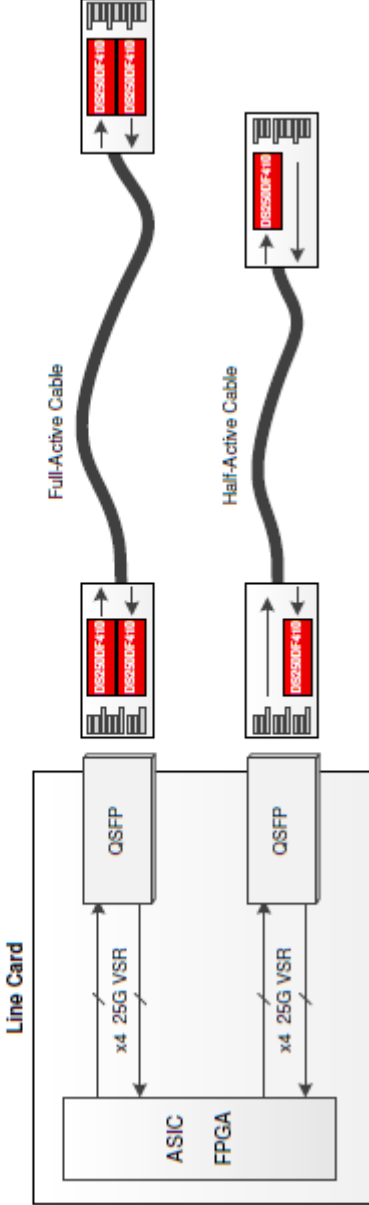
<p>Claim 1</p> <p>1 [pre] A cable that comprises:</p>	<p>Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)</p> <p>To the extent the preamble is limiting, DS250DF410 discloses and/or renders obvious this limitation.</p> <p>9.2.2 Active Cable Applications</p> <p>The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.</p> <p>Figure 20 illustrates these configurations, Figure 21 shows an example simplified schematic for a half-active cable application, and Figure 22 shows an example simplified schematic for a full-active cable application.</p>  <p>Figure 20. Active Cable Application Block Diagram</p> <p>DS250DF410, 81.</p>
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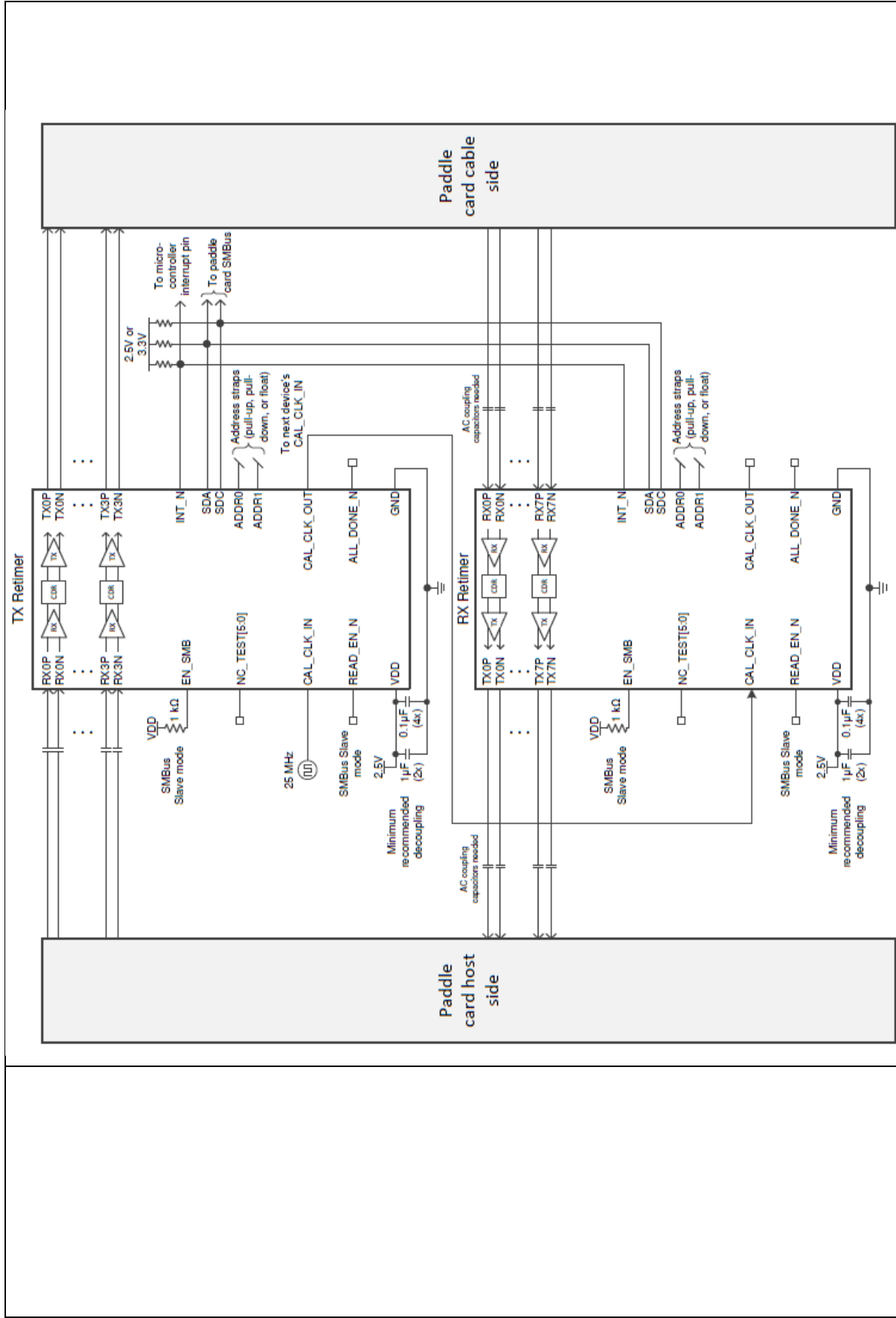


Figure 22. Full-Active Cable Application Schematic

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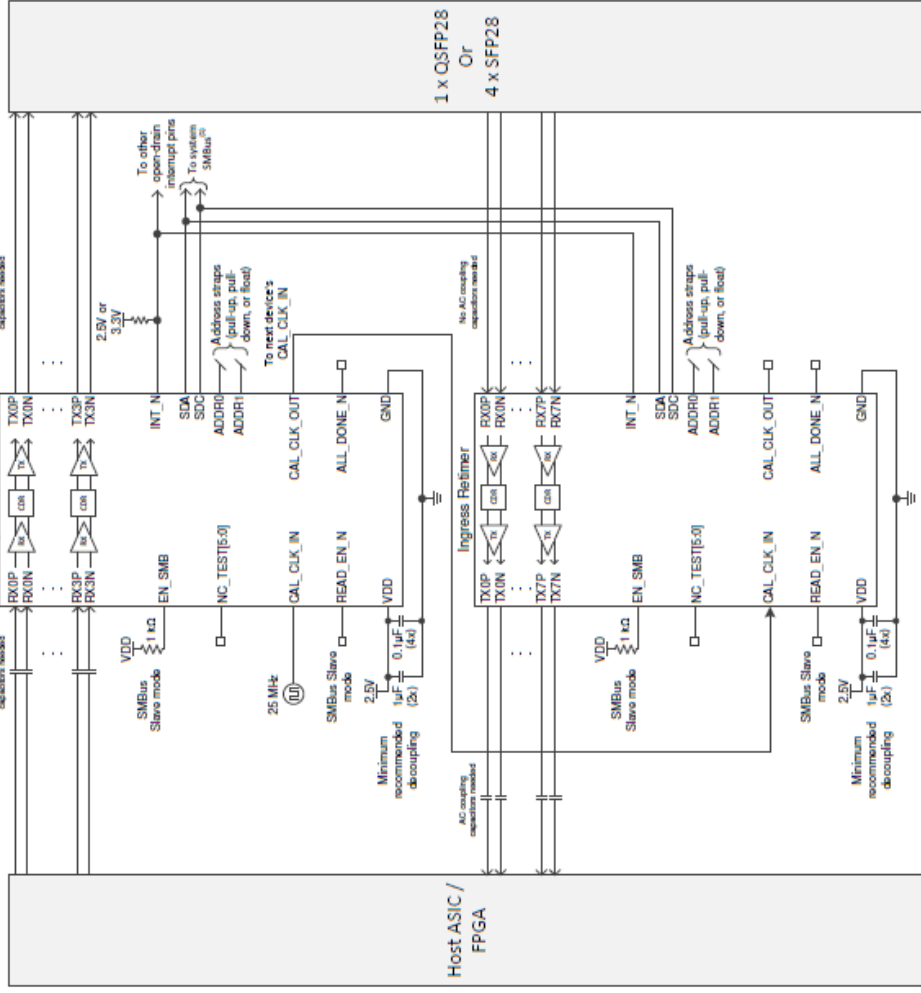
<p>Claim 1</p>	<p>Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”) DS250DF410, 83.</p>								
<p>1[a] a first data recovery and remodulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface</p>	<p style="text-align: center;">Table 14. Full-Active Cable Application Design Guidelines</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">DESIGN PARAMETER</th> <th style="text-align: center;">REQUIREMENT</th> </tr> </thead> <tbody> <tr> <td>Device placement</td> <td>A full-active QSFP cable will utilize two pieces of DS250DF410 per paddle card. Typically, one device will be placed on each side of the paddle card.</td> </tr> <tr> <td>AC coupling capacitors</td> <td><i>Transmit-side Retimer:</i> 100 nF AC coupling capacitors are required for the RX inputs and are not required for the TX outputs. This link segment will be AC coupled on the paddle card at the opposite end of the cable. <i>Receive-side Retimer:</i> 100 nF AC coupling capacitors are required for the RX inputs and the TX outputs.</td> </tr> <tr> <td>Cable insertion loss</td> <td>The raw cable insertion loss including the insertion loss of the paddle card should be ≤ 35 dB at 25.78125 Gbps Nyquist frequency (12.9 GHz).</td> </tr> </tbody> </table> <p>DS250DF410, 84.</p> <p>To the extent that this preamble is not disclosed, either explicitly or inherently, by DS250DF410, this preamble is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>	DESIGN PARAMETER	REQUIREMENT	Device placement	A full-active QSFP cable will utilize two pieces of DS250DF410 per paddle card. Typically, one device will be placed on each side of the paddle card.	AC coupling capacitors	<i>Transmit-side Retimer:</i> 100 nF AC coupling capacitors are required for the RX inputs and are not required for the TX outputs. This link segment will be AC coupled on the paddle card at the opposite end of the cable. <i>Receive-side Retimer:</i> 100 nF AC coupling capacitors are required for the RX inputs and the TX outputs.	Cable insertion loss	The raw cable insertion loss including the insertion loss of the paddle card should be ≤ 35 dB at 25.78125 Gbps Nyquist frequency (12.9 GHz).
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Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

port via a first end connector plug;

Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Front-Port Application Schematic

DS250DF410, 78.

Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

Figure 20 illustrates these configurations, Figure 21 shows an example simplified schematic for a half-active cable application, and Figure 22 shows an example simplified schematic for a full-active cable application.

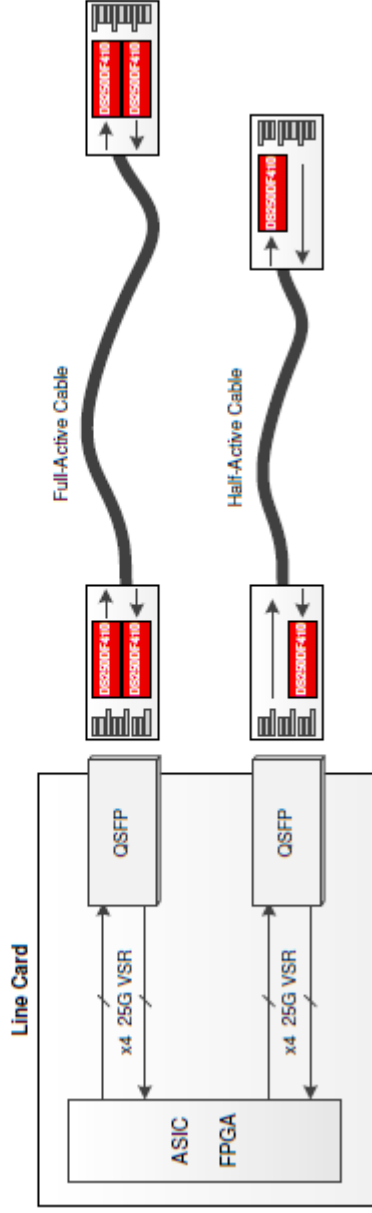


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

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Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

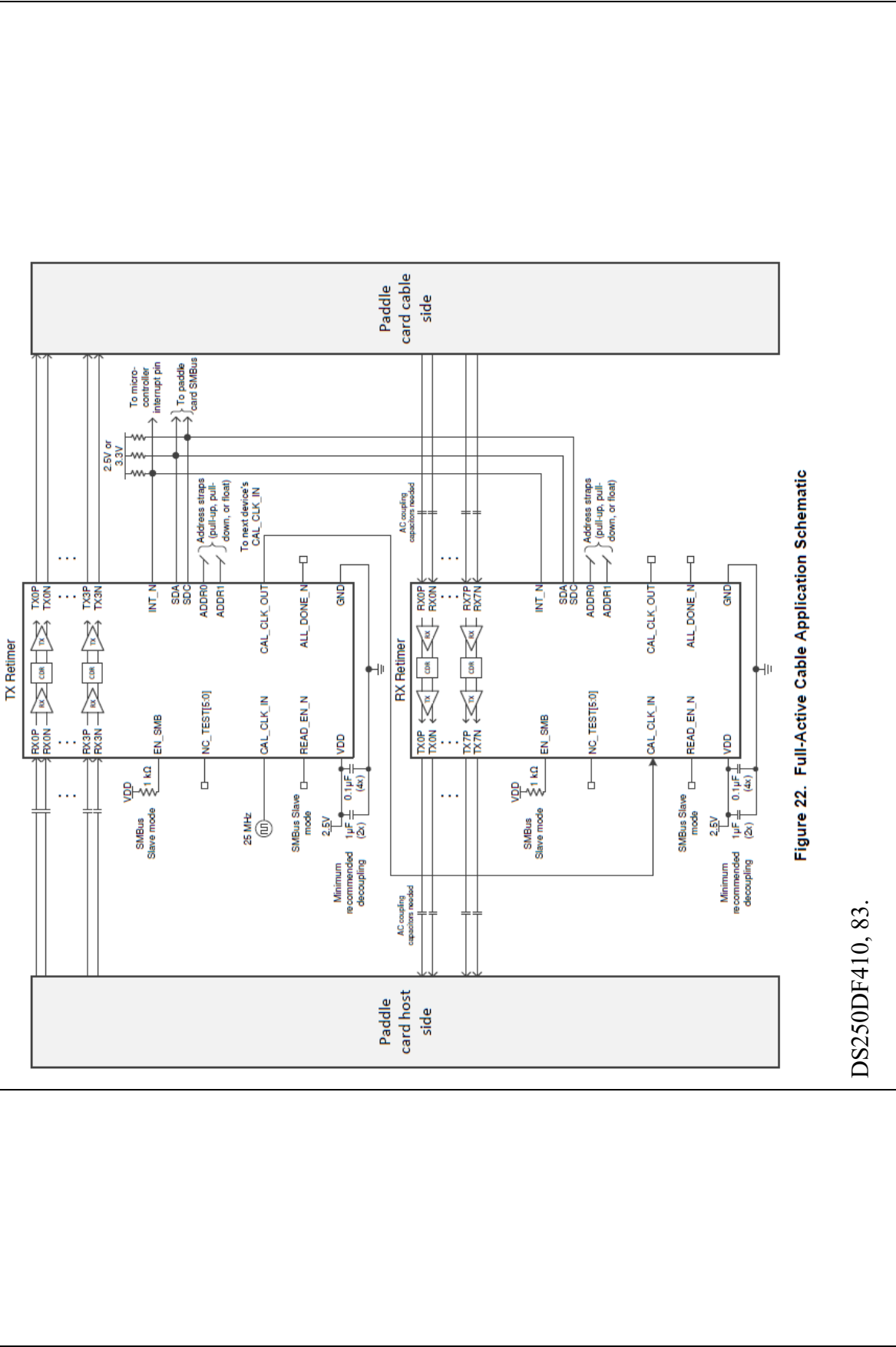


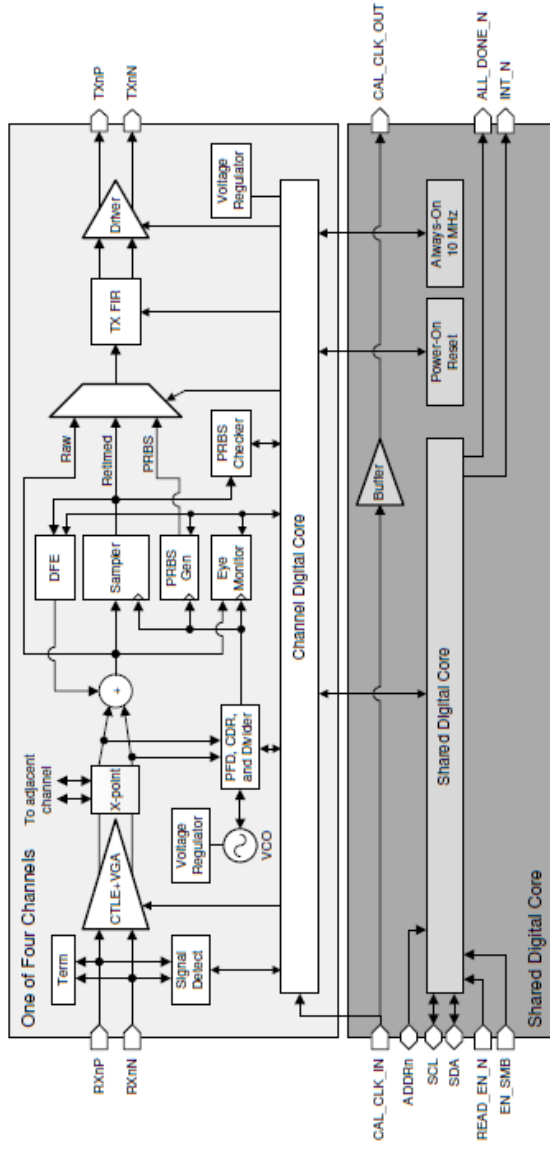
Figure 22. Full-Active Cable Application Schematic

DS250DF410, 83.

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Claim 1	Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)
	<p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>

Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”) 8.2 Functional Block Diagram



DS250DF410, 17.

<p>Claim 1</p>	<p>Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)</p> <p>8.3.7 Clock and Data Recovery (CDR)</p> <p>The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes.</p> <p>By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF410 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator.</p> <p>The CDR requires the following to be properly configured:</p> <ul style="list-style-type: none"> • 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN). • Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF410, 19.</p> <p>8.3.9 Differential Driver with FIR Filter</p> <p>The DS250DF410 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. C[0] can take on values in the range [-31, +31]. C[-1] and C[+1] can take on values in the range [-15, 15].</p>
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Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

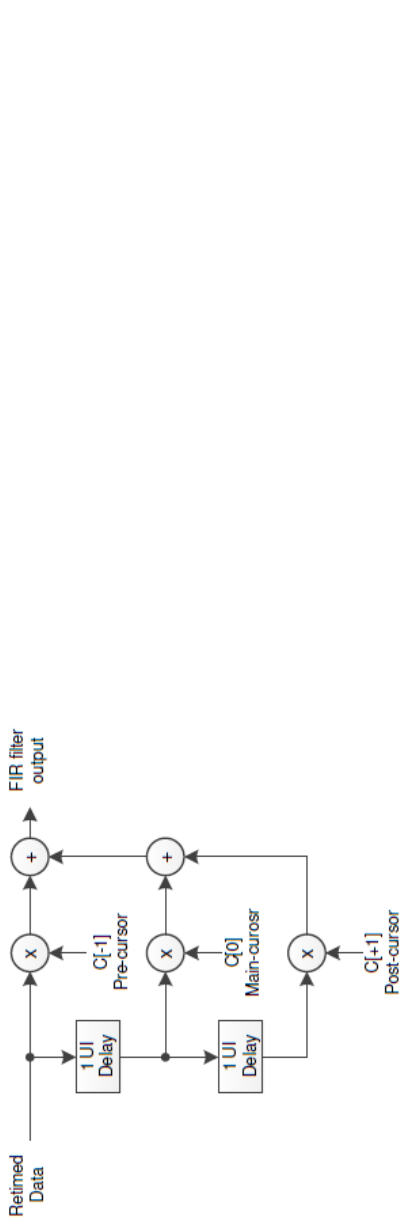


Figure 7. FIR Filter Functional model

When utilizing the FIR filter, it is important to abide by the following general rules:

- $|C[-1]| + |C[0]| + |C[+1]| \leq 31$; the FIR tap coefficients absolute sum must be less or equal to 31
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
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DS250DF410, 19-20.

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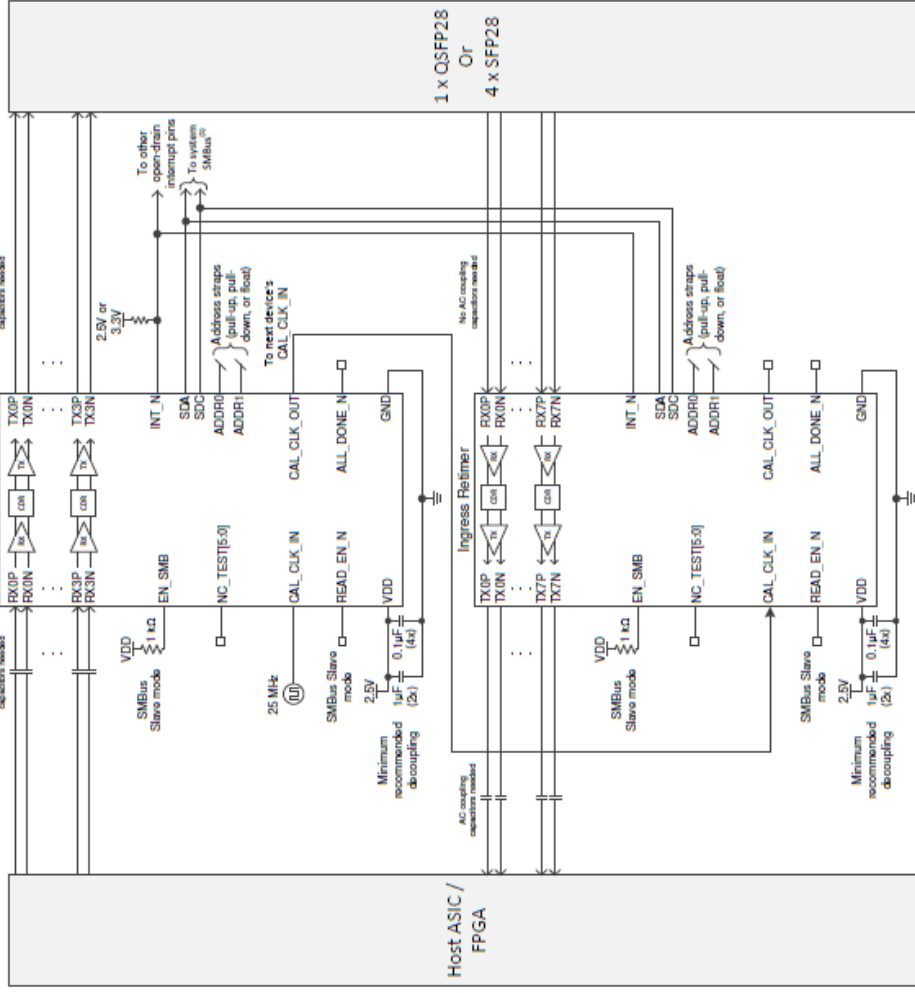
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	<p>knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>1[b] a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p>

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Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.

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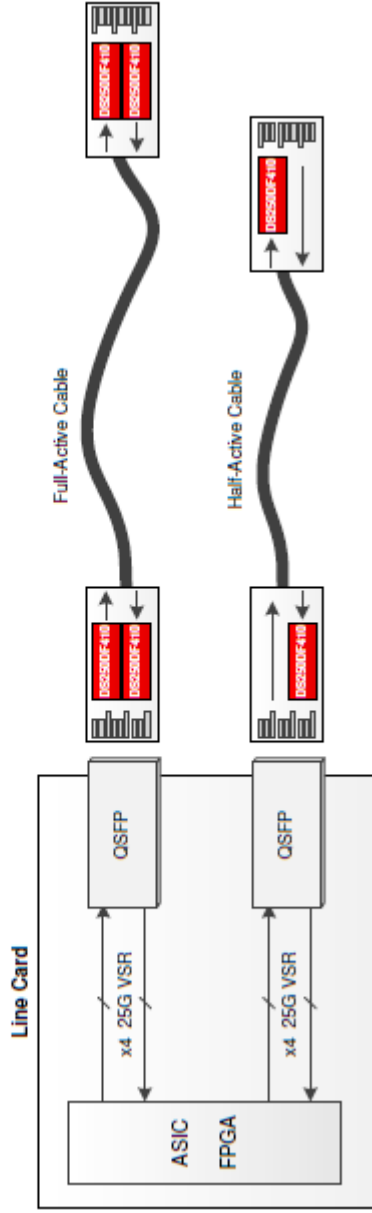


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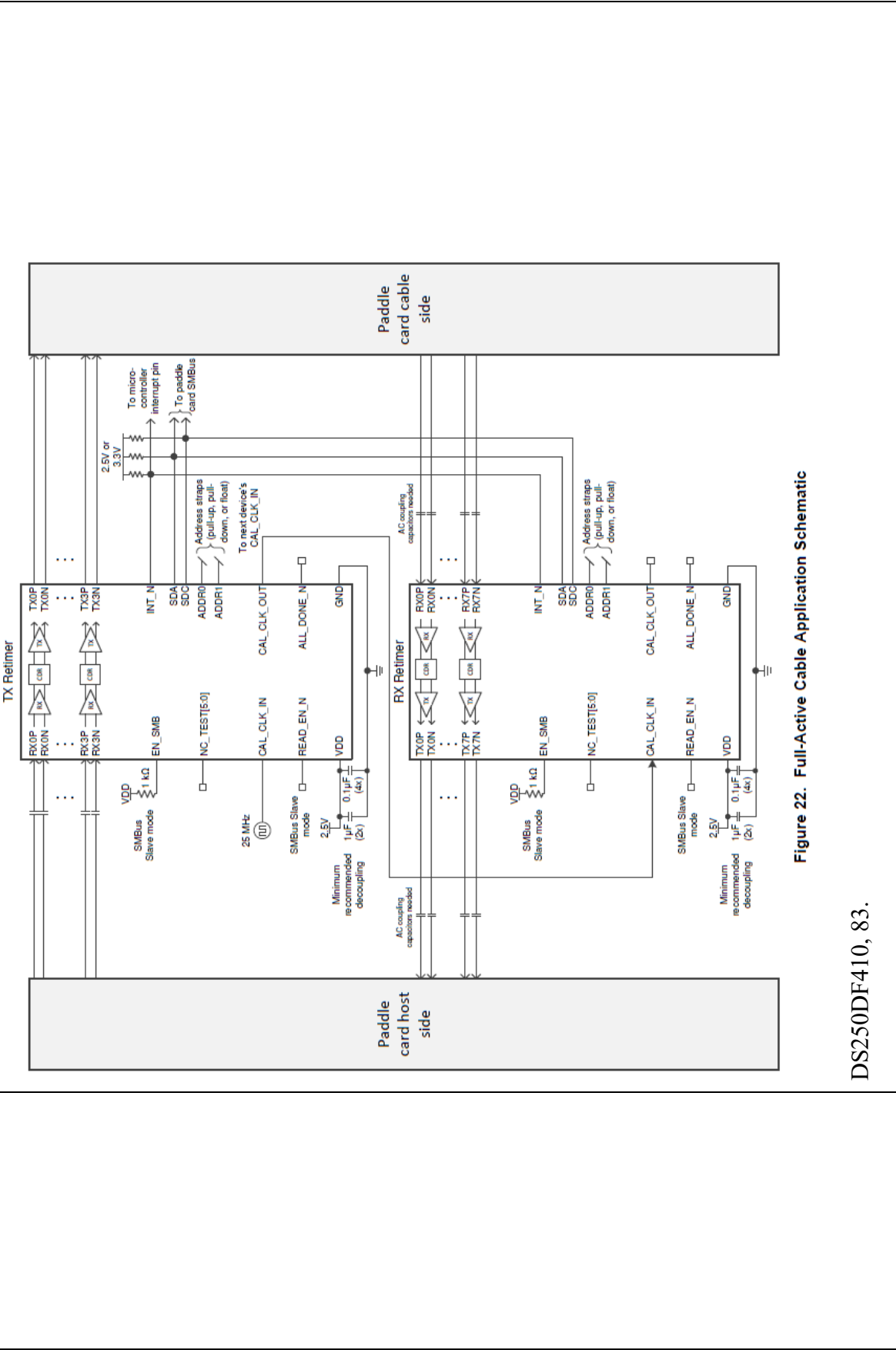


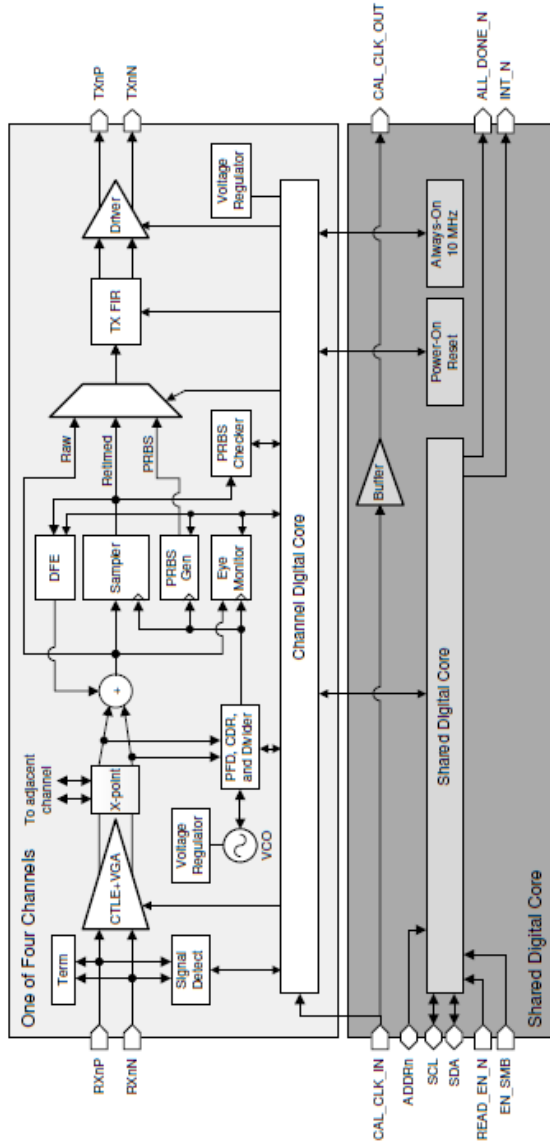
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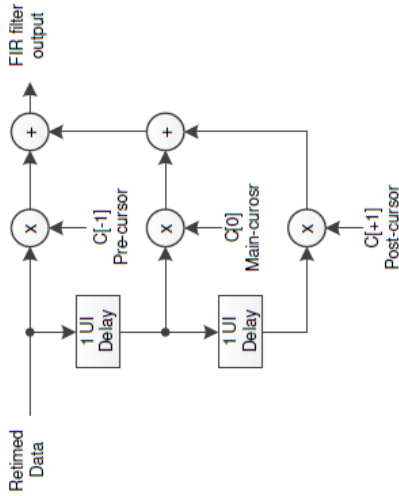


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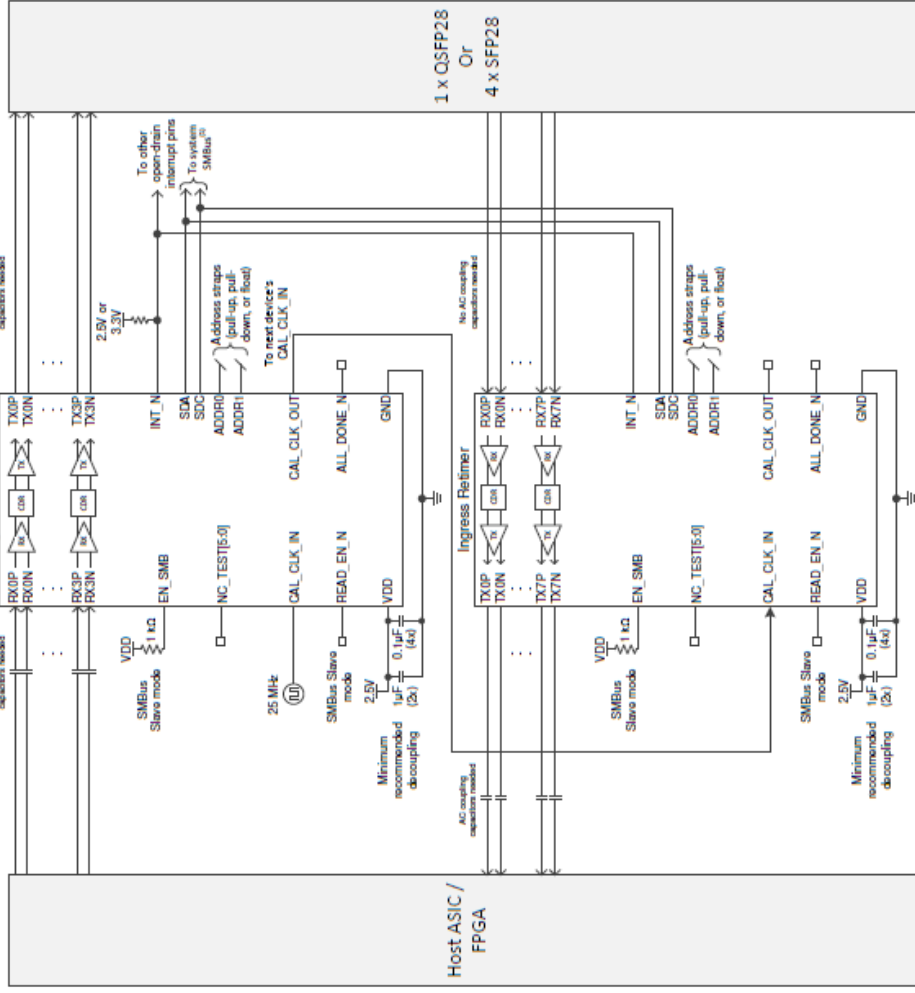
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1[c] electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,	DS250DF410 discloses and/or renders obvious this limitation.

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Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.

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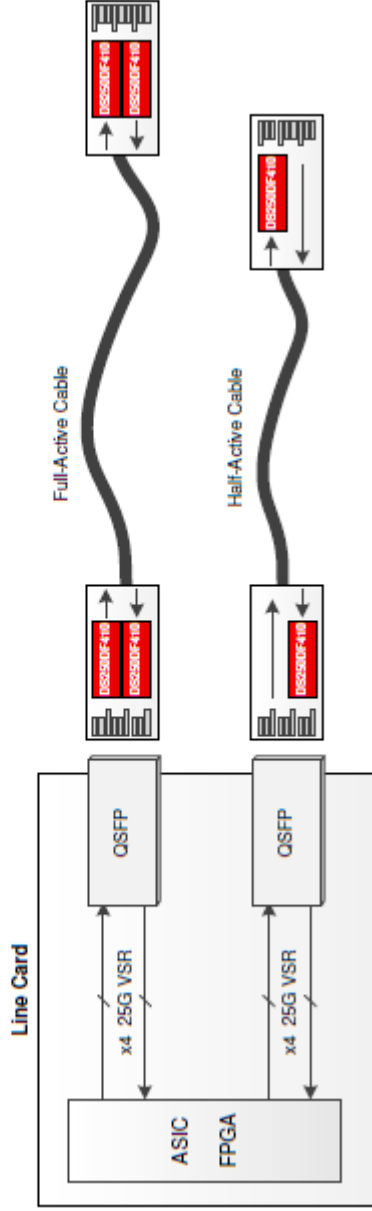


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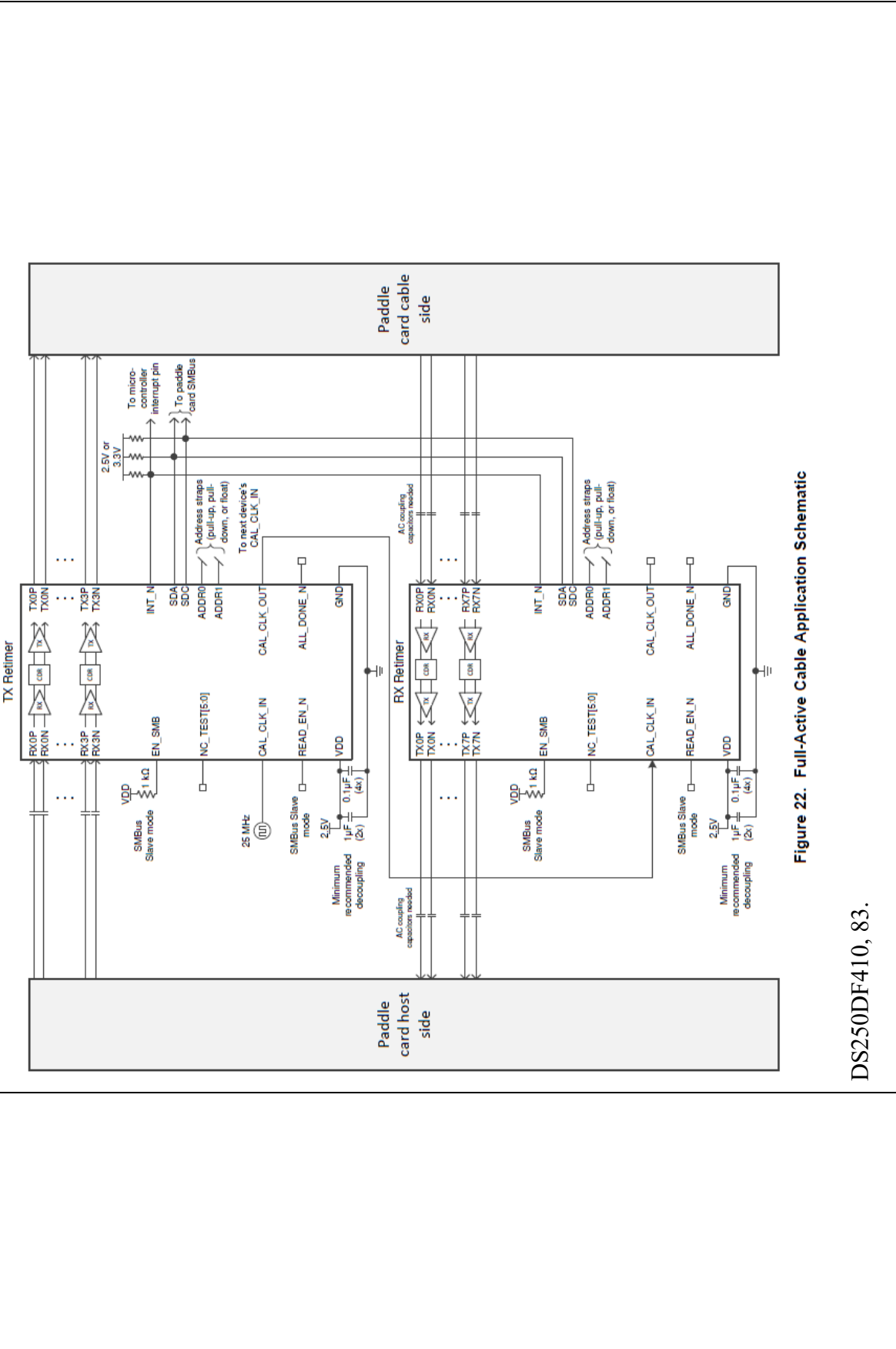


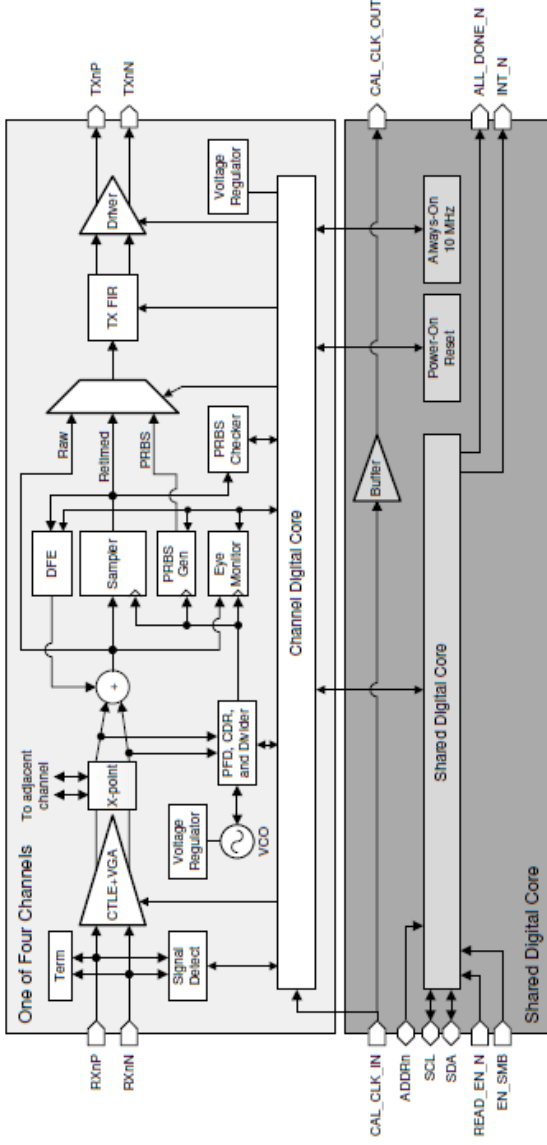
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DS250DF410, 83.

Claim 1	Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)
	<p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>

Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

8.2 Functional Block Diagram



DS250DF410, 17.

To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

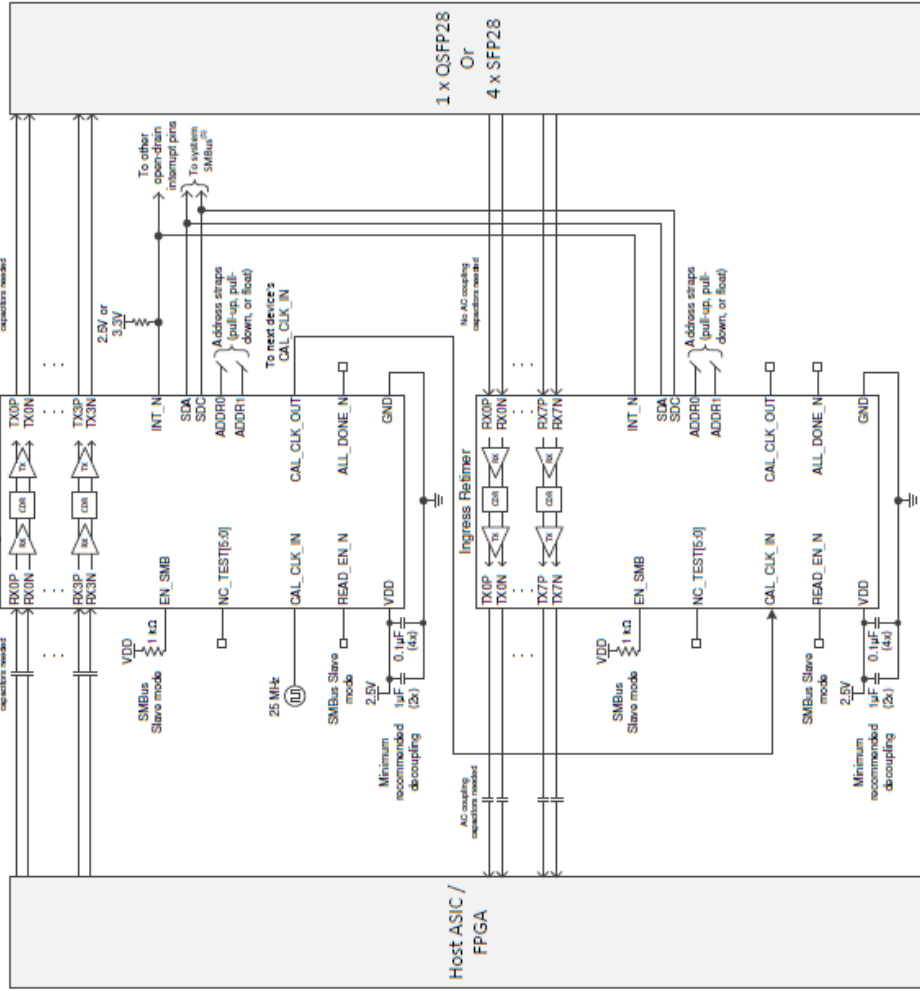
1[d] the first DRP device

DS250DF410 discloses and/or renders obvious this limitation.

Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

converting between said electrical transit signals and said inbound and outbound multilane data streams for the first host interface port, and

Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Front-Port Application Schematic

Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

DS250DF410, 78.

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

Figure 20 illustrates these configurations, Figure 21 shows an example simplified schematic for a half-active cable application, and Figure 22 shows an example simplified schematic for a full-active cable application.

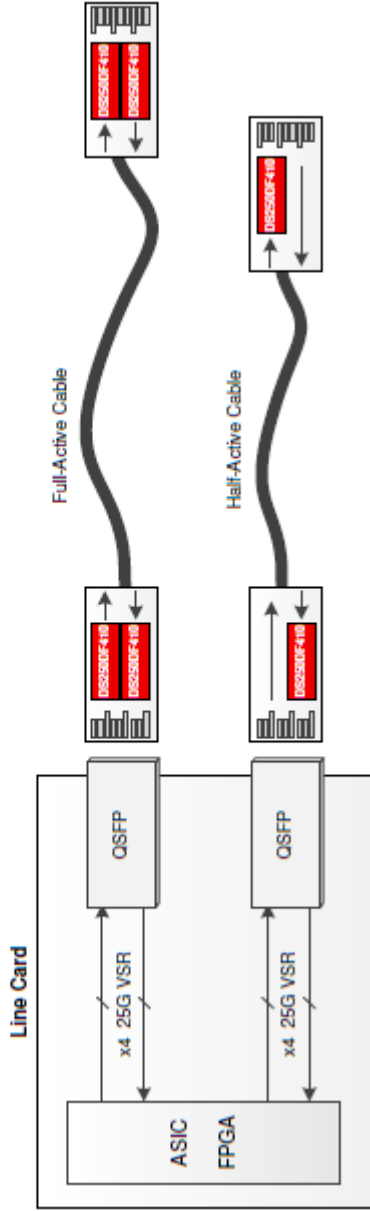


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

Exhibit A-6

Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

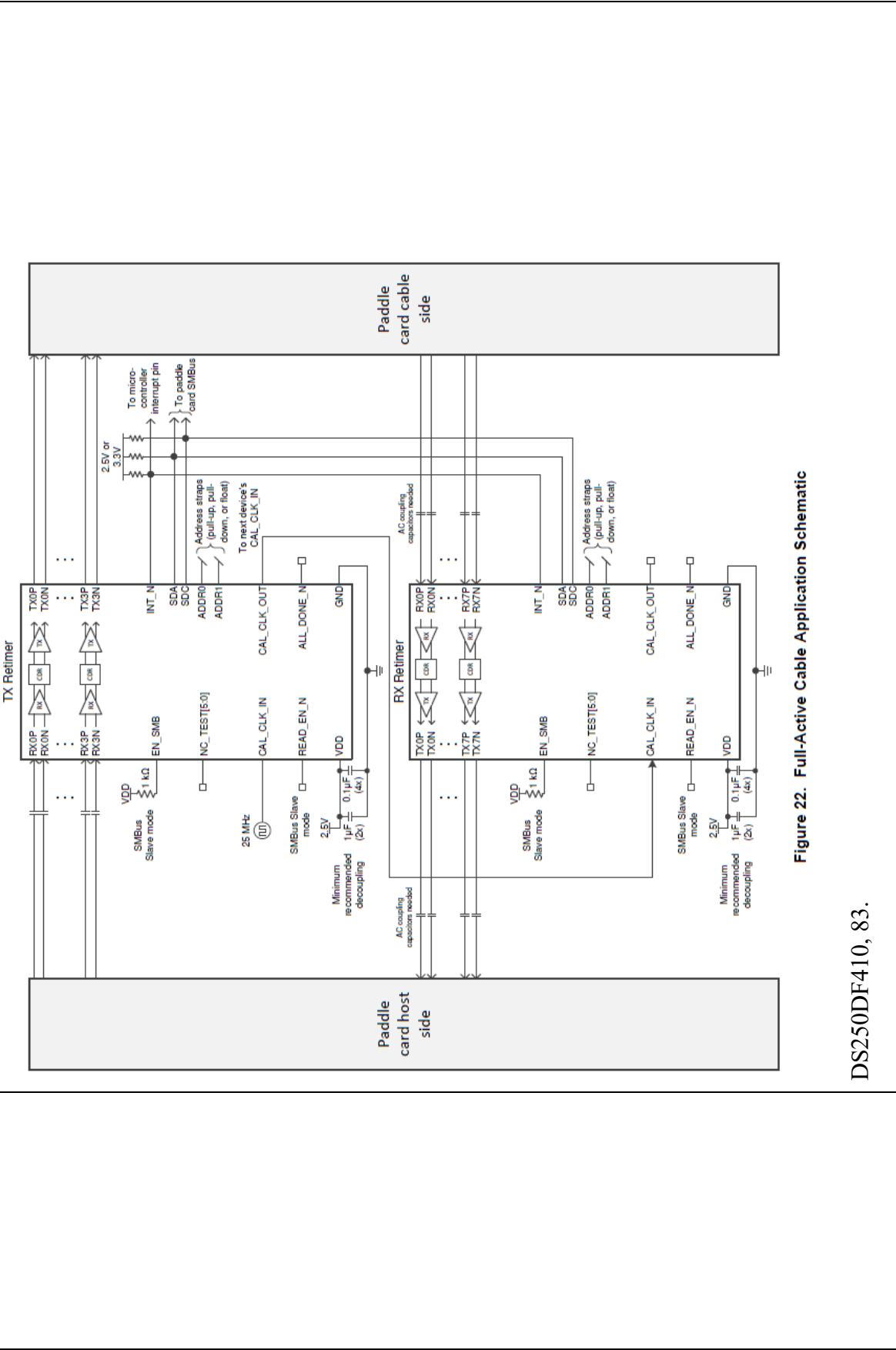
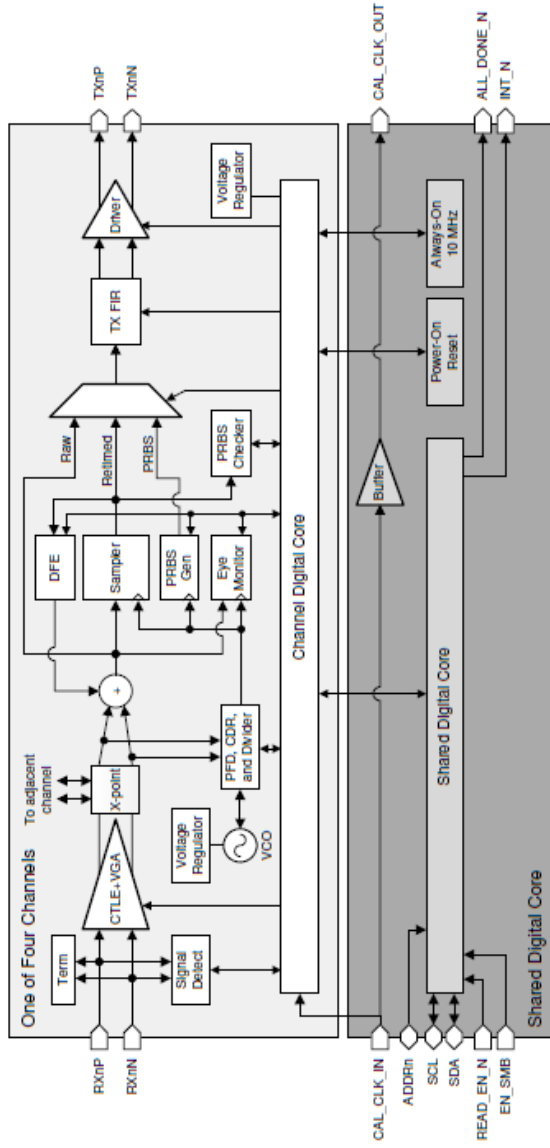


Figure 22. Full-Active Cable Application Schematic

DS250DF410, 83.

<p>Claim 1</p>	<p>Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)</p> <p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”) 8.2 Functional Block Diagram



DS250DF410, 17.

<p>Claim 1</p>	<p>Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)</p> <p>8.3.7 Clock and Data Recovery (CDR)</p> <p>The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes.</p> <p>By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF410 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator.</p> <p>The CDR requires the following to be properly configured:</p> <ul style="list-style-type: none"> • 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN). • Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF410, 19.</p> <p>8.3.9 Differential Driver with FIR Filter</p> <p>The DS250DF410 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. C[0] can take on values in the range [-31, +31]. C[-1] and C[+1] can take on values in the range [-15, 15].</p>
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Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

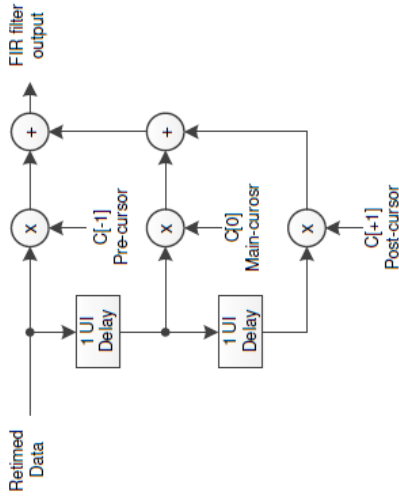


Figure 7. FIR Filter Functional model

When utilizing the FIR filter, it is important to abide by the following general rules:

- $|C[-1]| + |C[0]| + |C[+1]| \leq 31$; the FIR tap coefficients absolute sum must be less or equal to 31
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
- $VOD_{low-frequency} = V_2 - V_5$
- $R_{pre-dB} = 20 * \log_{10} (V_3/V_2)$
- $R_{pst-dB} = 20 * \log_{10} (V_1/V_2)$

DS250DF410, 19-20.

To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or

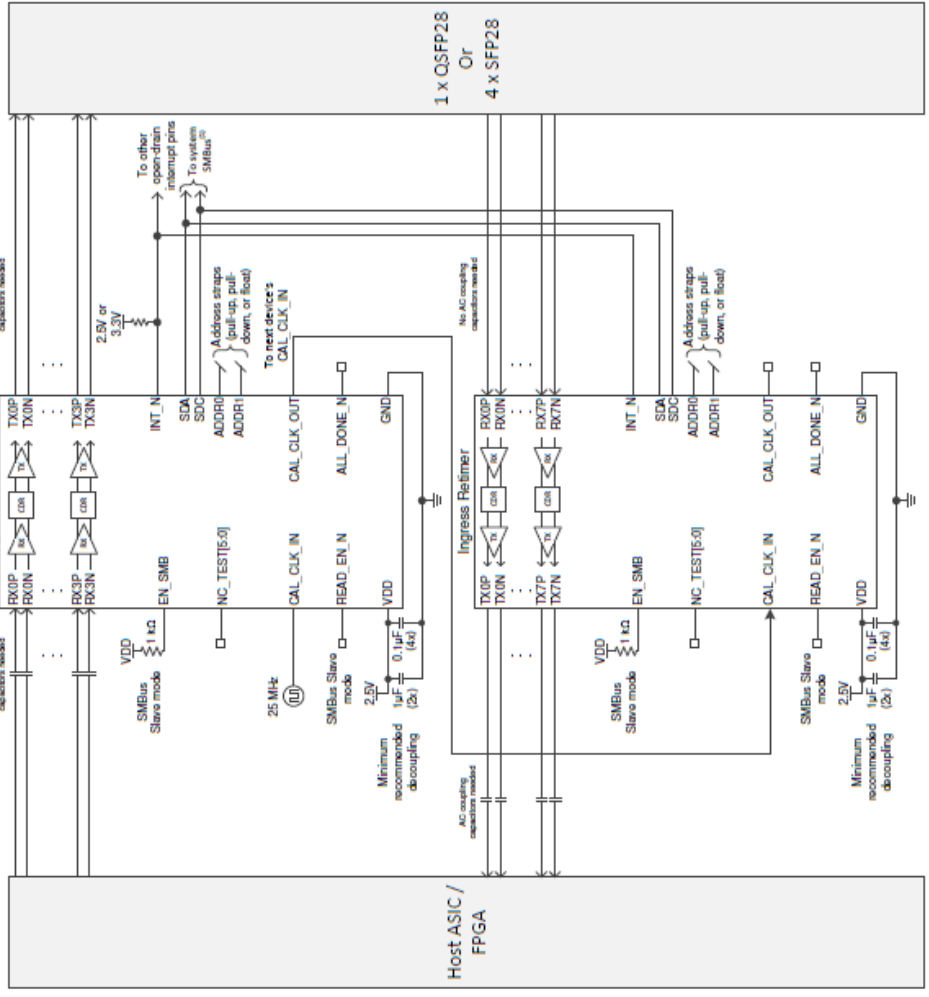
Exhibit A-6

<p>Claim 1</p>	<p>Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”) combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>1[e] the second DRR device converting between said electrical transit signals and said inbound and outbound multilane data streams for the second host interface port,</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p>

Exhibit A-6

Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Front-Port Application Schematic

DS250DF410, 78.

Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

Figure 20 illustrates these configurations, Figure 21 shows an example simplified schematic for a half-active cable application, and Figure 22 shows an example simplified schematic for a full-active cable application.

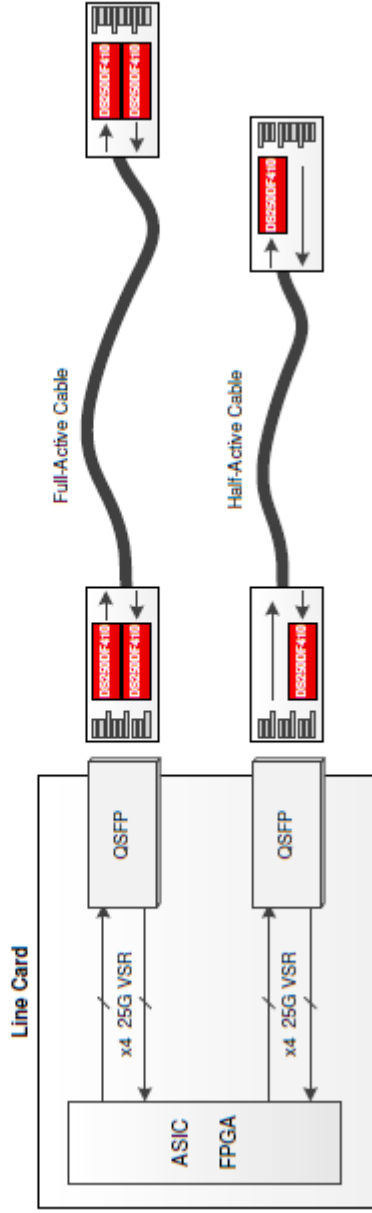


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

Exhibit A-6

Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

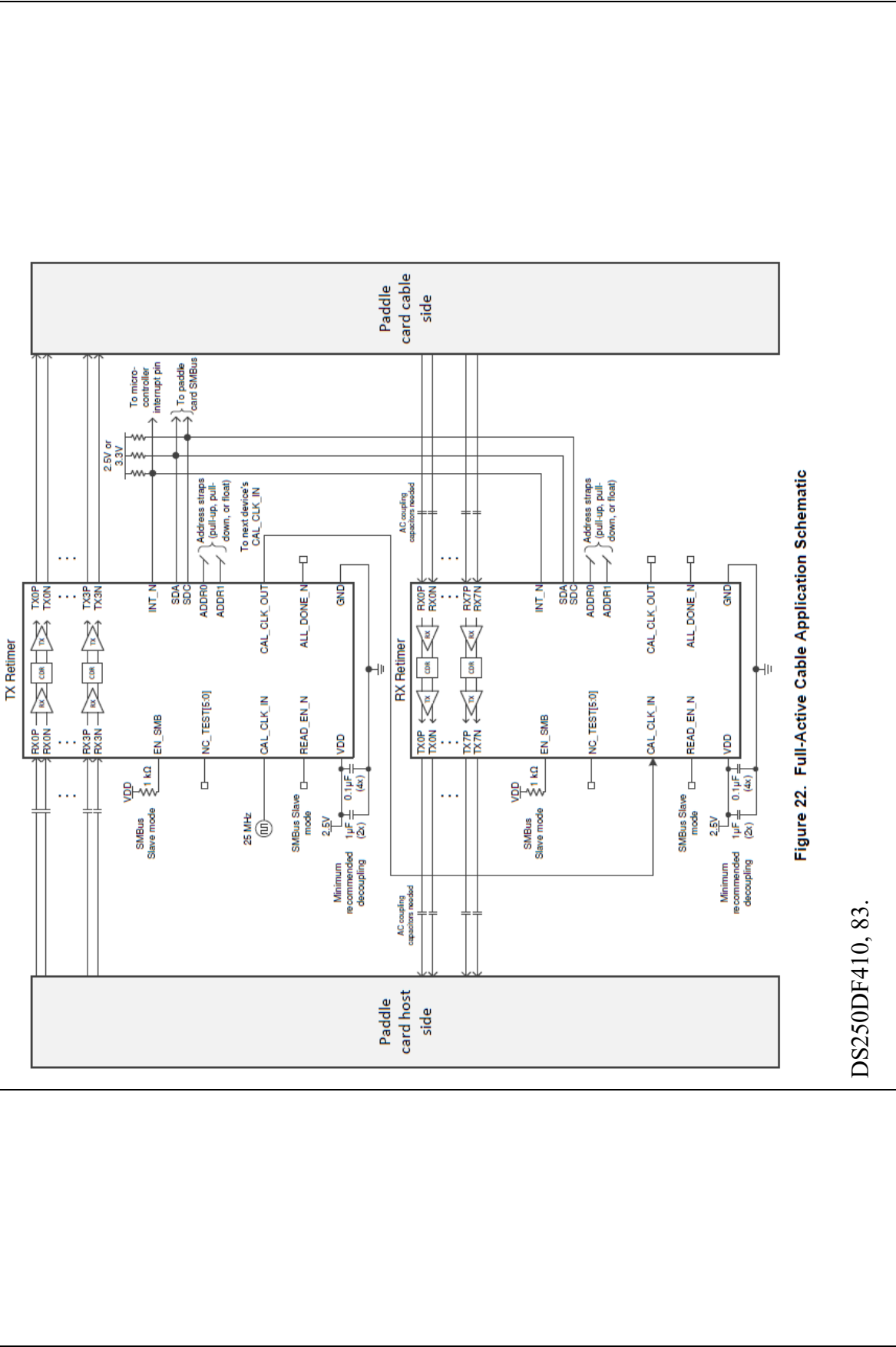
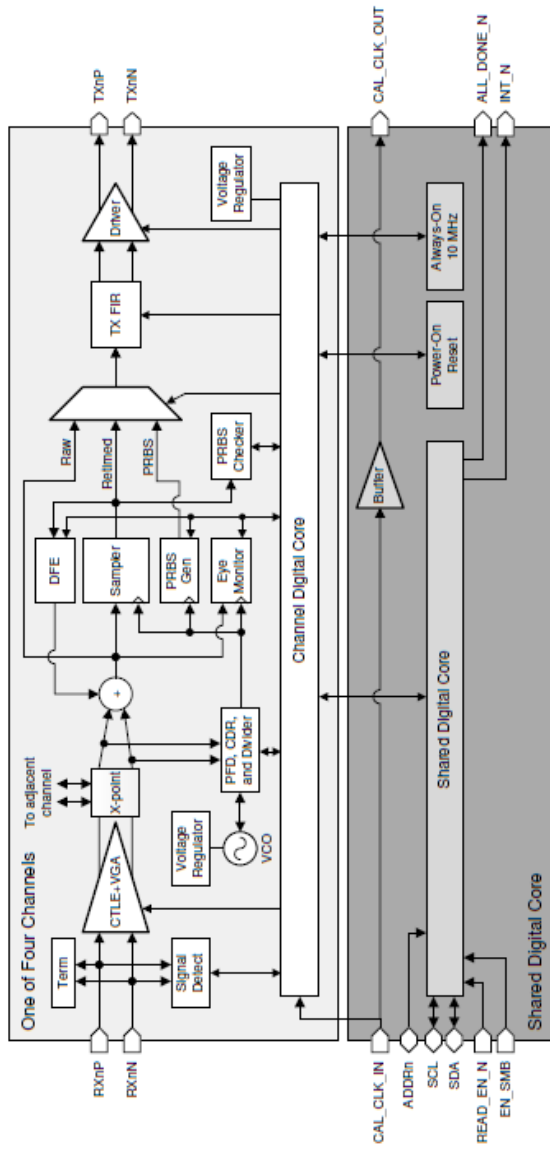


Figure 22. Full-Active Cable Application Schematic

DS250DF410, 83.

<p>Claim 1</p>	<p>Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)</p> <p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”) 8.2 Functional Block Diagram



DS250DF410, 17.

<p>Claim 1</p>	<p>Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)</p> <p>8.3.7 Clock and Data Recovery (CDR)</p> <p>The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes.</p> <p>By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF410 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator.</p> <p>The CDR requires the following to be properly configured:</p> <ul style="list-style-type: none"> • 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN). • Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF410, 19.</p> <p>8.3.9 Differential Driver with FIR Filter</p> <p>The DS250DF410 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. C[0] can take on values in the range [-31, +31]. C[-1] and C[+1] can take on values in the range [-15, 15].</p>
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Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

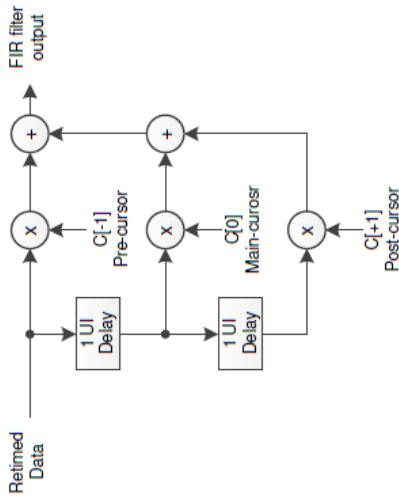


Figure 7. FIR Filter Functional model

When utilizing the FIR filter, it is important to abide by the following general rules:

- $|C[-1]| + |C[0]| + |C[+1]| \leq 31$; the FIR tap coefficients absolute sum must be less or equal to 31
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

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- $VOD_{low-frequency} = V_2 - V_5$
- $R_{pre-dB} = 20 * \log_{10} (V_3/V_2)$
- $R_{pst-dB} = 20 * \log_{10} (V_1/V_2)$

DS250DF410, 19-20.

To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or

Exhibit A-6

<p>Claim 1</p>	<p>Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”) combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>1[f] the first and second DRR devices providing preequalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p> <p>8.3.9.1 Setting the Output V_{OD}, Pre-Cursor, and Post-Cursor Equalization</p> <p>The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.</p>

Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.695	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.890	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+18	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+28	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.195	NA	1.1

INVESTIGATION No. 337-T/
RESPONDENTS' INITIAL INV

Exhibit A-6

Claim 1 Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 1		Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)						
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)		
	6	0	RW	Y	FIR_CO_SGN	Main-cursor sign bit 0: positive 1: negative		
	5	0	RW	Y	RESERVED	RESERVED		
	4	1	RW	Y	FIR_CO[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)		
	3	1	RW	Y	FIR_CO[3]			
	2	0	RW	Y	FIR_CO[2]			
	1	1	RW	Y	FIR_CO[1]			
	0	0	RW	Y	FIR_CO[0]			
	3E	7	0	RW	Y	FIR_PD_TX		
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive	
		5	0	RW	Y	RESERVED	RESERVED	
		4	0	RW	Y	RESERVED	RESERVED	
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)	
2		0	RW	Y	FIR_CN1[2]			
1		0	RW	Y	FIR_CN1[1]			
0	0	RW	Y	FIR_CN1[0]				

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

<p>Claim 1</p>	<p>Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”) DS250DF410, 53-54.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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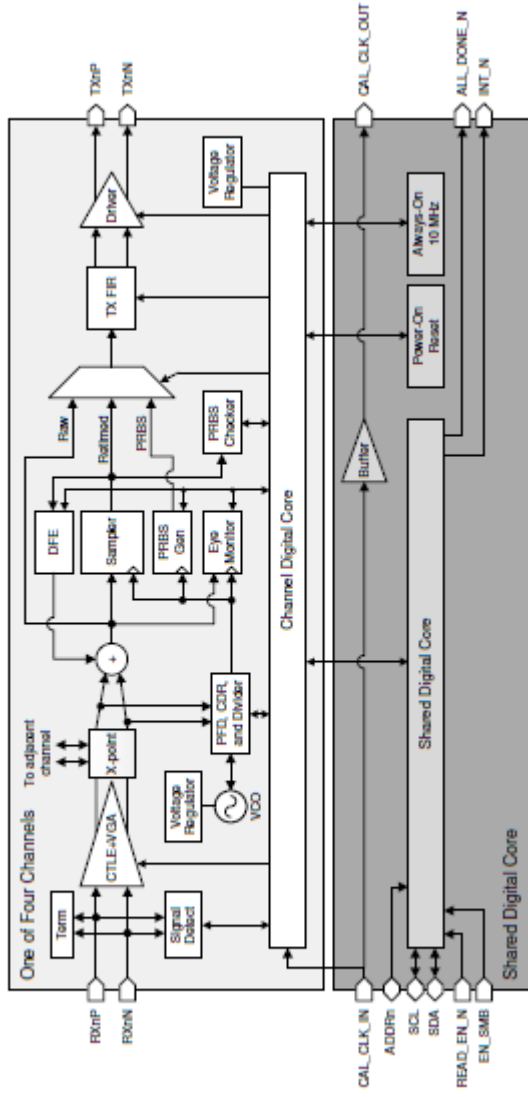
B. DEPENDENT CLAIM 2

<p>Claim 2</p> <p>2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.</p>	<p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Exhibit A-6

Claim 2

8.2 Functional Block Diagram



DS250DF410, 17.

Exhibit A-6

<p>Claim 2</p>	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none">• R - Read only• RW - Read/Write• RWSC - Read/Write, self-clearing
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<p>Claim 2</p>	<p>8.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF410 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other. <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.</p> <p>Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.</p> <p>DS250DF410, 30-31.</p> <p>8.3.9.1 Setting the Output V_{OD}, Pre-Cursor, and Post-Cursor Equalization</p> <p>The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.</p>
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Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

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Exhibit A-6

Claim 2

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPOST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]				
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 2							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0		0	RW	Y	FIR_CN1[0]		

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

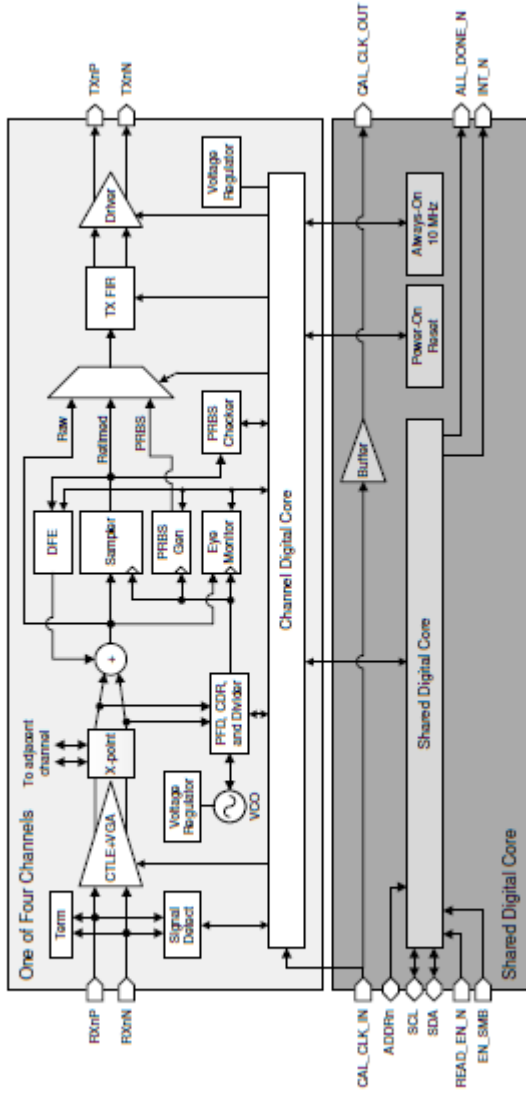
Claim 2	DS250DF410, 53-54. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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C. DEPENDENT CLAIM 3

<p>Claim 3</p> <p>3. The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p> <p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 3

8.2 Functional Block Diagram



DS250DF410, 17.

Exhibit A-6

Claim 3	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing
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<p>Claim 3</p>	<p>8.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF410 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other. <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.</p> <p>Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type command can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.</p> <p>DS250DF410, 30-31.</p> <p>8.3.9.1 Setting the Output V_{OD}, Pre-Cursor, and Post-Cursor Equalization</p> <p>The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.</p>
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Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

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Exhibit A-6

Claim 3

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURS- REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RFPST(dB)
	MAIN-CURS- REG_0x3D[6:0]	POST-CURS- REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 3							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0		0	RW	Y	FIR_CN1[0]		

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

Claim 3	DS250DF410, 53-54. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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D. DEPENDENT CLAIM 4

Claim 4

4. The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.

DS250DF410 discloses and/or renders obvious this limitation.

8.1 Overview

The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.

Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.

Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.

Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.

Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).

The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.

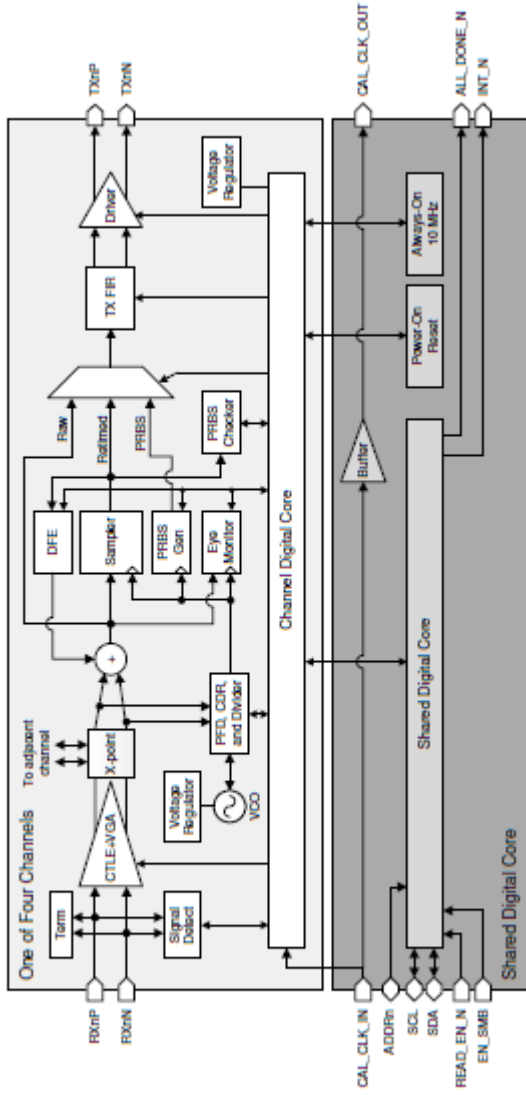
The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.

DS250DF410, 17.

Exhibit A-6

Claim 4

8.2 Functional Block Diagram



DS250DF410, 17.

Exhibit A-6

<p>Claim 4</p>	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none">• R - Read only• RW - Read/Write• RWSC - Read/Write, self-clearing
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<p>Claim 4</p>	<p>8.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF410 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other. <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.</p> <p>DS250DF410, 30-31.</p> <p>8.3.9.1 Setting the Output V_{OD}, Pre-Cursor, and Post-Cursor Equalization</p> <p>The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.</p>
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Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.8	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

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RESPONDENTS' INITIAL INVALIDITY C

Exhibit A-6

Claim 4

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 4							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0		0	RW	Y	FIR_CN1[0]		

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

Claim 4	<p>DS250DF410, 53-54.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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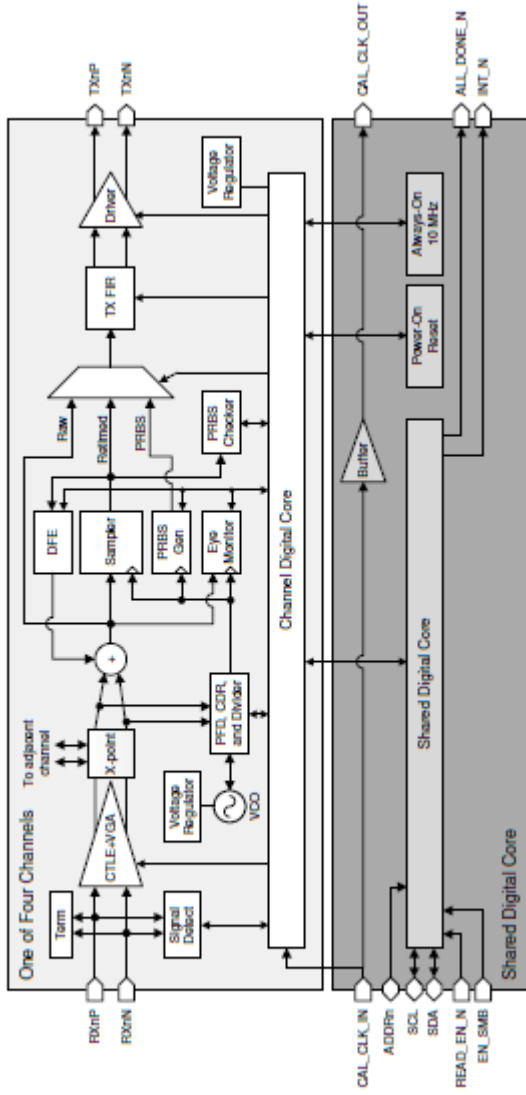
E. DEPENDENT CLAIM 5

<p>Claim 5</p> <p>5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p> <p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Exhibit A-6

Claim 5

8.2 Functional Block Diagram



DS250DF410, 17.

Exhibit A-6

<p>Claim 5</p>	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none">• R - Read only• RW - Read/Write• RWSC - Read/Write, self-clearing
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<p>Claim 5</p>	<p>8.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF410 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other. <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.</p> <p>Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.</p> <p>DS250DF410, 30-31.</p> <p>8.3.9.1 Setting the Output V_{OD}, Pre-Cursor, and Post-Cursor Equalization</p> <p>The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.</p>
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Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

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RESPONDENTS' INITIAL INVALIDITY C

Exhibit A-6

Claim 5

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPOST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 5							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0		0	RW	Y	FIR_CN1[0]		

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Table 11. Channel Registers, 3A to A9 (continued)

Exhibit A-6

Claim 5	<p>DS250DF410, 53-54.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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F. DEPENDENT CLAIM 6

Claim 6	<p>DS250DF410 discloses and/or renders obvious this limitation.</p>
<p>6. The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.</p>	

Exhibit A-6

Claim 6

Typical Applications (continued)

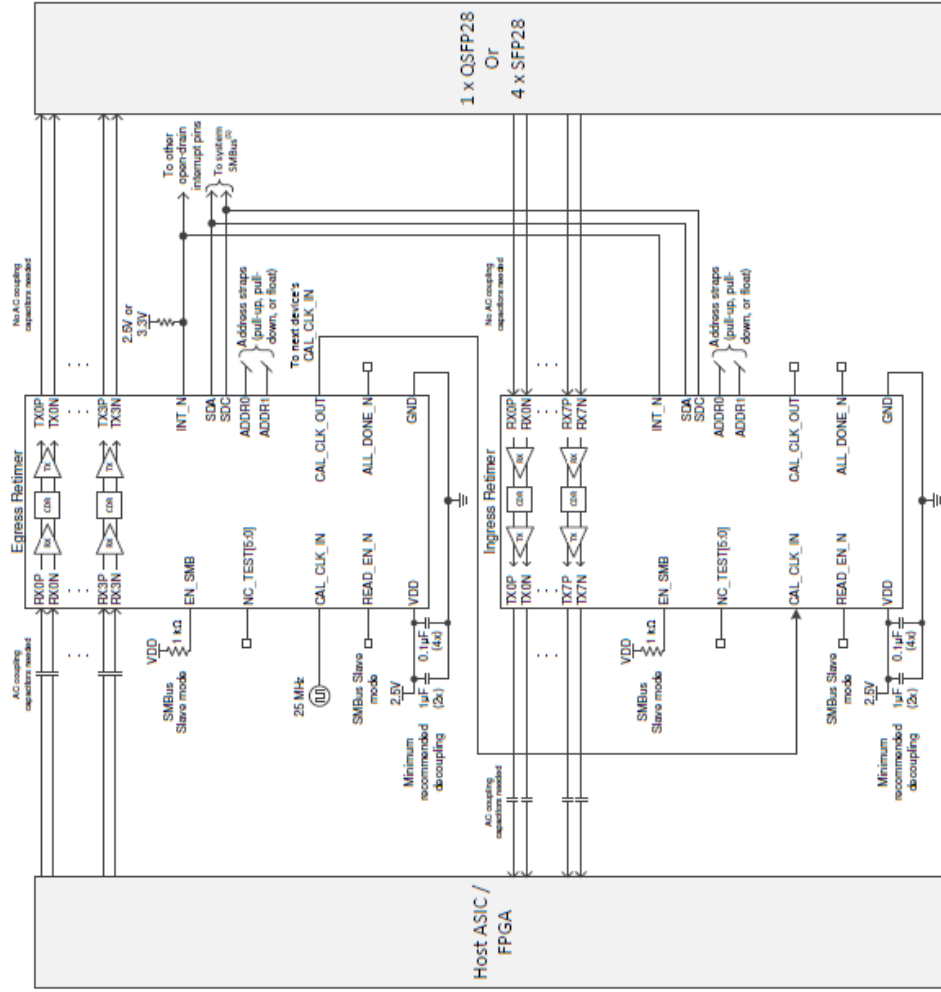


Figure 17. Front-Port Application Schematic

DS250DF410, 78.

Exhibit A-6

Claim 6

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

Figure 20 illustrates these configurations, Figure 21 shows an example simplified schematic for a half-active cable application, and Figure 22 shows an example simplified schematic for a full-active cable application.

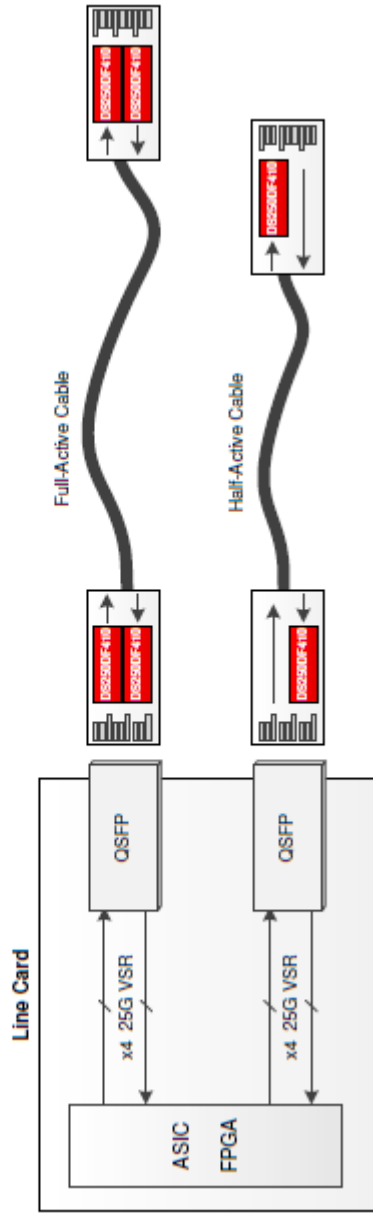


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

Exhibit A-6

Claim 6

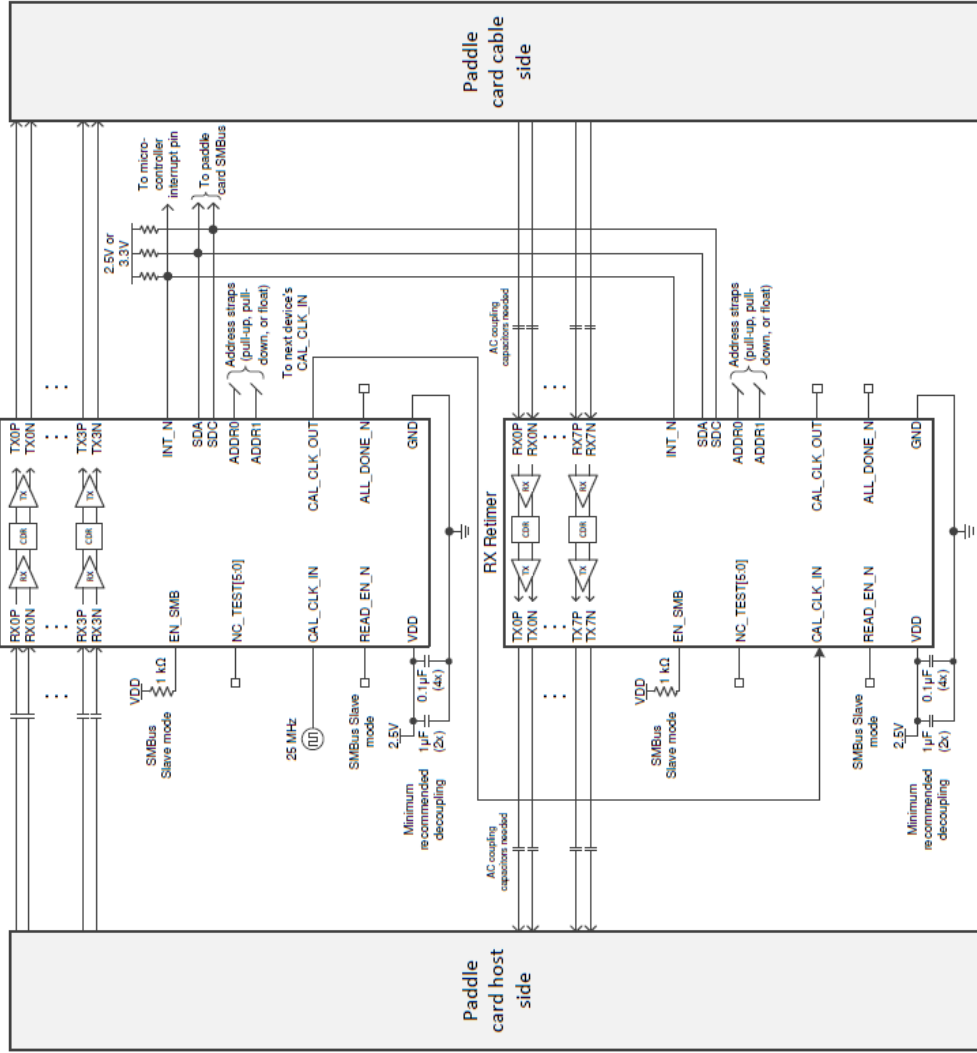


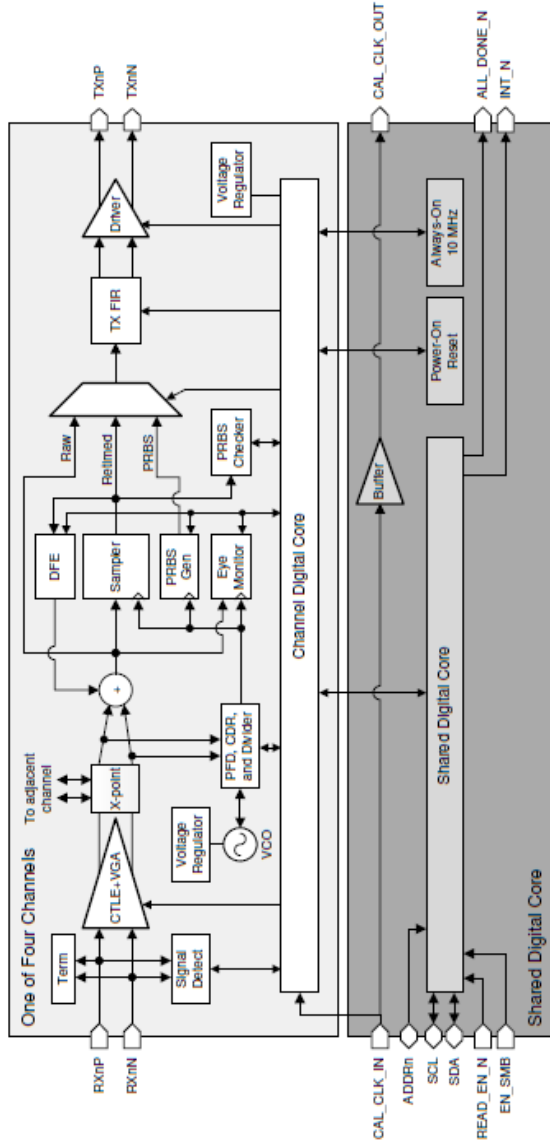
Figure 22. Full-Active Cable Application Schematic

DS250DF410, 83.

Exhibit A-6

<p>Claim 6</p>	<p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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8.2 Functional Block Diagram



DS250DF410, 17.

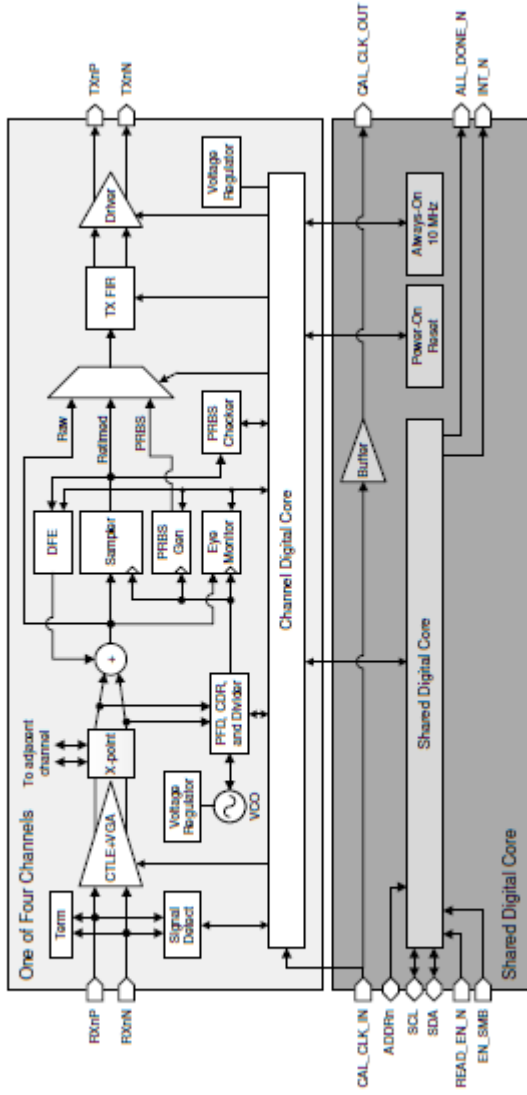
To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

G. DEPENDENT CLAIM 7

<p>Claim 7</p>	<p>7. The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.</p>
<p>DS250DF410 discloses and/or renders obvious this limitation.</p>	<p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>

Claim 7

8.2 Functional Block Diagram



DS250DF410, 17.

Exhibit A-6

<p>Claim 7</p>	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none">• R - Read only• RW - Read/Write• RWSC - Read/Write, self-clearing
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<p>Claim 7</p>	<p>8.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF410 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other. <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.</p> <p>Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type command can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.</p> <p>DS250DF410, 30-31.</p> <p>8.3.9.1 Setting the Output V_{OD}, Pre-Cursor, and Post-Cursor Equalization</p> <p>The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.</p>
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Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

INVESTIGATION No. 337-TA-1446
RESPONDENTS' INITIAL INVALIDITY C

Exhibit A-6

Claim 7

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPOST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]				
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 7							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0	0	RW	Y	FIR_CN1[0]			

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

Claim 7	DS250DF410, 53-54. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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H. INDEPENDENT CLAIM 8

Claim 8
 8[pre] A cable manufacturing method that comprises:

To the extent the preamble is limiting, DS250DF410 discloses and/or renders obvious this limitation.

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

Figure 20 illustrates these configurations, Figure 21 shows an example simplified schematic for a half-active cable application, and Figure 22 shows an example simplified schematic for a full-active cable application.

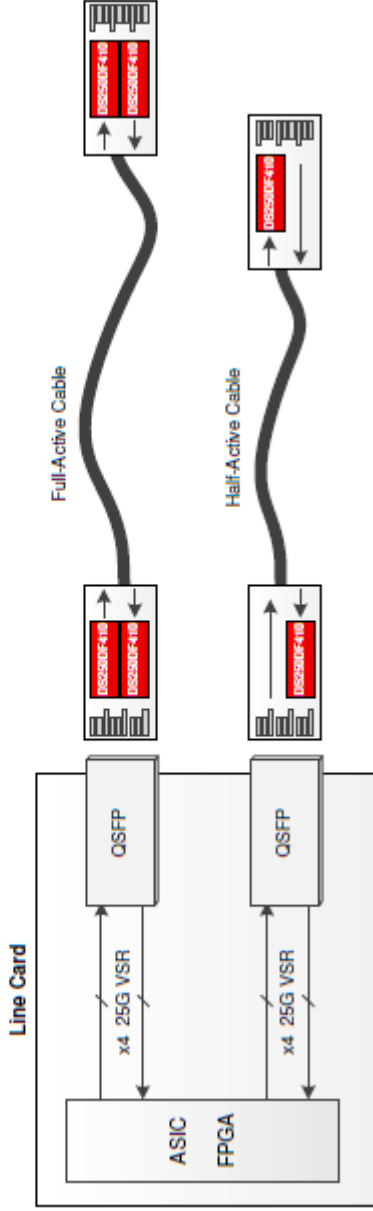


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

Exhibit A-6

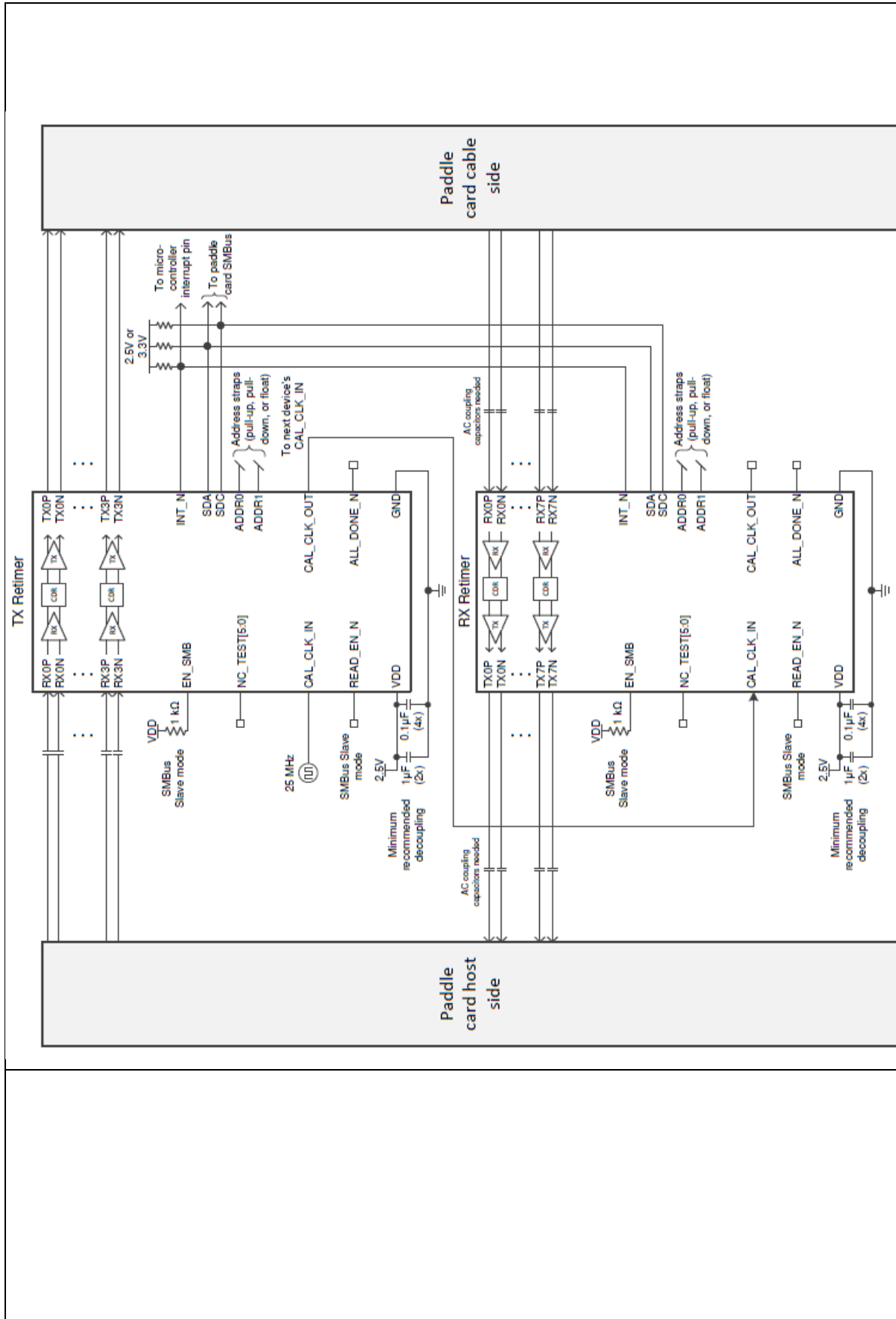


Figure 22. Full-Active Cable Application Schematic

Exhibit A-6

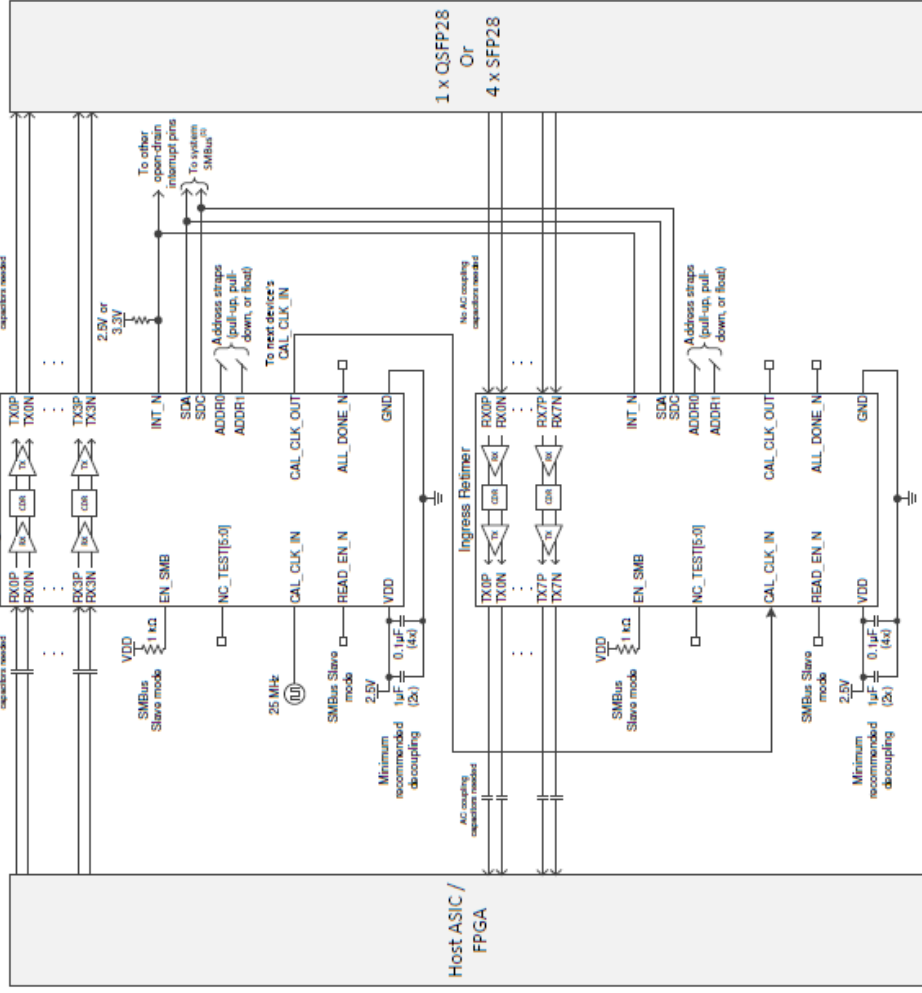
<p>Claim 8</p>	<p>DS250DF410, 83.</p> <p style="text-align: center;">Table 14. Full-Active Cable Application Design Guidelines</p> <table border="1"> <thead> <tr> <th>DESIGN PARAMETER</th> <th>REQUIREMENT</th> </tr> </thead> <tbody> <tr> <td>Device placement</td> <td>A full-active QSFP cable will utilize two pieces of DS250DF410 per paddle card. Typically, one device will be placed on each side of the paddle card.</td> </tr> <tr> <td>AC coupling capacitors</td> <td><i>Transmit-side Retimer:</i> 100 nF AC coupling capacitors are required for the RX inputs and are not required for the TX outputs. This link segment will be AC coupled on the paddle card at the opposite end of the cable. <i>Receive-side Retimer:</i> 100 nF AC coupling capacitors are required for the RX inputs and the TX outputs.</td> </tr> <tr> <td>Cable insertion loss</td> <td>The raw cable insertion loss including the insertion loss of the paddle card should be ≤ 35 dB at 25.78125 Gbps Nyquist frequency (12.9 GHz).</td> </tr> </tbody> </table> <p>DS250DF410, 84.</p> <p>To the extent that this preamble is not disclosed, either explicitly or inherently, by DS250DF410, this preamble is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p> <p>DS250DF410 discloses and/or renders obvious this limitation.</p>	DESIGN PARAMETER	REQUIREMENT	Device placement	A full-active QSFP cable will utilize two pieces of DS250DF410 per paddle card. Typically, one device will be placed on each side of the paddle card.	AC coupling capacitors	<i>Transmit-side Retimer:</i> 100 nF AC coupling capacitors are required for the RX inputs and are not required for the TX outputs. This link segment will be AC coupled on the paddle card at the opposite end of the cable. <i>Receive-side Retimer:</i> 100 nF AC coupling capacitors are required for the RX inputs and the TX outputs.	Cable insertion loss	The raw cable insertion loss including the insertion loss of the paddle card should be ≤ 35 dB at 25.78125 Gbps Nyquist frequency (12.9 GHz).
DESIGN PARAMETER	REQUIREMENT								
Device placement	A full-active QSFP cable will utilize two pieces of DS250DF410 per paddle card. Typically, one device will be placed on each side of the paddle card.								
AC coupling capacitors	<i>Transmit-side Retimer:</i> 100 nF AC coupling capacitors are required for the RX inputs and are not required for the TX outputs. This link segment will be AC coupled on the paddle card at the opposite end of the cable. <i>Receive-side Retimer:</i> 100 nF AC coupling capacitors are required for the RX inputs and the TX outputs.								
Cable insertion loss	The raw cable insertion loss including the insertion loss of the paddle card should be ≤ 35 dB at 25.78125 Gbps Nyquist frequency (12.9 GHz).								
<p>8[a] connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges multi-lane data streams with a</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p>								

Exhibit A-6

Claim 8

first host interface port via the first connector plug;

Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.
Figure 17. Front-Port Application Schematic

DS250DF410, 78.

Claim 8

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

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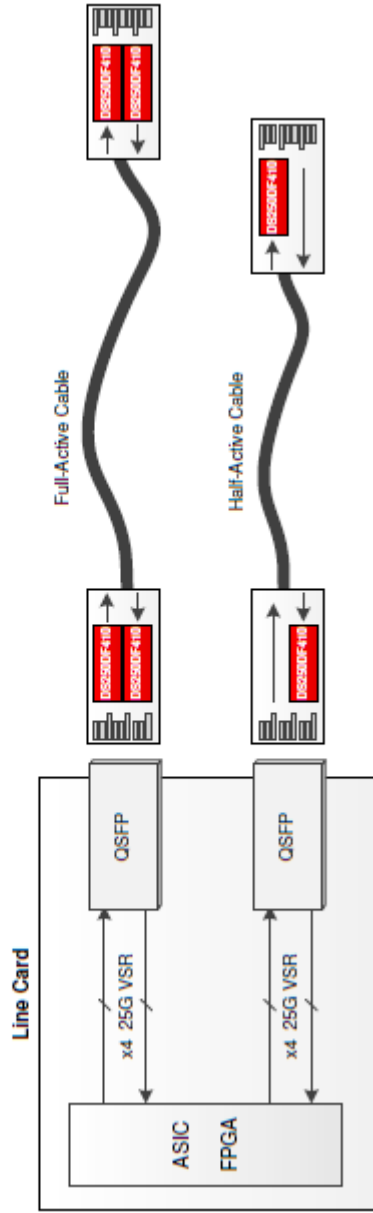


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

Exhibit A-6

Claim 8

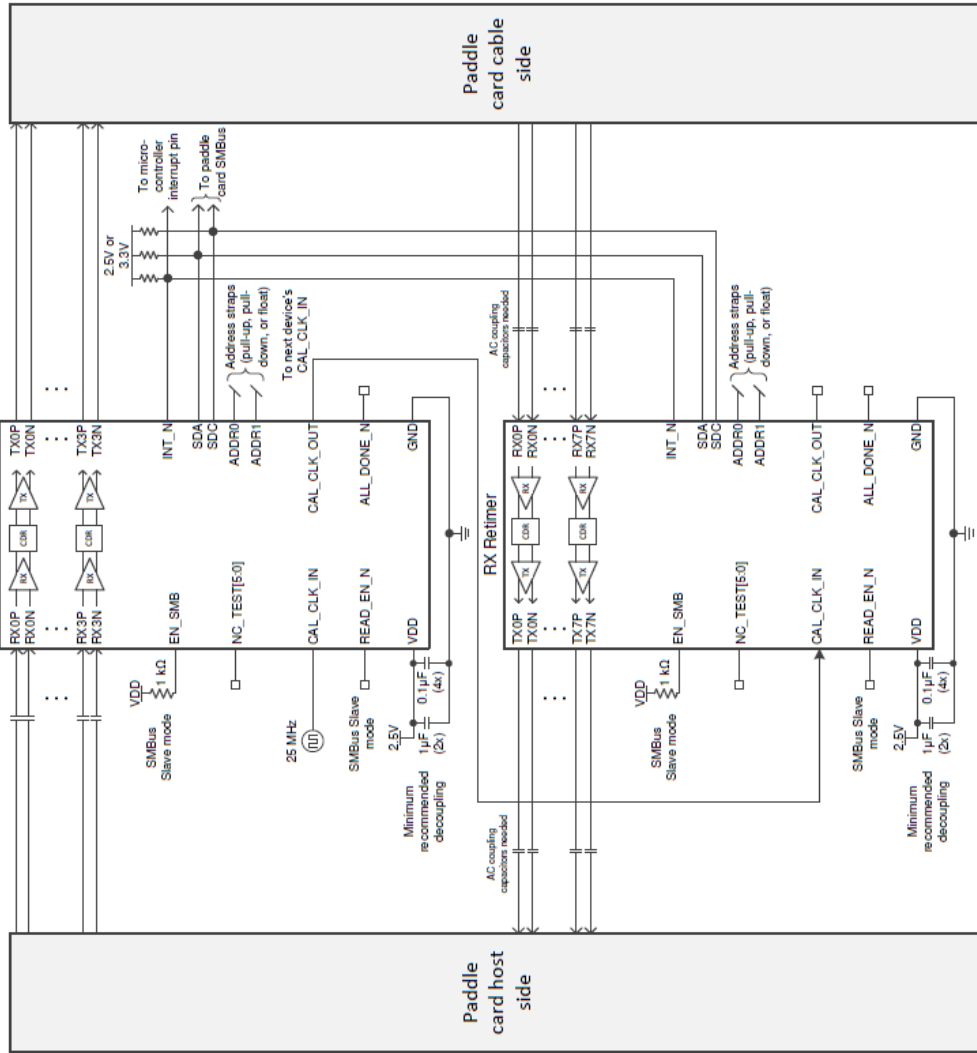


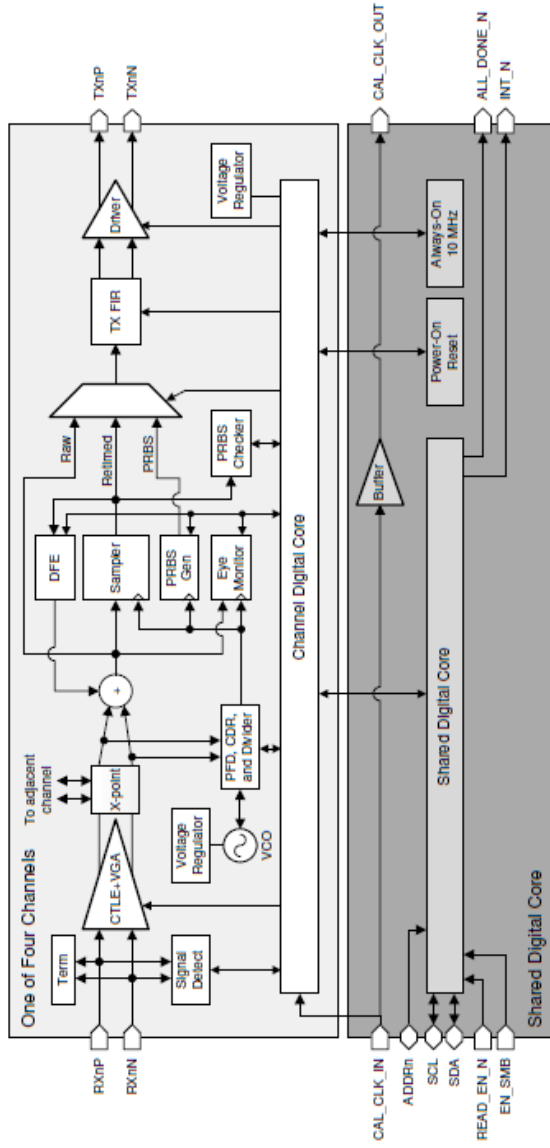
Figure 22. Full-Active Cable Application Schematic

DS250DF410, 83.

<p>Claim 8</p>	<p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 8

8.2 Functional Block Diagram



DS250DF410, 17.

Claim 8	<p>8.3.7 Clock and Data Recovery (CDR)</p> <p>The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes.</p> <p>By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF410 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator.</p> <p>The CDR requires the following to be properly configured:</p> <ul style="list-style-type: none"> • 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN). • Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF410, 19.</p> <p>8.3.9 Differential Driver with FIR Filter</p> <p>The DS250DF410 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. C[0] can take on values in the range [-31, +31]. C[-1] and C[+1] can take on values in the range [-15, 15].</p>
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Claim 8

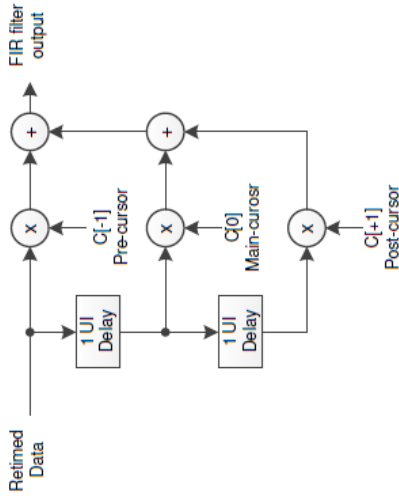


Figure 7. FIR Filter Functional model

When utilizing the FIR filter, it is important to abide by the following general rules:

- $|C[-1]| + |C[0]| + |C[+1]| \leq 31$; the FIR tap coefficients absolute sum must be less or equal to 31
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
- $VOD_{low-frequency} = V_2 - V_5$
- $R_{pre-dB} = 20 * \log_{10} (V_3/V_2)$
- $R_{pst-dB} = 20 * \log_{10} (V_1/V_2)$

DS250DF410, 19-20.

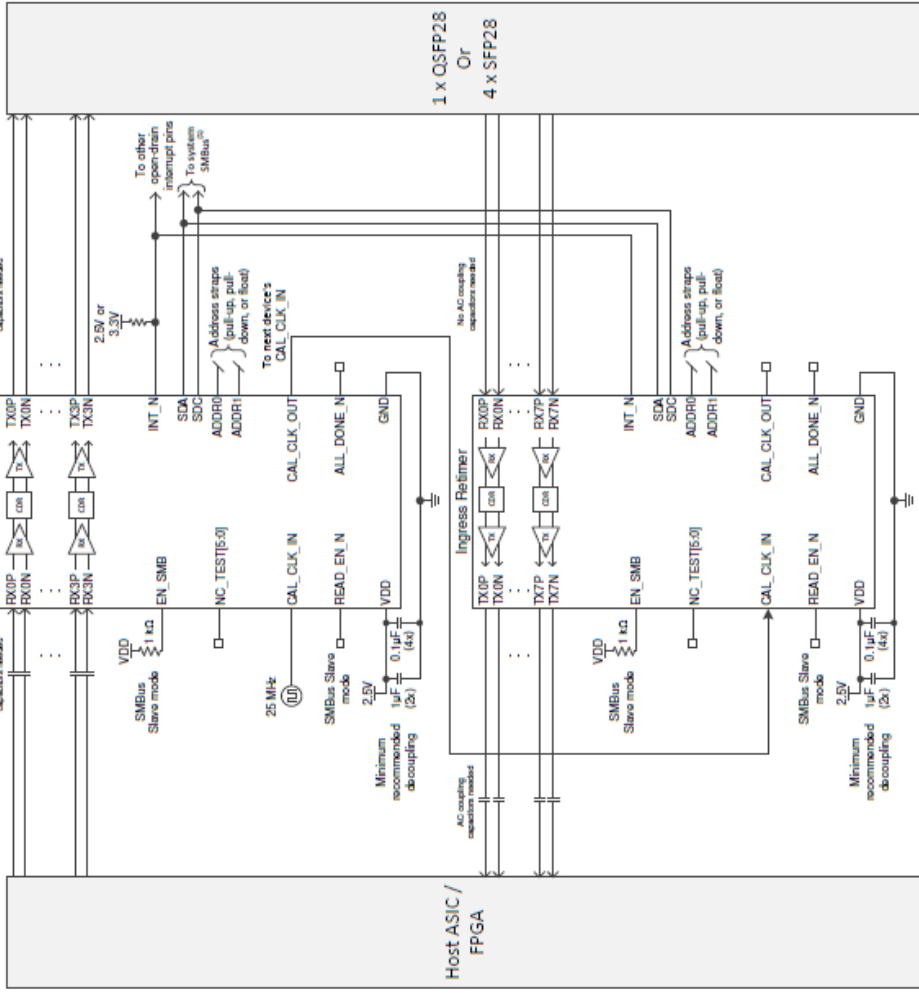
To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or

Exhibit A-6

<p>Claim 8</p>	<p>combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>8[b] connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p>

Claim 8

Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Front-Port Application Schematic

DS250DF410, 78.

Exhibit A-6

Claim 8

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

Figure 20 illustrates these configurations, Figure 21 shows an example simplified schematic for a half-active cable application, and Figure 22 shows an example simplified schematic for a full-active cable application.

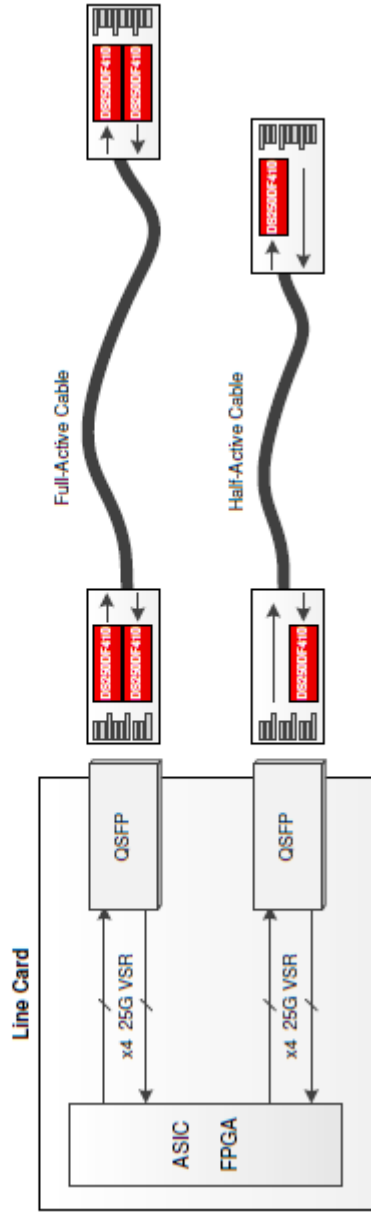


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

Exhibit A-6

Claim 8

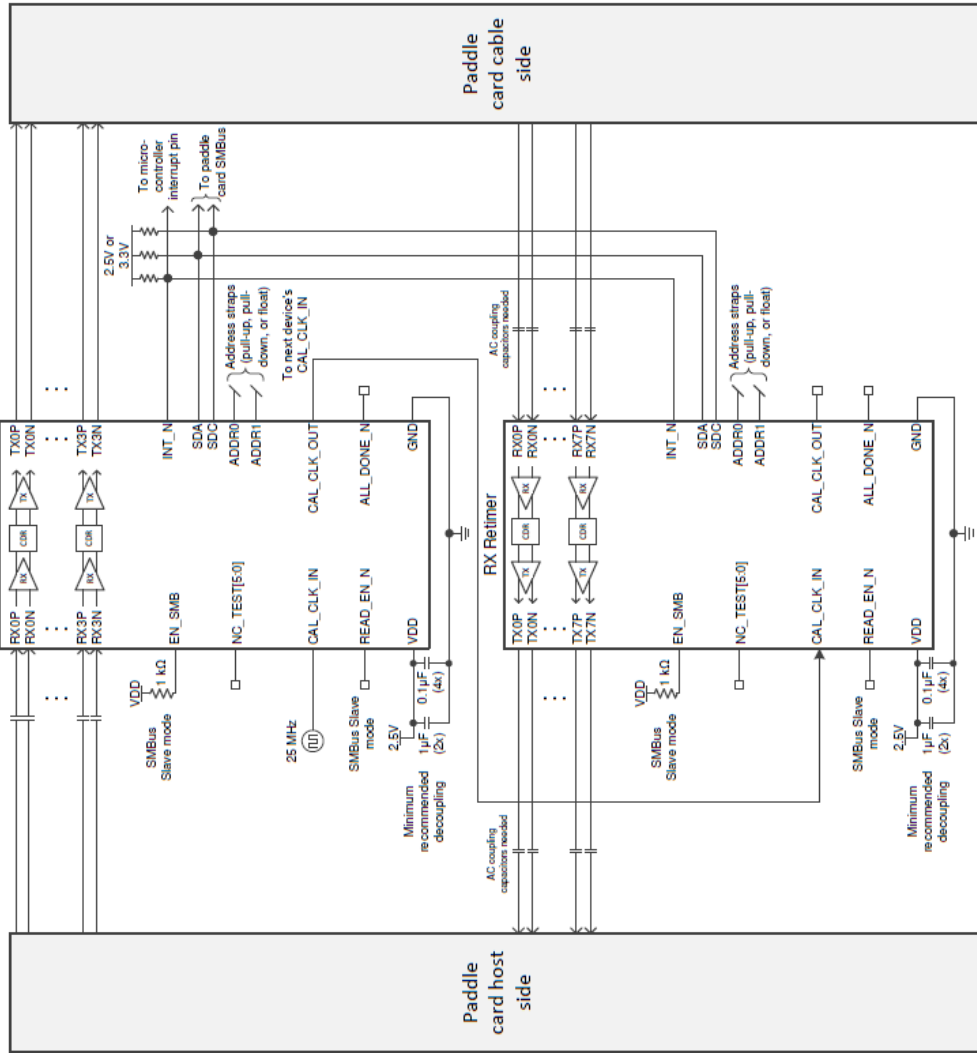


Figure 22. Full-Active Cable Application Schematic

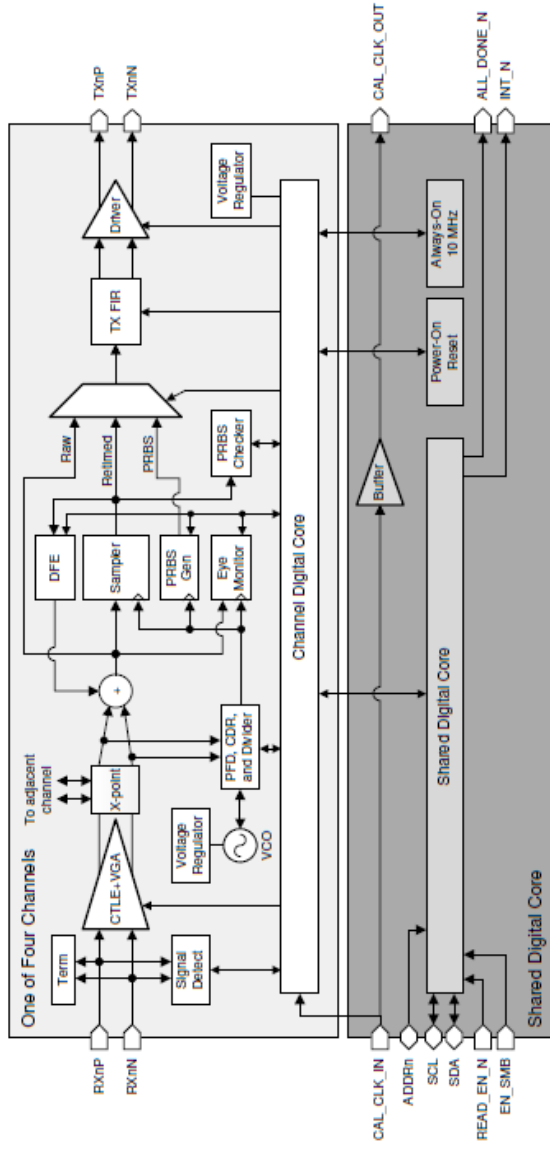
DS250DF410, 83.

Exhibit A-6

<p>Claim 8</p>	<p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 8

8.2 Functional Block Diagram



DS250DF410, 17.

Claim 8	<p>8.3.7 Clock and Data Recovery (CDR)</p> <p>The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes.</p> <p>By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF410 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator.</p> <p>The CDR requires the following to be properly configured:</p> <ul style="list-style-type: none"> • 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN). • Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF410, 19.</p> <p>8.3.9 Differential Driver with FIR Filter</p> <p>The DS250DF410 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. C[0] can take on values in the range [-31, +31]. C[-1] and C[+1] can take on values in the range [-15, 15].</p>
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Claim 8

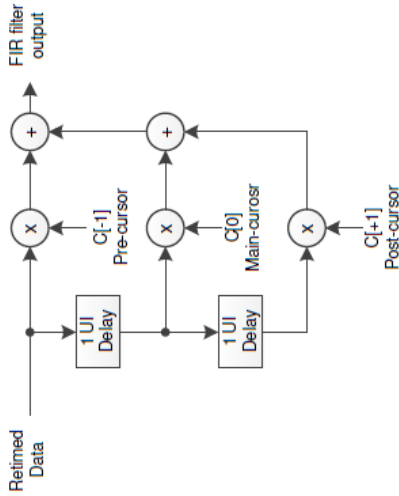


Figure 7. FIR Filter Functional model

When utilizing the FIR filter, it is important to abide by the following general rules:

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The FIR filter is used to pre-distort the transmitted waveform to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

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- $R_{pre-dB} = 20 * \log_{10} (V_3/V_2)$
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DS250DF410, 19-20.

To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or

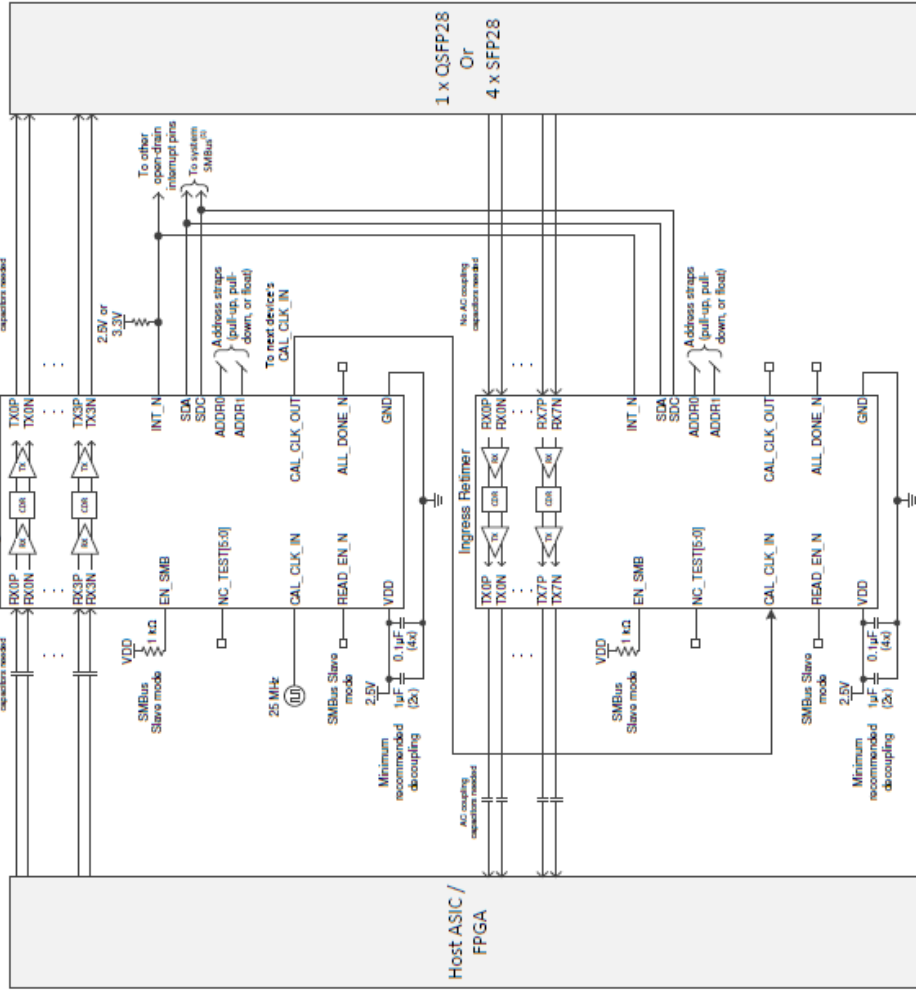
Exhibit A-6

<p>Claim 8</p>	<p>combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p> <p>DS250DF410 discloses and/or renders obvious this limitation.</p>
<p>8[c] connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween,</p>	

Exhibit A-6

Claim 8

Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Front-Port Application Schematic

DS250DF410, 78.

Claim 8

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

Figure 20 illustrates these configurations, Figure 21 shows an example simplified schematic for a half-active cable application, and Figure 22 shows an example simplified schematic for a full-active cable application.

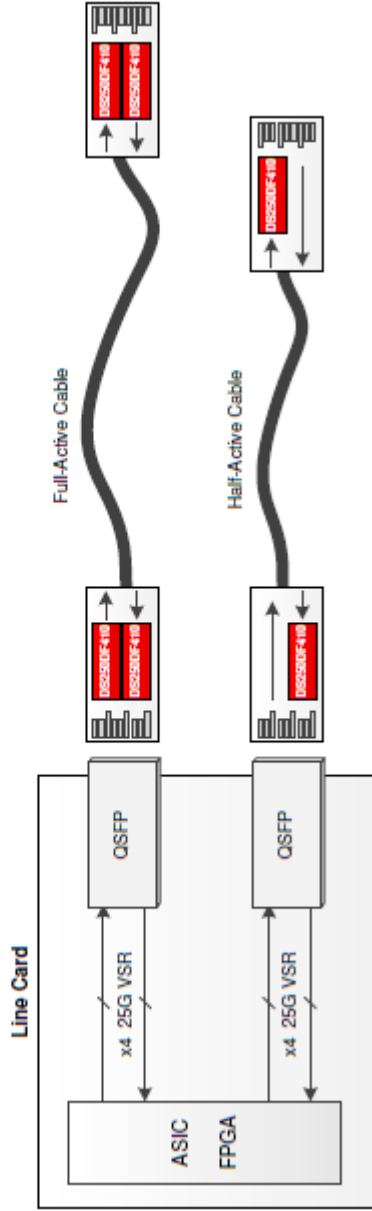


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

Exhibit A-6

Claim 8

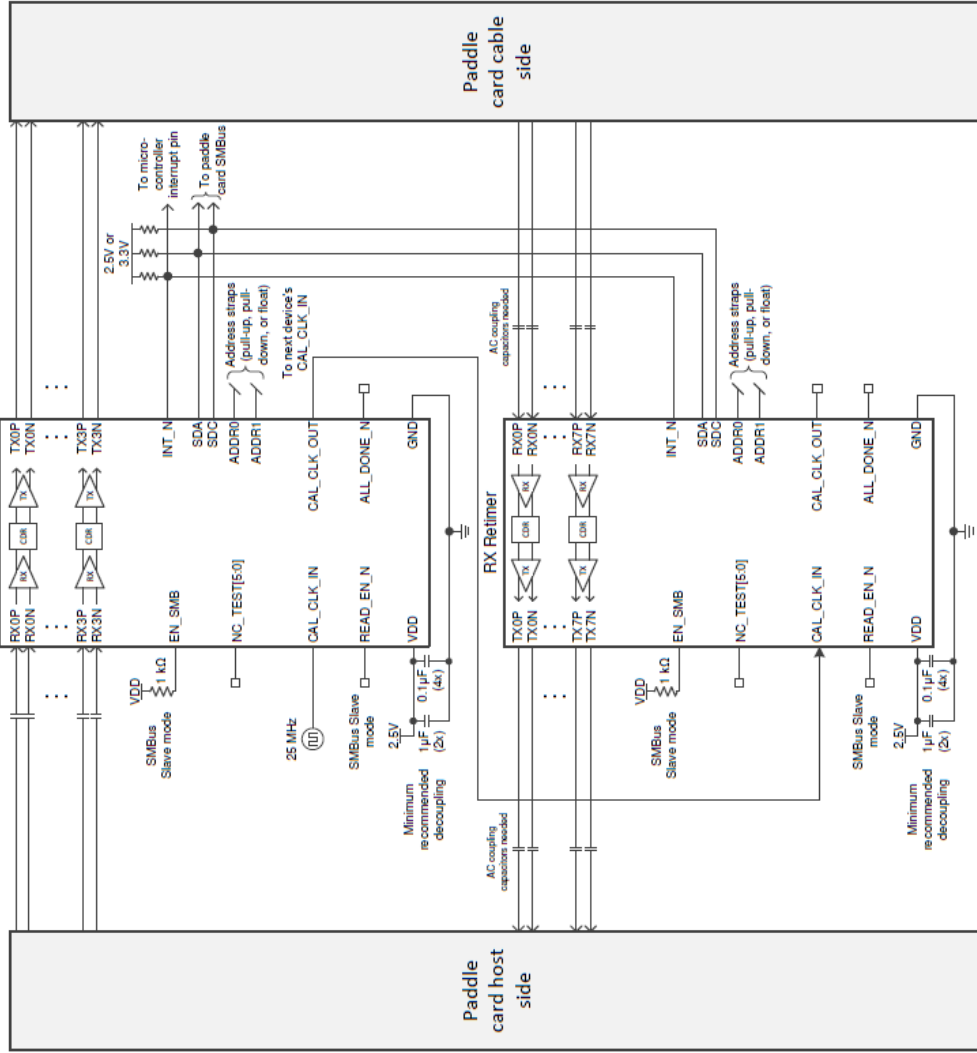


Figure 22. Full-Active Cable Application Schematic

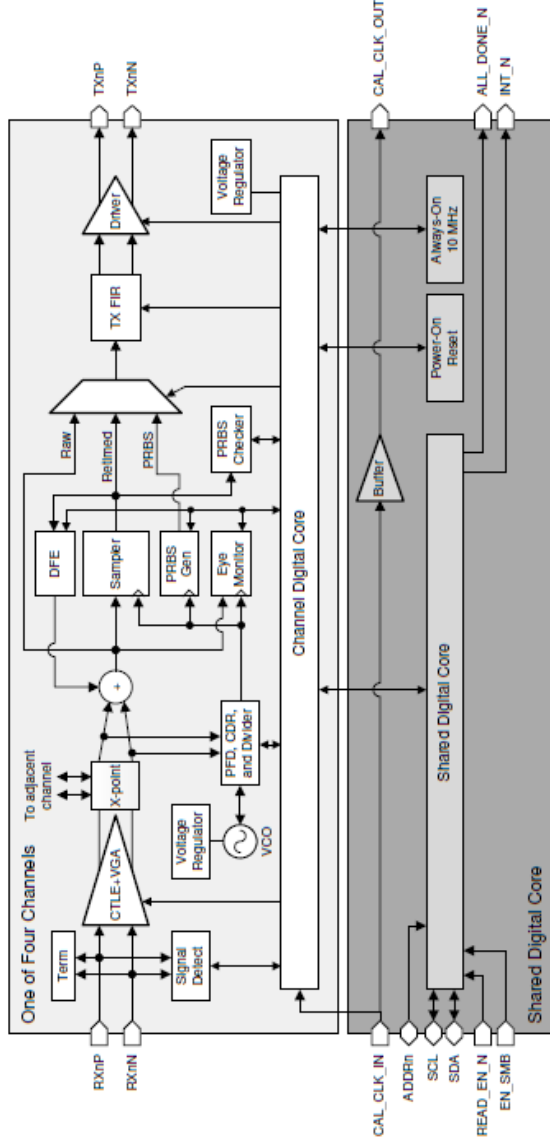
DS250DF410, 83.

Exhibit A-6

<p>Claim 8</p>	<p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 8

8.2 Functional Block Diagram



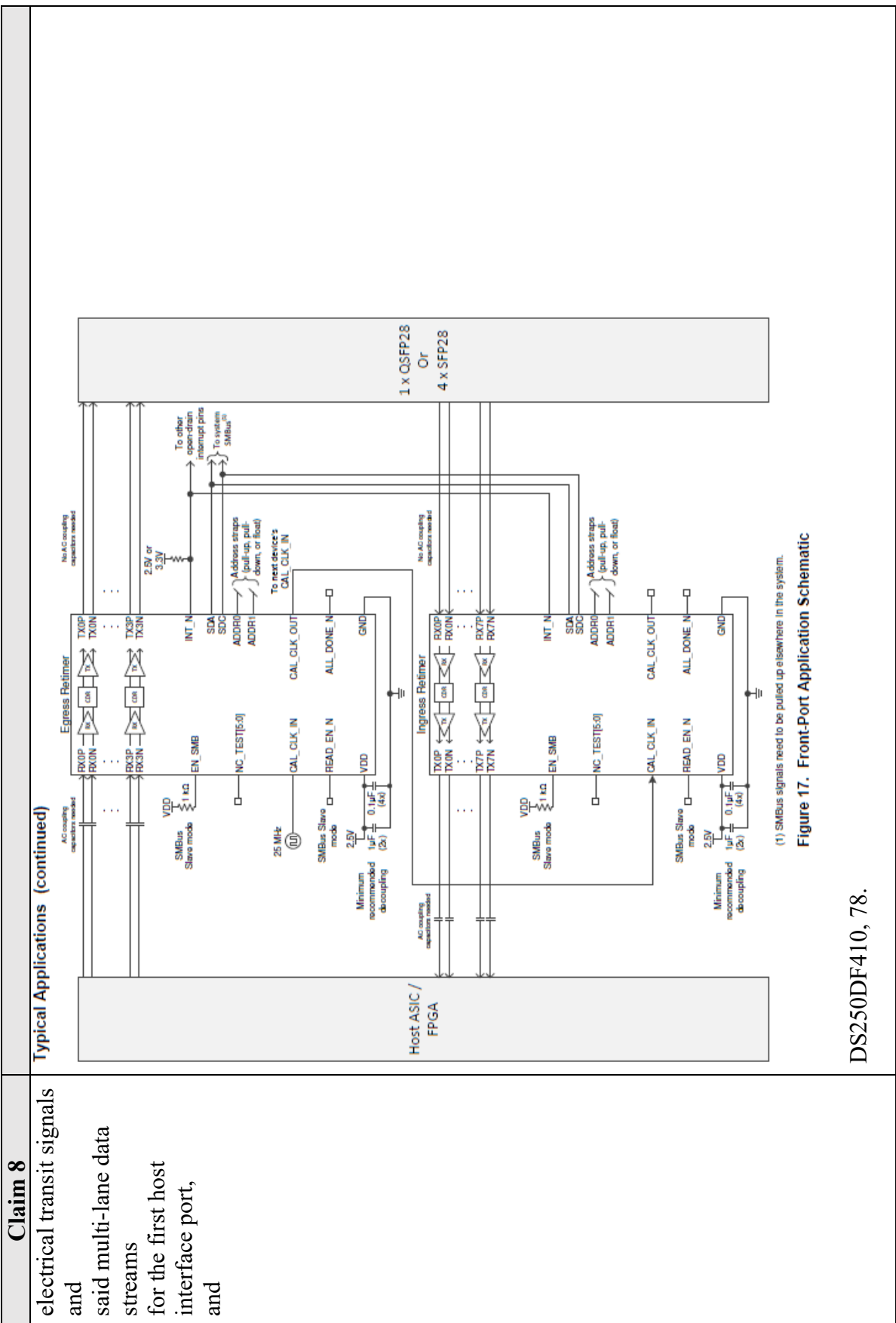
DS250DF410, 17.

To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

8[d] the first DDR device converting between said

DS250DF410 discloses and/or renders obvious this limitation.

Exhibit A-6



DS250DF410, 78.

Exhibit A-6

Claim 8

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

Figure 20 illustrates these configurations, Figure 21 shows an example simplified schematic for a half-active cable application, and Figure 22 shows an example simplified schematic for a full-active cable application.

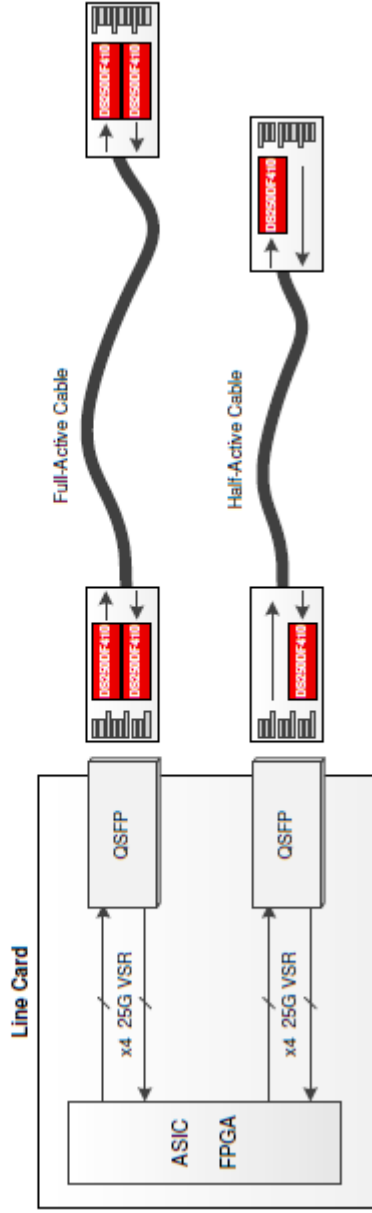


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

Exhibit A-6

Claim 8

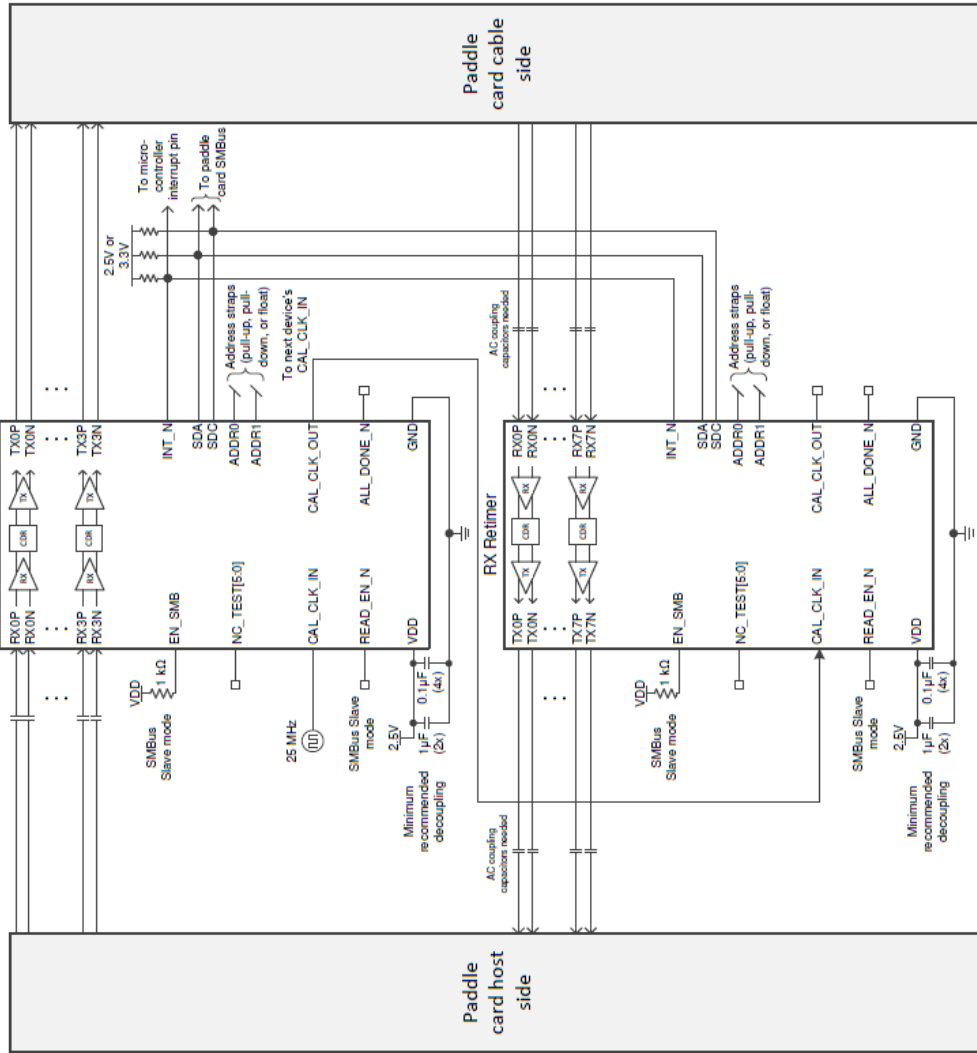


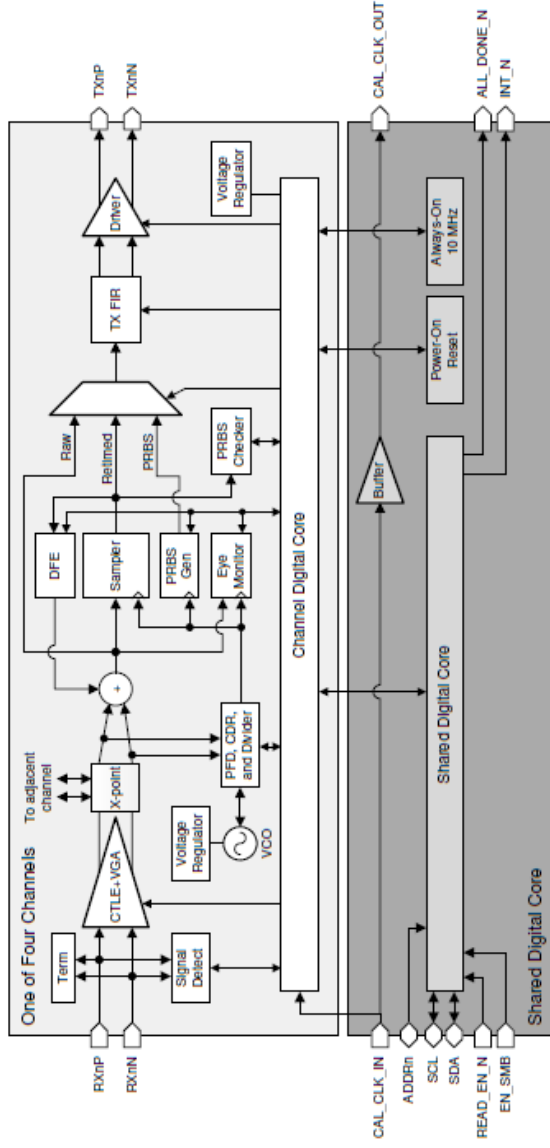
Figure 22. Full-Active Cable Application Schematic

DS250DF410, 83.

<p>Claim 8</p>	<p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 8

8.2 Functional Block Diagram



DS250DF410, 17.

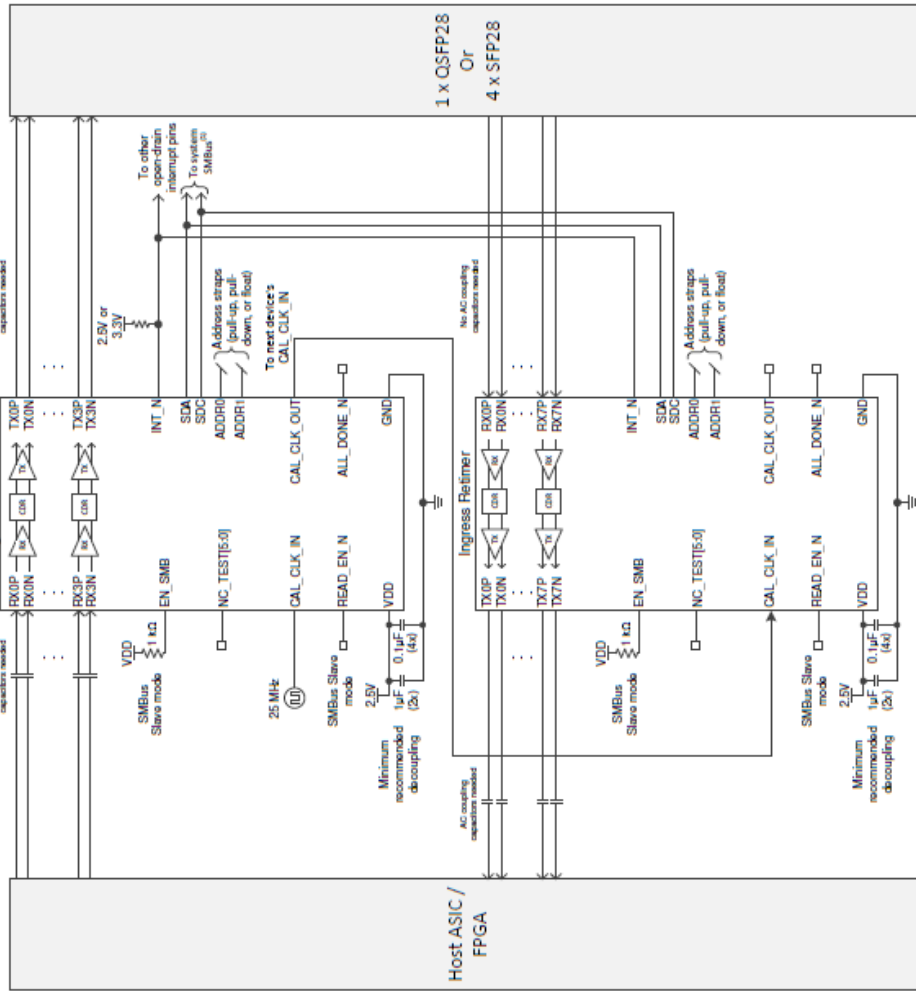
<p>Claim 8</p>	<p>8.3.7 Clock and Data Recovery (CDR) The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes. By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF410 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator.</p> <p>The CDR requires the following to be properly configured:</p> <ul style="list-style-type: none"> • 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN). • Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF410, 19.</p> <p>8.3.9 Differential Driver with FIR Filter The DS250DF410 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. C[0] can take on values in the range [-31, +31]. C[-1] and C[+1] can take on values in the range [-15, 15].</p>
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Exhibit A-6

<p>Claim 8</p>	<p>combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>8[e] the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port,</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p>

Claim 8

Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Front-Port Application Schematic

DS250DF410, 78.

Claim 8

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

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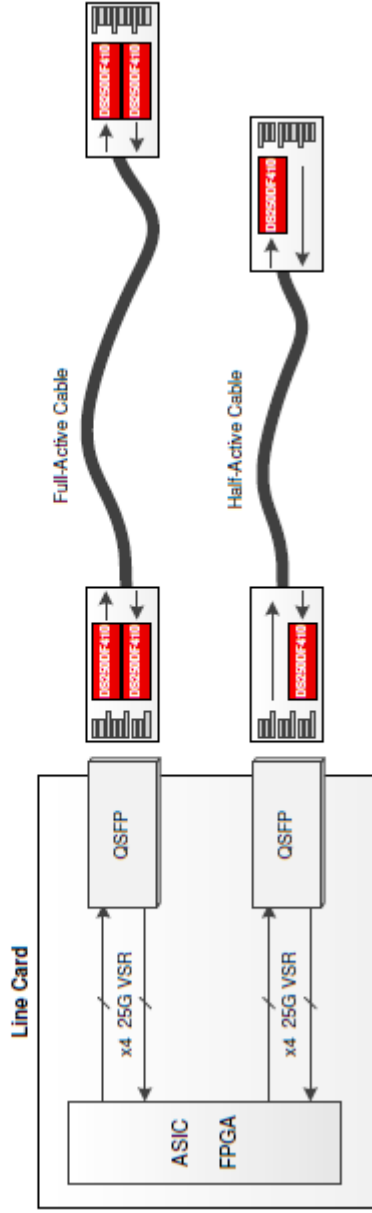


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

Exhibit A-6

Claim 8

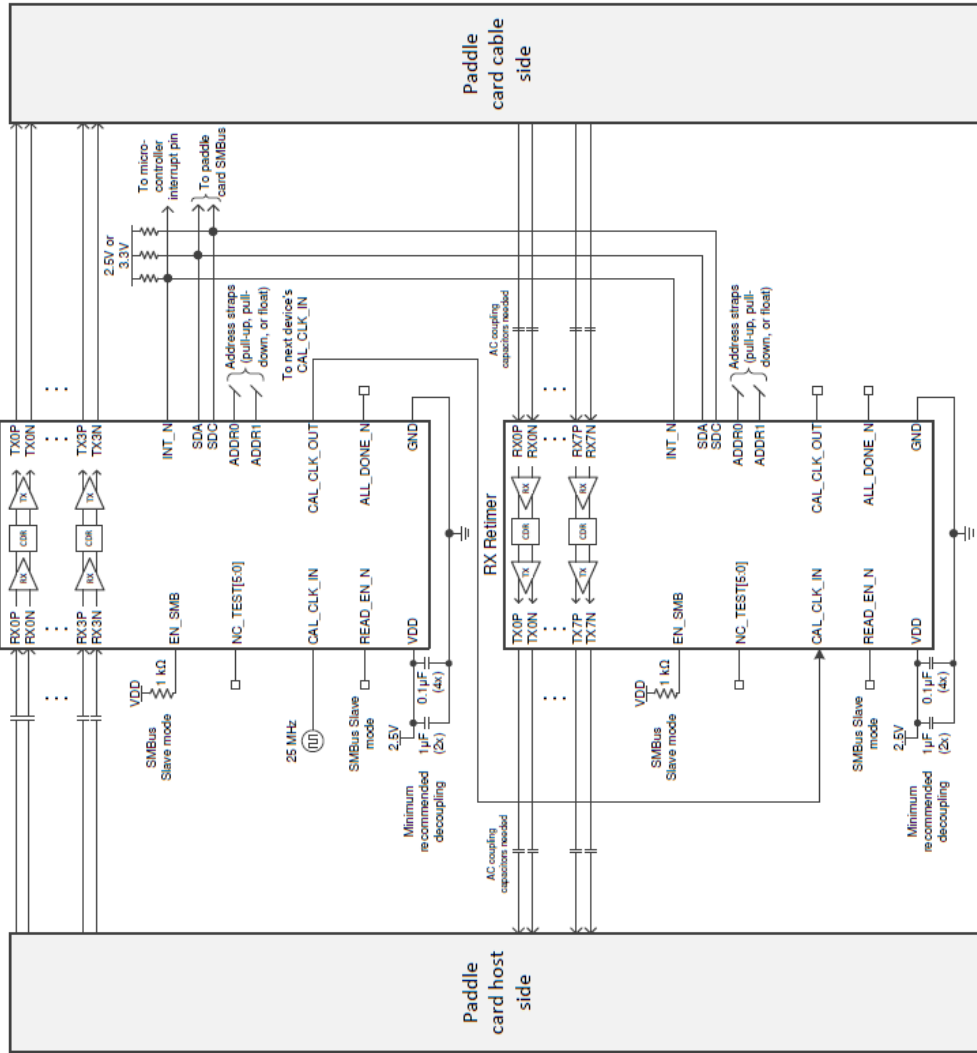


Figure 22. Full-Active Cable Application Schematic

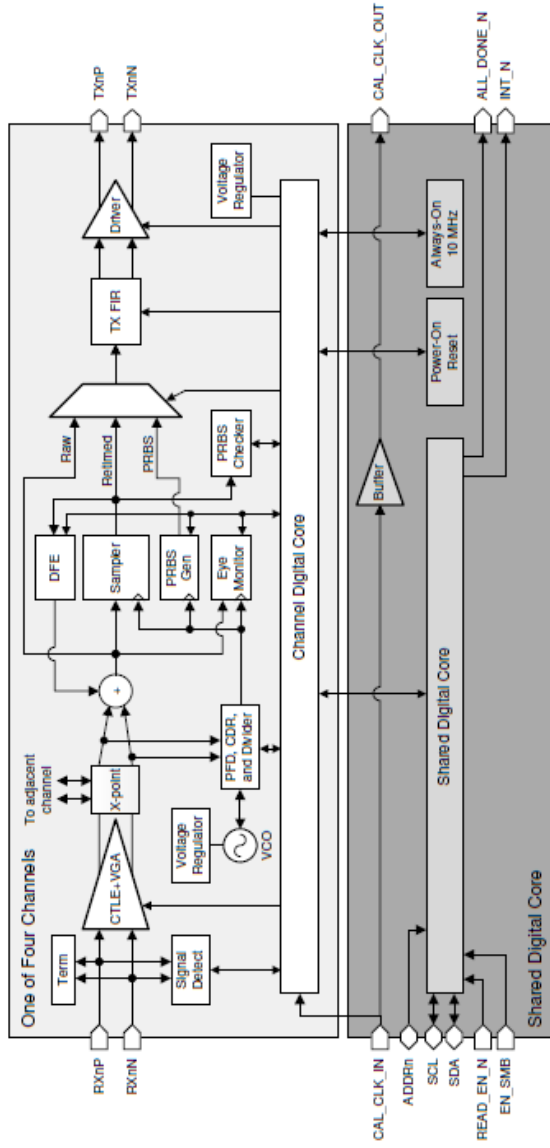
DS250DF410, 83.

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<p>Claim 8</p>	<p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 8

8.2 Functional Block Diagram



DS250DF410, 17.

<p>Claim 8</p>	<p>8.3.7 Clock and Data Recovery (CDR) The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes. By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF410 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator. The CDR requires the following to be properly configured:</p> <ul style="list-style-type: none"> • 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN). • Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF410, 19.</p> <p>8.3.9 Differential Driver with FIR Filter The DS250DF410 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. C[0] can take on values in the range [-31, +31]. C[-1] and C[+1] can take on values in the range [-15, 15].</p>
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Claim 8

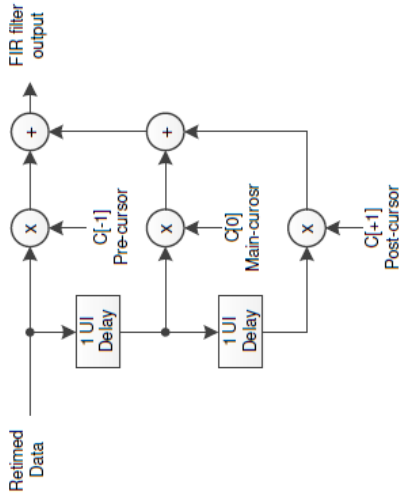


Figure 7. FIR Filter Functional model

When utilizing the FIR filter, it is important to abide by the following general rules:

- $|C[-1]| + |C[0]| + |C[+1]| \leq 31$; the FIR tap coefficients absolute sum must be less or equal to 31
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
- $VOD_{low-frequency} = V_2 - V_5$
- $R_{pre-dB} = 20 * \log_{10} (V_3/V_2)$
- $R_{pst-dB} = 20 * \log_{10} (V_1/V_2)$

DS250DF410, 19-20.

To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or

Exhibit A-6

<p align="center">Claim 8</p>	<p>combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>8[f] the first and second DRR devices providing preequalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p> <p>8.3.9.1 Setting the Output V_{OD}, Pre-Cursor, and Post-Cursor Equalization</p> <p>The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.</p>

Exhibit A-6

Table 2. Typical VOD and FIR Values

FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURS: REG_0x3E[6:0]	MAIN-CURS: REG_0x3D[6:0]			
0	0	0	NA	NA
0	+1	0	NA	NA
0	+2	0	NA	NA
0	+3	0	NA	NA
0	+4	0	NA	NA
0	+5	0	NA	NA
0	+6	0	NA	NA
0	+7	0	NA	NA
0	+8	0	NA	NA
0	+9	0	NA	NA
0	+10	0	NA	NA
0	+11	0	NA	NA
0	+12	0	NA	NA
0	+13	0	NA	NA
0	+14	0	NA	NA
0	+15	0	NA	NA
0	+16	0	NA	NA
0	+17	0	NA	NA
0	+18	0	NA	NA
0	+20	0	NA	NA
0	+21	0	NA	NA
0	+22	0	NA	NA
0	+23	0	NA	NA
0	+24	0	NA	NA
0	+25	0	NA	NA
0	+26	0	NA	NA
0	+27	0	NA	NA
0	+28	0	NA	NA
0	+28	0	NA	NA
0	+28	0	NA	NA
0	+30	0	NA	NA
0	+31	0	NA	NA
0	+18	-1	NA	2.1
0	+17	-2	NA	2.5
0	+16	-3	NA	3.1
0	+15	-4	NA	3.8
0	+14	-5	NA	4.7
0	+13	-6	NA	5.8
0	+12	-7	NA	7.2
0	+11	-8	NA	9.0
0	+10	-9	NA	11.6
-1	18	0	NA	NA
-2	17	0	NA	NA
-3	16	0	NA	NA
-4	15	0	NA	NA
0	26	-1	NA	1.1

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Exhibit A-6

Claim 8

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

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Claim 8											
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)					
	6	0	RW	Y	FIR_CO_SGN	Main-cursor sign bit 0: positive 1: negative					
	5	0	RW	Y	RESERVED	RESERVED					
	4	1	RW	Y	FIR_CO[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)					
	3	1	RW	Y	FIR_CO[3]						
	2	0	RW	Y	FIR_CO[2]						
	1	1	RW	Y	FIR_CO[1]						
	0	0	RW	Y	FIR_CO[0]						
	3E	7	0	RW	Y	FIR_PD_TX					
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive				
		5	0	RW	Y	RESERVED	RESERVED				
		4	0	RW	Y	RESERVED	RESERVED				
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)				
		2	0	RW	Y	FIR_CN1[2]					
1		0	RW	Y	FIR_CN1[1]						
0		0	RW	Y	FIR_CN1[0]						

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

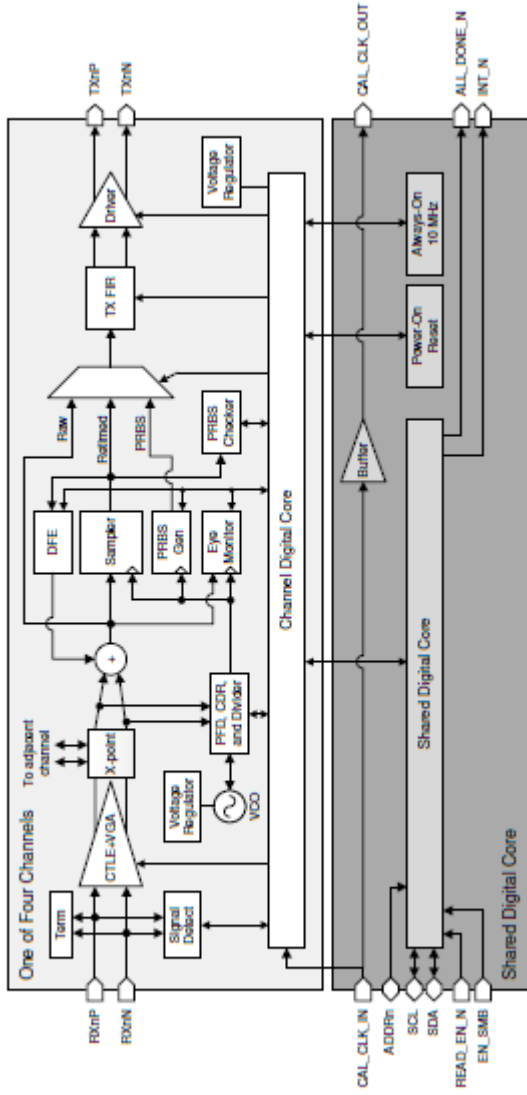
Claim 8	DS250DF410, 53-54. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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I. DEPENDENT CLAIM 9

<p>Claim 9</p> <p>9. The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p> <p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 9

8.2 Functional Block Diagram



DS250DF410, 17.

Claim 9	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing
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<p>Claim 9</p>	<p>8.5.2 Writing to and Reading from the Global/Shared/Channel Registers</p> <p>The DS250DF410 has 3 types of registers:</p> <ol style="list-style-type: none"> 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information. 2) Shared Registers – These registers are used for device-level configuration, status read back or control. 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other. <p>The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:</p> <ul style="list-style-type: none"> • Channel selection and share enabling – Registers 0xFC and 0xFF • Device and version information – Registers 0xEF-0xF3 • Reserved/unused registers – all other addresses <p>Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.</p> <p>Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type command can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.</p> <p>TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.</p> <p>DS250DF410, 30-31.</p> <p>8.3.9.1 Setting the Output V_{OD}, Pre-Cursor, and Post-Cursor Equalization</p> <p>The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.</p>
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Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

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Claim 9

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

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Claim 9							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0		0	RW	Y	FIR_CN1[0]		

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

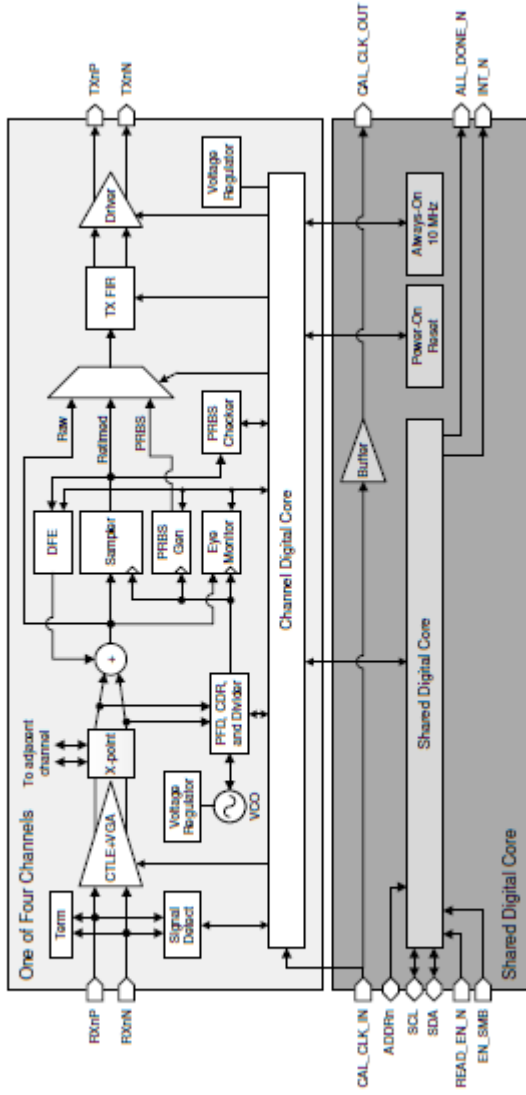
<p>Claim 9</p>	<p>DS250DF410, 53-54.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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J. DEPENDENT CLAIM 10

<p>Claim 10</p> <p>10. The method of claim 8, further comprising the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p> <p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 10

8.2 Functional Block Diagram



DS250DF410, 17.

Claim 10	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing
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Claim 10

8.5.2 Writing to and Reading from the Global/Shared/Channel Registers

The DS250DF410 has 3 types of registers:

- 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information.
- 2) Shared Registers – These registers are used for device-level configuration, status read back or control.
- 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other.

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:

- Channel selection and share enabling – Registers 0xFC and 0xFF
- Device and version information – Registers 0xEF-0xF3
- Reserved/unused registers – all other addresses

Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.

Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.

TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.

DS250DF410, 30-31.

8.3.9.1 Setting the Output V_{OD} , Pre-Cursor, and Post-Cursor Equalization

The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

INVESTIGATION No. 337-TA-1446
RESPONDENTS' INITIAL INVALIDITY C

Exhibit A-6

Claim 10

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 10							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0		0	RW	Y	FIR_CN1[0]		

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

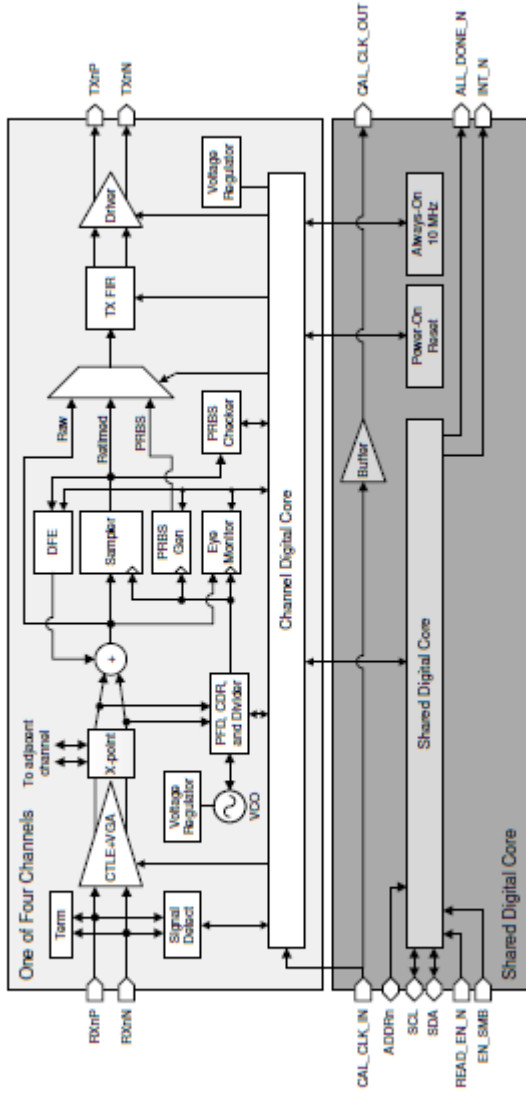
<p>Claim 10</p>	<p>DS250DF410, 53-54.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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K. DEPENDENT CLAIM 11

<p>Claim 11</p> <p>11. The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p> <p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 11

8.2 Functional Block Diagram



DS250DF410, 17.

Claim 11	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing
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Claim 11

8.5.2 Writing to and Reading from the Global/Shared/Channel Registers

The DS250DF410 has 3 types of registers:

- 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information.
- 2) Shared Registers – These registers are used for device-level configuration, status read back or control.
- 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other.

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:

- Channel selection and share enabling – Registers 0xFC and 0xFF
- Device and version information – Registers 0xEF-0xF3
- Reserved/unused registers – all other addresses

Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.

Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.

TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.

DS250DF410, 30-31.

8.3.9.1 Setting the Output V_{OD} , Pre-Cursor, and Post-Cursor Equalization

The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

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RESPONDENTS' INITIAL INVALIDITY C

Exhibit A-6

Claim 11

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 11							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0		0	RW	Y	FIR_CN1[0]		

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

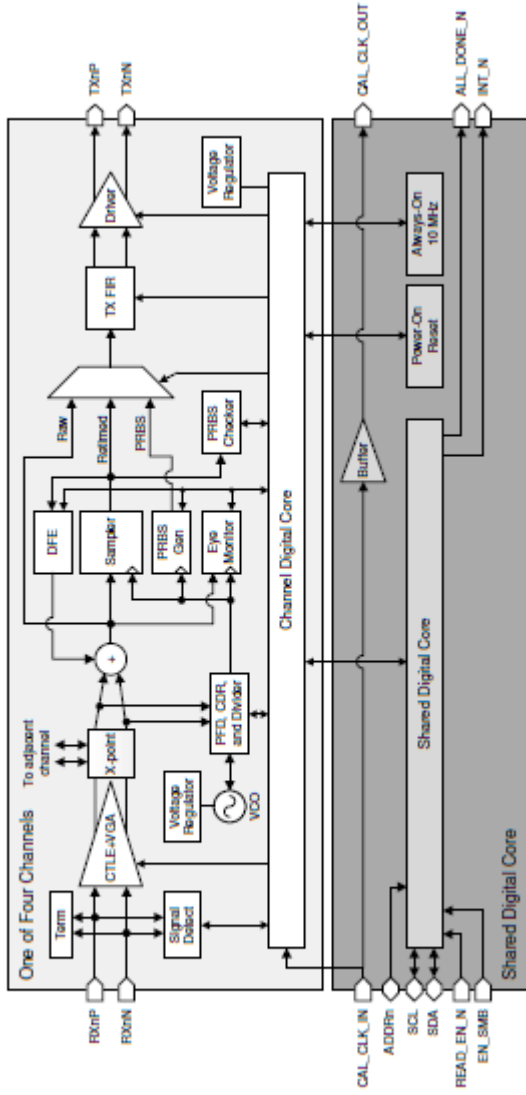
<p>Claim 11</p>	<p>DS250DF410, 53-54.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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L. DEPENDENT CLAIM 12

<p>Claim 12</p> <p>12. The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p> <p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 12

8.2 Functional Block Diagram



DS250DF410, 17.

<p>Claim 12</p>	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing
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8.5.2 Writing to and Reading from the Global/Shared/Channel Registers

The DS250DF410 has 3 types of registers:

- 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information.
- 2) Shared Registers – These registers are used for device-level configuration, status read back or control.
- 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other.

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:

- Channel selection and share enabling – Registers 0xFC and 0xFF
- Device and version information – Registers 0xEF-0xF3
- Reserved/unused registers – all other addresses

Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.

Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.

TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.

DS250DF410, 30-31.

8.3.9.1 Setting the Output V_{OD} , Pre-Cursor, and Post-Cursor Equalization

The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

INVESTIGATION No. 337-TA-1446
RESPONDENTS' INITIAL INVALIDITY C

Exhibit A-6

Claim 12

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 12							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0		0	RW	Y	FIR_CN1[0]		

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

Claim 12	DS250DF410, 53-54. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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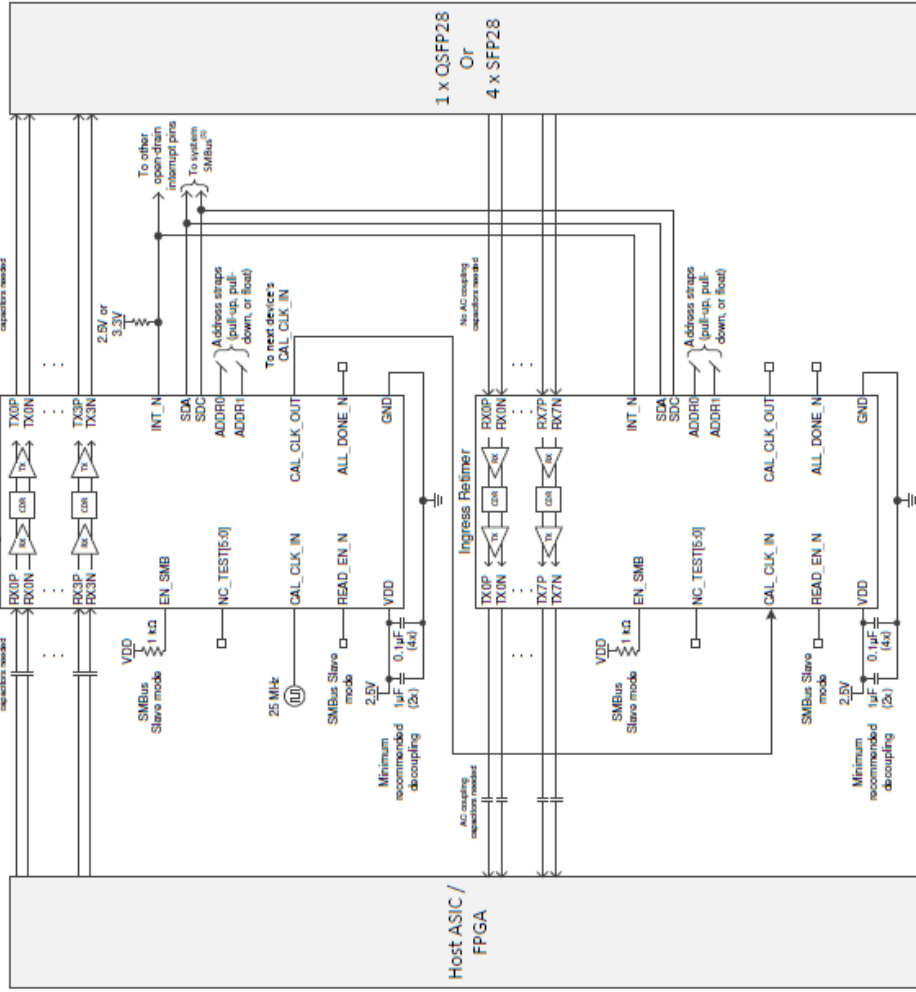
M. DEPENDENT CLAIM 13

Claim 13 13. The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.	DS250DF410 discloses and/or renders obvious this limitation.
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Exhibit A-6

Claim 13

Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Front-Port Application Schematic

DS250DF410, 78.

Exhibit A-6

Claim 13

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

Figure 20 illustrates these configurations, Figure 21 shows an example simplified schematic for a half-active cable application, and Figure 22 shows an example simplified schematic for a full-active cable application.

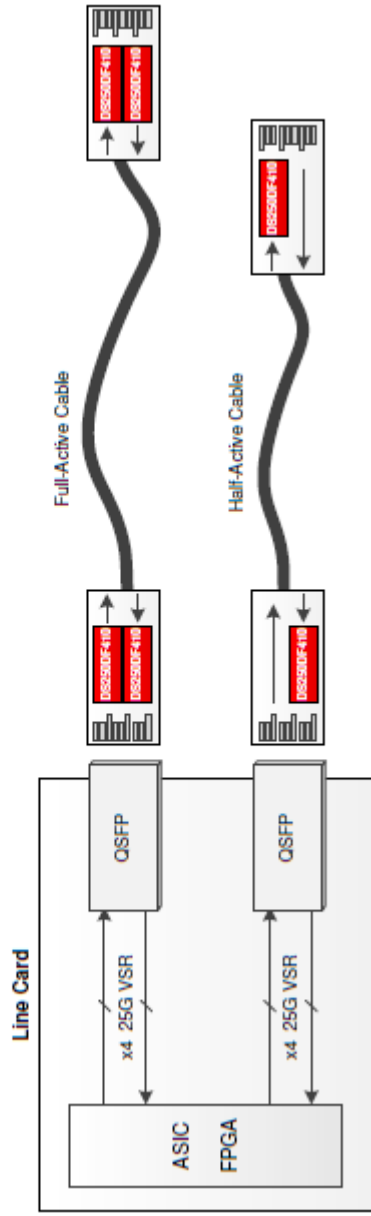


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

Exhibit A-6

Claim 13

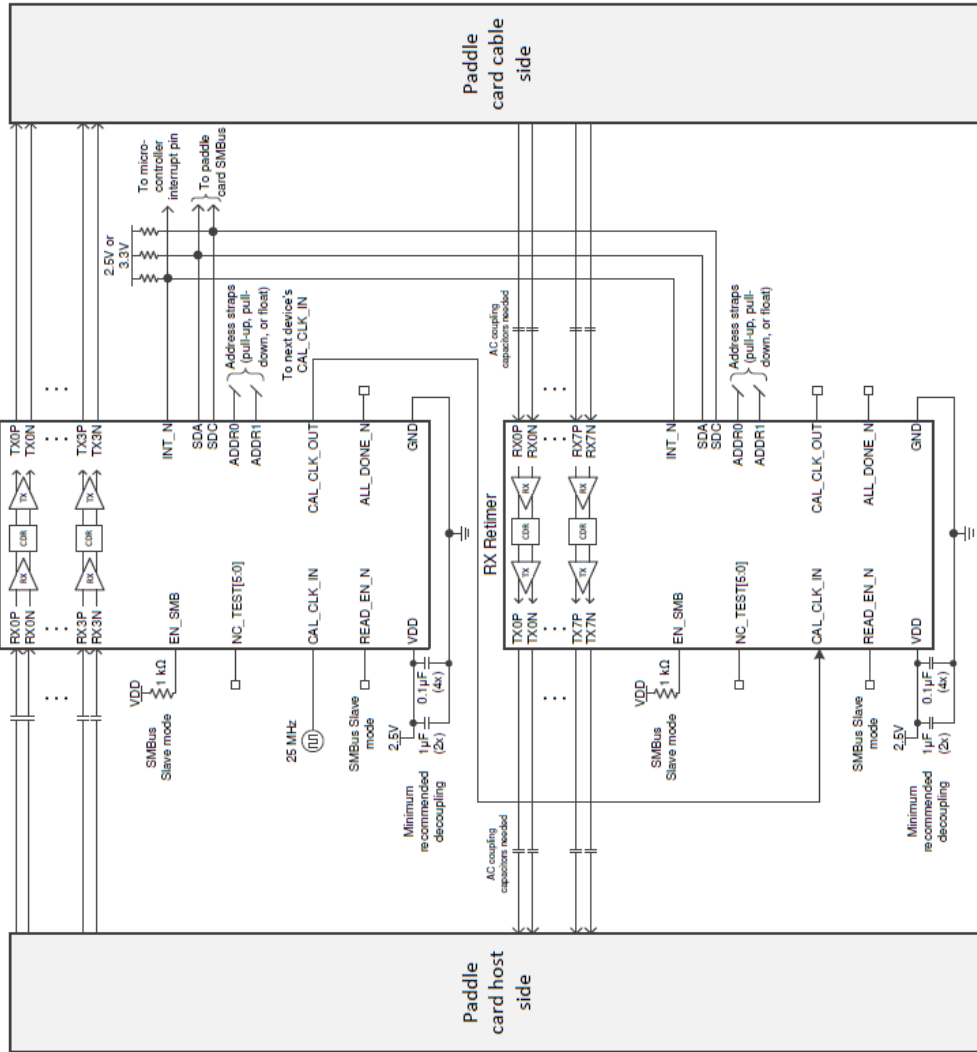
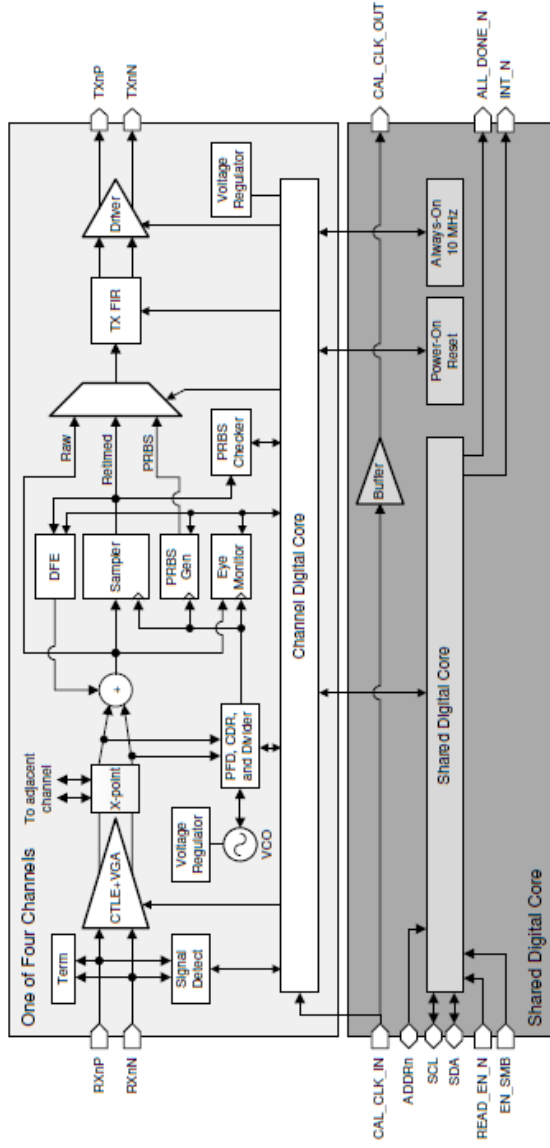


Figure 22. Full-Active Cable Application Schematic

DS250DF410, 83.

<p>Claim 13</p>	<p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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8.2 Functional Block Diagram



DS250DF410, 17.

To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

N. DEPENDENT CLAIM 14

Claim 14

14. The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

DS250DF410 discloses and/or renders obvious this limitation.

8.1 Overview

The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.

Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.

Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.

Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.

Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).

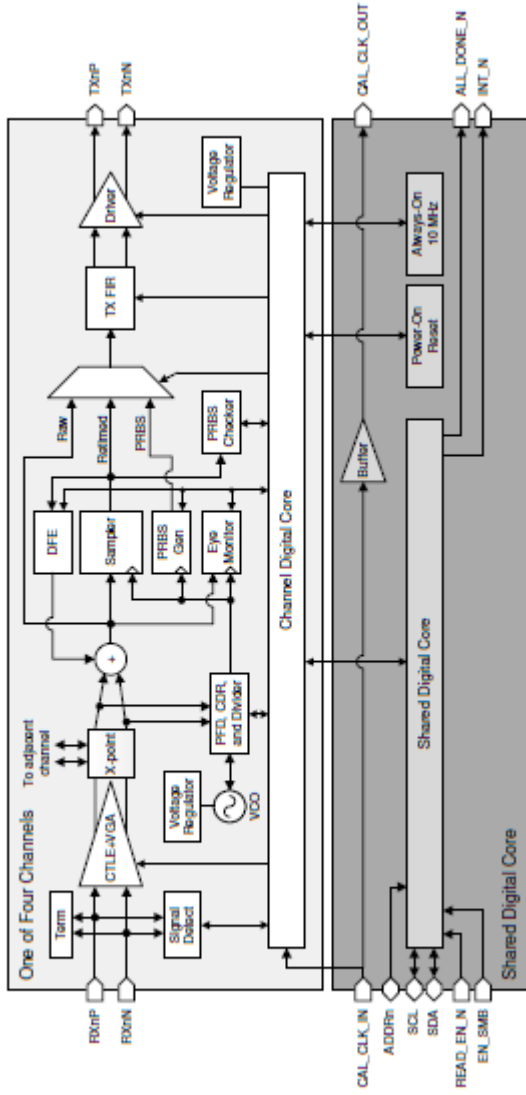
The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.

The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.

DS250DF410, 17.

Claim 14

8.2 Functional Block Diagram



DS250DF410, 17.

Claim 14	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing
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Claim 14

8.5.2 Writing to and Reading from the Global/Shared/Channel Registers

The DS250DF410 has 3 types of registers:

- 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information.
- 2) Shared Registers – These registers are used for device-level configuration, status read back or control.
- 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other.

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:

- Channel selection and share enabling – Registers 0xFC and 0xFF
- Device and version information – Registers 0xEF-0xF3
- Reserved/unused registers – all other addresses

Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.

Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.

TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.

DS250DF410, 30-31.

8.3.9.1 Setting the Output V_{OD} , Pre-Cursor, and Post-Cursor Equalization

The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

INVESTIGATION No. 337-TA-1446
RESPONDENTS' INITIAL INVALIDITY C

Exhibit A-6

Claim 14

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPOST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 14							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0		0	RW	Y	FIR_CN1[0]		

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

Claim 14	<p>DS250DF410, 53-54.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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O. INDEPENDENT CLAIM 15

Claim 15	<p>To the extent the preamble is limiting, DS250DF410 discloses and/or renders obvious this limitation.</p>
15[pre] A communications method that comprises:	

Exhibit A-6

Claim 15

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

Figure 20 illustrates these configurations, Figure 21 shows an example simplified schematic for a half-active cable application, and Figure 22 shows an example simplified schematic for a full-active cable application.

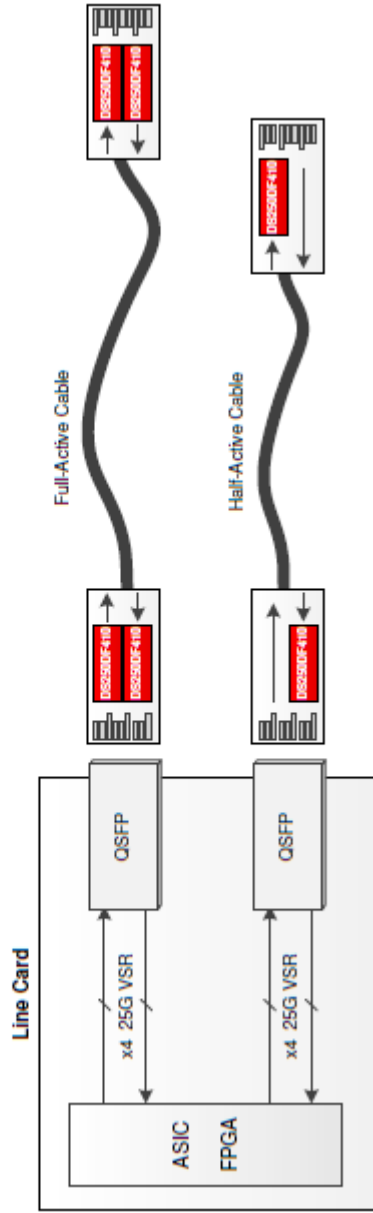


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

Exhibit A-6

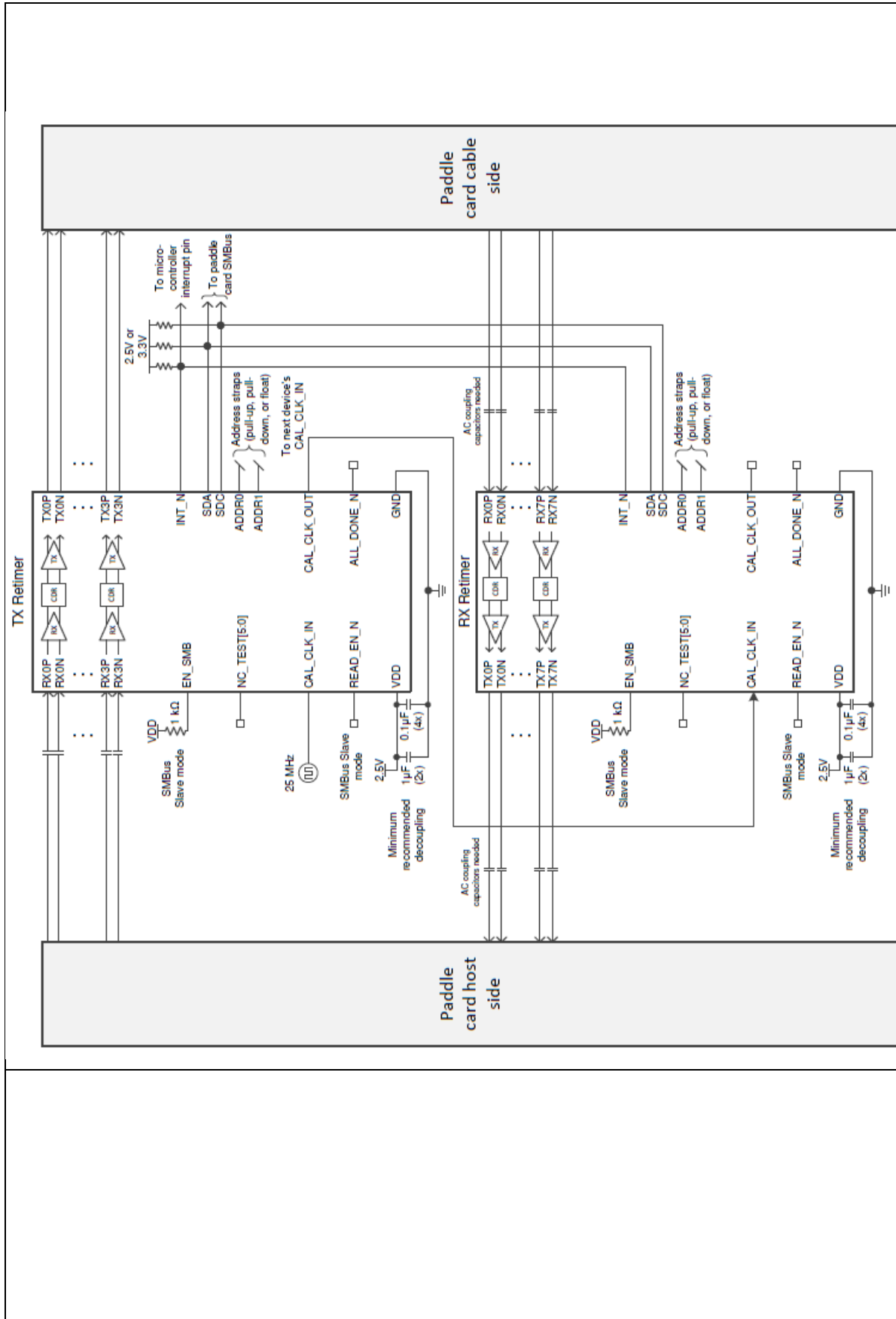


Figure 22. Full-Active Cable Application Schematic

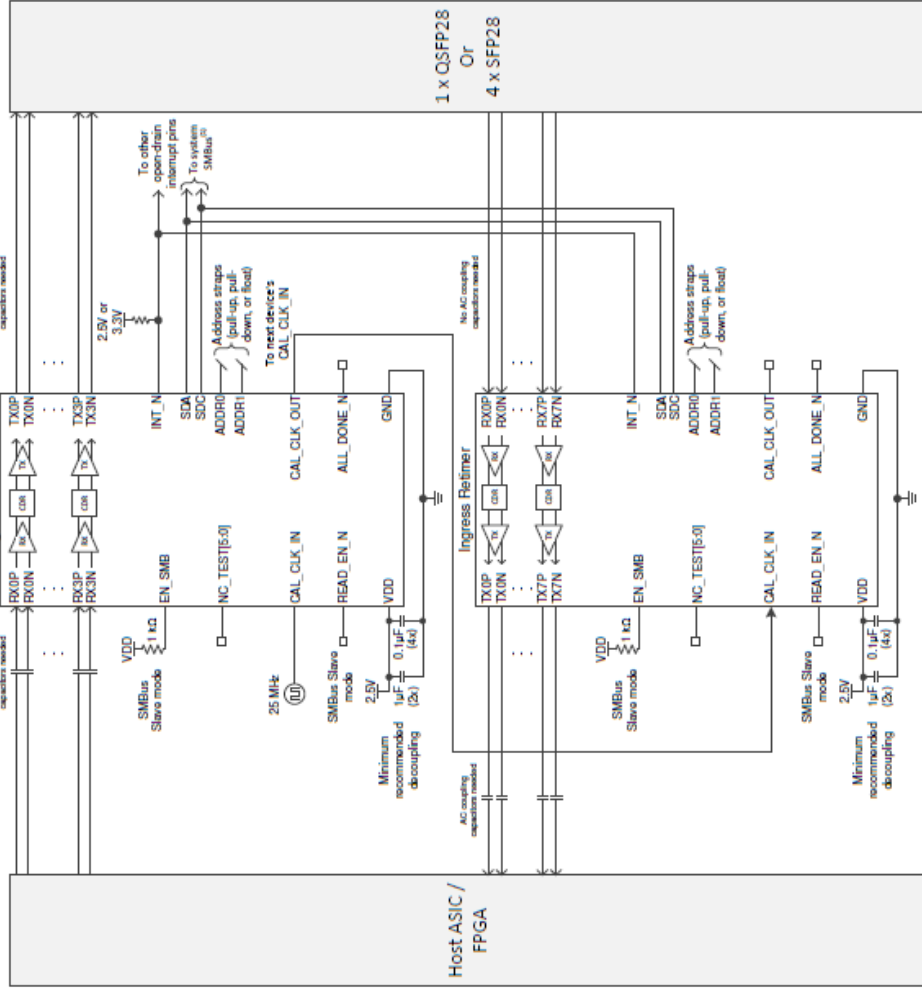
Exhibit A-6

<p>Claim 15</p>	<p>DS250DF410, 83.</p> <p style="text-align: center;">Table 14. Full-Active Cable Application Design Guidelines</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">DESIGN PARAMETER</th> <th style="text-align: center;">REQUIREMENT</th> </tr> </thead> <tbody> <tr> <td>Device placement</td> <td>A full-active QSFP cable will utilize two pieces of DS250DF410 per paddle card. Typically, one device will be placed on each side of the paddle card.</td> </tr> <tr> <td>AC coupling capacitors</td> <td><i>Transmit-side Retimer</i>: 100 nF AC coupling capacitors are required for the RX inputs and are not required for the TX outputs. This link segment will be AC coupled on the paddle card at the opposite end of the cable. <i>Receive-side Retimer</i>: 100 nF AC coupling capacitors are required for the RX inputs and the TX outputs.</td> </tr> <tr> <td>Cable insertion loss</td> <td>The raw cable insertion loss including the insertion loss of the paddle card should be ≤ 35 dB at 25.78125 Gbps Nyquist frequency (12.9 GHz).</td> </tr> </tbody> </table> <p>DS250DF410, 84.</p> <p>To the extent that this preamble is not disclosed, either explicitly or inherently, by DS250DF410, this preamble is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p> <p>DS250DF410 discloses and/or renders obvious this limitation.</p>	DESIGN PARAMETER	REQUIREMENT	Device placement	A full-active QSFP cable will utilize two pieces of DS250DF410 per paddle card. Typically, one device will be placed on each side of the paddle card.	AC coupling capacitors	<i>Transmit-side Retimer</i> : 100 nF AC coupling capacitors are required for the RX inputs and are not required for the TX outputs. This link segment will be AC coupled on the paddle card at the opposite end of the cable. <i>Receive-side Retimer</i> : 100 nF AC coupling capacitors are required for the RX inputs and the TX outputs.	Cable insertion loss	The raw cable insertion loss including the insertion loss of the paddle card should be ≤ 35 dB at 25.78125 Gbps Nyquist frequency (12.9 GHz).
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Cable insertion loss	The raw cable insertion loss including the insertion loss of the paddle card should be ≤ 35 dB at 25.78125 Gbps Nyquist frequency (12.9 GHz).								
<p>15[a] inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p>								

Claim 15

recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and

Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.
Figure 17. Front-Port Application Schematic

DS250DF410, 78.

Claim 15

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

Figure 20 illustrates these configurations, Figure 21 shows an example simplified schematic for a half-active cable application, and Figure 22 shows an example simplified schematic for a full-active cable application.

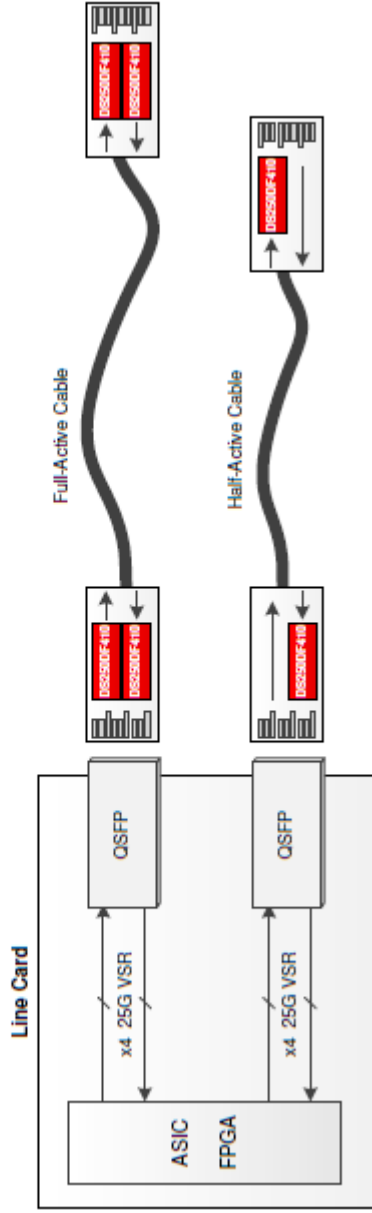


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

Exhibit A-6

Claim 15

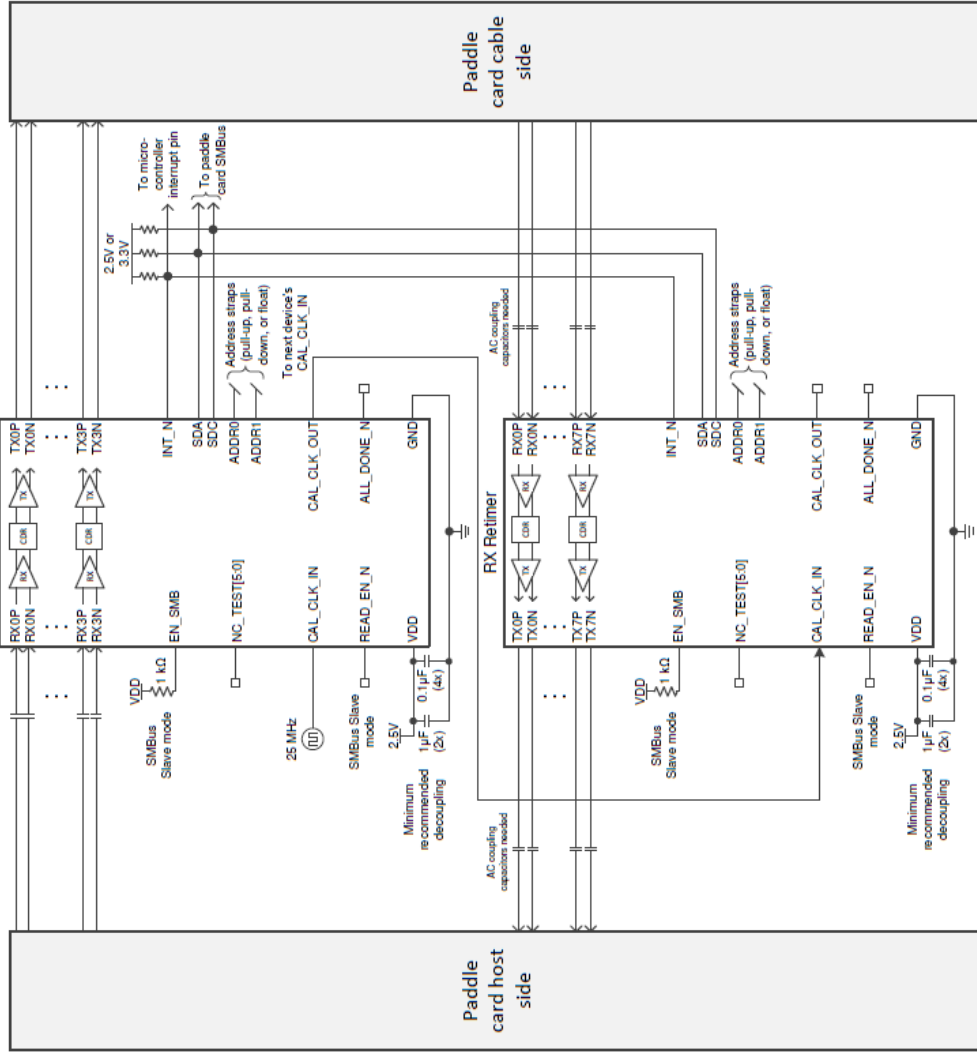


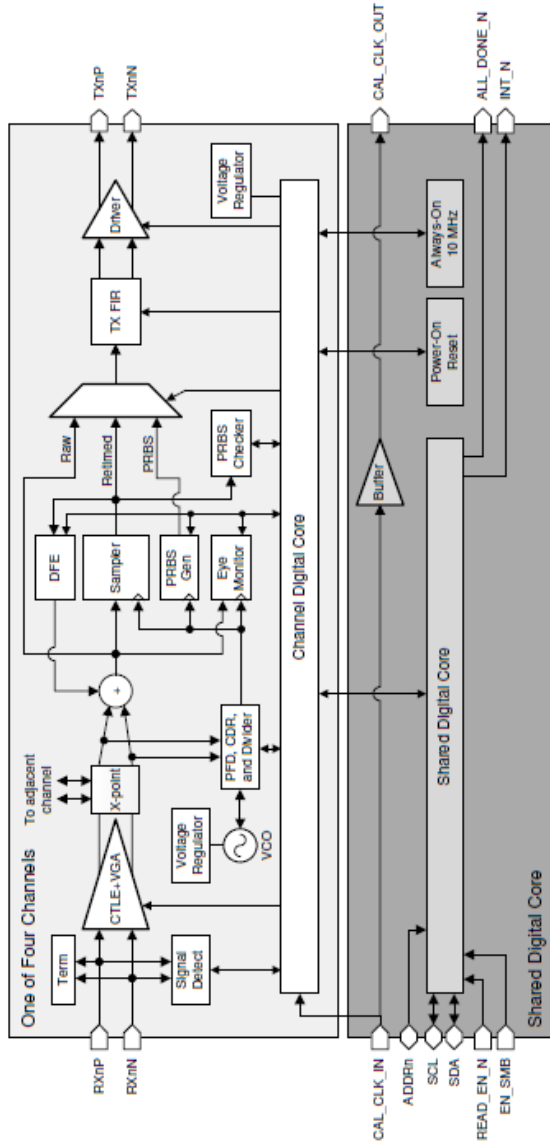
Figure 22. Full-Active Cable Application Schematic

DS250DF410, 83.

<p>Claim 15</p>	<p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 15

8.2 Functional Block Diagram



DS250DF410, 17.

<p>Claim 15</p>	<p>8.3.7 Clock and Data Recovery (CDR) The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes. By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF410 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator. The CDR requires the following to be properly configured:</p> <ul style="list-style-type: none"> • 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN). • Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF410, 19.</p> <p>8.3.9 Differential Driver with FIR Filter The DS250DF410 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. C[0] can take on values in the range [-31, +31]. C[-1] and C[+1] can take on values in the range [-15, 15].</p>
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Claim 15

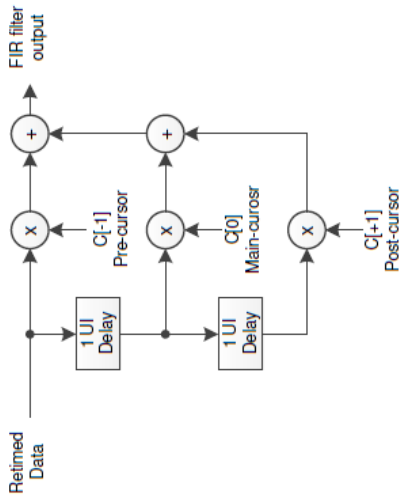


Figure 7. FIR Filter Functional model

When utilizing the FIR filter, it is important to abide by the following general rules:

- $|C[-1]| + |C[0]| + |C[+1]| \leq 31$; the FIR tap coefficients absolute sum must be less or equal to 31
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
- $VOD_{low-frequency} = V_2 - V_5$
- $R_{pre-dB} = 20 * \log_{10} (V_3/V_2)$
- $R_{pst-dB} = 20 * \log_{10} (V_1/V_2)$

DS250DF410, 19-20.

To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or

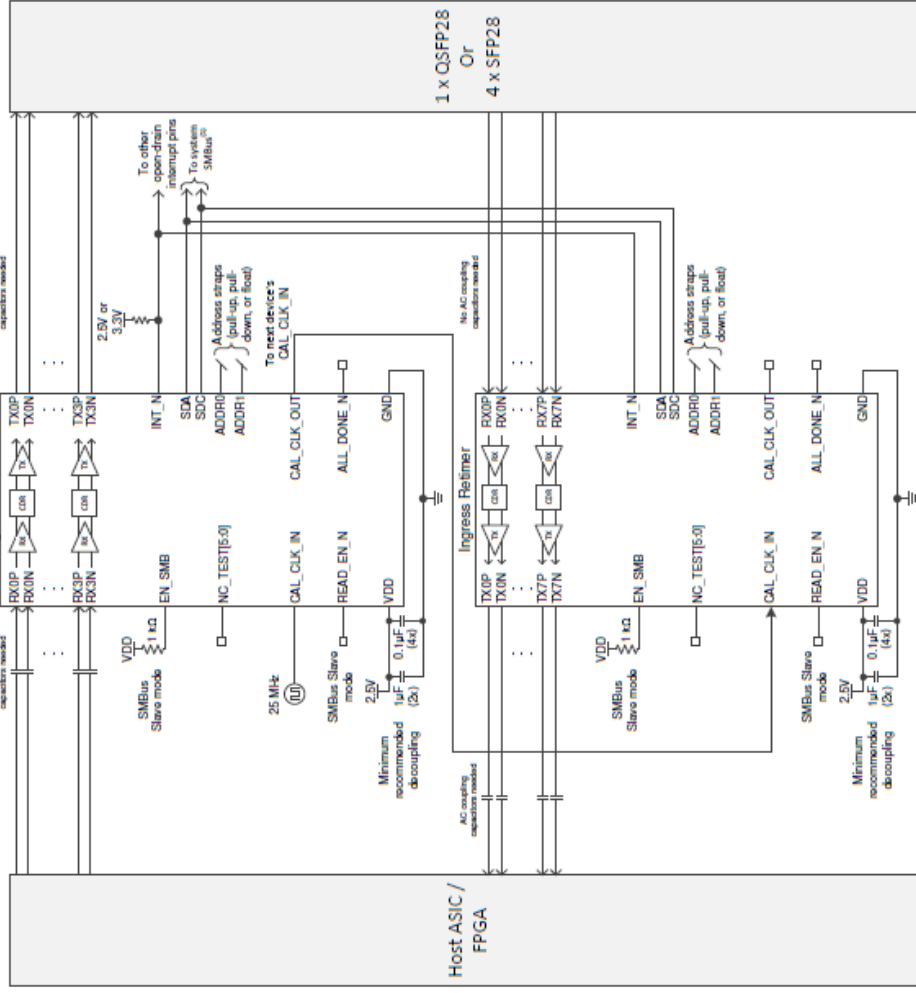
Exhibit A-6

<p>Claim 15</p>	<p>combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>15[b] inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p>

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Claim 15

Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.

Figure 17. Front-Port Application Schematic

DS250DF410, 78.

Claim 15

9.2.2 Active Cable Applications

The DS250DF410 has strong equalization capabilities that allow it to recover data over long and/or thin-gauge copper cables. A single DS250DF410 can be used on a QSFP28 paddle card to create a half-active cable assembly which is longer and/or thinner than passive cables. Alternatively, two DS250DF410 devices can be used on a QSFP28 paddle card to create a full-active cable assembly and achieve even longer reach and/or thinner cables.

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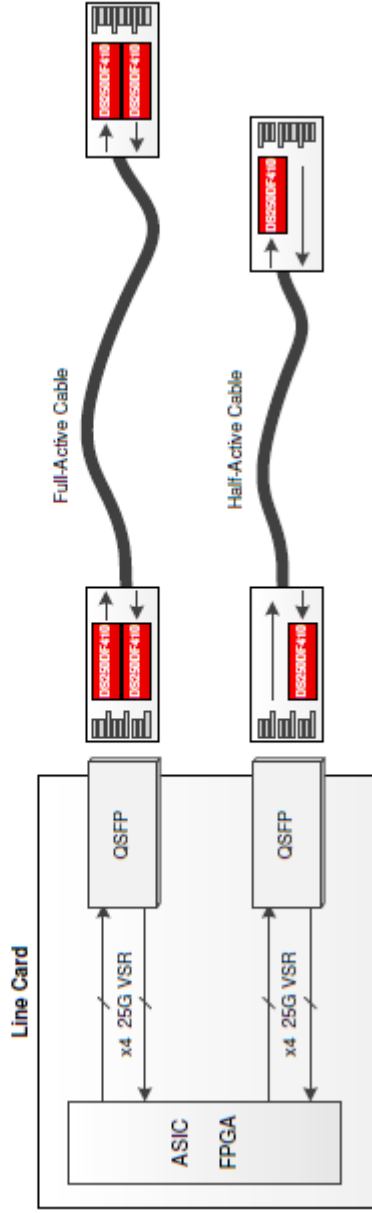


Figure 20. Active Cable Application Block Diagram

DS250DF410, 81.

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Claim 15

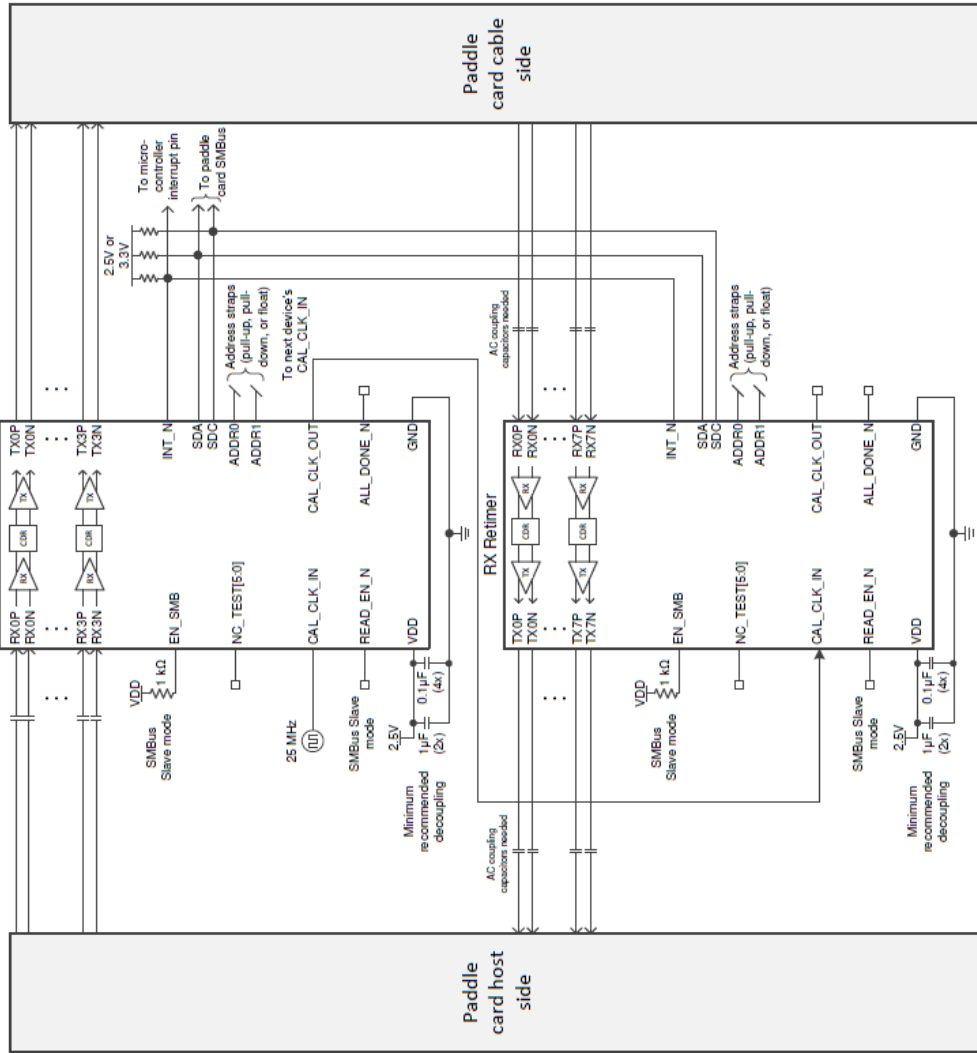


Figure 22. Full-Active Cable Application Schematic

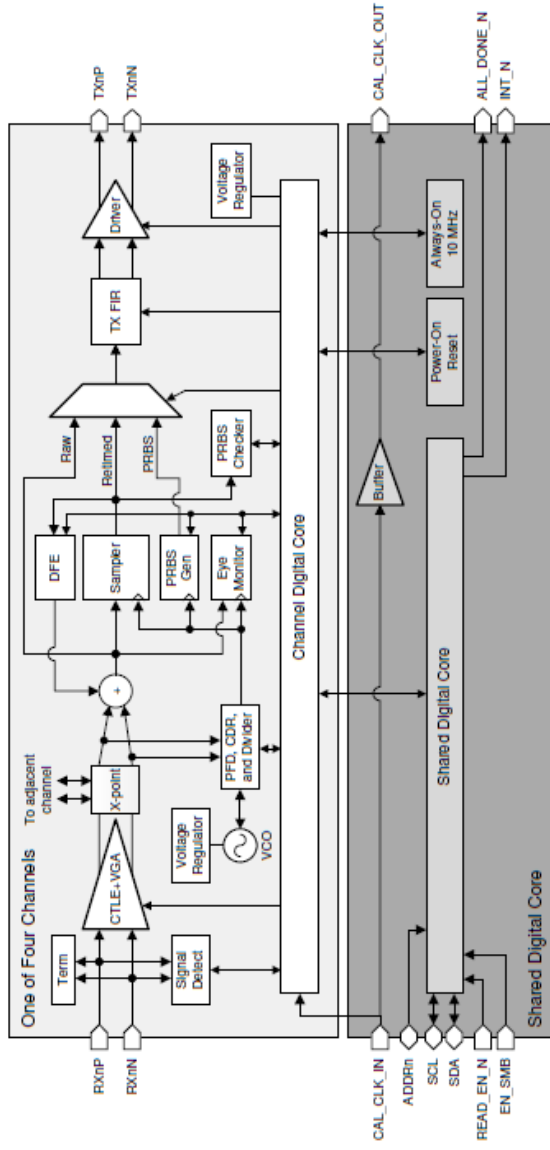
DS250DF410, 83.

Exhibit A-6

<p>Claim 15</p>	<p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 15

8.2 Functional Block Diagram



DS250DF410, 17.

<p>Claim 15</p>	<p>8.3.7 Clock and Data Recovery (CDR) The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes. By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typ) in full-rate (divide-by-1) mode and 5.3 MHz (typ) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS250DF410 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator. The CDR requires the following to be properly configured:</p> <ul style="list-style-type: none"> • 25 MHz calibration clock to run the PPM counter (CAL_CLK_IN). • Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates. <p>DS250DF410, 19.</p> <p>8.3.9 Differential Driver with FIR Filter The DS250DF410 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. C[0] can take on values in the range [-31, +31]. C[-1] and C[+1] can take on values in the range [-15, 15].</p>
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Claim 15

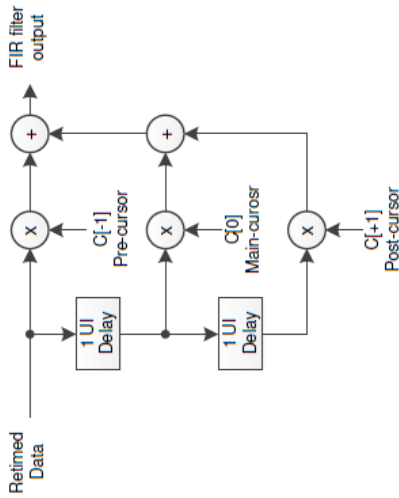


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- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the pre-cursor and/or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
- $VOD_{low-frequency} = V_2 - V_5$
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DS250DF410, 19-20.

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Exhibit A-6

<p align="center">Claim 15</p>	<p>combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
<p>15[c] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p> <p>8.3.9.1 Setting the Output V_{OD}, Pre-Cursor, and Post-Cursor Equalization</p> <p>The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.</p>

Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.695	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.890	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+18	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+28	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.195	NA	1.1

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Exhibit A-6

Claim 15

Table 2. Typical VOD and FIR Values (continued)

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS			Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]				
0	25	-2		1.165	NA	1.3
0	24	-3		1.165	NA	1.8
0	23	-4		1.165	NA	2.2
0	22	-5		1.165	NA	2.7
0	21	-6		1.165	NA	3.3
0	20	-7		1.165	NA	3.9
0	19	-8		1.165	NA	4.7
0	18	-9		1.165	NA	5.7
0	17	-10		1.165	NA	6.9
0	16	-11		1.165	NA	8.4
0	15	-12		1.165	NA	10.1
-1	26	0		1.165	0.7	NA
-2	25	0		1.165	1.2	NA
-3	24	0		1.165	1.5	NA
-4	23	0		1.165	2.0	NA
-5	22	0		1.165	2.6	NA
-6	21	0		1.165	3.2	NA
-7	20	0		1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

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Claim 15

3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_CO_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_CO[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_CO[3]		
	2	0	RW	Y	FIR_CO[2]		
	1	1	RW	Y	FIR_CO[1]		
	0	0	RW	Y	FIR_CO[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0	0	RW	Y	FIR_CN1[0]			

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

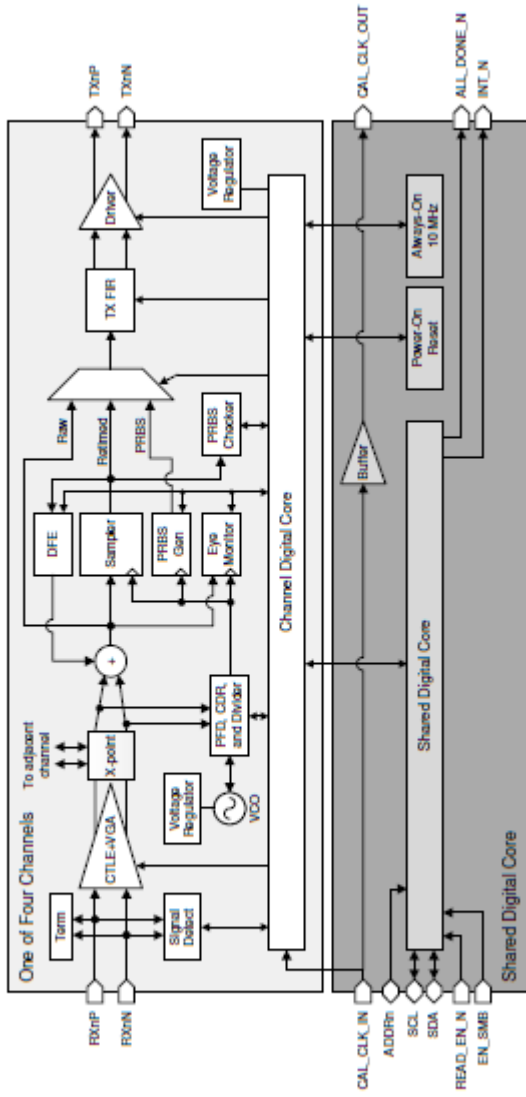
Claim 15	DS250DF410, 53-54. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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P. DEPENDENT CLAIM 16

<p>Claim 16</p> <p>16. The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively, each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p> <p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 16

8.2 Functional Block Diagram



DS250DF410, 17.

Claim 16	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing
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Claim 16

8.5.2 Writing to and Reading from the Global/Shared/Channel Registers

The DS250DF410 has 3 types of registers:

- 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information.
- 2) Shared Registers – These registers are used for device-level configuration, status read back or control.
- 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other.

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:

- Channel selection and share enabling – Registers 0xFC and 0xFF
- Device and version information – Registers 0xEF-0xF3
- Reserved/unused registers – all other addresses

Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.

Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.

TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.

DS250DF410, 30-31.

8.3.9.1 Setting the Output V_{OD} , Pre-Cursor, and Post-Cursor Equalization

The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

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Exhibit A-6

Claim 16

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPOST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 16							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0		0	RW	Y	FIR_CN1[0]		

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

Claim 16	<p>DS250DF410, 53-54.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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Q. DEPENDENT CLAIM 17

Claim 17

17. The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

DS250DF410 discloses and/or renders obvious this limitation.

8.1 Overview

The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.

Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.

Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.

Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.

Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).

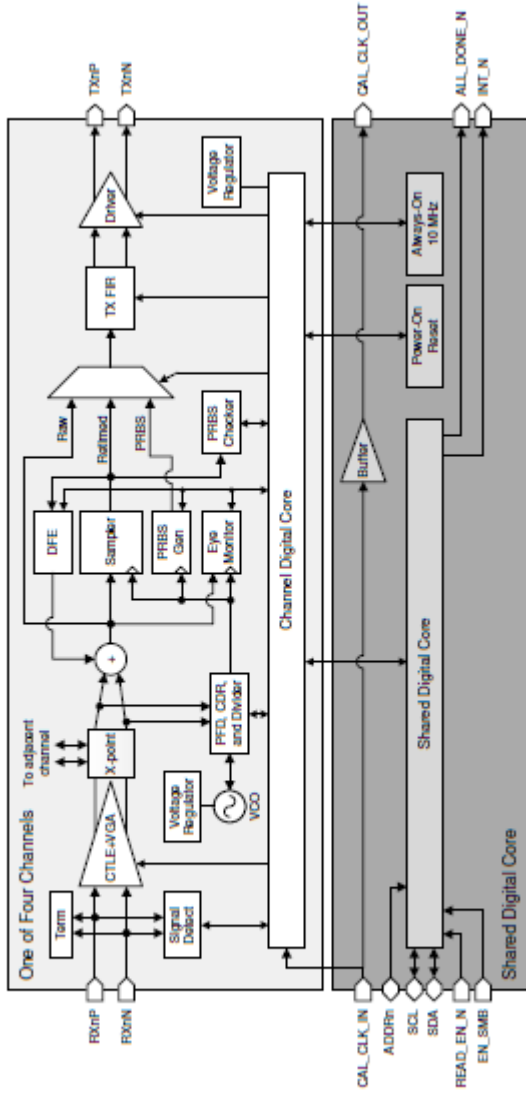
The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.

The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.

DS250DF410, 17.

Claim 17

8.2 Functional Block Diagram



DS250DF410, 17.

<p>Claim 17</p>	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing
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8.5.2 Writing to and Reading from the Global/Shared/Channel Registers

The DS250DF410 has 3 types of registers:

- 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information.
- 2) Shared Registers – These registers are used for device-level configuration, status read back or control.
- 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other.

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:

- Channel selection and share enabling – Registers 0xFC and 0xFF
- Device and version information – Registers 0xEF-0xF3
- Reserved/unused registers – all other addresses

Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.

Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.

TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.

DS250DF410, 30-31.

8.3.9.1 Setting the Output V_{OD} , Pre-Cursor, and Post-Cursor Equalization

The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

INVESTIGATION No. 337-TA-1446
RESPONDENTS' INITIAL INVALIDITY C

Exhibit A-6

Claim 17

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 17							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0		0	RW	Y	FIR_CN1[0]		

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

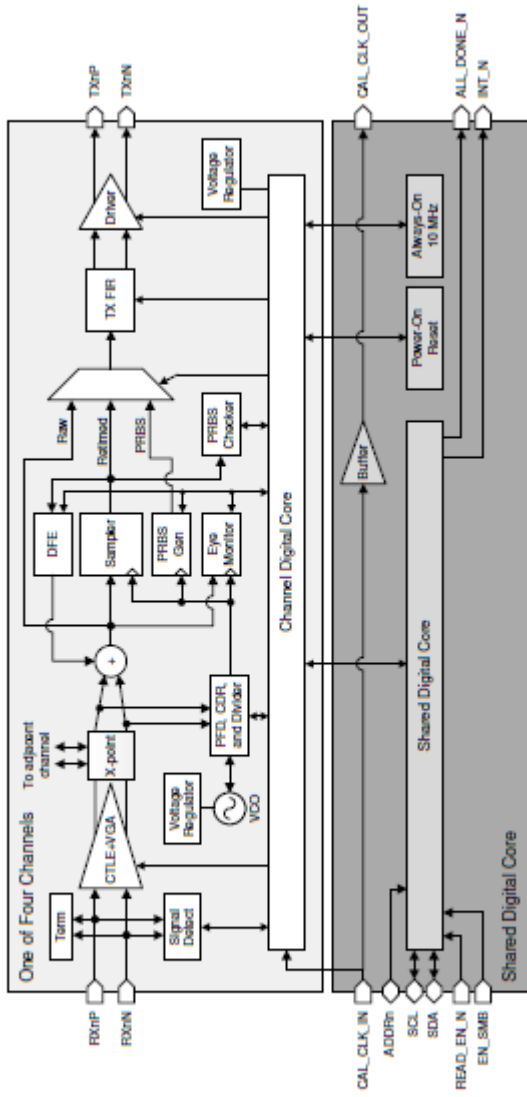
<p>Claim 17</p>	<p>DS250DF410, 53-54.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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R. DEPENDENT CLAIM 18

<p>Claim 18</p> <p>18. The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p> <p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 18

8.2 Functional Block Diagram



DS250DF410, 17.

Claim 18	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing
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8.5.2 Writing to and Reading from the Global/Shared/Channel Registers

The DS250DF410 has 3 types of registers:

- 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information.
- 2) Shared Registers – These registers are used for device-level configuration, status read back or control.
- 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other.

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:

- Channel selection and share enabling – Registers 0xFC and 0xFF
- Device and version information – Registers 0xEF-0xF3
- Reserved/unused registers – all other addresses

Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.

Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.

TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.

DS250DF410, 30-31.

8.3.9.1 Setting the Output V_{OD} , Pre-Cursor, and Post-Cursor Equalization

The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSORS: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSORS: REG_0x3D[6:0]	POST-CURSORS: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

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Exhibit A-6

Claim 18

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 18							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0		0	RW	Y	FIR_CN1[0]		

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

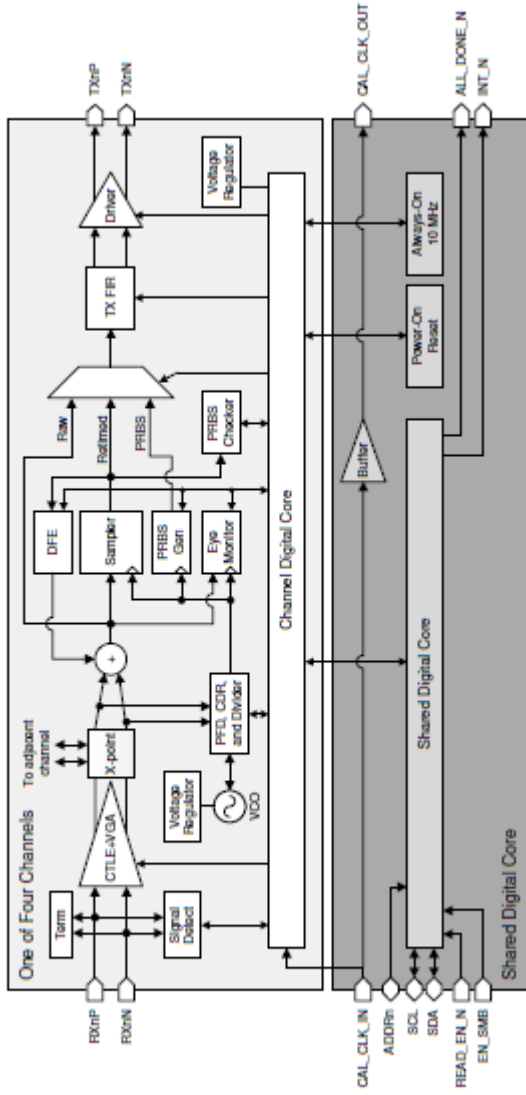
<p>Claim 18</p>	<p>DS250DF410, 53-54.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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S. DEPENDENT CLAIM 19

<p>Claim 19</p> <p>19. The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p> <p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 19

8.2 Functional Block Diagram



DS250DF410, 17.

Claim 19	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing
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8.5.2 Writing to and Reading from the Global/Shared/Channel Registers

The DS250DF410 has 3 types of registers:

- 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information.
- 2) Shared Registers – These registers are used for device-level configuration, status read back or control.
- 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other.

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:

- Channel selection and share enabling – Registers 0xFC and 0xFF
- Device and version information – Registers 0xEF-0xF3
- Reserved/unused registers – all other addresses

Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.

Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.

TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.

DS250DF410, 30-31.

8.3.9.1 Setting the Output V_{OD} , Pre-Cursor, and Post-Cursor Equalization

The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

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Exhibit A-6

Claim 19

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPOST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 19							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude (Refer to the Programming Guide for more details)	
	3	1	RW	Y	FIR_C0[3]		
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude (Refer to the Programming Guide for more details)
		2	0	RW	Y	FIR_CN1[2]	
1		0	RW	Y	FIR_CN1[1]		
0		0	RW	Y	FIR_CN1[0]		

Table 11. Channel Registers, 3A to A9 (continued)

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude (Refer to the Programming Guide for more details)
	2	0	RW	Y	FIR_CP1[2]	
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Exhibit A-6

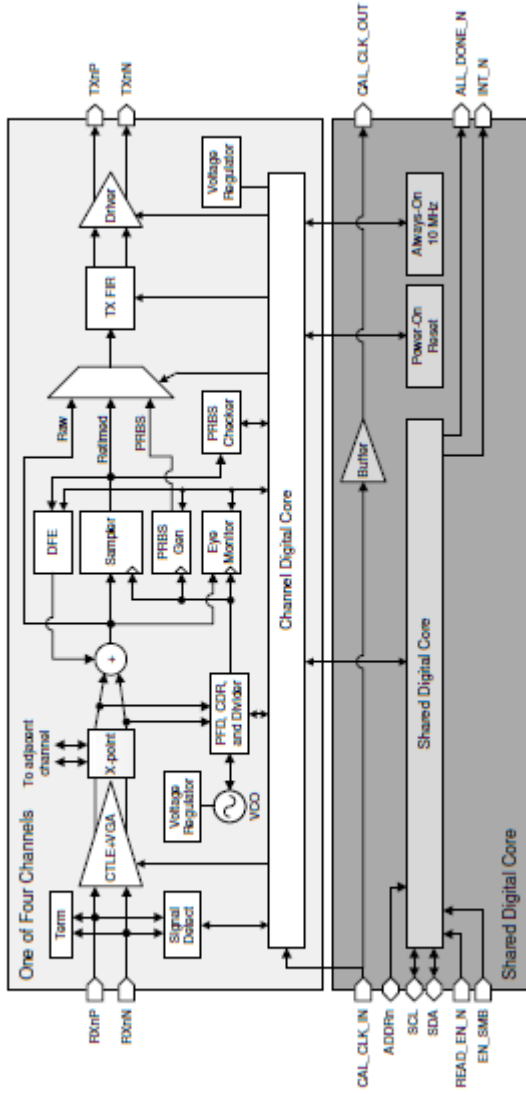
Claim 19	<p>DS250DF410, 53-54.</p> <p>To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.</p>
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T. DEPENDENT CLAIM 20

<p>Claim 20</p> <p>20. The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.</p>	<p>DS250DF410 discloses and/or renders obvious this limitation.</p> <p>8.1 Overview</p> <p>The DS250DF410 is a four-channel multi-rate retimer with integrated signal conditioning. Each of the four channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF410 receiver. The CTLE and DFE are self-adaptive.</p> <p>Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.</p> <p>Each channel of the DS250DF410 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF410.</p> <p>Between each group of two adjacent channels (e.g. between channels 0 and 1, 2 and 3) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.</p> <p>Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).</p> <p>The DS250DF410 is configurable through a single SMBus port. The DS250DF410 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF410 devices can share a single SMBus.</p> <p>The sections which follow describe the functionality of various circuits and features within the DS250DF410. For more information about how to program or operate these features, consult the DS250DF410 Programming Guide.</p> <p>DS250DF410, 17.</p>
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Claim 20

8.2 Functional Block Diagram



DS250DF410, 17.

<p>Claim 20</p>	<p>8.5 Programming</p> <p>8.5.1 Bit Fields in the Register Set</p> <p>Many of the registers in the DS250DF410 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF410 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.</p> <p>Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.</p> <p>Register bits can have the following interface constraints:</p> <ul style="list-style-type: none"> • R - Read only • RW - Read/Write • RWSC - Read/Write, self-clearing
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Claim 20

8.5.2 Writing to and Reading from the Global/Shared/Channel Registers

The DS250DF410 has 3 types of registers:

- 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information.
- 2) Shared Registers – These registers are used for device-level configuration, status read back or control.
- 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independently of each other.

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF410 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:

- Channel selection and share enabling – Registers 0xFC and 0xFF
- Device and version information – Registers 0xEF-0xF3
- Reserved/unused registers – all other addresses

Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected in register 0xFC when attempting to perform an SMBus read, the device will return 0xFF.

Register 0xFF bit 1 can be used to perform broadcast writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.

TI repeaters/retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF410.

DS250DF410, 30-31.

8.3.9.1 Setting the Output V_{OD} , Pre-Cursor, and Post-Cursor Equalization

The output differential voltage (V_{OD}), pre-cursor, and post-cursor equalization of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre- and post-cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre- and post-cursor tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

Exhibit A-6

Table 2. Typical VOD and FIR Values

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.480	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1

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Exhibit A-6

Claim 20

Table 2. Typical VOD and FIR Values (Continued)

PRE-CURSOR: REG_0x3E[6:0]	FIR SETTINGS		Peak-to Peak VOD(V)	RPRE(dB)	RPOST(dB)
	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF410 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre- or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF410 receiver.

DS250DF410, 21-23.

Exhibit A-6

Claim 20							
3D	7	0	RW	Y	EN_FIR_CURSOR	1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power)	
	6	0	RW	Y	FIR_C0_SGN	Main-cursor sign bit 0: positive 1: negative	
	5	0	RW	Y	RESERVED	RESERVED	
	4	1	RW	Y	FIR_C0[4]	Main-cursor magnitude	
	3	1	RW	Y	FIR_C0[3]	(Refer to the Programming Guide for more details)	
	2	0	RW	Y	FIR_C0[2]		
	1	1	RW	Y	FIR_C0[1]		
	0	0	RW	Y	FIR_C0[0]		
	3E	7	0	RW	Y	FIR_PD_TX	
		6	1	RW	Y	FIR_CN1_SGN	Pre-cursor sign bit 1: negative 0: positive
		5	0	RW	Y	RESERVED	RESERVED
		4	0	RW	Y	RESERVED	RESERVED
		3	0	RW	Y	FIR_CN1[3]	Pre-cursor magnitude
2		0	RW	Y	FIR_CN1[2]	(Refer to the Programming Guide for more details)	
1		0	RW	Y	FIR_CN1[1]		
0	0	RW	Y	FIR_CN1[0]			

ADDRESS (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
3F	7	0	RW	Y	RESERVED	RESERVED
	6	1	RW	Y	FIR_CP1_SGN	Post-cursor sign bit 1: negative 0: positive
	5	0	RW	Y	RESERVED	RESERVED
	4	0	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	FIR_CP1[3]	Post-cursor magnitude
	2	0	RW	Y	FIR_CP1[2]	(Refer to the Programming Guide for more details)
	1	0	RW	Y	FIR_CP1[1]	
	0	0	RW	Y	FIR_CP1[0]	

Table 11. Channel Registers, 3A to A9 (continued)

Exhibit A-6

Claim 20	DS250DF410, 53-54. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS250DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS250DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
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