

U.S. Patent No. 10,877,233 Claim Limitation Comparison Chart

I. LIMITATIONS [8.PRE]-[8.f]

Ref	Limitation	Ref	Corresponding limitation
8.PRE	A cable manufacturing method that comprises:	1.PRE	A cable that comprises:
8.a	connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges multi-lane data streams with a first host interface port via the first connector plug;	1.a	a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;
8.b	connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;	1.b	a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and
8.c	connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween,	1.c	electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,
8.d	the first DRR device converting between said electrical transit signals and said multi-lane data streams for the first host interface port, and	1.d	the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and

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Ref	Limitation	Ref	Corresponding limitation
8.e	the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port,	1.e	the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,
8.f	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.	1.f	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

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II. CLAIMS 7, 14, 20

Claim	Limitation	Claim	Corresponding limitation	Claim	Corresponding limitation
7	The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.	14	The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.	20	The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

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III. CLAIMS 9-14

Claim	Limitation	Claim	Corresponding limitation
9	The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.	2	The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.
10	The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.	3	The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.
11	The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.	4	The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.

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Claim	Limitation	Claim	Corresponding limitation
12	The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.	5	The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.
13	The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.	6	The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.

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IV. LIMITATIONS [15.PRE]-[15.c]

Ref	Limitation	Ref	Corresponding limitation
15.PRE	A communications method that comprises:	1.PRE	A cable that comprises:
15.a	inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and	1.a	a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;
		1.d	the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and
		1.c	electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,
15.b	inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,	1.b	a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and
		1.c	electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,

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Ref	Limitation	Ref	Corresponding limitation
		1.e	the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,
15.c	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.	1.f	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

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V. CLAIMS 17-19

Claim	Limitation	Claim	Corresponding limitation
17	The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.	3	The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.
18	The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.	4	The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.
19	The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.	5	The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.