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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,
Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC
Patent Owner

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IPR2025-00832
U.S. Patent 8,796,779

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PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 8,796,779

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1016	"International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures" (2007 Edition) ("ITRS")

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1020	H.-J. Li and M. Gardner, "Dual high-k gate dielectric with poly gate electrode: HfSiON on nMOS and Al2O3 capping layer on pMOS," IEEE Electron Device Lett., vol. 26, no. 7, pp. 441-443, 2005. ("Li/Gardner")
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1023	"Semiconductor Devices: Physics and Technology" by Sze (Second Edition, 2002) ("Sze")
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1033	“Dual Work Function Metal Gate CMOS Transistors by Ni-Ti Interdiffusion”, Polishchuk, et al., IEEE Electron Device Letters, Vol. 23, No. 4, April 2002

I. Introduction

Taiwan Semiconductor Manufacturing Company, Limited ("Petitioner") petitions for *inter partes* review of U.S. Patent 8,796,779 ("'779 patent"; TSMC-1001) claims 1 and 8-15 ("the challenged claims"). The challenged claims are directed to "a semiconductor device" comprising two MIS transistors, each having a "gate insulating film" including an "interface layer" and "high dielectric constant insulating film." (*See* TSMC-1001, claim 1.) The allegedly novel feature, that the "interface layer" of one transistor "has a thickness larger than" the "interface layer" of the other transistor, was determined by the Japanese Examiner to be known during prosecution of the Japanese counterpart application. Applicant acquiesced and narrowed the independent claim in Japan, a fact not shared with the U.S. Examiner.

Petitioner, supported by the declaration of Dr. Jakub Kedzierski, having over two decades of experience, demonstrates the challenged claims are unpatentable.

II. Grounds for Standing

Petitioner certifies the '779 patent is available for IPR and it is not barred or estopped from requesting IPR on the grounds herein.

III. Identification of Challenge

A. Prior Art

The ’779 patent was filed on October 31, 2012 as a continuation of PCT/JP2011/002868 (“PCT application”), filed May 24, 2011, which claims priority to JP2010-205599 (“JP application”), filed September 14, 2010. Petitioner does not acquiesce the ’779 patent is entitled to priority benefit of the PCT or the JP applications. Regardless, each applied reference was filed or published before September 14, 2010.

1. **U.S. Patent 6,881,657 to Torii, et al.** (“Torii”; TSMC-1005), issued April 19, 2005, is prior art under 35 U.S.C. §102(b).

2. **U.S. Publication 2010/0258878 to Mise, et al.** (“Mise”; TSMC-1006), filed November 26, 2008, is prior art under 35 U.S.C. §102(e).

3. **U.S. Patent 6,693,333 to Yu** (“Yu”; TSMC-1008), issued February 17, 2004, is prior art under 35 U.S.C. §102(b).

4. **U.S. Patent 6,787,421 to Gilmer, et al.** (“Gilmer”; TSMC-1009), issued September 7, 2004, is prior art under 35 U.S.C. §102(b).

5. **U.S. Patent 7,382,023 to Chen, et al.** (“Chen”; TSMC-1010), issued June 3, 2008, is prior art under 35 U.S.C. §102(b).

B. Grounds for Challenge

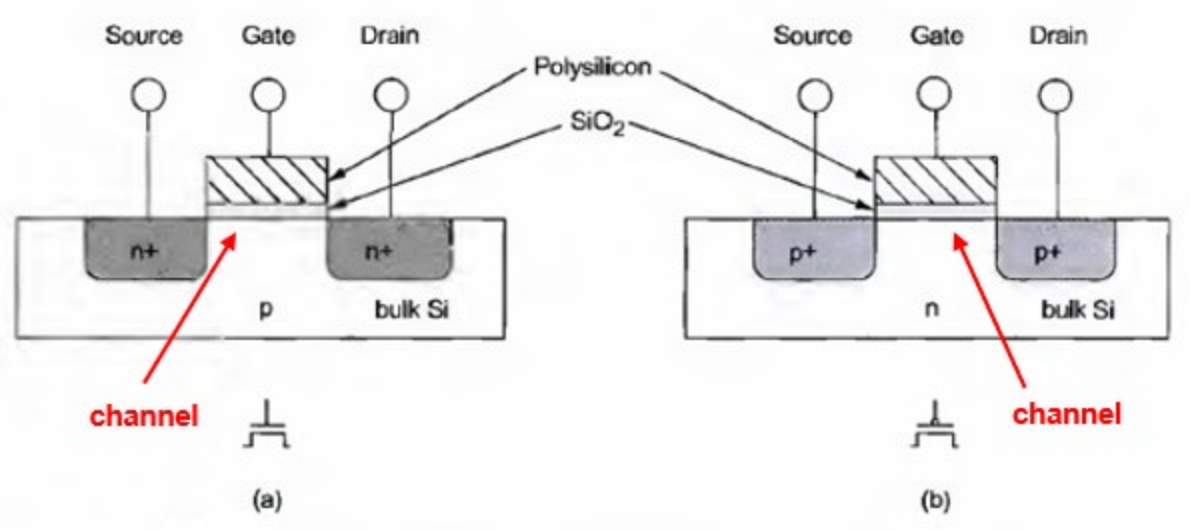
Ground		Claims	Prior Art
1	102	1, 12-15	Torii
2	103	8-11	Torii + Mise
3	103	15	Torii + Yu
4	103	1, 12-15	Gilmer
5	103	1, 12-15	Gilmer + Chen
6	103	8-11	Gilmer, Chen, + Mise

IV. The '779 patent.

A. Technical Background

A metal-insulating-semiconductor transistor (MISFET or MOSFET) generally includes a conducting gate electrode, an insulating layer, and "the silicon wafer, also called the substrate, body or bulk." (TSMC-1012, 8.) An nMOS transistor "is built with a p-type body and has regions of n-type semiconductor adjacent to the gate called the source and drain." (TSMC-1012, 8, Figure 1.8(a)(below).) A pMOS transistor "is just the opposite, consisting of p-type source and drain regions with an n-type body." (TSMC-1012, 8, Figure 1.8(b)(below)[1].)

[1] Unless otherwise noted, all shading and annotations added.



Weste, Figure 1.8

A key device feature is the gate insulating film, commonly referred to as a "gate dielectric", which separates the gate electrode from the semiconductor channel between the source and drain. For over 40 years (1961-2007), silicon-based oxides were the primary materials used for gate dielectrics in MOSFETs due to their excellent insulating properties, thermal stability, and compatibility with silicon. However, as transistors scaled down, the silicon-based oxide layer had to become thinner, leading to increased gate leakage due to quantum tunneling. (TSMC-1013, 5-8.) High-k dielectrics, which allow for a thicker gate insulator while maintaining the same capacitance, replaced silicon-based oxides to address these challenges. (TSMC-1013, 8-9.)

Equivalent Oxide Thickness (EOT) is a key concept used in assessing high-k dielectrics. The EOT (t_{eq}) of a material "is defined as the thickness of the SiO_2

layer that would be required to achieve the same capacitance density as the high-k material in consideration." (TSMC-1013, 9.) The EOT of a gate dielectric having only a high-k layer is given by the following equation:

$$\frac{t_{eq}}{\varepsilon_{r,SiO_2}} = \frac{t_{high\text{-}\kappa}}{\varepsilon_{r,high\text{-}\kappa}} \qquad (1.1.2)$$

"where $t_{high\text{-}k}$ and $\varepsilon_{r,high\text{-}k}$ are the thickness and relative dielectric constant of the high-k material, respectively." (*Id.*) For example, "using ZrO_2 as gate dielectric ($\varepsilon_r \approx 20$)" allows "use a 5.1 nm thick layer in order to achieve a capacitance equivalent to a 1 nm thick SiO_2 layer; the equivalent oxide thickness of this ZrO_2 layer is thus 1 nm." (*Id.*)

The threshold voltage is the voltage applied at the gate which brings the onset of inversion (formation of the current-carrying channel)—i.e., the transistor's "turn-on" voltage. (TSMC-1011, 526.) Because pMOS and nMOS transistors are built on different dopant type bodies and feature different types of dopants for their respective source/drain terminals, nMOS transistors, which use electrons in a p-type body to form the channel between the source and drain terminals, have a **positive** threshold voltage and pMOS transistors, which use holes in an n-type body to form the channel between the source and drain terminals, have a **negative** threshold voltage. (*See, e.g.,* TSMC-1012, 74, 293-296, 302; TSMC-1003, ¶54.)

Consumer devices often have multiple transistors of the same conductivity types but with different threshold voltages to cope with various demands on standby power and operation speed. For example, a device may include transistors for low operating power (LOP), transistors for low stand-by power (LSTP), and transistors for high performance (HP). (TSMC-1003, ¶55; TSMC-1016, 5.) HP transistors have the highest operating speed, the shortest gate length, the thinnest gate oxide, and the lowest threshold voltage among the three. (TSMC-1016, 11, 17, 21.) LSTP transistors are designed for low performance and low leakage current and therefore have thicker gate oxides and higher threshold voltage, while LOP transistors are between the HP and LSTP devices in terms of performance, leakage current, and threshold voltage. (TSMC-1016, 11, 17, 21.)

Threshold voltage has three main components: flatband voltage (V_{FB}), voltage drop across the gate oxide (V_o), and semiconductor potential at the semiconductor surface during strong inversion ($\psi_s(inv)$). (TSMC-1023, 175, 178, 194; TSMC-1003, ¶¶57-59.) For a given semiconductor and dielectric material, the primary "knobs" that can be used to predictably tune a transistor's threshold voltage are substrate doping, oxide thickness t_{ox}, and the metal work function Φ_m. (TSMC-1013, 535, 537; TSMC-1003, ¶59.) When the substrate doping and gate oxide thickness are carefully engineered to control channel mobility and the gate

capacitance, respectively, the gate electrode work function is the "knob" of choice to optimize (fine-tune) the threshold voltage further. (TSMC-1003, ¶59.)

A material's "work function" is "the minimum energy required to bring an electron from the Fermi level to the vacuum level." (TSMC-1029, 117; *see, e.g.,* TSMC-1003, ¶¶42-53, 60.) However, in MOS/MIS structures, the metal is in direct contact with a dielectric, not with the vacuum. Moreover, work functions of metal gates are highly dependent on material properties and interfaces. To differentiate this, an "effective work function" of **the metal gate**[2] is commonly used to refer to the metal work function as measured, e.g., through the threshold voltage of the device. (TSMC-1003, ¶61.)

Metal gates are commonly used in gate stacks with high-k gate dielectrics because metal gates eliminate the polysilicon depletion effect, have very low resistance, and have better compatibility with high-k dielectrics (e.g., are immune to Fermi level pinning). (TSMC-1003, ¶32.) Because the work function of a metal is an intrinsic material property that cannot be easily tuned via doping as in the case of polysilicon gates, introducing metal gates into transistors means the threshold voltage of the MOSFET becomes tied to the metal selection. (TSMC-

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[2] The '779 patent's use of the term "effective work function of **the transistor"** is discussed in §IV.B.

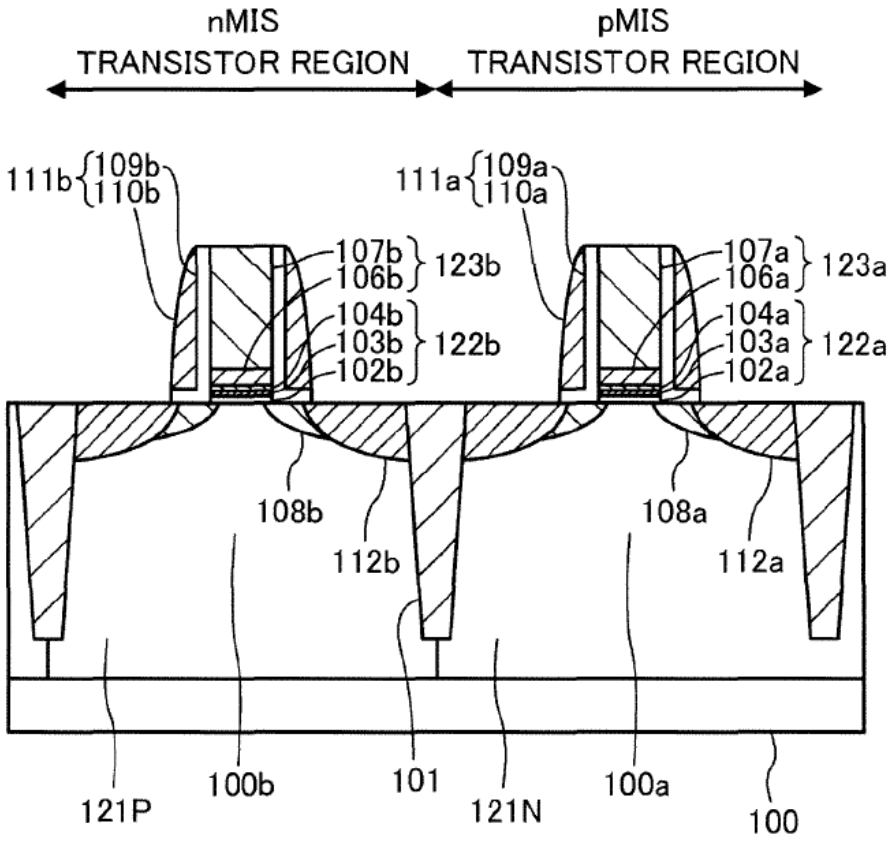
1016, 3; TSMC-1003, ¶64.) Many techniques existed prior to the '779 patent to tune the work function of a metal gate including, for example, adjusting the gate electrode composition and adding metal layer(s). (*See* TSMC-1003, ¶¶65-66.)

B. '779 Patent's Background

The '779 patent describes a conventional "complementary metal insulator semiconductor (CMIS) device composed of an n-type MIS transistor and a p-type MIS transistor which are provided on an identical substrate." (TSMC-1001, 1:48-51.) The pMIS/nMIS transistors in the conventional device include a gate insulating film having interface layer 102, high-k dielectric 103, and cap layer 104 and a gate electrode having a metal film and a polysilicon film. (*See* TSMC-1001, 1:61-2:31; Figure 13 (below).) The background section acknowledges pMIS cap film 104a and nMIS cap film 104b "enable control of a work function of each of the gate electrodes 123a and 123b." (TSMC-1001, 2:24-27.) The '779 patent also refers to an effective work function of **a transistor** which it describes as "a work function obtained from electrical characteristics of a MIS transistor." (TSMC-1001, 3:18-19.) The '779 patent contends the transistor's "effective work function is obtained by incorporating influence such as a **level in an insulating film**[3] into a

[3] Unless otherwise noted, all emphasis added.

work function related to physical properties and representing a difference between a vacuum level and an energy level of a metal." (TSMC-1001, 3:20-24.)

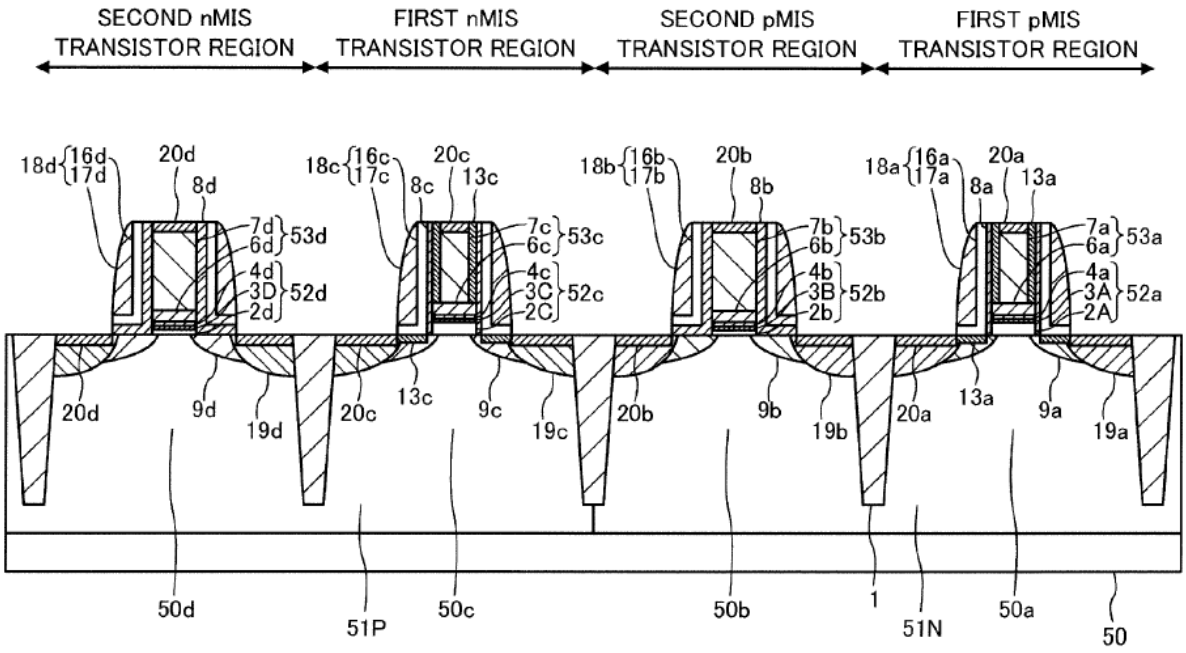


'779 Patent, Figure 13 [Admitted Prior Art]

C. '779 Patent Overview

The '779 patent's purported objective is to "enable formation of a plurality of transistors of the same conductivity type having different work functions in a semiconductor device having a MIS structure in which a high-k film is used as a gate insulating film." (TSMC-1001, 3:50-54.) The '779 patent's semiconductor device includes first and second pMIS transistor regions and first and second nMIS

transistor regions. (TSMC-1001, 7:13-14, Figure 9 (below).) Each transistor includes gate electrode (53a-d) with gate insulating film (52a-52d) interposed between the gate electrode and an active region of the substrate (50a-d). (TSMC-1001, 8:47-60.) Each gate insulating film includes interface layer 2a-2d, high-k film 3a-3d, and cap film 4a-4d. (TSMC-1001, 8:61-67.) The interface layers 2A and 2C in the first nMIS and pMIS regions are thicker than the interface layers 2b and 2d in the second nMIS and pMIS regions. (*See* TSMC-1001, 9:55-10:5.)



'779 Patent, Figure 9

The '779 patent concludes the increased interface layer thickness of the first pMIS and nMIS transistors leads to an increased EOT which results in an increased "effective work function of the transistors": "Accordingly, the EOT of the gate insulating film 52a of the first pMIS transistor and that of the gate insulating film

52c of the first nMIS transistor increase, **thereby causing** the effective work functions of the first pMIS transistor and the first nMIS transistor to increase." (TSMC-1001, 13:23-27; *see also*, 12:47-54, 13:19-23.)

D. Prosecution History

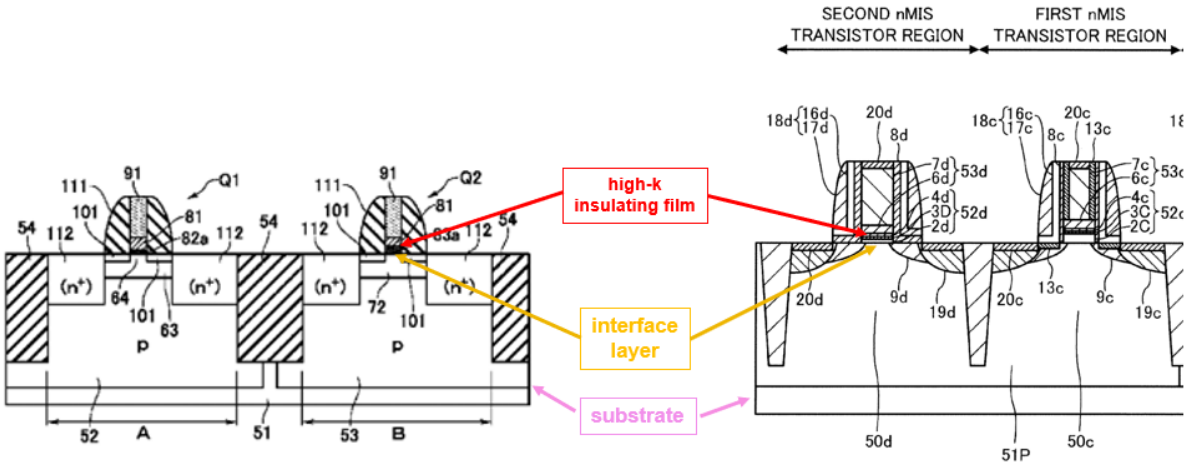
1. '779 Patent

The U.S. application was filed with one independent semiconductor device claim corresponding to issued claim 1. The Examiner rejected the claim as anticipated by U.S. Patent 8,492,230 to Ishikawa, et al. ("Ishikawa"). (TSMC-1002, 204-205.) In response, Applicant argued Ishikawa's gate insulating films "are formed above different base substrate[s]" and therefore Ishikawa does not anticipate claim 1. (TSMC-1002, 300-301.) Notably, Applicant did not dispute Ishikawa discloses two transistors with different interface layer thicknesses. Applicant also amended claim 1 to recite "each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film." (TSMC-1002, 294.) The Examiner subsequently allowed the claims. (TSMC-1002, 312-313.)

2. JP Application

The JP priority application was filed with a device claim having nearly identical scope as the '779 patent's issued claim 1. (TSMC-1030, 1.) On August 20, 2013, before issuance of the '779 patent, the JP Examiner found the claims

unpatentable over three separate JP publications including JP2003-100896 to Fujiwara ("Fujiwara"). (TSMC-1030, 4-5.) Fujiwara, illustrated in Figure 11 (below left), discloses transistors of the same conductivity type formed on the same substrate with different interfacial layer thicknesses, like the '779 patent's claimed transistors.



Fujiwara's, Figure 11; '779 Patent, Figure 9-Excerpt

In response, on September 13, 2013, Applicant narrowed the independent claim to recite sidewall spacer limitations corresponding to the '779 patent's issued claim 2. (TSMC-1030, 7.) The JP Examiner allowed the claims based on this amendment.

Thus, Applicant acquiesced during JP prosecution that the scope of issued claim 1 of the '779 patent was unpatentable. Though the JP refusal and Applicant's subsequent JP amendment occurred before the '779 patent's issuance, Applicant

did not provide a translation of the JP refusal notice or its response to the U.S. Examiner.

E. Claim Construction

Petitioner does not believe any claims require construction to resolve the patentability disputes in this proceeding. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)

F. Level of Ordinary Skill in the Art

A POSITA would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing, including planar transistors. (TSMC-1003, ¶89.) Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. (*Id*.)

V. GROUNDS OVERVIEW

The Petition presents Grounds 1, 4 and 5 demonstrating independent claim 1 and dependent claims 12-14 are unpatentable and Grounds 2 and 6 demonstrating dependent claims 8-11 are unpatentable. Regarding claim 15, the '779 patent describes the **effective work function of a transistor** and discloses only one technique for adjusting it—altering the thickness of the interfacial layer of the gate insulating layer and hence the EOT of the gate insulating layer. Claim 15 is

specifically directed to this concept, reciting "*an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor.*" Grounds 1 and 4 establish claim 15 is anticipated or obvious in the same manner as disclosed in the '779 patent.

Despite this limited disclosure, PO alleges in the co-pending district court litigation a transistor with an additional metal layer in its gate electrode would demonstrate a slightly higher effective work function than another MIS transistor missing this layer because the additional layer allegedly possesses a higher effective work function[4]. Regardless, adjusting the **work function of a metal gate electrode** in this and other ways was well known before the '779 patent. (TSMC-1003, ¶¶62-67.) Grounds 3 and 5 establish claim 15 is obvious under PO's litigation allegations.

VI. GROUND 1: Torii Anticipates Claims 1, 12-15

A. Torii Overview

Torii's first embodiment device includes MISFET 110 for LOP (low operating power), MISFET 120 for LSTP (low stand-by power), and MISFET 130

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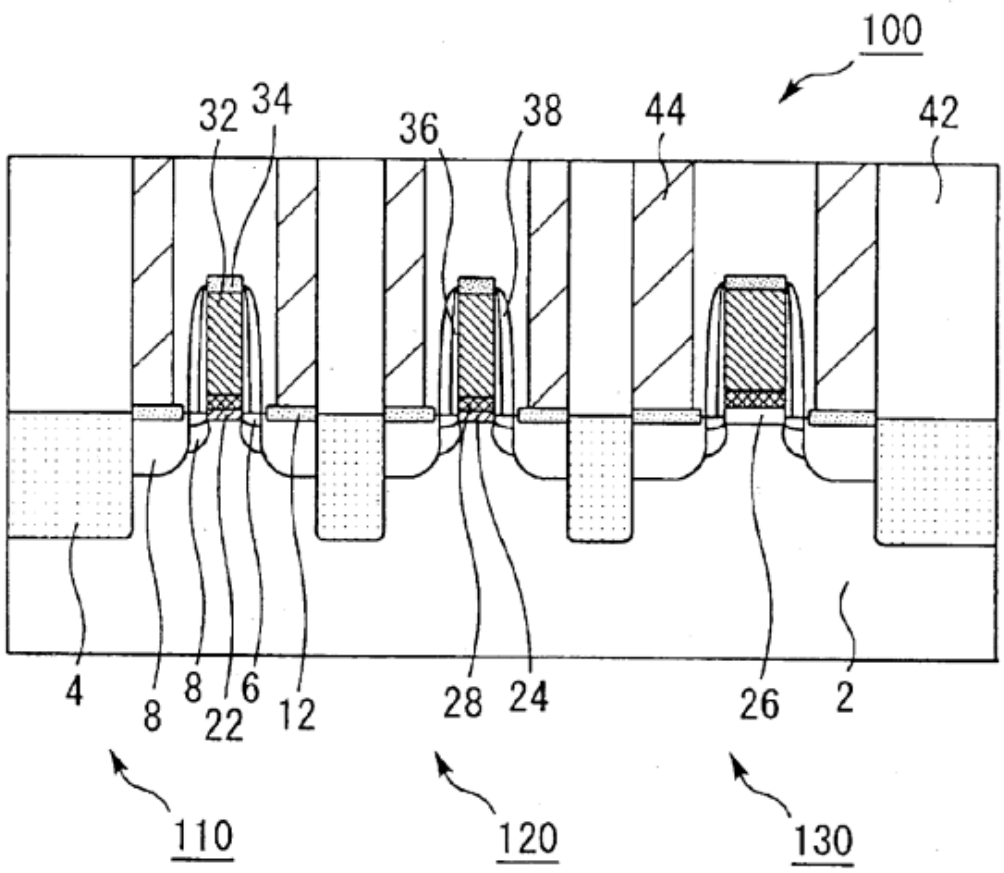
[4] PO's litigation allegations are subject to the district court's protective order. Petitioner reserves the right to seek discovery in the present proceeding should PO take an inconsistent position.

for high withstand voltage. (TSMC-1005, 4:61-5:4, Figure 1(below).) The LOP and LSTP FETs each includes a gate electrode and a "gate insulating film includ[ing] a silicon oxynitride film [22, 24] and a high-dielectric constant film [28]." (TSMC-1005, 3:65-4:4, 5:62-6:1.)



Torii, Figure 1

Torii's device has the same structure as the '779 patent's claim 1, as evidenced by the striking similarity between Torii's claim 1 and '779 patent claims 1 and 13.

Torii – Claim 1	'779 Patent – Claims 1 and 13
1. A semiconductor device comprising; a substrate, **a first field-effect transistor**, including a **first gate insulating film** and **a first gate electrode**, **on the major surface of said substrate**, and	1. A semiconductor device comprising: **a first MIS transistor** and a **second MIS transistor** of an identical conductivity type provided on an **identical semiconductor substrate**, wherein the first MIS transistor includes a **first gate insulating film** formed on a first active region in the semiconductor substrate and a **first gate electrode** formed on the first gate insulating film,
a **second field-effect transistor**, including a **second gate insulating film** and **a second gate electrode**, on the **major surface of said substrate**, wherein	the **second MIS transistor** includes a **second gate insulating film** formed on a second active region in the semiconductor substrate and **a second gate electrode** formed on the second gate insulating film,
each of said first gate insulating film and said second gate insulating film includes a silicon oxynitride film and a **high-dielectric-constant film**,	the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first **high dielectric constant insulating film** formed on the first interface layer, the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second **high dielectric constant insulating film** formed on the second interface layer,
equivalent-oxide thickness of said first gate insulating film is thicker than	the first interface layer has a thickness larger than that of the second interface layer, and

Torii – Claim 1	'779 Patent – Claims 1 and 13
equivalent-oxide thickness of said second gate insulating film, and	
	each of the first interface layer and the second interface layer is made of a silicon dioxide film or a **silicon oxynitride film**.
the high-dielectric-constant film in said first gate insulating film-has the same thickness as the high-dielectric-constant film in said second gate insulating film.	13. The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.

B. Independent Claim 1

1. Preamble [1P]

Torii discloses "*a semiconductor device*[5]" [1P]: "present invention relates to a **semiconductor device** having a plurality of transistors comprising gate insulating films of different film thickness." (TSMC-1005, 1:11-14; *see also,* TSMC-1005, 3:54-60, claim 1 (claiming a "semiconductor device"); TSMC-1003, ¶¶103-105.)

[5] Claim language indicated by italics throughout. A challenged claim listing with labels is provided in the Appendix.

2. Limitations [1A]-[2A]

Torii teaches "[1A] *a first MIS transistor and* [2A] *a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate*." (TSMC-1003, ¶¶107-110.)

Torii's device includes Si substrate 2 ("*semiconductor substrate*") having regions "isolated by STI (shallow trench isolation) 4." (TSMC-1005, 5:1-4; Figure 1 (below).) The "Si substrate 2 is divided into a region for forming **an MISFET**[6] for LOP [low operating power] 110, a region for forming **an MISFET** for LSTP [low stand-by power] 120, and a region for forming an MISFET for high withstand voltage 130." (TSMC-1005, 6:14-18; *see also*, 4:61-67.) The LSTP

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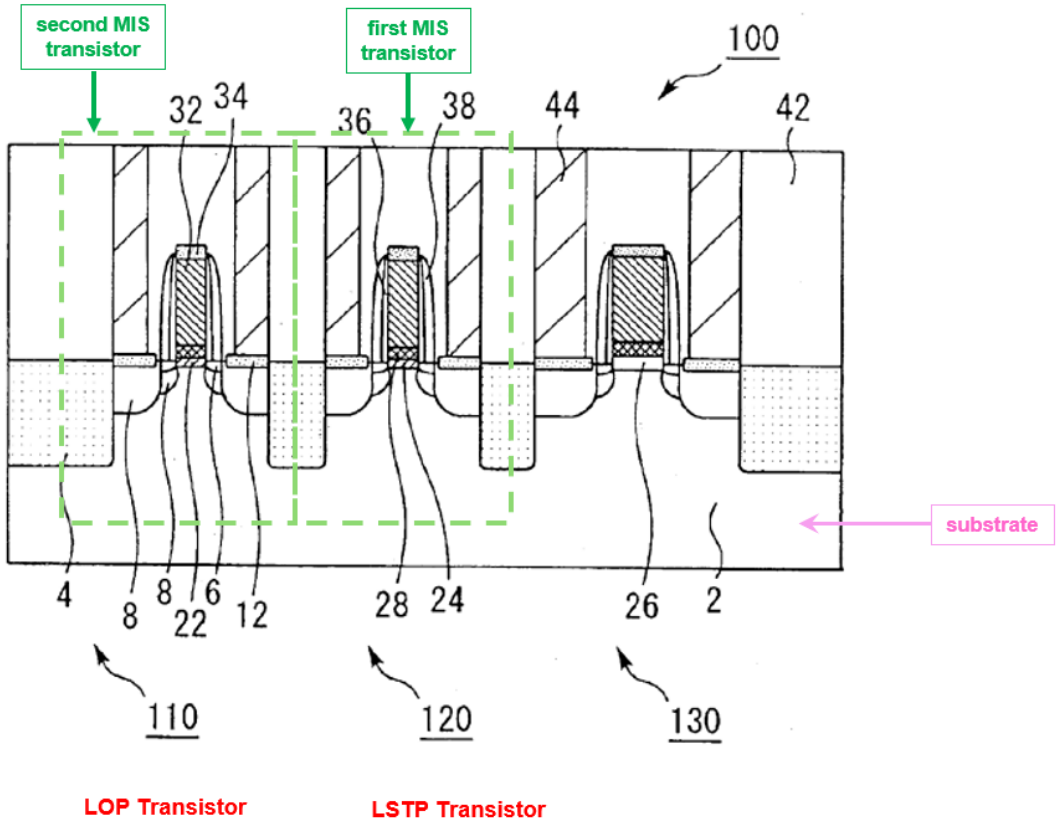
[6] Torii uses a "polycrystalline silicon film" for its gate electrode, which is a conductive, non-metal. (TSMC-1005, 7:6-10.) Torii's usage of "MIS" to refer to its transistors with a conductive gate electrode is consistent with the common convention in the field prior to the '779 patent. (TSMC-1003, ¶107, *citing* TSMC-1012, 8 ("Gates of early transistors were built from metal, so the stack was called metal-oxide-semiconductor, or MOS. Now the gate is typically formed from polycrystalline silicon (*polysilicon*), but the name stuck") (emphasis in original), ¶32; *see also*, TSMC-1007, 2:22-29.) Indeed, the '779 patent's gate electrode also includes "a silicon film 7." (*See, e.g.,* TSMC-1001, 9:1-2.)

transistor is "*a first MIS transistor*" [1A] and the LOP transistor is "*a second MIS transistor*" [2A]. (TSMC-1003, ¶107.) Because the LSTP and LOP transistors are formed on the same substrate, the LOP and LSTP transistors are "*provided on an identical semiconductor substrate.*" (*See* TSMC-1005, 3:62-65 ("[a]ccording to one aspect of the present invention, a semiconductor device comprises a substrate, and a first field-effect transistor and a second field effect transistor **formed on the substrate**"); TSMC-1003, ¶108.)



Torii, Figure 1

Torii teaches the LOP transistor and LSTP transistor are "n-type transistor[s]." (TSMC-1005, 10:39-40.) However, "the present invention may be applied to the case wherein a p-type transistor is formed." (TSMC-1005, 10:40-42.) The LOP and LSTP transistors are therefore "*of an identical conductivity type.*" (TSMC-1003, ¶¶109-110; *see also*, TSMC-1003, ¶¶22-24, 38-41.)

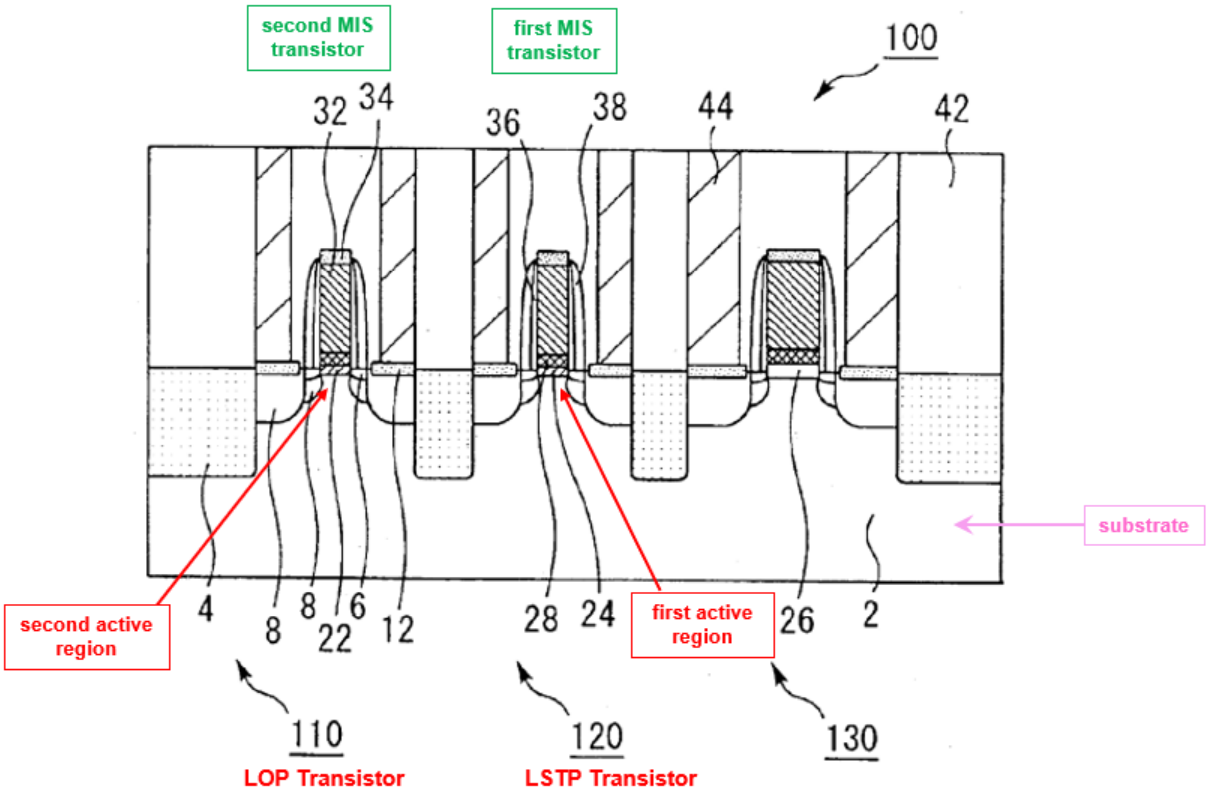
3. Limitations [1A.1]-[1A.2]/[2A.1]-[2A.2]

Torii's LSTP transistor ("*first MIS transistor*") includes "*a first* ***gate insulating film*** *formed on a first active region in the semiconductor substrate and a* ***first gate electrode*** *formed on the first gate insulating film*" [1A.1], "*the first gate insulating film includes a* ***first interface layer*** *being in contact with the semiconductor substrate and a* ***first high dielectric constant insulating film*** *formed on the first interface layer*" [1A.2]. (TSMC-1003, ¶¶112-127.)

Torii's LOP transistor ("*second MIS transistor*") includes "*a second* ***gate insulating film*** *formed on a second active region in the semiconductor substrate and a* ***second gate electrode*** *formed on the second gate insulating film*" [2A.1], "*the second gate insulating film includes a* ***second interface layer*** *being in contact with the semiconductor substrate and a* ***second high dielectric constant insulating film*** *formed on the second interface layer*" [2A.2]. (TSMC-1003, ¶¶112-126, 128.)

a. "Active Region[s] in the Semiconductor Substrate"

The LSTP transistor ("*first MIS transistor*") and LOP transistor ("*second MIS transistor*") each has an "*active region in the semiconductor substrate*" between isolation (STI) structures. (TSMC-1003, ¶¶112-114; TSMC-1005, Figure 1 (below); TSMC-1015, 52-53 (regions between isolation structures "where transistors will be built, are called the 'active' regions of the substrate"); TSMC-1001, 1:67-2:3 (describing "a portion of the semiconductor substrate 100 surrounded by the shallow trench isolation 101 … **serves as an active region 100b**"); §IV.A.)



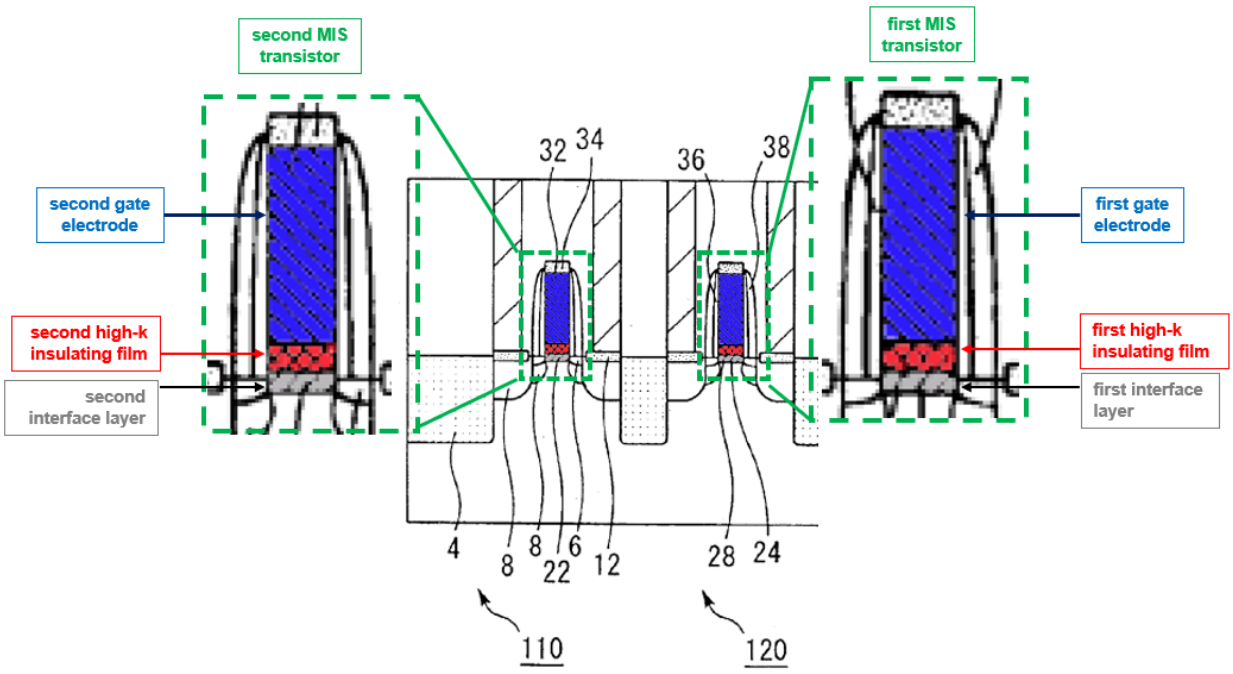
Torii, Figure 1

Torii's fabrication method confirms the presence of an "*active region*" in both the LSTP and LOP transistors. (TSMC-1003, ¶113.) Specifically, after dividing the substrate into regions for forming transistors (TSMC-1005, 6:14-18), "implantation of p-type ions for controlling the impurity content in the substrate, heat treatment the impurity diffusion, ion implantation for controlling the threshold voltage, and heat treatment for activation are performed." (TSMC-1005, 6:24-27.) Further, "[o]n each region of the Si substrate isolated by STI 4", source-drain extension 6, punch-through stopper 8, and source-drain region 10 are formed. (TSMC-1005, 5:5-12.)

b. "Gate Insulating Film"

As shown in the enlargements of the LSTP and LOP transistors in Figure 1 below, the gate stack of Torii's LOP transistor 110 includes silicon oxynitride film 22 (shaded grey) and high-k film 28 (shaded red); the gate stack of LSTP transistor 120 includes silicon oxynitride film 24 (shaded grey) and high-k film 28 (shaded red). (TSMC-1005, 5:14-18, 5:33-36; *see also*, TSMC-1005, 6:66-7:5, 8:14-23.) Torii refers to oxynitride film and high-k film collectively as a "*gate insulating film*." (*See* TSMC-1005, 4:1-4 ("Each of the first gate insulating film and the second gate insulating film includes a silicon oxynitride film and a high-dielectric-constant film"), 8:14-18.) Accordingly, oxynitride film 24 and high-k film 28 in the LSTP transistor are collectively "*a first gate insulating film*" and oxynitride

film 22 and high-k film 28 in the LOP transistor are collectively "*a second gate insulating film*." (TSMC-1003, ¶¶115-117.)

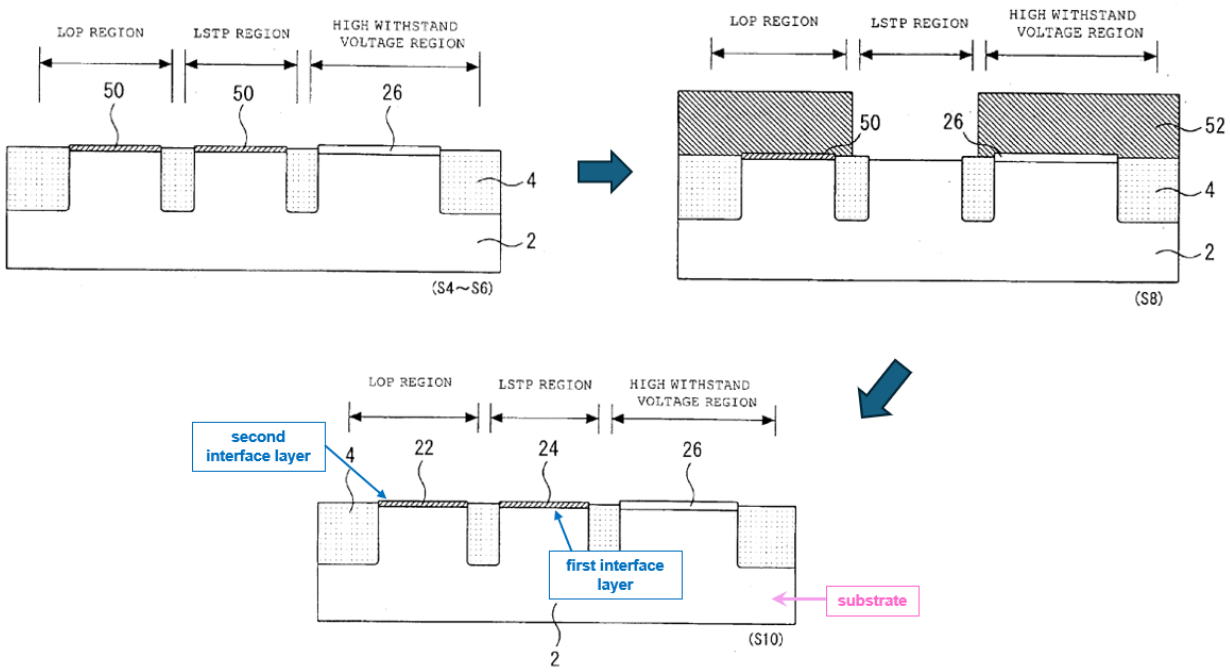


Torii, Excerpt from Figure 1 with enlargements

Silicon oxynitride films 22, 24 are each an "*interface layer.*" (*See* TSMC-1005, 9:32-38 (referring to oxynitride films 22/24 as "interfacial gate insulating films"); TSMC-1003, ¶118.) In Torii's LOP transistor, "silicon oxynitride film 22 [shaded grey] is formed as an **interfacial** gate insulating film in the area sandwiched by source-drain extensions 6 **on the Si substrate 2**." (TSMC-1005, 5:14-17.) In the LSTP transistor, "a silicon oxynitride film 24 [shaded grey] is formed in an equivalent area." (TSMC-1005, 5:17-18, 9:32-38.) Thus, as shown in Figure 1, silicon oxynitride films 24/22 ("*first/second interface layer*") are each "*in*

contact with the semiconductor substrate" [1A.2]/[2A.2] and therefore the "*gate insulating film*" of both the LSTP and LOP transistors is "*formed on a [first/second] active region in the semiconductor substrate*" [1A.1]/[2A.1]. (TSMC-1003, ¶¶118-119.)

Torii's manufacturing method confirms the Figure 1 structure. During manufacture, "silicon nitride film 50 is formed in each of the regions for LOP and LSTP." (TSMC-1005, 6:36-37, Figure 4 (top-left).) After silicon nitride film 50 is removed in the LSTP region (Figure 5, top-right), "heat treatment in a nitrogen monoxide (NO) environment" is performed which forms silicon oxynitride film 24 in the LSTP region (Figure 6, bottom). (TSMC-1005, 6:46-56.) Silicon nitride film 50 in the LOP region "is oxidized to form a silicon oxynitride film 22." (TSMC-1005, 6:57-59.) For both the LOP and LSTP transistors, the silicon oxynitride film ("*interface layer*") of the "*gate insulating film*" is formed on an active region of the substrate. (TSMC-1003, ¶¶119-123.)



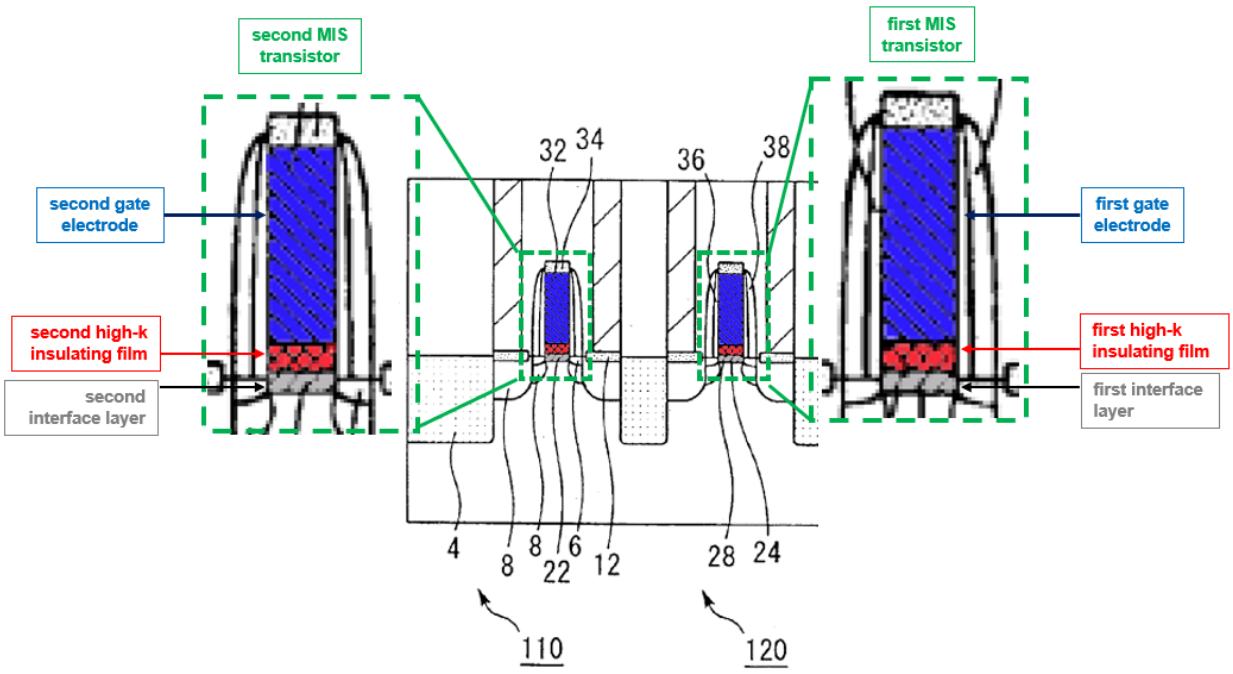
Torii, Figures 4 (top-left), 5 (top-right), 6 (bottom)

On each silicon oxynitride film 24/22, a "**high-k film** [shaded red] such as a hafnia (HfO_2) film 28" is formed. (TSMC-1005, 5:33-36; *see also*, TSMC-1005, 6:66-7:5, 8:14-23, Figure 1.) That is, in the LSTP and LOP transistors, a "[*first*]/[*second*] *high dielectric constant insulating film* [high-k film 28] *is formed on the* [*first*]/[*second*] *interface layer* [oxynitride films 24/22]." (TSMC-1003, ¶¶124-125.)

c. "Gate Electrode"

In Torii, "[o]n each high-k film 28, a **gate electrode** 32 [shaded blue] is formed." (TSMC-1005, 5:42, Figure 1 (below); *see also*, TSMC-1005, 7:6-22.)

Accordingly, each LSTP and LOP transistor includes a "*gate electrode formed on the [first/second] gate insulating film*." (TSMC-1003, ¶126.)



Torii, Excerpt from Figure 1 with enlargements

4. Limitation [1B]

Torii teaches "*the first interface layer has a thickness larger than that of the second interface layer*" [1B]. (TSMC-1003, ¶¶130-132.)

Torii's "relates to a semiconductor device having a plurality of transistors comprising **gate insulating films of different film thicknesses**." (TSMC-1005, 1:11-13; *see also*, TSMC-1005, 4:4-6, claim 1.) Specifically, in the LSTP transistor (the "*first MIS transistor*"), the thickness of silicon oxynitride film 24 ("*first interface layer*") "is about 1.3 nm; and the EOT thereof is about 1.0 nm." (TSMC-1005, 5:23-25.) In the LOP transistor (the "*second MIS transistor*"), the thickness

of silicon oxynitride film 22 ("*second interface layer*") "is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm." (TSMC-1005, 5:20-23.) That is, silicon oxynitride film 24 in the LSTP MISFET is thicker than silicon oxynitride film 22 in the LOP MISFET. (TSMC-1003, ¶¶129-132.)

5. Limitation [1C]

Torii teaches "*each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film*" [1C]. (TSMC-1003, ¶133.) As discussed in §VI.B.3.b, the "*first interface layer*" is silicon oxynitride film 24 and the "*second interface layer*" is silicon oxynitride film 22. (*See also*, TSMC-1005, claim 1, 5:14-18.)

C. Claims 12-13

Torii teaches "*each of the first and second high dielectric constant insulating films contains hafnium or zirconium*" [12]. (TSMC-1003, ¶134.) In Torii, a "high-k film such as a **hafnia (HfO_2)** film 28" is formed on each of silicon oxynitride films 22 and 24. (TSMC-1005, 5:33-36; *see also*, TSMC-1005, 6:66-7:3, 8:14-18; *see also*, TSMC-1005, 10:9-16 (listing alternative high-k materials including **hafnia (HfO_2), hafnium aluminate ($Hf_xAl_{1-x}O_y$)**).)

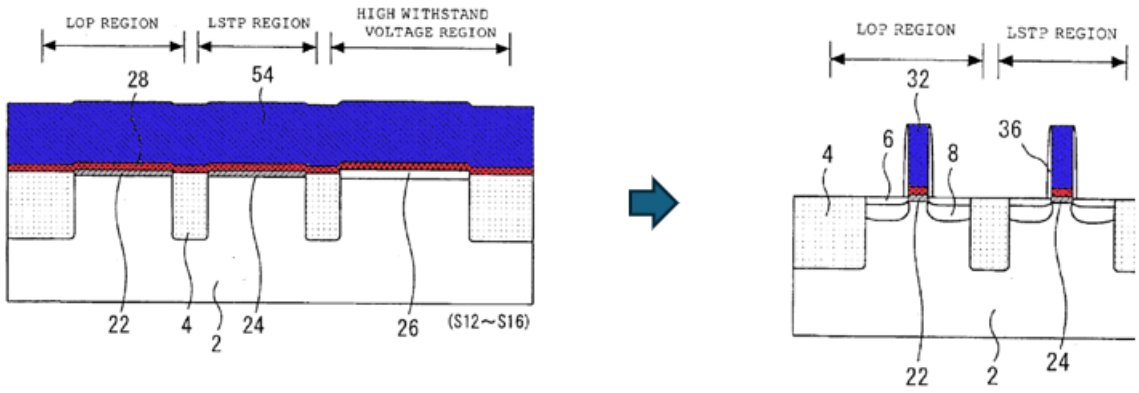
Torii further teaches "*the first and second high dielectric constant insulating films are equal in thickness*" [13]. (TSMC-1003, ¶¶135-137.) In Torii, a high-k film "of a **thickness of about 3.0 nm**" with an EOT "**of about 0.5 nm**" is formed

"[o]n each of the silicon oxynitride films 22 and 24." (TSMC-1005, 5:33-37.) That is, the physical thickness and EOT of the high-k film in both the LOP and LSTP transistors is equal. (TSMC-1003, ¶¶135-137; *see also*, TSMC-1005, 4:6-9 ("high-dielectric-constant film in the first gate insulating film has the **same thickness** as the high-dielectric-constant film in the second gate insulating film"), 6:66-7:3, claim 1.)

D. Claim 14

Torii teaches "*the first and second gate electrodes are made of an identical material*" [14]. (TSMC-1003, ¶138.)

To form Torii's gate electrodes in the LSTP and LOP transistors, "polycrystalline silicon film 54 is formed on the high-k film." (TSMC-1005, 6:66-7:7, Figure 7 (below-left).) A "resist mask of a width of the gate electrode is formed on the polycrystalline silicon film 54 … and etching is performed using the resist mask to process the polycrystalline silicon film 54 and the high-k film 28 to have the width of the gate electrode 32." (TSMC-1005, 7:13-19.) "Thereby, a **gate electrode 32** and a gate insulating film are **formed in each of the regions for LOP, LSTP**, and high withstand voltage." (TSMC-1005, 7:20-22, Figure 8 (below-right).)



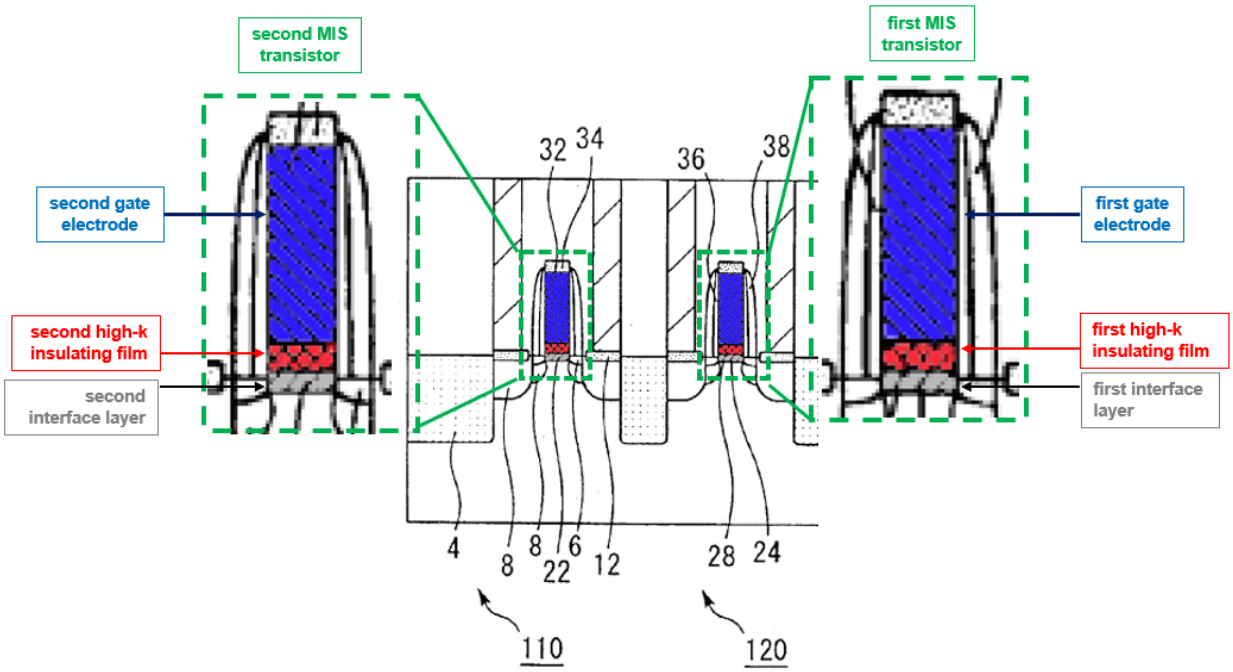
Torii, Figure 7 (left), Excerpt of Figure 8 (right)

Because the gate electrodes of both the LSTP and LOP transistors are formed from the same polycrystalline silicon film layer, "*the first and second gate electrodes are made of an identical material*" [14]. (TSMC-1003, ¶138; *see also*, §VI.B.3.c (discussing gate electrode).)

E. Claim 15

Torii discloses "*the effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor*." (TSMC-1003, ¶¶139-144.)

Torii's device includes an LSTP transistor ("*first MIS transistor*") with a gate insulating film comprising silicon oxynitride film 24 and high-k film 28 and an LOP transistor ("*second MIS transistor*") with a gate insulating film comprising silicon oxynitride film 22 and high-k film 28. (TSMC-1005, 5:14-17, 5:33-36, 6:55-7:5; Figure 1 (below).)



Torii, Excerpt from Figure 1 with enlargements

The '779 patent relates a transistor's "effective work function" to the transistor's EOT. Specifically, the '779 patent states "since an EOT of the gate insulating film of the first MIS transistor increases, an effective work function of the first MIS transistor increases." (TSMC-1001, 4:29-31, 13:23-27 ("Accordingly, the EOT of the gate insulating film 52a of the first pMIS transistor and that of the gate insulating film 52c of the first nMIS transistor increase, **thereby causing** the effective work functions of the first pMIS transistor and the first nMIS transistor to increase").)

Torii teaches the high-k film of both the LSTP and LOP transistors is formed in the same process step and therefore has the same thickness and is formed of the

same material (i.e., same dielectric constant). (TSMC-1005, 6:66-7:3.) Accordingly, the contribution of the high-k film to the EOT of both transistors is the same, "about 0.5 nm" as taught by Torii. (TSMC-1005, 5:36-37; TSMC-1003, ¶141; *See* §VI.C.)

As discussed in §VI.D, the gate electrodes of the LSTP and LOP transistors are the same. When comparing the two transistors' EOT as shown in the below equation, the high-k contributions effectively cancel one another (and are therefore greyed out). (TSMC-1003, ¶¶140-141.)

EOT (LSTP) **EOT (LOP)**

$$\left(\frac{t_{28}}{\varepsilon_{28}}\right)\varepsilon_{SiO_2} + \left(\frac{t_{24}}{\varepsilon_{24}}\right)\varepsilon_{SiO_2}\,[1.0\text{ nm}] \;>\; \left(\frac{t_{28}}{\varepsilon_{28}}\right)\varepsilon_{SiO_2} + \left(\frac{t_{22}}{\varepsilon_{22}}\right)\varepsilon_{SiO_2}[0.7\text{ nm}]$$

Torii teaches the contribution of the silicon oxynitride film 24 to the LSTP transistor's EOT is greater than contribution of the silicon oxynitride film 22 to the LOP transistor's EOT: "thickness of the silicon oxynitride film 24 ["*first interface layer*"] … is about 1.3 nm; and the EOT [equivalent oxide thickness] thereof is about 1.0 nm" (TSMC-1005, 5:23-25.) and "the thickness of the silicon oxynitride film 22 ["*second interface layer*"] … is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm." (TSMC-1005, 5:20-23.)

Accordingly, because the LSTP transistor ("*first MIS transistor*") has a greater EOT than the LOP transistor ("*second MIS transistor*"), the "*effective work*

function of the" LSTP transistor ("*first MIS transistor*") "*is higher than an effective work function of the*" LOP transistor ("*second MIS transistor*"), according to the disclosure of the '779 patent. (TSMC-1003, ¶¶139-144.)

VII. GROUND 2: Combination of Torii and Mise Renders Claims 8-11 Obvious.

Torii discloses the "*first and second MIS transistors*" of its semiconductor device are "*pMIS transistors*" [8A] or alternatively "*nMIS transistors*" [10A]. (§VI.B.2; TSMC-1005, 10:39-42.) Torii however does not explicitly disclose that when "*the first and second MIS transistors are pMIS transistors*" [8A], "*the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing aluminum, and the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing aluminum*" [9] or when "*the first and second MIS transistors are nMIS transistors*" [10A], "*the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing lanthanum, and the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing lanthanum*" [11]. Mise provides these teachings.

A. Combination Overview

1. Mise

Mise describes a CMOS device having "an n-type MOSFET 101 and a p-type MOSFET 102[7]." (TSMC-1006, ¶69, Figure 1(k) (below).) The n-type MOSFET includes gate stack 10 having gate insulation layer 11 "composed of a high-k material such as HfLaO or HfMgO", cap layer 12 "composed of MgO or LaO", and gate metal layers 13 and 14. (TSMC-1006, ¶71.) The p-type MOSFET includes gate stack 20 having gate insulation layer 21 "composed of a high-k material such as HfAlO", cap layer 22 "composed of AlO", and gate metal layers 23 and 24. (TSMC-1006, ¶72.) Mise discloses gate metal layers 13 and 23 are "composed of a mid-gap material … such as TiN, TaN, TaSiN, NiSi, PtS, or $CoSi_2$" and gate metal layers 14 and 24 are "made of a low resistance material such as W." (TSMC-1006, ¶71, ¶72 ("gate metal layers 23 and 24 are composed of the same materials as those of the gate metal layers 13 and 14").)

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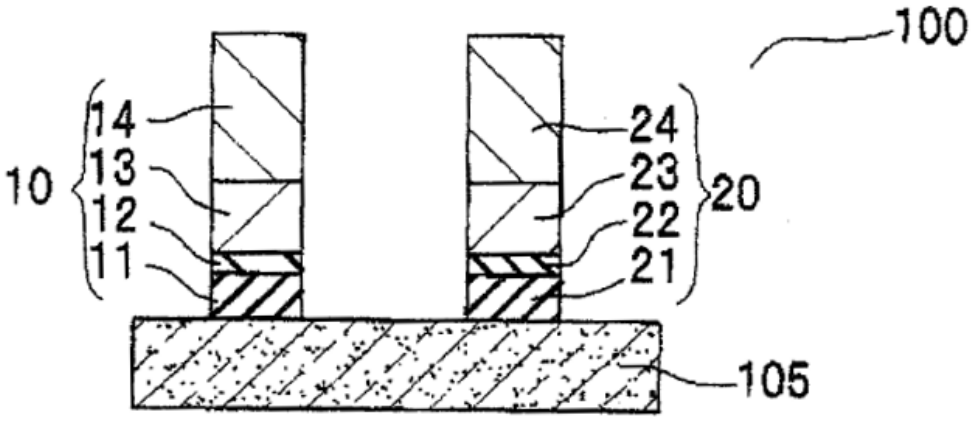
[7] Mise's specification contains a typographical error, stating p-type MOSFET 102 has p-type well region 120 and n-type MOSFET 101 has n-type well region 110. (TSMC-1006, ¶70.) A POSITA would have understood the p-type MOSFET has an n-type well and the n-type MOSFET has a p-type well. (TSMC-1003, ¶149, *citing* TSMC-1017, 8-9.)



Mise, Figure 1(k)

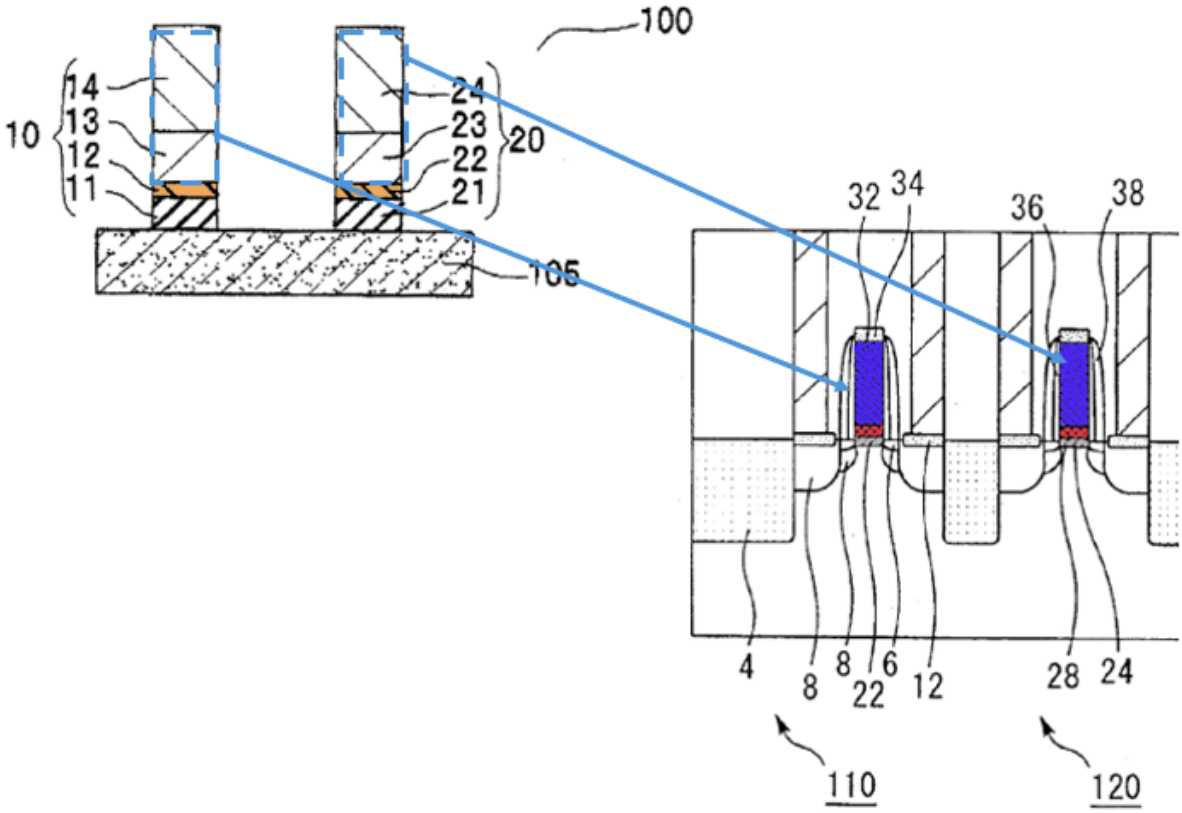
2. Motivation to Combine

Both Torii and Mise are in the same field as the '779 patent—"semiconductor devices and methods for fabricating the same." (TSMC-1001, 1:15-16; TSMC-1005, 1:9-10; TSMC-1006, ¶1.) A POSITA would have motivated to make at least the following two combinations of Mise's teachings with Torii.

a. Combining Mise's teaching of a two-layer metal gate electrode with Torii.

A POSITA would have been motivated to integrate Mise's teaching of using a two-layer metal gate electrode in Torii's transistors, as illustrated below. (TSMC-

1003, ¶¶153-155.)



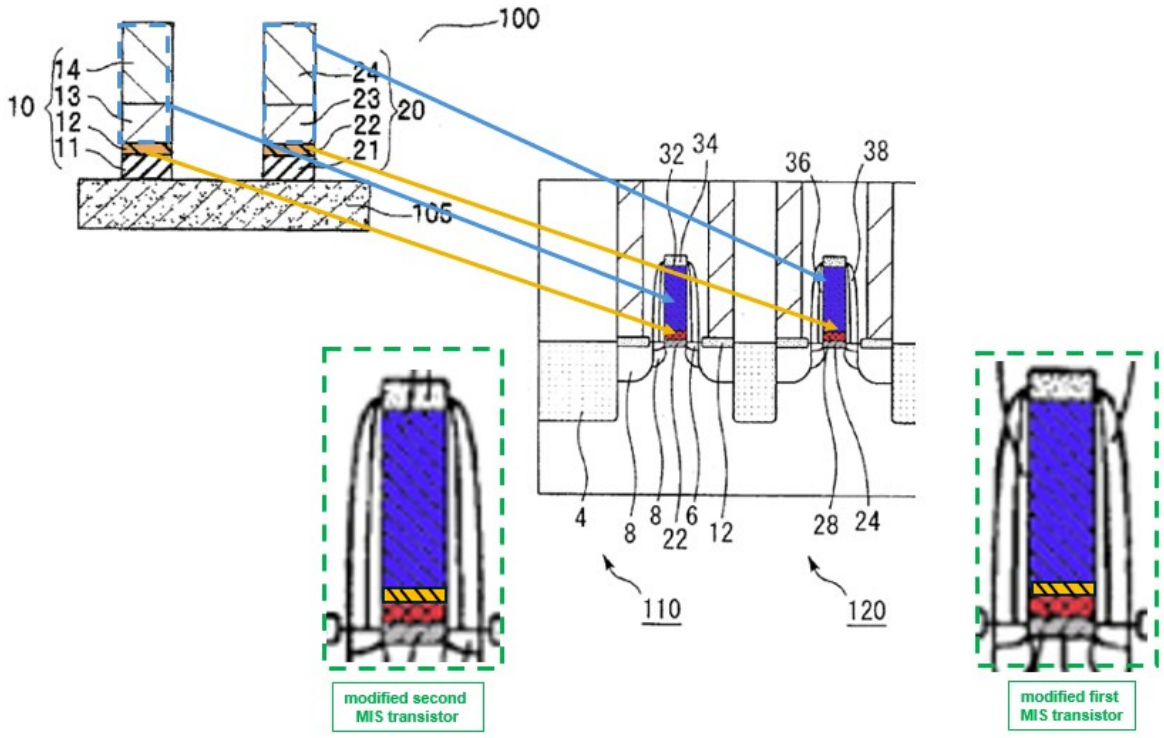
Mise, Figure 1 (left); Torii, Figure 1 (right)

Torii's LSTP and LOP transistors include a "*gate insulating film*" having a high-k film and a polysilicon "*gate electrode*" on the high-k film. (*See* TSMC-1005, 5:33-36, 5:42, 6:66-7:15; §VI.B.3.) A POSITA would have been motivated to make the above combination because the challenges with using high-k dielectrics with polysilicon ("polySi") gates were known prior to the '779 patent. (TSMC-1003, ¶154.) For example, due to Fermi level pinning at the interface between high-k dielectrics and polySi, the threshold voltage shifts. (TSMC-1006, ¶23; TSMC-1018, 1.) PolySi/high-k transistors also exhibit lower channel

mobility. (*See* TSMC-1018, 1.) A POSITA would have understood that metal gates are more effective with high-k gate dielectrics but require additional adjustment to achieve an optimal threshold voltage which, as discussed below, is a motivation to use a cap layer. (*See* TSMC-1018, 1; TSMC-1003, ¶¶154-155.) A POSITA would have therefore been motivated to improve Torii's device using the metal gate electrodes discussed by Mise to avoid Fermi level pinning and improve channel mobility. (TSMC-1003, ¶¶153-155.)

b. Combining Mise's teaching of a cap layer with Torii.

A POSITA would also have been motivated to integrate a cap layer over the high-k dielectric as taught by Mise in Torii's gate stack in addition to using Mise's gate electrode, as illustrated in the figure below. (TSMC-1003, ¶¶156-162.) Specifically, a POSITA would have been motivated to include an Al containing cap layer in Torii's p-type MISFETs and a La containing cap layer in Torii's n-type MISFETs. (TSMC-1003, ¶156.)



Mise, Figure 1 (top-left); Torii, Figure 1 (top-right)
enlargements showing transistors of combination of Torii and Mise

A POSITA would have been motivated to make the above combination to improve transistor operation. (TSMC-1003, ¶¶157-162.) A POSITA would have understood a cap layer helps reduce defects that negatively impact electrical performance when metal gate electrodes are used. (TSMC-1003, ¶157; *see also*, TSMC-1009, 5:25-31, 5:38-39 ("Metal gate electrodes may also benefit from use of a capping layer over the bulk dielectric material [i.e., gate dielectric]").) For example, use of a cap layer helps reduce leakage current by misaligning "the grain boundaries within the layers." (*See* TSMC-1009, 5:21-24.) A POSITA would have also understood the cap layer improves the interface between the gate electrode

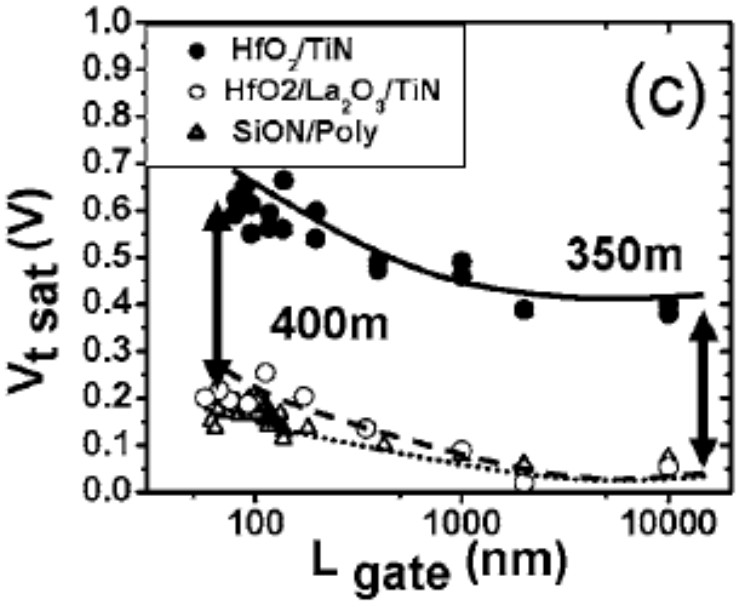
and gate insulating film, alleviating compatibility issues. (TSMC-1003, ¶157; *see* TSMC-1009, 5:25-35.) A POSITA would have also understood the cap layer permits the threshold voltage of the transistor to be adjusted. (TSMC-1003, ¶¶158-162.) Indeed, Mise discloses use of an AlO/LaO cap layer for the pMOS/nMOS transistors respectively to adjust the threshold voltage, as discussed further below. (*See, e.g.,* TSMC-1006, ¶¶154, 183-193, 195.)

A POSITA would have been motivated to use a cap film containing aluminum as taught by Mise with Torii's pMIS transistors. (TSMC-1003, ¶158.) Mise's gate electrode includes a gate metal layer 13/23 composed of a mid-gap material. (TSMC-1006, ¶¶71-72*,* TSMC-1019, 1.) A POSITA would have understood use of aluminum in the cap layer lowers the threshold voltage, making it ideal for pMOS devices. (*See* TSMC-1006, ¶¶154, 183-193, 195, Figure 11; TSMC-1020, 441-444; *see also,* TSMC-1021, 12:8-23; TSMC-1003, ¶158.)

A POSITA would have been motivated to use a cap film containing lanthanum as taught by Mise with Torii's nMIS transistors. (TSMC-1003, ¶¶159-162.) Mise's gate electrode includes a gate metal layer 13/23 "composed of a mid-gap material" which is too high for an nMIS transistor. (*See* TSMC-1006, ¶¶71-72, Figure 11; TSMC-1019, 1 (noting the "resulting threshold voltages" for a HfO_2 dielectric and TiN electrode "are unacceptably high and an additional threshold adjustment technique is needed to produce devices suitable for high performance

logic applications").) A POSITA would have therefore been motivated to form the cap layer in the combination of Torii and Mise using lanthanum to adjust the threshold voltage to a value suitable for nMIS devices. (TSMC-1003, ¶159, *citing* TSMC-1019, 1 ("We have recently solved this problem and shown that be introducing ultrathin La_2O_3 cap layers between the HfO_2 dielectric and TiN electrode, the threshold voltage can be controllably shifted to a position ideal for nMOSFETs").)

The following figure from Guha (TSMC-1019) highlights this motivation. For example, Guha explains a TiN gate electrode layer by itself on a high-k dielectric (i.e., without an intervening cap layer) results in a threshold voltage of 0.6V at 100 nm gate length. (*See,* TSMC-1019, 2.) A POSITA would have understood this threshold voltage is too high for an nMIS device. (TSMC-1003, ¶160.) The traditional nMOS device with SiON and poly-silicon gate is shown in the bottom curve. As shown, a lanthanum containing cap layer (HfO_2-La_2O_3-TiN) shifts the threshold voltage closer to that of traditional device.



* * *

Adding cap layers and using metal gate layers in Torii's transistors would be nothing more than using a known technique (e.g., incorporating cap layers between the high-k dielectric and the gate electrode material and using metal gate layers according to Mise's teachings) to improve similar devices in the same way for the above reasons. (TSMC-1003, ¶¶155, 162.) A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Mise forms the cap layers and metal gate layers through conventional, well-known processes. (*Id*.) For example, Mise describes that its cap layers are "made by the ALD method, the MOCVD method, the sputtering method, or the like" and its metal layers are formed "by the sputtering method." (TSMC-1006, ¶¶80, 85, 94.) A POSITA would have known these were conventional and

well known deposition methods in semiconductor fabrication prior to the '779 patent. (TSMC-1003, ¶¶155, 162.) Further, high-k metal gate devices were known before the '779 patent. (*See, e.g.,* TSMC-1013, Figure 5.1.18; TSMC-1009, 4:38-40 (indicating either a metal or polysilicon gate can be used with a high-k dielectric).)

B. PMIS Claims 8-9

Torii teaches the "*first and second MIS transistors are pMIS transistors*" [8A]: "the present invention may be applied to the case wherein a p-type transistor is formed." (TSMC-1005, 10:40-42; TSMC-1003, ¶163; §VI.B.2.)

The combination of Torii and Mise uses a cap layer containing aluminum on the high-k insulating film in Torii's LSTP and LOP pMIS transistors, as taught by Mise. (§VII.A.2; TSMC-1006, ¶72 (cap layer 22 of pMOS transistor "is composed of AlO").) Thus, the combination provides "*the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing aluminum*" [9A] and "*the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing aluminum*" [9B]. (TSMC-1003, ¶164.)

Torii teaches the material for the high-k gate insulating film in its transistors includes hafnium aluminate ($Hf_xAl_{1-x}O_y$) and alumina (Al_2O_3). (TSMC-1005, 10:8-16.) Mise similarly teaches the pMOS transistor's gate insulating film "is

composed of a high-k material such as **HfAlO**." (TSMC-1006, ¶72.) A POSITA would have understood the high-k gate insulating material in the combination contains aluminum, as taught by Torii and Mise, at least as a result of diffusion during later thermal processing of Torii (e.g., source-drain activation, silicidation). (*See, e.g.,* TSMC-1005, 7:54-58, 7:63-66; TSMC-1003, ¶166; TSMC-1021, 11:1-26 (describing Al diffusion through the gate insulating stack); TSMC-1022, ¶19 (mentioning diffusion of metal atoms across the gate stack).) Thus, in the combination of Torii and Mise, the "*high dielectric constant insulating films*" of both the LSTP and LOP transistors "*contain aluminum*" [8B]. (TSMC-1003, ¶¶165-168.)

C. NMIS Claims 10-11

Torii teaches the "*first and second MIS transistors are nMIS transistors*" [10A]: LOP transistor and LSTP transistor are "n-type transistor[s]." (TSMC-1005, 10:39-40; TSMC-1003, ¶169; §VI.B.2.)

The combination of Torii and Mise uses a cap layer containing lanthanum on the high-k insulating film in Torii's LSTP and LOP nMIS transistors, as taught by Mise. (§VII.A.2; TSMC-1006, ¶71 (cap layer 22 of nMOS transistor "is composed of MgO or LaO").) Thus, in the combination of Torii and Mise, "*the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing lanthanum*" [11A] and "*the second gate*

insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing lanthanum" [11B]. (TSMC-1003, ¶170.)

Torii teaches the high-k insulating film in its transistors include lanthanum oxide. (TSMC-1005, 10:8-16.) Mise similarly teaches the gate insulation film of its nMOS transistor "is composed of a high-k material such as **HfLaO** or HfMgO." (TSMC-1006, ¶71.) A POSITA would have also understood the high-k material in the combination contains lanthanum, as taught by Torii and Mise, at least because of diffusion as a result of thermal processing as discussed in §VII.B. (*See, e.g.,* TSMC-1005, 7:54-58 (describing heat treatment to activate source/drain), 7:63-66 (describing heat treatment for silicidation); TSMC-1003, ¶166; TSMC-1022, ¶19 (discussing diffusion of metal atoms across the gate stack).) Thus, in the combination of Torii and Mise, the "*high dielectric constant insulating films*" of both the LSTP and LOP transistors "*contain lanthanum*" [10B]. (TSMC-1003, ¶¶171-172.)

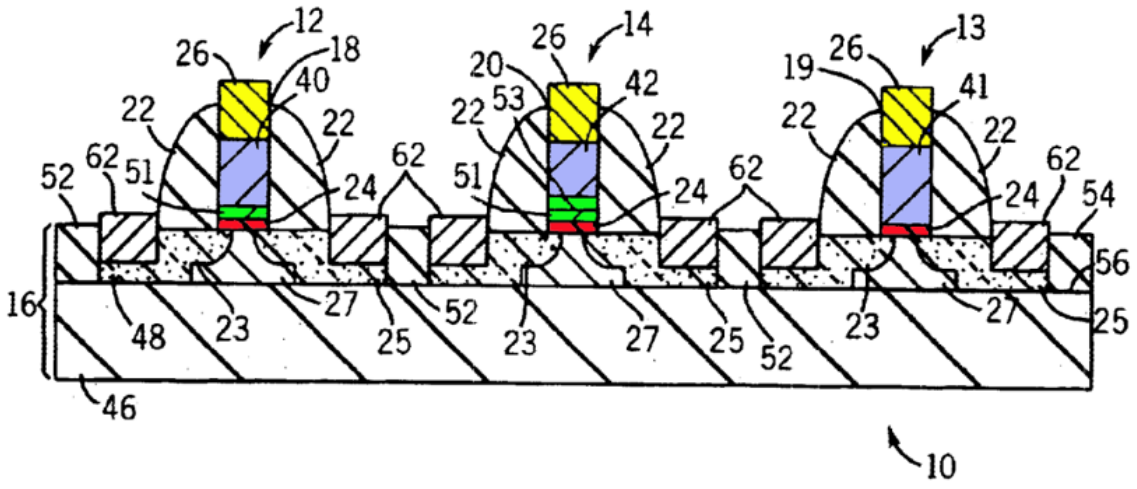
VIII. GROUND 3: Combination of Torii and Yu Renders Claim 15 Obvious.

Torii anticipates claim 15 based on the '779 patent's disclosure. (§VI.E.) Torii does not disclose modifying the work function of a metal gate electrode to adjust the effective work function (and threshold voltage) of a transistor under PO's litigation allegations. (*See* §V.) However, Yu discloses varying the metal gate

work function of transistors having the same conductivity type formed on the same substrate.

A. Yu Overview

Yu generally relates "to an integrated circuit (IC) and the fabrication of an integrated circuit" which is a semiconductor device and is therefore in the same field as Torii and the '779 patent. (TSMC-1008, 1:27-28; *see also* TSMC-1001, 1:15-16; TSMC-1005, 1:9-10.) Yu specifically "relates to an integrated circuit with transistors having multiple threshold voltage values." (TSMC-1008, 1:28-31.) Yu's integrated circuit includes transistors 12, 13, and 14 having "a threshold voltage between 0.15V and 0.4V or less." (TSMC-1008, 5:16-17, Figure 1 (below).) Each transistor is "disposed on a substrate 16" separated by isolation structures 52. (TSMC-1008 5:9-11, 6:56-63.) Although Yu teaches substrate 16 "provides an SOI substrate," Yu discloses transistors 12, 13, and 14 could "utilize the principles of the present invention on a bulk-type substrate." (TSMC-1008, 6:65-67.)



Yu, Figure 1

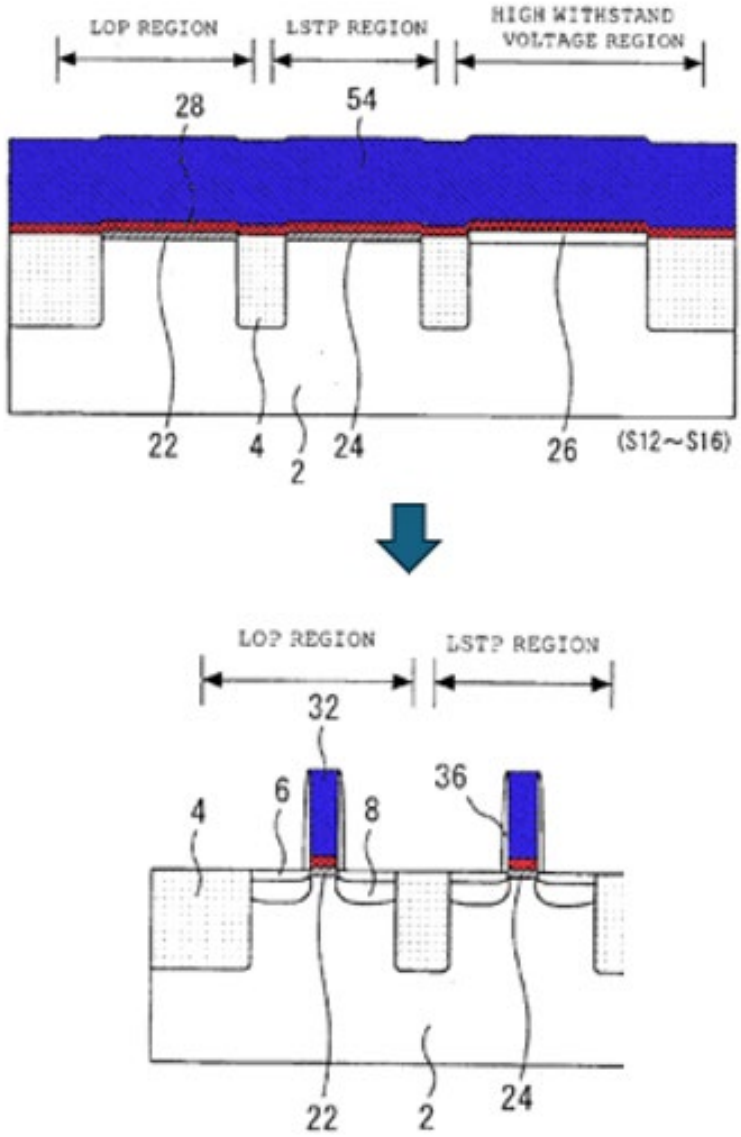
Gate stacks 18, 19, and 20 include gate dielectric 24 (shaded red) and doped polysilicon gate conductor 40, 41, and 42 (shaded blue). (TSMC-1008, 5:30-34.) The threshold voltages of transistors 12 and 14 are adjusted by inserting metal layer 51 (shaded green) in gate stack 18 and metal layers 51 and 53 (shaded green) in gate stack 20. (TSMC-1008, 5:51-53.)

B. Claim 15

The combination of Torii and Yu discloses or suggests "*an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor*" under PO's litigation allegations. (TSMC-1003, ¶¶173-203; §V.)

Torii discloses a semiconductor device composed of LOP, LSTP, and high withstand voltage transistors. As discussed in §VI.B.3.c, to form the gate

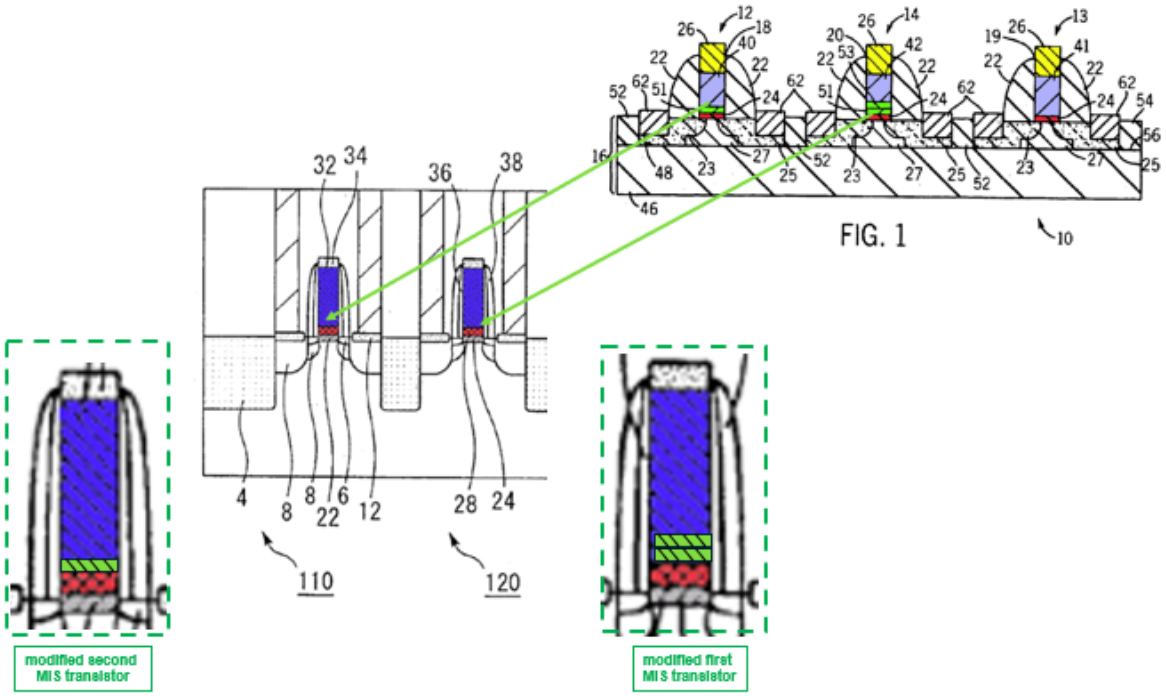
electrodes of Torii's transistors, non-doped polycrystalline silicon film 54, "a material film for gate electrodes", "is formed on the high-k film 28", as shown in Figure 7 (top). (TSMC-1005, 7:6-9.) "Thereafter, impurity ions for the gate electrodes are implanted into the non-doped polycrystalline silicon film 54." (TSMC-1005, 7:10-12.) Polycrystalline silicon film 54 is then "processed for a gate electrode 32 of each region", illustrated in the excerpt from Figure 8 (bottom). (TSMC-1005, 7:13-15.)



Torii, Figure 7 (top),
Excerpt from Figure 8 (bottom)

A POSITA would have been motivated to combine Yu's teachings regarding inserting metal layers into the LOP and LSTP nMIS transistors of Torii to vary the work functions of the gate electrode and hence the threshold voltages of the LOP and LSTP nMIS transistors. (TSMC-1003, ¶194; TSMC-1005, 10:39-40;

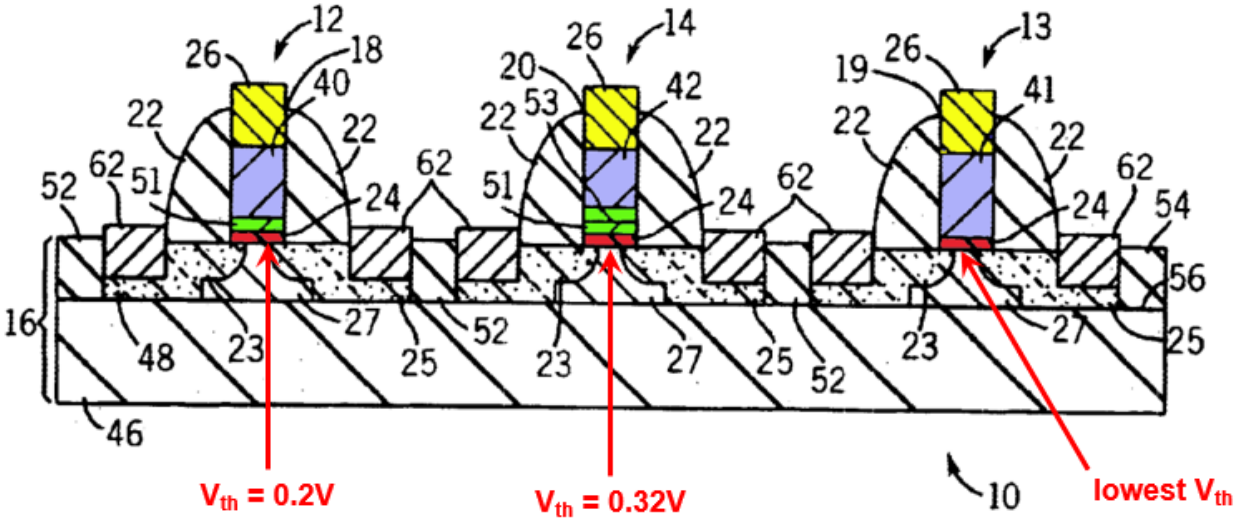
§§VI.B.2.) Because both Torii and Yu's gate electrode use polysilicon, a POSITA would have understood that Yu's process steps associated with forming the metal layers by masking and metal layer deposition can be used with Torii's fabrication process. (TSMC-1003, ¶194) Specifically, as illustrated below, a POSITA would have been motivated to insert a metal layer into the LOP transistor ("*second MIS transistor*") and first and second metal layers into the LSTP transistor ("*first MIS transistor*"), as taught by Yu using a similar process as Yu. (*Id*.)



Torii, Modified Figure 1 (left); Yu, Figure 1 (right)

In Yu, the thickness and types of materials for layers 51 and 53 used in the gate stacks "can be controlled to control the adjustment to the work function, thereby selecting threshold voltage." (TSMC-1008, 6:1-3.) Yu teaches that "[i]f

transistors 12 and 14 are N-channel transistors, transistor 12 has a lower threshold voltage than transistor 14." (INTEL-1008, 6:26-31.) For example, if transistors are nMOS transistors, transistor 12 "has a threshold voltage of approximately 0.2V" and transistor 14 "has a threshold voltage of approximately 0.32V." (TSMC-1008, 6:36-38.) Transistor 13 "has the lowest threshold voltage." (TSMC-1008, 6:34-35.) That is, for nMOS transistors, the transistor with two metal layers has higher threshold voltage than the transistor with one metal layer which has a higher threshold voltage than the transistor without a metal layer. (TSMC-1003, ¶195.)



Yu, Figure 1

Thus, in the combination of Torii and Yu, the LSTP nMIS transistor (with two added metal layers) has a higher threshold voltage than the LOP nMIS transistor (with one added metal layer), as taught by Yu, consistent with Torii's disclosure that the LSTP has a higher threshold voltage than LOP transistor.

Based on this disclosure, the combination of Torii and Yu also discloses or suggests claim 15 under PO's litigation allegations. PO alleges in the co-pending district court litigation a transistor with an additional metal layer in its gate electrode would demonstrate a slightly higher effective work function than another MIS transistor missing this layer because the additional layer allegedly possesses a higher effective work function. The combination of Torii and Yu teaches addition of a metal layer with a higher work function into the gate stack of the LSTP transistor ("*first*" MIS transistor).

In the combination of Torii and Yu, the LSTP nMIS transistor has two metal layers 51 and 53 and the LOP nMIS transistor has a single metal layer 51. In Yu, layers 51 and 53 "can be nickel or titanium layers formed on top of each other or on top of gate dielectric 24." (TSMC-1008, 5:56-58; *see also*, TSMC-1008, 7:22-30.) Yu stresses the second metal layer (layer 53) "preferably has a different work function associated with it than" the first layer. (TSMC-1008, 7:63-67.) Accordingly, Yu teaches two options for the LSTP gate stack: Ti (layer 51)-Ni (layer 53) or Ni (layer 51)-Ti (layer 53). Each ordering would have been obvious to try because only two alternatives exist. *See KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 421 (2007). A POSITA would have had a reasonable expectation of success in pursuing both ordering alternatives. (TSMC-1003, ¶198.) Indeed, the order of depositing Ti and Ni layers is "the product **not of innovation** but of ordinary skill

and **common sense**." *See Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1331 (Fed. Cir. 2004), *quoting KSR,* 550 U.S. at 421.

A POSITA would have understood that Ti is a low work function metal (Φ_m ~ 4eV) and Ni is a high work function metal (Φ_m ~ 5eV). (*See* TSMC-1033[8], 200.) Thus, when layer 51 is Ti (Φ_m ~ 4eV) and layer 53 is Ni (Φ_m ~ 5eV), the additional layer 53 in the LSTP transistor has a higher work function than layer 51, the only layer present in the LOP transistor. According to PO's litigation allegations, the LSTP transistor (having both Ti (layer 51) and Ni (layer 53)) will exhibit a higher effective work function than the LOP transistor (having only the Ti layer (layer 51)). (TSMC-1003, ¶199.)

The combination of Torii and Yu therefore discloses or suggests "*an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor*" under PO's litigation allegations.

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[8] Polishchuk expresses the work function of Ti and Ni in volts (V) rather than the customary energy units of electron volts (eV). (TSMC-1003, ¶199.) Because an eV is defined as the product of voltage (V) and the elementary charge (e), a POSITA would recognize 1eV is equivalent to 1V × e, or that 1V produces 1eV of energy for a single electron (e). (*Id.*) That is, in this context, V and eV are interchangeable. (*Id.*)

A POSITA would have been motivated to make the above combination for numerous reasons. (TSMC-1003, ¶¶200-203.) Torii suggests, and a POSITA would have known, that LOP and LSTP nMIS transistors require different threshold voltages. (TSMC-1005, 2:51-54, 3:2-10; TSMC-1016, 11, 17, 21; TSMC-1003, ¶200.). A POSITA would have been motivated to combine Torii and Yu to fine tune the gate effective work functions of the LOP and LSTP transistors by adding metal layers so that their threshold voltages can be set to the desired values without having to rely on gate dielectric thickness engineering and channel and gate electrode doping engineering, which can be burdensome and fabrication intensive. (TSMC-1003, ¶¶200-201.) Yu confirms this motivation, explaining that "[u]tilizing channel implants to adjust the threshold voltages of transistors can be problematic because transistor short-channel performance is very susceptible to process variations" which "is particularly problematic as transistors become smaller and packing densities increase." (TSMC-1008, 3:27-37.) Accordingly, a POSITA would have been motivated to modify the metal work function to fine tune the threshold voltages of Torii's nMIS transistors. (TSMC-1003, ¶¶200-201.)

A POSITA would have been further motivated to apply Yu's teaching in Torri to address the challenges with using high-k dielectrics with polysilicon gates, as discussed in §VII.A.2 in the combination of Torii and Mise. (TSMC-1003, ¶202.) For example, the metal layers in Yu shield Torii's polysilicon gate electrode

from Fermi level pinning by spatially moving the polysilicon gate away from the high-k dielectric. (*Id.*)

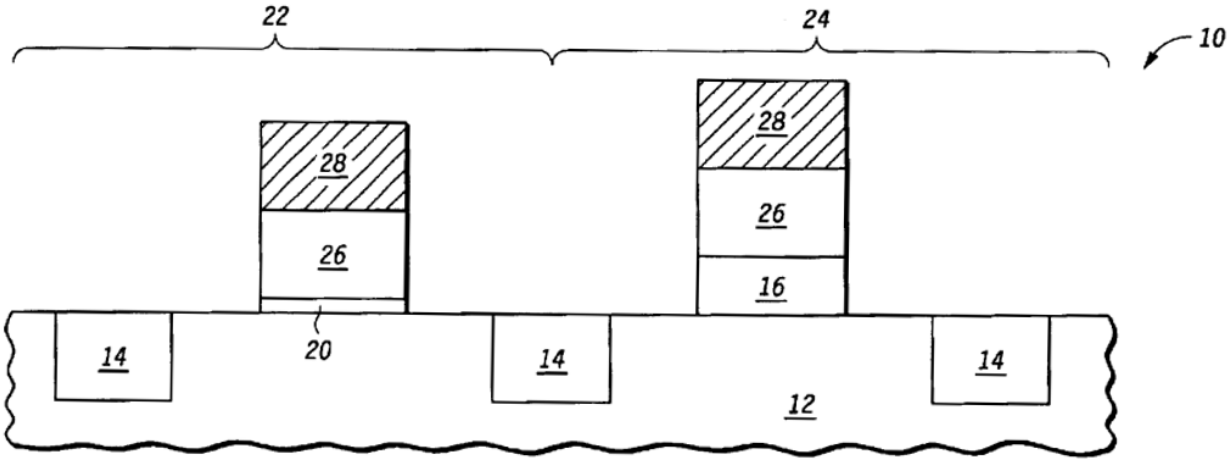
Finally, the combination is merely the application of a known technique (inserting one or more metal layers into the gate stack and adjusting the thicknesses and types of materials of those meta layers) to a known device (Torii's semiconductor device) ready for improvement for the above reasons. (TSMC-1003, ¶203.) Yu's gate electrode uses polysilicon, like Torii's gate electrode. (TSMC-1005, 7:13-19; TSMC-1008, 5:30-34.) Therefore, applying Yu's teaching regarding inserting one or more metal layers to Torii's transistors would be nothing more than applying the fabrication process disclosed in Yu for forming the additional metal layers of the gate electrode to Torii's fabrication process. (TSMC-1003, ¶203.) The results of the combination would have been predictable and a POSITA would have had a reasonable expectation of success. (*Id*.) Both Yu and Torii describe devices having transistors of the same conductivity device with different threshold voltages and Yu teaches that its technique is applicable to both SOI and "bulk-type substrates." (TSMC-1008, 6:25-35, 6:65-67; *see also*, 5:60-67.) Moreover, Yu, filed a decade before the '779 patent, uses conventional photolithography and processes to add the metal layers to a gate stack. Such conventional techniques would have been well-known and understood by a POSITA. (TSMC-1003, ¶203.)

Thus, the combination of Torii and Yu renders claim 15 obvious under PO's litigation allegations.

IX. GROUND 4: Gilmer Renders Claims 1, 12-15 Obvious.

A. Gilmer

Gilmer discloses a semiconductor device "having dual gate dielectric thicknesses and utilizing high-k gate dielectric materials such as metal oxides." (TSMC-1009, 1:7-10.) Gilmer's device 10 includes transistors in core region 22 and I/O region 24. (*See* TSMC-1009, 4:43-47, Figure 4 (below).) Core transistor 22 includes a gate stack having gate dielectric 20, high-k dielectric (metal oxide) 26, and gate electrode 28. (TSMC-1009, 4:35-38.) I/O transistor 24 includes gate dielectric 16, high-k dielectric (metal oxide) 26, and gate electrode 28. (TSMC-1009, 4:35-38.)



Gilmer, Figure 4

B. Independent Claim 1

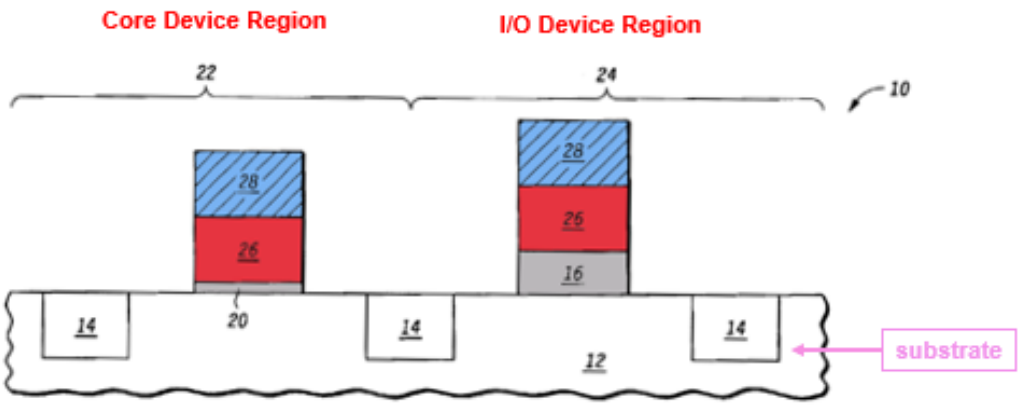
1. Preamble [1P]

Gilmer discloses "*a semiconductor device*" [1P]: "present invention relates generally to **semiconductor devices**." (TSMC-1009, 1:7-8; *see also,* TSMC-1009, Abstract, 1:57-60 (Figures 1-4 illustrate "views of a semiconductor device … as it undergoes processing")); TSMC-1003, ¶211.)

2. Limitations [1A]-[2A]

Gilmer teaches or at least suggests "[1A] *a first MIS transistor and* [2A] *a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate*." (TSMC-1003, ¶¶212-224.)

Gilmer's "semiconductor device 10 includes a **semiconductor substrate 12** which in a preferred embodiment is a single crystal silicon substrate." (TSMC-1009, 2:38-40.) Gilmer's device "includes two different device regions, namely a core device region 22 and an I/O device region 24." (TSMC-1009, 2:59-60.) Core device region 22 and I/O device region 24 each includes a "*transistor*." (*See* TSMC-1009, 4:43-44 ("conventional processing occurs to complete the **transistor**"; TSMC-1003, ¶212.)



Gilmer, Figure 4

Gilmer's core transistor and I/O transistor are each an "***MIS*** *transistor*." (TSMC-1003, ¶213.) The gate stacks of both transistors include gate dielectric 16/20 (shaded grey), high-k metal oxide layer 26, and gate electrode material 28. (*See* TSMC-1009, 4:40-41, 2:46-48 (dielectric 16), 3:9-11 (dielectric 20), 3:44-47 (high-k layer), 4:38-40 (gate electrode).) Gate dielectric 16, gate dielectric 20 and high-k metal oxide 26 are each dielectrics (insulators) and gate electrode material 28 is "conductive (doped) polysilicon or a metal (e.g., titanium nitride)." (TSMC-1009, 2:48-50.) Each transistor therefore has a metal-insulator-silicon (MIS) structure. (TSMC-1003, ¶213.)

Accordingly, I/O region transistor 24 is a "*first MIS transistor*" [1A] and core region transistor 22 is a "*second MIS transistor*" [2A]. (TSMC-1003, ¶214.) As shown in Figure 4 (above), both transistors are provided on the same silicon

substrate 12 and are therefore "*provided on an identical semiconductor substrate.*" (*Id*.)

Gilmer does not explicitly specify the I/O and core transistors are "*of an identical conductivity type.*" However, it would have been obvious to a POSITA that both transistors share the same conductivity type (e.g., n-type or p-type). (TSMC-1003, ¶¶215-224.)

First, Gilmer provides I/O transistors (with higher voltage requirements) and logic transistors (with lower voltage requirements) having interface layers of different thicknesses. (*See, e.g.,* TSMC-1009, 2:60-65 (discussing voltages for core and I/O devices).) Gilmer compares electrical characteristics of these I/O and core transistors. (*See, e.g.,* TSMC-1009, 2:60-65 (discussing voltages for core and I/O devices).) A POSITA would have understood such comparisons apply to transistors of an identical conductivity type. (TSMC-1003, ¶220, *see also*, TSMC-1003, ¶¶54-56.)

Second, Gilmer extensively discusses the concept of Dual Gate Oxide (DGO), which relates to the formation of transistors having different gate dielectric thickness on the same semiconductor substrate or wafer. (TSMC-1009, 1:14-16.) A POSITA would have understood the core and I/O transistors of Gilmer formed by DGO process have the same conductivity type. (TSMC-1003, ¶215, *citing* TSMC-

1026, 3:45-4:36 (describing formation of nMOS devices with differing gate oxide thicknesses using DGO), *see also*, TSMC-1003, ¶¶68-69; TSMC-1027, 5:61-7:58.)

Third, a substrate typically has a conductivity type (e.g., n-type or p-type). For example, a NMOS transistor "is built with a p-type body [or p-type well] and has regions of n-type semiconductor adjacent to the gate called the source and drain" and a PMOS transistor "is just the opposite, consisting of p-type source and drain regions with an n-type body [or n-type well]." (TSMC-1012, 8.) To form a transistor of a different conductivity type on the same substrate, a structure (e.g., a well) having a different conductivity type must be present in the substrate. (TSMC-1003, ¶¶216-218.) A POSITA would ascertain from Gilmer's description that both transistors share at least the same conductivity type because Gilmer does not disclose (i) the formation of any particular doped regions (i.e., wells) within the substrate in either the core or I/O regions which would provide for a conductivity type separate from that of the substrate, or (ii) any indication that each of the transistors in the core or I/O regions are formed on different conductivity type regions (i.e., wells) on the substrate. (TSMC-1003, ¶219.)

Fourth, a POSITA would have further understood CMOS was the dominant processing technology in the semiconductor industry prior to the '779 patent. (TSMC-1015, 42.) CMOS processing technology integrates both n- and p-type MOS devices side-by-side. (*Id*.) Therefore, although only one is depicted in

Gilmer's figures, a POSITA would have understood the I/O device had both an n-type and a p-type transistor and the core device had both an n-type and p-type device. (TSMC-1003, ¶221.) That is, for every pair of DGO nMOS transistors, there is a corresponding pair of DGO pMOS transistors. (*Id*.)

Additionally, making both transistors the same conductivity type would have been obvious to try. *See KSR*, 550 U.S. at 421. A POSITA would have understood only two alternatives exist for the conductivity type of Gilmer's transistors: (1) core and I/O transistors are of an identical conductivity type or (2) core and I/O transistors are of different conductivity types. (TSMC-1003, ¶¶222-223.)

A POSITA would have had a reasonable expectation of success in pursuing both alternatives. (TSMC-1003, ¶223.) Forming transistors of the same conductivity type (e.g., nMIS/nMOS or pMIS/pMOS transistors) in a substrate was well-known long before the '779 patent. (*See, e.g.,* TSMC-1012, 8; TSMC-1003, ¶223.) Additionally, CMOS processing which forms both nMIS/nMOS and pMIS/pMOS transistors was also well-known before the '779 patent. (*See, e.g.,* TSMC-1012, 113-125.) For these reasons, trying these two alternatives would have led a POSITA to anticipated success with either alternative. (TSMC-1003, ¶223.) Accordingly, having two transistors of the same conductivity type in Gilmer's semiconductor device is "the product **not of innovation** but of ordinary skill and **common sense**." *See Perfect Web*, 587 F.3d at 1331.

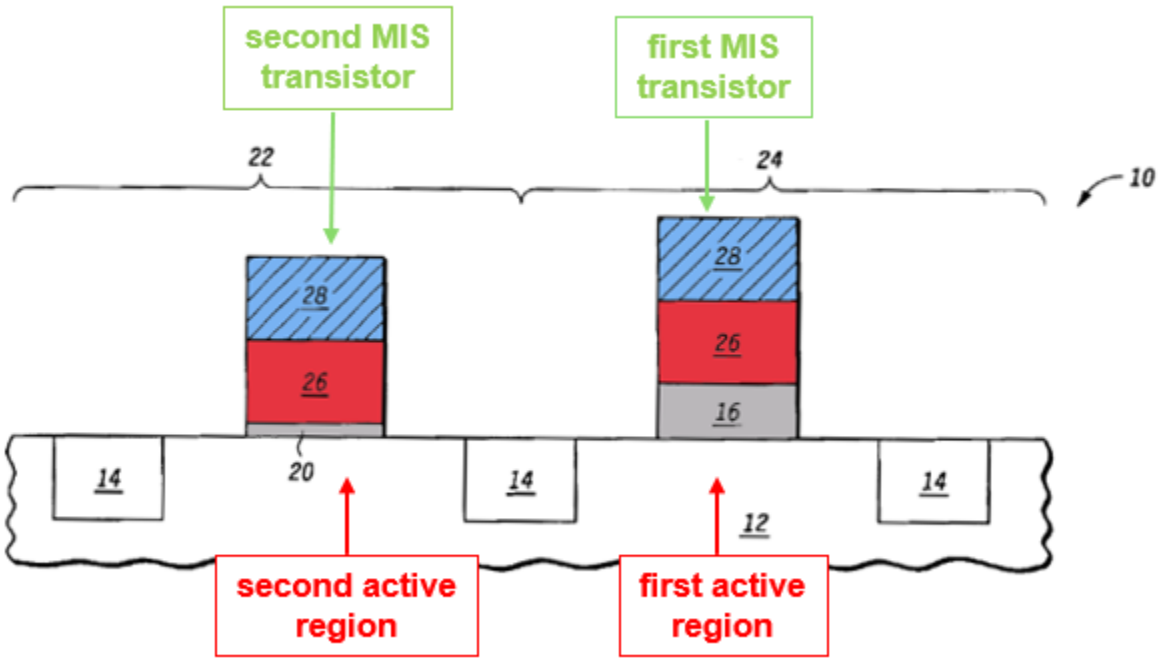
Gilmer therefore teaches or at least suggests "[1A] *a first MIS transistor and* [2A] *a second MIS transistor*" are "*of an identical conductivity type provided on an identical semiconductor substrate*." (TSMC-1003, ¶¶212-224.)

3. Limitations [1A.1]-[1A.2]/[2A.1]-[2A.2]

Gilmer's I/O transistor ("*first MIS transistor*") teaches limitations [1A.1]-[1A.2] and Gilmer's core transistor ("*second MIS transistor*") teaches limitations [2A.1]-[2A.2]. (TSMC-1003, ¶¶226-231.)

a. "Active Region[s] in the Semiconductor Substrate"

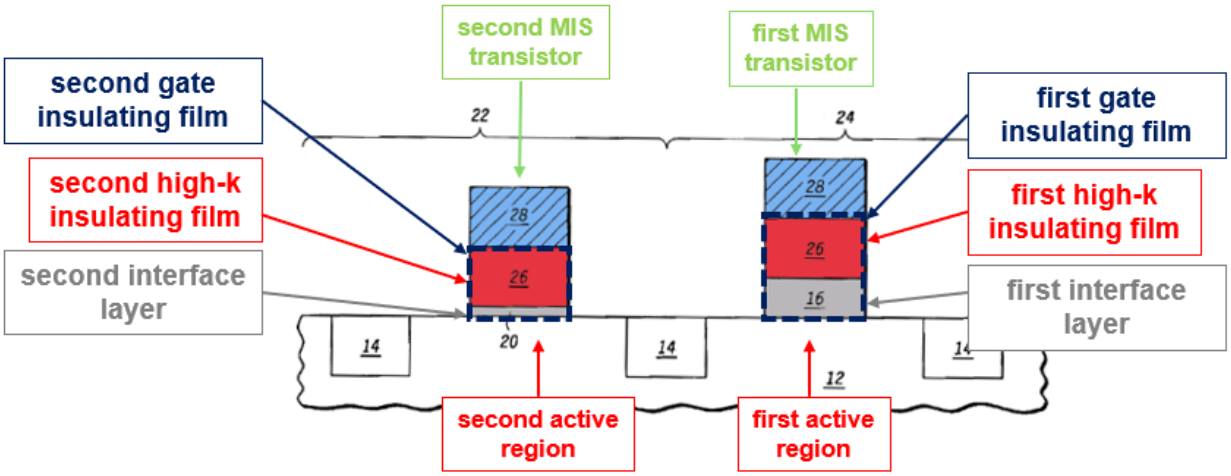
The I/O and core transistors in Gilmer's device each has an "*active region in the semiconductor substrate.*" (TSMC-1003, ¶226.) As shown in Figure 4 below, "[w]ithin substrate 12, trench isolation regions 14, preferably shallow trench isolation regions, are formed in a conventional manner for the purpose of electrically isolating different individual devices to be formed." (TSMC-1009, 2:43-46.) I/O region 24 is a "*first active region in the semiconductor substrate*" and core region 22 is a "*second active region in the semiconductor substrate.*" (TSMC-1003, ¶226; *see* TSMC-1001, 1:67-2:3; TSMC-1015, 52-53.)



Gilmer, Figure 4

b. Limitations [1A.1]-[1A.2]/[2A.1]-[2A.2]

The gate stack of Gilmer's I/O transistor ("*first MIS transistor*") includes gate dielectric 16 (shaded grey) "formed over substrate 12" and metal oxide 26 (shaded red) formed on dielectric 16. (*See* TSMC-1009, 2:46-48, 3:44-47, Figure 4 (below).) Metal oxide layer 26 is a "high-k dielectric." (TSMC-1009, 3:44-54.) Gate dielectric 16 is a "*first interface layer being in contact with the semiconductor substrate*" and metal oxide 26 is a "*first high dielectric constant insulating film formed on the first interface layer* [gate dielectric 16]" [1A.2]. (TSMC-1003, ¶227.) These layers, which are dielectrics, are collectively the "*first gate insulating film formed on a first active region in the semiconductor substrate*" [1A.1]. (*Id.*)



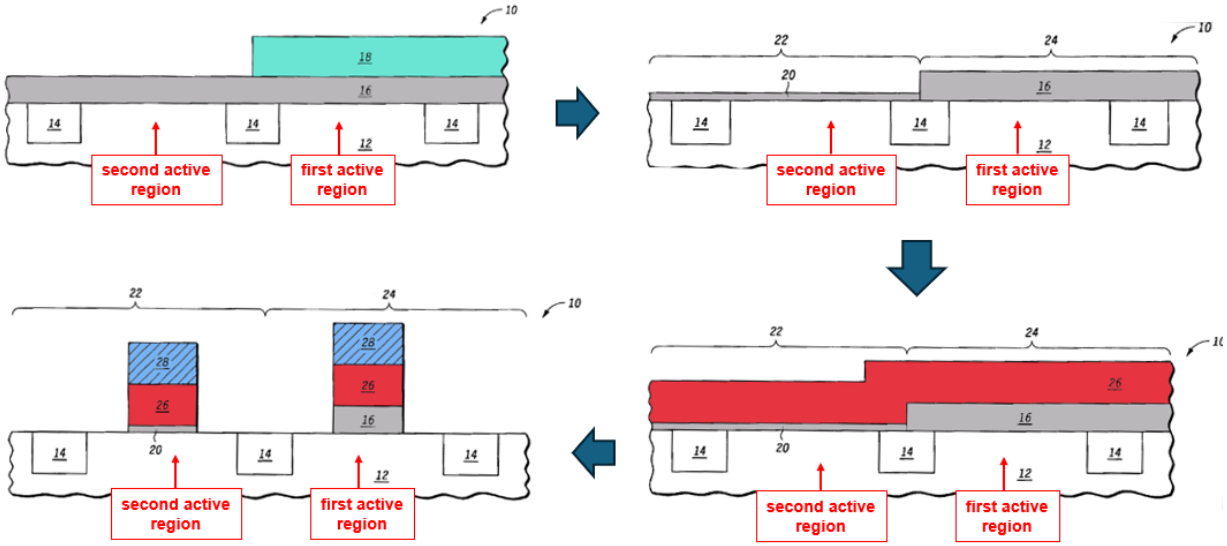
Gilmer, Figure 4

Similarly, the gate stack of Gilmer's core transistor ("*second MIS transistor*") includes gate dielectric 20 (shaded grey) and metal oxide 26 (shaded red) formed on dielectric 20. (*See* TSMC-1009, 2:46-48, 3:44-47, Figure 4 (above).) Gate dielectric 20 is the "*second interface layer being in contact with the semiconductor substrate*" and metal oxide 26 is a "*second high dielectric constant insulating film formed on the second interface layer* [gate dielectric 20]" [2A.2]. (TSMC-1003, ¶228.) These layers, which are dielectrics, are collectively the "*second gate insulating film formed on a second active region in the semiconductor substrate*" [2A.1]. (*Id.*)

The gate stack of I/O transistor 24 and core transistor 22 each also includes gate electrode 28 "deposited over the metal oxide" (the high-k dielectric) which is the top layer of the "*gate insulating film*." (TSMC-1009, 4:35-38.) Thus, the I/O transistor includes a "*first gate electrode formed on the first gate insulating film*"

and the core logic transistor includes a "*second gate electrode formed on the second gate insulating film.*" (TSMC-1003, ¶229.)

Gilmer's fabrication process confirms the Figure 4 device structure. Specifically, "after forming trench isolation regions 14, a first gate dielectric 16 [shaded grey] is formed over substrate 12." (TSMC-1009, 2:46-48, Figure 1 (top-left).) After masking a portion of the first gate dielectric layer, device 10 is then etched "to remove unprotected portions of first gate dielectric 16 in core device region 22" and after removal of the mask, "second gate dielectric 20 [shaded grey] is formed on exposed portions of substrate 12 within the core device region 22." (TSMC-1009, 2:25-67, 3:7-12, Figure 2 (top-right).)



Gilmer, Figures 1 (top-left), 2 (top-right)
3 (bottom-right), 4 (bottom-left)

After the first and second gate dielectrics with "two different thicknesses have been formed, a high-k dielectric … is deposited over semiconductor device 10." (TSMC-1009, 3:44-47, Figure 3 (bottom-right). Gate electrode material 28 (shaded blue) is subsequently "deposited over the metal oxide, and semiconductor device 10 is patterned and etched to form the gate stacks." (TSMC-1009, 4:35-38, Figure 4 (bottom-left).)

c. Limitation [1B]

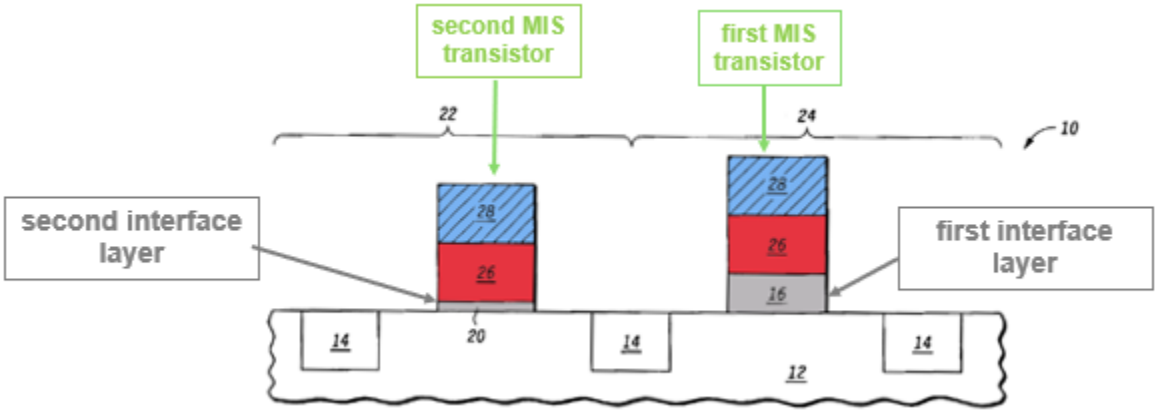
Gilmer teaches "*the first interface layer has a thickness larger than that of the second interface layer*" [1B]. (TSMC-1003, ¶¶232-233.)

Gilmer repeatedly teaches gate dielectric 16 ("*first interface layer*") of I/O transistor 24 "*has a thickness larger than that of*" the second gate dielectric 20 ("*second interface layer*") of core transistor 22:

- "[i]n operation, devices to be formed in core device region 22 require thinner gate dielectrics that operate at lower voltages than, e.g., I/O devices to be formed in I/O device region 24 that can withstand higher voltages required for I/O functions." (TSMC-1009, 2:60-65.)
- "A thicker first gate dielectric (16) is formed in a region of the device for higher voltage requirements, e.g. an I/O region (24). A thinner second gate dielectric (20) is formed in a region of the device for lower voltage requirements, e.g. a core device region (22)." (TSMC-1009, Abstract)

- "forming a second gate dielectric layer overlying the first region of the semiconductor substrate, the second gate dielectric layer having a second thickness less than the first thickness" (TSMC-1009, claim 1)

Specifically, Gilmer teaches the "thickness of gate dielectric 16 … generally will be within a range of 30-50 Angstroms (3-5 nanometers)" (2:51-55) whereas the "thickness of gate dielectric 20 … will be within a range of 4-12 Angstroms (0.4-1.2 nanometers)" (3:17-21). As shown in Figure 4 below, "*the first interface layer* [gate dielectric 16] *has a thickness larger than that of the second interface layer* [gate dielectric 20]" [1B]. (TSMC-1003, ¶233.)



Gilmer, Figure 4

d. Limitation [1C]

Gilmer teaches "*each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film*" [1C]. (TSMC-1003, ¶234.)

In Gilmer, "[f]irst gate dielectric 16 ["*first interface layer*"] is preferably silicon dioxide or **silicon oxynitride**." (TSMC-1009, 2:48-51.) Gilmer similarly teaches "second gate dielectric 20 ["*second interface layer*"] is also silicon dioxide or **silicon oxynitride**." (TSMC-1009, 3:12-14.) Thus, Gilmer teaches "*each of the first interface layer and the second interface layer is made of … a silicon oxynitride film*" [1C].

C. Claims 12-13

Gilmer teaches "*each of the first and second high dielectric constant insulating films contains hafnium or zirconium*" [12]. (TSMC-1003, ¶236.) As discussed in §IX.B.3, after the "gate dielectrics of two different thicknesses have been formed, a **high-k dielectric** … is deposited over semiconductor device 10." (TSMC-1009, 3:44-47.) Preferably, the high-k dielectric is a metal oxide 26 such as "**hafnium** oxide (HfO_2), **hafnium** silicate ($Hf_xSi_yO_z$), or lanthanum aluminate ($LaAlO_3$), but lanthanum oxide, **hafnium** aluminate, **zirconium** oxide, and **zirconium** silicate, and other like materials, may also be suitable high-k dielectrics." (TSMC-1009, 3:49-54.) A POSITA would have been motivated to select, e.g., HfO_2, as the high-k dielectric given its known benefits, e.g., "its superior thermal stability with poly-Si and reasonable band alignment." (TSMC-1024, 2.4.1; *see also* TSMC-1013, 207; TSMC-1025, 134; TSMC-1003, ¶236.)

Gilmer explains "[b]ecause metal oxide 26 is deposited as **a single blanket deposition**, its **thickness will not vary much** across the substrate surface and thus one should use the thicknesses of the first and second dielectrics as the 'variables' to achieve the final EOTs for the core and I/O devices." (TSMC-1009, 4:2-7.) A POSITA would understand from this language the metal oxide film, which is deposited as a single blanket deposition, is "*equal in thickness*" in both the I/O and core region subject to very minor variations. (TSMC-1003, ¶237.) Gilmer's teaching is consistent with the '779 patent that only discloses the "first and second high dielectric insulating films may be **substantially equal** in thickness." (TSMC-1001, 5:31-33.) Gilmer therefore teaches "*the first and second high dielectric constant insulating films are equal in thickness*" [13]. (TSMC-1003, ¶237.)

D. Claim 14

Gilmer teaches "*the first and second gate electrodes are made of an identical material*" [14]. (TSMC-1003, ¶238.)

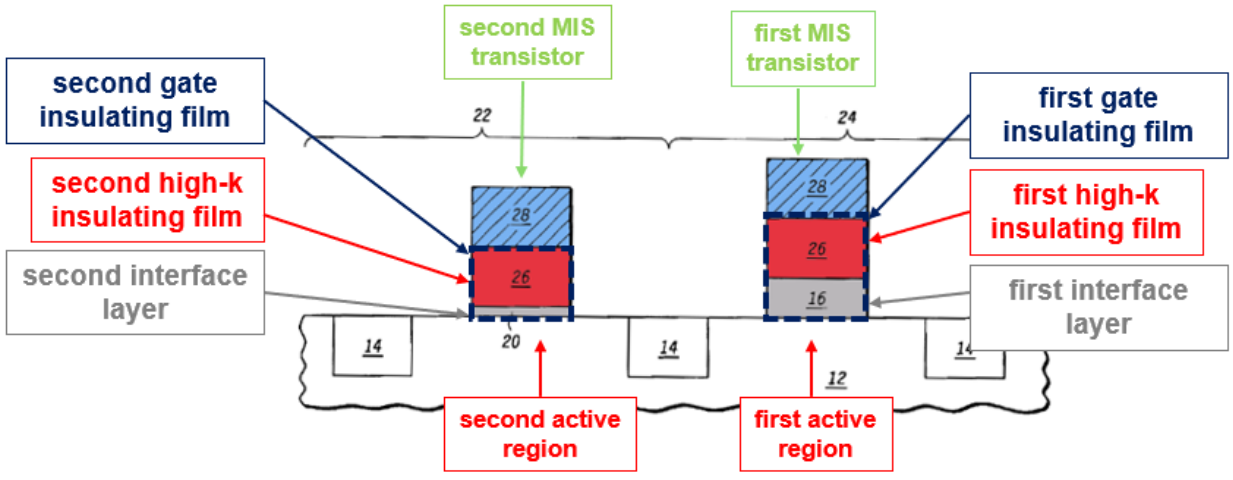
As discussed in §IX.B.3, "[a]fter metal oxide layer 26 has been deposited, a gate electrode material 28 is deposited over the metal oxide, and semiconductor device 10 is patterned and etched to form the gate stacks as shown in FIG. 4." (TSMC-1009, 4:35-38.) Gilmer's gate electrode material 28 is "conductive (doped) polysilicon or a metal (e.g. titanium nitride)." (TSMC-1009, 4:38-40.) Because the gate electrode layer is blanket deposited over the entire substrate and subsequently

etched when gate stacks of the core and I/O transistors are formed, gate electrode layer 28 in both the I/O and core transistors "*are made of an identical material.*" (TSMC-1003, ¶238.)

E. Claim 15

Gilmer discloses "*the effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor.*" (TSMC-1003, ¶¶239-242.)

Gilmer's device includes an I/O transistor with a gate insulating film comprising gate dielectric 16 (shaded grey) and high-k metal oxide 26 (shaded red) and a core transistor with a gate insulating film comprising gate dielectric 20 (shaded grey) and high-k metal oxide 26 (shaded red). (TSMC-1009, Figure 4 (below).)



Gilmer, Figure 4

The high-k film of both the I/O and core transistors is formed in the same process step and therefore has the same thickness and same material (i.e., the same dielectric constant) in both transistors. (TSMC-1009, 3:44-47.) The contributions of the high-k layer to each transistor's EOT are the same and therefore cancel each other in the below equation comparing the EOTs of the two transistors. As discussed in §IX.D, the gate electrodes of the I/O and core transistors are the same. Gilmer teaches the I/O transistor's gate dielectric 16 and core transistor's gate electrode 20 are each preferably silicon oxynitride. (TSMC-1009, 2:48-49, 3:12-13.) Because the interface layers of both the I/O and core transistors use the same material (silicon oxynitride; i.e., $\varepsilon_{16} = \varepsilon_{20}$) but have different thicknesses (i.e., the $t_{16} > t_{20}$), the EOT of the I/O transistor is greater than the EOT of the core transistor. (TSMC-1003, ¶241.)

EOT (I/O) **EOT (Core)**

$$\left(\frac{t_{26}}{\varepsilon_{26}}\right)\varepsilon_{SiO_2} + \left(\frac{t_{16}}{\varepsilon_{16}}\right)\varepsilon_{SiO_2} > \left(\frac{t_{26}}{\varepsilon_{26}}\right)\varepsilon_{SiO_2} + \left(\frac{t_{20}}{\varepsilon_{20}}\right)\varepsilon_{SiO_2}$$

Accordingly, because the I/O transistor ("*first MIS transistor*") has a greater EOT than the core transistor ("*second MIS transistor*"), the "*effective work function of the*" I/O transistor ("*first MIS transistor*") "*is higher than an effective work function of the*" core transistor ("*second MIS transistor*"), according to the disclosure of the '779 patent. (TSMC-1003, ¶¶239-242.)

X. GROUND 5: Combination of Gilmer and Chen Renders Claims 1, 12-15 Obvious.

As discussed in §§IX.B-D, Gilmer alone renders claims 1 and 12-14 obvious and in §IX.E, Gilmer alone renders claim 15 obvious according to the disclosure of the '779 patent. Should an argument be made that Gilmer alone does not render obvious the "*first MIS*" and "*second MIS*" transistors are "*of the same conductivity type*", Chen provides this teaching as discussed in §X.B. Thus, the combination of Gilmer and Chen renders claims 1 and 12-14 obvious and claim 15 obvious according to the disclosure of the '779 patent.

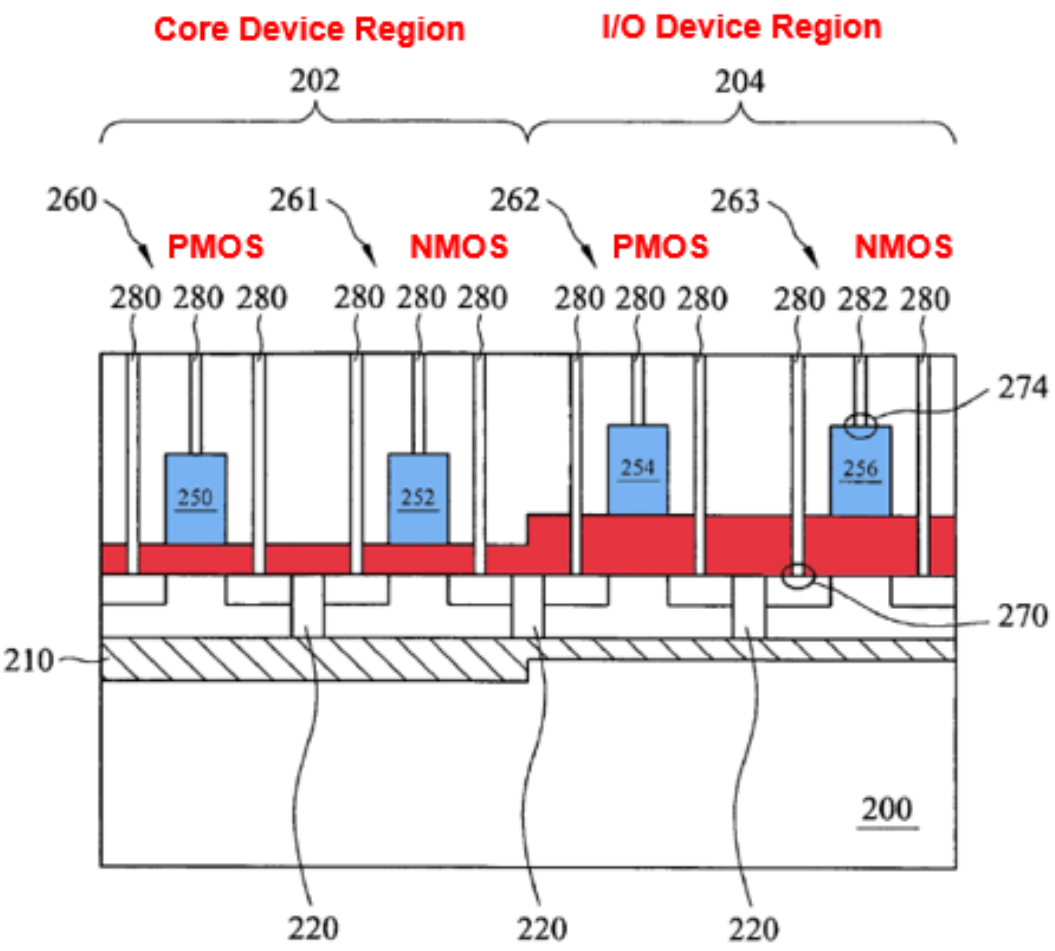
While Gilmer discloses claim 15 in the same manner as disclosed in the '779 patent, Gilmer does not disclose modifying the effective metal work function of the gate electrode under PO's litigation allegations. Chen discloses such metal work function engineering, as discussed in §X.C.

A. Chen

Chen explains that "to produce competitive electronic devices, it is often desired to produce semiconductor chips with several different regions (e.g., core region, low power region, I/O region) having semiconductor devices that vary according to speed and power, for example." (TSMC-1010, 1:18-22.) These devices have different threshold voltages, with the I/O devices having the highest threshold voltage and low operating power transistors having the lowest voltage. (TSMC-1010, 2:25-28.)

Chen's device, illustrated below, includes a pMOS transistor with a first metal alloy gate electrode and a nMOS transistor with an n-doped first metal alloy gate electrode in a first device region and a pMOS transistor with a second metal alloy gate electrode and a nMOS transistor with an n-doped second metal alloy gate electrode in a second device region[9]. (TSMC-1010, 8:13-18, Figure 3h (below).) The gate electrode 252 of the first region nMOS transistor has a work function ranging between about 4.2 eV and about 4.5 eV and the gate electrode 256 of the second region nMOS transistor has a higher work function, ranging between about 4.5 eV and about 4.8 eV. (TSMC-1010, 8:38-42.)

[9] Chen has a typographic error referring to devices 260 and 261 as pMOS devices and devices 262 and 263 as nMOS devices (*See* TSMC-1010, 8:27-29.) A POSITA would have understood devices 260 and 262 to be pMOS devices and devices 261 and 263 to be nMOS devices based on discussions, e.g., in columns 3, 7, and 9 and claim 31. (TSMC-1003, ¶256.)

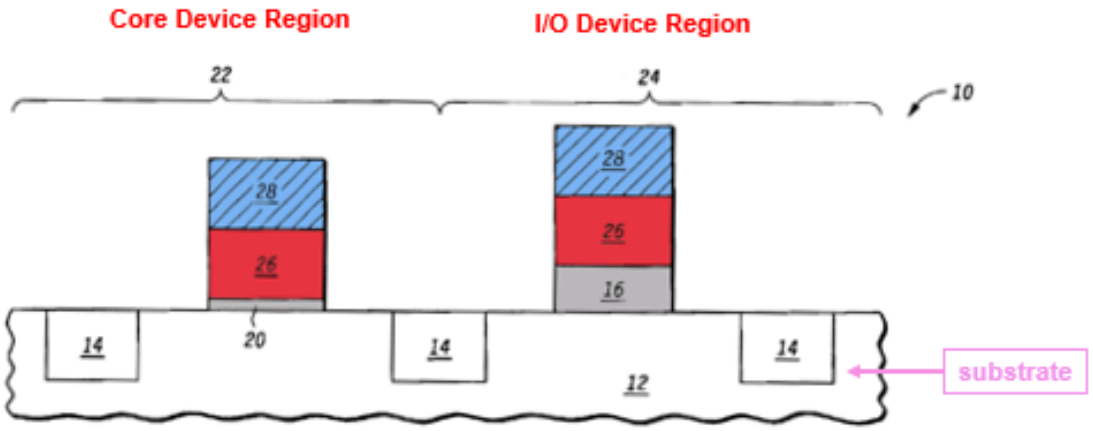


Chen, Figure 3h

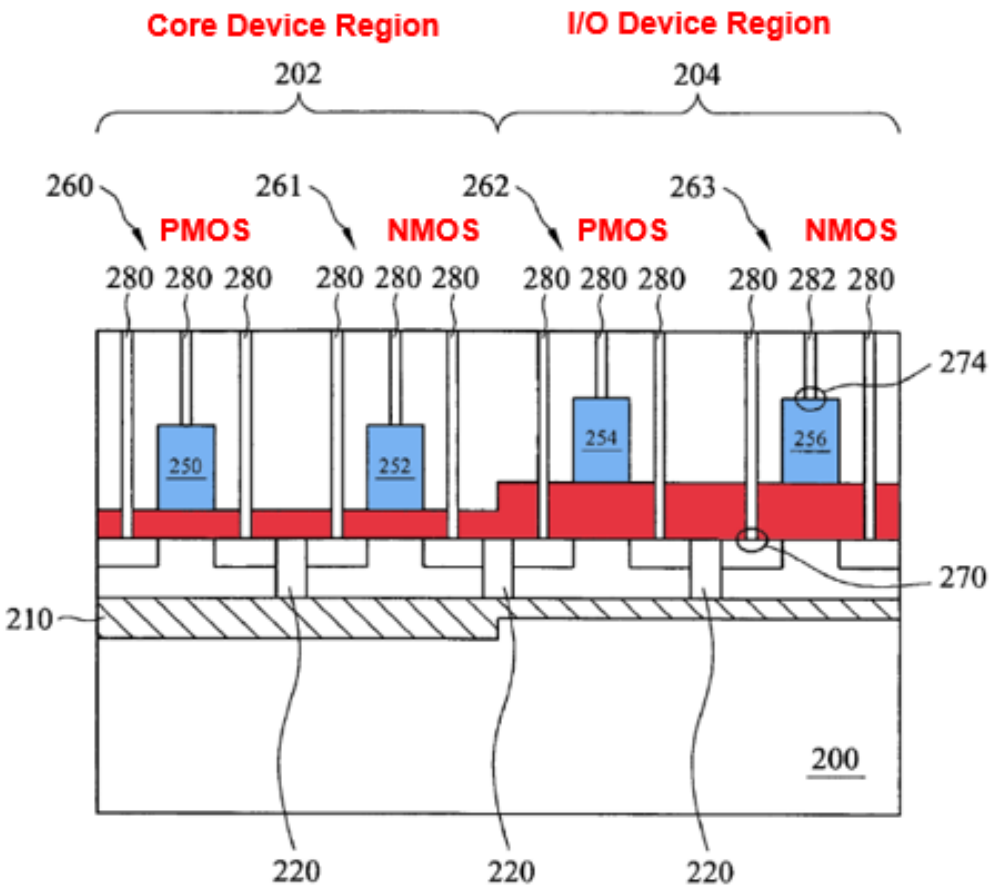
Chen teaches that "[v]arying the material composition, and thereby the work function of the gate electrodes 250, 252, 254, and 256, provides a corresponding difference in voltage threshold" between devices 260, 261, 262, and 263. (TSMC-1010, 8:29-33.) That is, the voltage thresholds of the transistors "are partially controlled by the work function of" their respective gate electrodes. (TSMC-1010, 8:33-35.)

B. Combination of Chen's Core and I/O transistors of the same conductivity type with Gilmer

Gilmer discloses core and I/O transistors formed in a shared substrate as illustrated in Figure 4 (below-top). Chen teaches core and I/O transistors having similar structures formed in the same substrate and having "*the same conductivity type*", as shown in Figure 3h (below-bottom). (TSMC-1010, 3:39-60, 8:27-42 (describing two pMOS and two NMOS transistors).)



Gilmer, Figure 4



Chen, Figure 3h

Both Gilmer and Chen are in the same field as the ’779 patent, “semiconductor devices and methods for fabricating the same.” (TSMC-1001, 1:15-16; TSMC-1009, 1:7-10, 2:36-38; TSMC-1010, 1:12-14, 4:14-16.)

A POSITA would have been motivated to combine Chen’s teachings regarding forming transistors having the same conductivity type (e.g., two nMIS transistors or two pMIS transistors) with Gilmer’s semiconductor device. (TSMC-1003, ¶259.) Gilmer suggests forming transistors of the same conductivity type as

discussed in §IX.B.2. For these same reasons, Gilmer suggests the combination with Chen. (TSMC-1003, ¶259.) Additionally, a POSITA would have been motivated to make the combination based on his/her background knowledge in the relevant art and common sense. *See Perfect Web*, 587 F.3d at 328-29 ("[M]otivation to combine may be found explicitly or implicitly in … the background knowledge, creativity, and common sense of the person of ordinary skill."); TSMC-1003, ¶259. The '779 patent acknowledges in its background section the well-known fact that devices have conductivity types and describes use of an n-well for pMIS transistors and a p-well for nMIS transistors. (TSMC-1001, 1:61-2:15; §IV.B.) Based on this background knowledge, a POSITA would have been motivated to combine Gilmer and Chen and would have had a reasonable expectation of success in forming devices of the same conductivity type in Gilmer, as taught by Chen. (TSMC-1003, ¶259.)

1. Independent Claim 1

Gilmer teaches every limitation of claim 1 but does not expressly state the "*first*" and "*second*" MIS transistors are "*of the same conductivity type.*" Chen discloses its Figure 3h device includes pMOS transistor 260 and nMOS transistor 261 in the core device region and pMOS transistor 262 and nMOS transistor in the I/O device region. (*See* TSMC-1010, 3:39-60, 8:27-29.) That is, the device includes two nMOS transistors (i.e., two transistors "*of the same conductivity*

type") and two pMOS transistors (i.e., two transistors "*of the same conductivity type*"). Thus, the combination of Gilmer and Chen provides explicitly "[1A] *a first MIS transistor and* [2A] *a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate.*" (TSMC-1003, ¶260.)

For this reason and the reasons discussed in §IX.B for the preamble [1P] and limitations [1A.1]-[1A.2], [2A.1]-[2A.2], [1B] and [1C], the combination of Gilmer and Chen renders claim 1 obvious.

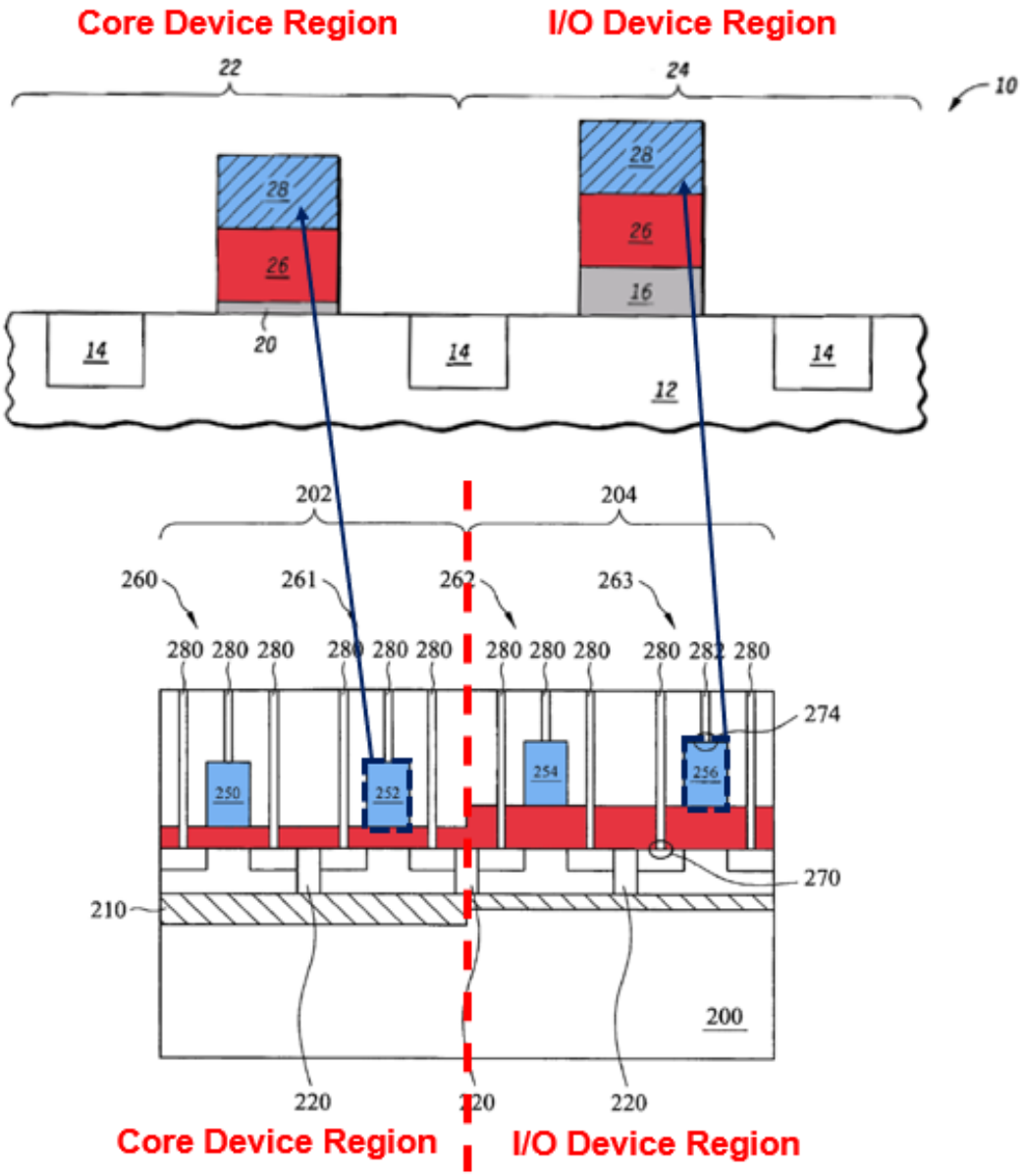
2. Claims 12-15

The combination of Gilmer and Chen renders claims 12-14 obvious for the same reasons discussed in §§IX.C-D and claim 15 obvious according to the disclosure of the '779 patent for the same reasons discussed in §IX.E.

C. Combination of Chen's gate electrode work function variation teachings with Gilmer's transistors renders claim 15 obvious.

Gilmer describes that after deposition of high-k layer 26, "gate electrode material 28 is deposited." (TSMC-1009, 4:35-38.) In Gilmer, the gate electrode material "will generally be conductive (doped) polysilicon or a metal (e.g., titanium nitride)." (TSMC-1009, 4:38-40.) A POSITA would have been motivated to combine Chen's teachings regarding varying the composition of the gate electrode to vary the gate electrode work functions and hence better control the threshold voltage of the core and I/O transistors of Gilmer. (TSMC-1003, ¶¶263-264.) Specifically, as illustrated below, a POSITA would have been motivated to

use Chen's first metal alloy gate electrode in Gilmer's core transistor and Chen's second metal alloy gate electrode in Gilmer's I/O transistor. (*Id.*)



Gilmer, Figure 4 (top); Chen, Figure 3h (bottom)

A POSITA would have been motivated to make the above combination because Chen expressly motivates the combination. (TSMC-1003, ¶265.) Chen

teaches that the threshold voltage of a core transistor differs from the threshold voltage of an I/O transistor, which is consistent with POSITA's knowledge of the art. (TSMC-1003, ¶265; §IV.A.) Further, Chen, like Gilmer, discloses transistors in the core device region are built with a thinner gate dielectric stack compared to the transistors in the I/O device region. (*Id.*) In other words, the transistors disclosed by Chen are similar to those of Gilmer and therefore suggest the combination. (TSMC-1003, ¶265.)

Chen further teaches "gate workfunction (ϕ_m) is a good candidate for V_{th} tuning" and discloses adjusting the gate work function to achieve multiple threshold voltage devices on the same substrate. (TSMC-1010, 2:49-51.) A POSITA would be motivated to use Chen's teachings to further tune or control the V_{th} of the I/O transistor (e.g., by adjusting up its gate work function) if the thicker oxide in Gilmer's I/O transistor did not offer sufficient V_{th} adjustment and to further tune or better control the V_{th} of the core transistor (e.g., by adjusting down its gate work function) if the thinner oxide of the core transistor did not offer sufficient V_{th} adjustment. (TSMC-1003, ¶266.) The additional adjustment can be done, for example, by "[v]arying the material composition." (TSMC-1010, 8:27-33.)

In the combination, gate electrode 252 of the nMOS core device "has a work function ranging between about 4.2 eV and about 4.5 eV" and gate electrode 256

of the respective nMOS I/O device "has a work function ranging between 4.5 eV and about 4.8 eV." (Chen, 8:39-42.) Thus, the "*effective work function*" of the nMOS I/O transistor ("*first MIS transistor*") in the combination of Gilmer and Chen "*is higher than an effective work function*" of the NMOS core transistor ("*second MIS transistor*") under PO's litigation allegations. (TSMC-1003, ¶267.)

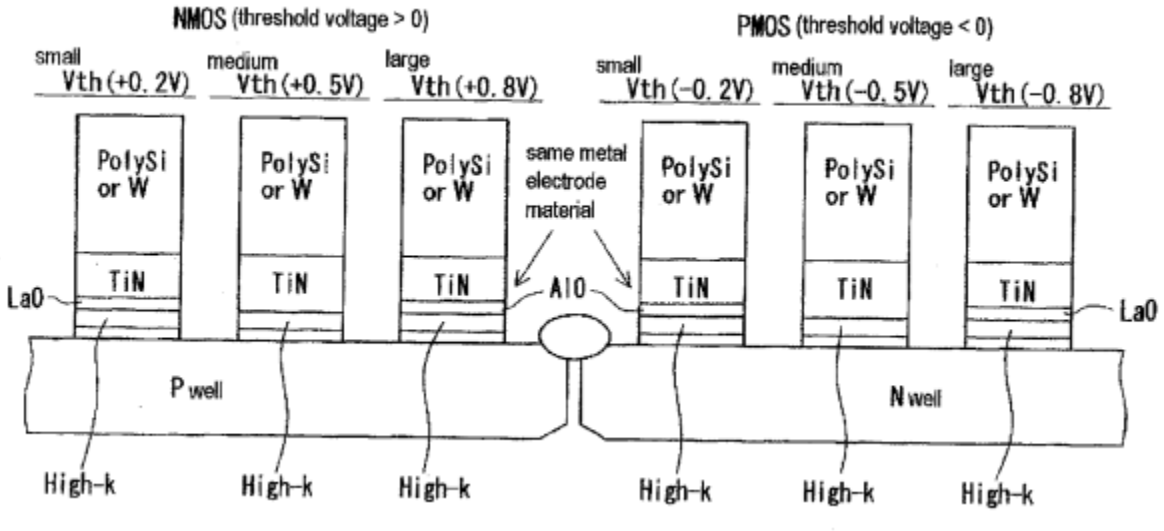
XI. GROUND 6: Combination of Gilmer, Chen, and Mise Renders Claims 8-11 Obvious.

In the combination of Gilmer and Chen, the "*first and second MIS transistors*" of its semiconductor device are "*pMIS transistors*" [8A] or "*nMIS transistors*" [10A], as taught by Chen. Neither Gilmer nor Chen however explicitly discloses the remaining limitations of claims 8-11. Mise provides these teachings, as discussed in §VII.A-C. Gilmer, Chen, and Mise are in the same field as the '779 patent "semiconductor devices and methods for fabricating the same." (TSMC-1001, 1:15-16; TSMC-1009, 1:7-10, 2:36-38; TSMC-1010, 1:12-14, 4:14-16; TSMC-1006, ¶1.)

A. Combination of Gilmer, Chen, and Mise

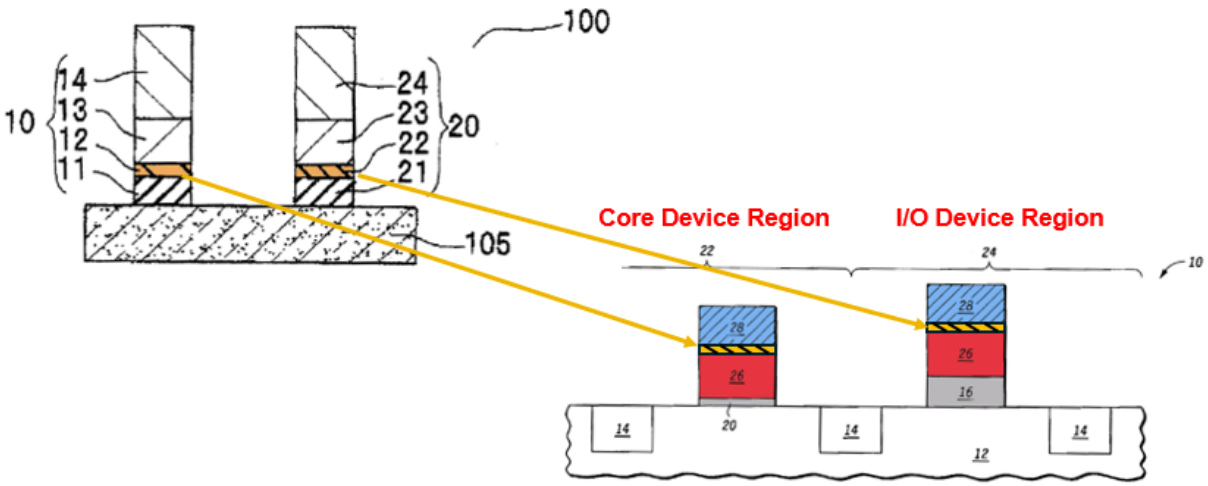
Gilmer discloses core and I/O transistors formed on a common substrate. (Gilmer, Figure 4.) Chen teaches two core and I/O transistors having similar structures formed on the same substrate and having "*the same conductivity type.*" (*See,* Chen, 3:39-60.) Mise teaches three NMIS transistors with the same conductivity type and different threshold voltages by incorporating capping layers

in the gate stacks. (Mise, Figure 11-ninth embodiment (below).) Mise teaches three PMIS transistors with the same conductivity type and different threshold voltages by varying the gate stack. (*Id.*)



Mise, Figure 11

The combination of Chen and Gilmer uses Gilmer's suggestion of a semiconductor device having two transistors of the same conductivity type, as confirmed by the teachings of Chen. A POSITA would have been motivated to apply Mise's teaching regarding use of a cap layer on a high-k film to the Gilmer-Chen device, illustrated in the figure below. (TSMC-1003, ¶270.)



Mise, Figure 1 (left); Gilmer, Modified Figure 4

A POSITA would have been motivated to make this combination to further adjust/fine-tune the threshold voltage of the transistors. (TSMC-1003, ¶¶270-271.) Gilmer teaches gate electrode material 28 "will generally be conductive (doped) polysilicon or a metal (e.g., titanium nitride)." (TSMC-1009, 4:38-40.) A POSITA would have been motivated to use the metal gate (TiN) for the reasons discussed in §VII.A.2.a. (TSMC-1003, ¶271; TSMC-1018, 1.) Gilmer also teaches "[m]etal gate electrodes may also benefit from use of a capping layer … ." (TSMC-1009, 5:38-39.) Indeed, a primary purpose of a cap layer is to adjust the threshold voltage of a transistor. (TSMC-1001, 2:24-27; TSMC-1022, ¶4.) A POSITA would have been further motivated to apply a cap layer to improve the operation of transistors by, e.g., reducing leakage current and improving compatibility between layers, as discussed in §VII.A.2.b. (TSMC-1003, ¶271.)

B. PMIS Claims 8-9

Chen's device includes first and second pMIS transistors. (§§X.A-B.) Therefore, the combination of Gilmer and Chen discussed in §X.B provides the "*first and second MIS transistors are pMIS transistors*" [8A]. (TSMC-1003, ¶272.)

Mise teaches cap layer 22 of the pMOS transistor's gate insulating film "is composed of AlO." (TSMC-1006, ¶72.) A POSITA would have been motivated to select a cap film containing aluminum, as taught by Mise in the pMIS devices of the combination of Gilmer and Chen. (TSMC-1003, ¶273.) In the combination, the metal gate material (TiN) is a "mid-gap" material, leading to a non-ideal threshold voltage. (*See, e.g.,* TSMC-1019, 1.) A POSITA would have therefore been motivated to include aluminum in the cap layer to shift the threshold voltage, making it suitable for pMIS devices. (*See* TSMC-1006, ¶¶154, 183-193, 195; TSMC-1020, 441-444; *see also,* TSMC-1021, 6:25-46, 12:8-23; §§VII.A-C.) The combination therefore provides "*the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing aluminum*" [9A] and "*the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing aluminum*" [9B]. (TSMC-1003, ¶273.)

Gilmer teaches suitable materials for the high-k film include "lanthanum aluminate (**$LaAlO_3$**), but lanthanum oxide, **hafnium aluminate**, zirconium oxide,

and zirconium silicate, and other like materials, may also be suitable." (TSMC-1009, 3:49-54.) Mise similarly teaches the high-k film used in the pMOS transistor is composed of, e.g., "**HfAlO**." (TSMC-1006, ¶72.) A POSITA would have also understood the high-k material in the combination device contains aluminum, as taught by Gilmer and Mise, at least because of diffusion as a result of thermal processing. (TSMC-1003, ¶274; *see also,* TSMC-1021, 6:25-37, 11:1-26 (describing Al diffusion through the gate insulating stack); TSMC-1022, ¶19 (mentioning diffusion of metal atoms across the gate stack).) Thus, in the combination of Gilmer, Chen, and Mise, the "*high dielectric constant insulating films*" of both pMIS transistors "*contain aluminum*" [8B]. (TSMC-1003, ¶274.)

C. NMIS Claims 10-11

Chen's device also includes first and second nMIS transistors. (§§X.A-B.) The combination of Gilmer and Chen discussed in §X.B therefore provides "*first and second MIS transistors are nMIS transistors*" [10A]. (TSMC-1003, ¶275.)

Mise teaches the cap layer 22 of the nMOS transistor's gate insulating film "is composed of MgO or LaO." (TSMC-1006, ¶71.) In the combination, the metal gate material (TiN) is a mid-gap material, leading to a non-ideal threshold voltage. (*See, e.g.,* TSMC-1019, 1.) A POSITA would have been motivated to select a cap layer containing lanthanum to shift the threshold voltage, making it suitable for nMIS devices, for the reasons discussed in §VII.A-C. (TSMC-1003, ¶276.) Thus,

the combination provides "*the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing lanthanum*" [11A] and "*the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing lanthanum*" [11B].

Gilmer teaches suitable materials for the high-k film include "lanthanum aluminate (**$LaAlO_3$**), but **lanthanum oxide**, hafnium aluminate, zirconium oxide, and zirconium silicate, and other like materials, may also be suitable." (TSMC-1009, 3:49-54.) Mise also teaches the gate insulation film of its nMOS transistor "is composed of a high-k material such as **HfLaO** or HfMgO." (TSMC-1006, ¶71.) A POSITA would have also understood that the high-k material in the combination device contains lanthanum, as taught by both Gilmer and Mise, at least because of diffusion as a result of thermal processing, discussed above. (*See* §§VII.A-C.) Thus, in the combination, the "*high dielectric constant insulating films*" of both nMIS transistors "*contain lanthanum*" [10B]. (TSMC-1003, ¶277.)

XII. Discretionary Denial In Not Appropriate

A. 35 U.S.C. §314(a)

Pursuant to the Stewart Memorandum dated March 26, 2025, titled "Interim Process for PTAB Workload Management," Petitioner will respond to any

discretionary denial arguments PO may raise through the Board's bifurcated briefing process.

Nevertheless, to simplify the *Fintiv* analysis, and following the precedential *Sotera* decision, Petitioner stipulates that, if IPR is instituted, Petitioner will not pursue in the related district court proceeding any ground that Petitioner raised or reasonably could have raised against the challenged claims during the instituted IPR.

B. 35 U.S.C. §325(d)

The Advanced Bionics framework favors institution. *See Advanced Bionics LLC v. MED-EL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 (P.T.A.B. Feb. 13, 2020) (precedential). Here, the corresponding U.S. Publication of Gilmer (U.S. Publication 2004/0032001) is the only asserted reference cited during prosecution of the '779 patent. However, the Gilmer Publication was not applied by the Examiner and therefore was not evaluated during examination. Even assuming the Gilmer publication was evaluated (which the record does not support), the Office erred in allowing the claims over Gilmer because Gilmer discloses "*a first MIS transistor and a second MIS transistor … provided on an identical semiconductor substrate*" and "*each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film*", features determined to be allowable by the Examiner. (EX-1002, 312-33;

§IX.B.) Moreover, the Petition's evidence warrants consideration because it presents a compelling case of unpatentability never considered by the Office. These circumstances weigh heavily against §325(d) discretionary denial.

XIII. Mandatory Notices (37 C.F.R. §42.8(b))

A. Real Parties-in-Interest

The Petitioner and real party-in-interest is Taiwan Semiconductor Manufacturing Company Ltd.

B. Related Matters

To the best of Petitioner's knowledge, the '779 patent is involved in the following ongoing litigations:

- *Advanced Integrated Circuit Process LLC, v. Taiwan Semiconductor Manufacturing Company Limited*, No. 2:24-CV-623 (E.D.T.X.)
- *Advanced Integrated Circuit Process LLC, v. United Microelectronics Corporation*, No. 2:24-CV-730 (E.D.T.X.)

C. Lead and Back-Up Counsel

Pursuant to 37 C.F.R. §§42.8(b)(3), 42.8(b)(4) and 42.10(a), Petitioner appoints the following lead and backup counsel:

Lead Counsel	Back Up Counsel
Lori A. Gordon (Reg. No. 50,633) Goodwin Procter LLP 1900 N. Street NW Washington, D.C. 20036 Phone: (202) 346-4000 Fax: (202) 346-4444 Gordon-PTAB@goodwinlaw.com	Andrew S. Ong (Reg. No. 69,076) Goodwin Procter LLP 601 Marshall Street Redwood City, CA 94063 Phone: (650) 752-3100 Fax: (650) 853-1038 AOng@goodwinlaw.com Theodoros Konstantakopoulos, Ph.D. (Reg. No. 74,155) Goodwin Procter LLP 620 Eighth Avenue New York, NY 10018 Phone: (212) 813-8800 Fax: (212) 355-3333 TKonstantakopoulos@goodwinlaw.com Jesse Cheng (*pro hac vice* forthcoming) Goodwin Procter LLP 601 Marshall Street Redwood City, CA 94063 Phone: (650) 752-3100 Fax: (650) 853-1038 JesseCheng@goodwinlaw.com Filippos Papadatos (Reg No. 78,834) Goodwin Procter LLP 620 Eighth Avenue New York, NY 10018 Phone: (212) 813-8800 Fax: (212) 355-3333 fpapadatos@goodwinlaw.com

Petitioner consents to electronic service by email at the addresses: Gordon-ptab@goodwinlaw.com, aong@goodwinlaw.com, TKonstantakopoulos@goodwinlaw.com, JesseCheng@goodwinlaw.com and fpapadatos@goodwinlaw.com.

XIV. Conclusion

Inter Partes Review of the challenged claims is respectfully requested.

Respectfully submitted,

/Lori A. Gordon/

Lori A. Gordon
Reg. No. 50,633
Attorney for Petitioner

Goodwin Procter LLP
1900 N. Street NW
Washington, D.C. 20036
Phone: (202) 346-4000
Fax: (202) 346-4444

Date: April 11, 2025

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(a), Petitioner hereby certifies that portions of the above-captioned **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 8,796,779**, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,982. Pursuant to 37 C.F.R. §42.24(a), this word count is in compliance and excludes the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing. This word count was prepared using Microsoft Word.

Respectfully submitted,

/Lori A. Gordon/

Lori A. Gordon
Reg. No. 50,633
Attorney for Petitioner

Goodwin Procter LLP
1900 N. Street NW
Washington, D.C. 20036
Phone: (202) 346-4000
Fax: (202) 346-4444

Date: April 11, 2025

CERTIFICATE OF SERVICE

The undersigned hereby certifies, in accordance with 37 C.F.R. § 42.105, that the foregoing **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,796,779,** TSMC's Power of Attorney, and all supporting exhibits were served via FedEx Next Business Day Delivery on April 11, 2025, in their entirety on the Patent Owner as detailed below:

Michael J. Cherskov & Szymon M. Gurda
Cherskov, Flaynik & Gurda, LLC
903 Commerce Drive, Suite 310
Oak Brook, IL 60523

Courtesy copies have been concurrently served by the electronic mail on Patent Owner's litigation counsel at:

Justin A. Nelson
SUSMAN GODFREY L.L.P.
1000 Louisiana Street, Suite 5100
Houston, TX 77002
Jnelson@susmangodfrey.com

Respectfully submitted,

/Lori A. Gordon/

Lori A. Gordon
Reg. No. 50,633
Attorney for Petitioner

Goodwin Procter LLP
1900 N. Street NW
Washington, D.C. 20036
Phone: (202) 346-4000
Fax: (202) 346-4444

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Appendix: Challenged Claim Listing

[1P] A semiconductor device comprising:

[1A] a first MIS transistor and [2A] a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate,

[1A.1] wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,

[2A.1] the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,

[1A.2] the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,

[2A.2] the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,

[1B] the first interface layer has a thickness larger than that of the second interface layer, and

[1C] each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.

[8] The semiconductor device of claim 1, wherein

[8A] the first and second MIS transistors are pMIS transistors, and

[8B] the first and second high dielectric constant insulating films contain aluminum.

[9] The semiconductor device of claim 8, wherein

[9A] the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing aluminum, and

[9B] the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing aluminum.

[10] The semiconductor device of claim 1, wherein

[10A] the first and second MIS transistors are nMIS transistors, and

[10B] the first and second high dielectric constant insulating films contain lanthanum.

[11] The semiconductor device of claim 10, wherein

[11A] the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing lanthanum, and

[11B] the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing lanthanum.

[12] The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.

[13] The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.

[14] The semiconductor device of claim 1, wherein the first and second gate electrodes are made of an identical material.

[15] The semiconductor device of claim 1, wherein an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor.