

The disadvantage of the type I hybrid ARQ is that the overhead due to the extra parity-check digits for error correction must be included in each transmission or retransmission regardless of the channel error rate. When the channel is quiet, this represents a waste. However, the type II hybrid ARQ removes this disadvantage. It is an adaptive scheme. This scheme is particularly attractive for high-speed data communication systems where round-trip delay is large and error rate is nonstationary such as satellite communication systems.

Various hybrid ARQ schemes and their analysis can be found in References 17 to 29.

15.5 CLASS OF HALF-RATE INVERTIBLE CODES

In a type II hybrid ARQ system, C_1 is chosen as a half-rate invertible code. The invertible property facilitates the data recovery process. During a retransmission, if the parity block $q(\mathbf{u})$ is successfully received (no errors being detected), the message \mathbf{u} can be reconstructed from $q(\mathbf{u})$ by a simple inversion process rather than by a more complicated decoding process. The inversion process also reduces the frequency of retransmission. For example, if the received message $\bar{\mathbf{u}}$ contains more than t errors and the received parity block $\bar{q}(\mathbf{u})$ is error-free, the decoding process based on $(\bar{q}(\mathbf{u}), \bar{\mathbf{u}})$ would not be able to recover the message \mathbf{u} . Hence, another retransmission would be required. However, taking the inverse of the error-free parity block $\bar{q}(\mathbf{u})$, we will be able to recover \mathbf{u} and thus avoid another retransmission.

In the following, a class of half-rate invertible block codes will be presented and we will show that inversion can be accomplished by a linear sequential circuit.

Let C be an (n, k) cyclic code with $n - k \leq k$. Let $g(X)$ be the generator polynomial of C with the form

$$g(X) = 1 + g_1X + g_2X^2 + \cdots + g_{n-k-1}X^{n-k-1} + X^{n-k}.$$

Let

$$v(X) = v_0 + v_1X + v_2X^2 + \cdots + v_{n-1}X^{n-1}$$

be a code polynomial. In systematic form, the k leading high-order coefficients $v_{n-k}, v_{n-k+1}, \dots, v_{n-1}$ are identical to k information digits, the $n - k$ low-order coefficients $v_0, v_1, \dots, v_{n-k-1}$ are parity-check digits. Consider the set of those code vectors in C whose $2k - n$ leading high-order components $v_{2(n-k)}, v_{2(n-k)+1}, \dots, v_{n-1}$ are zeros. There are 2^{n-k} such code vectors in C . If the $2k - n$ high-order zero components are removed from these code vectors, we obtain a set of 2^{n-k} vectors of length $2(n - k)$. These vectors form a half-rate $(2n - 2k, n - k)$ shortened cyclic code C_1 (see section 4.7). This shortened cyclic code has at least the same error-correcting capability as C . We have shown in Section 4.7 that the encoding and decoding of C_1 can be accomplished by the same circuits (or with a slight modification) as employed by C .

Next, we show that the shortened cyclic code C_1 has the invertible property.

Let

$$u(X) = u_0 + u_1X + \cdots + u_{n-k-1}X^{n-k-1}$$