

A DSP-BASED ALTERNATIVE TO DIRECT CONVERSION RECEIVERS FOR DIGITAL MOBILE COMMUNICATIONS

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ABSTRACT

Direct conversion, a one-step quadrature demodulation of the complex envelope, has several advantages. Recent direct conversion papers, though, have highlighted significant design problems. The present paper presents an alternative architecture, which features digitization at a low IF, rather than at baseband. By allocating the functions of frequency translation and precision signal manipulation to RF and DSP technologies, respectively, it eliminates the problems inherent to direct conversion, while retaining high adjacent channel rejection. The paper also develops a model for bandpass A/D conversion using conventional parameters, such as noise figure and dynamic range.

1 INTRODUCTION

The next generation of mobile radio will employ digital transmission. Its flexibility of format and relative immunity to noise make it more attractive than its traditional analog

counterparts. However, digital transmission is also less tolerant of distortion, which makes receiver design difficult with conventional analog circuitry. Digital signal processing (DSP) technology is a good alternative, since it offers ever-increasing computing power with decreasing electrical power consumption. An exciting development is the integration of RF and DSP technologies, as transceiver functions are converted, one by one, from analog to DSP based solutions.

Direct conversion, or homodyne, architectures (Figure 1) have been investigated in some detail recently [1,2]; in fact, simplified versions have been available for some time for low speed FSK radiopaging. By mixing the incoming signal with sine and cosine outputs of a local oscillator (LO) at the desired carrier frequency, the direct conversion receiver achieves a one-step conversion to baseband, where the real and imaginary components of the complex envelope are available for digitization. Apart from simplicity, direct conversion advantages include a wide tuning range and high selectivity (though both are limited by the dynamic range of the receiver) Unfortunately, it has a number of drawbacks for digital transmission. First, amplitude and phase imbalances between the two branches distort the

signal, thereby increasing the bit error rate (BER). Second, analog lowpass filters sharp enough to reject adjacent channels also distort the desired signal. Third, carrier feedthrough [1] and $1/f$ noise [2] in the mixers, and bias in the filters and in the sample and hold circuit all contribute to an unpredictable and time varying DC offset in the recovered components. Finally, quantization noise at typical sampling rates demands a full 16-bit converter.

This paper describes a DSP-based alternative architecture - the digital conversion receiver. Its overall function is similar to that of the direct conversion receiver: it converts the received RF signal to digitized samples of the real and imaginary components of the complex envelope. However, it allocates functions differently, with high frequency, low complexity processing performed in analog technology, and precision low speed processing performed in DSP. As a result, the digital conversion receiver eliminates all the problems cited above for direct conversion, and it does so with fewer RF components (in its single conversion format). In addition, it acts as a matched filter front end for the modem. Its principal disadvantage at present is the limited tuning range when the RF portion is implemented in single conversion form. However, increasing DSP speed or cascading DSP chips can extend the tuning range; alternatively, a double conversion receiver eliminates the problem. As a design example, we use transmission of 32 kbps QPSK through a 25 kHz mobile channel. The principles also apply, with some parameter changes, to transmission of 48.6 kbps $\pi/4$ QPSK in 30 kHz channels.

Section 2 describes the overall structure of the receiver. Section 3 describes the algorithms of the digital quadrature demodulator. Section 4 addresses issues of sensitivity and dynamic range, for comparison with direct conversion.

2 THE DIGITAL CONVERSION RECEIVER

The digital conversion receiver consists essentially of analog frequency translation to a low intermediate frequency (IF) (480 kHz for our design example), followed by digitization and DSP-based extraction of the complex envelope components. Figure 2 shows single and double conversion configurations, which require one or two LOs, respectively.

The digital quadrature demodulator is described in detail in Section 3. In effect, it provides an all-DSP equivalent of the direct

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CH2827-4/90/0000-2024 \$1.00 © 1990 IEEE

conversion functions of Figure 1, though applied to the low IF, rather than the original carrier. Among its advantages are the following. First, its digital implementation eliminates phase and gain imbalance, thereby removing a significant source of signal distortion. Second, digitization at IF eliminates DC offset problems: any bias in the sample and hold circuit is cancelled in subsequent processing; 1/f noise is negligible at IF; and there is no carrier feedthrough. Third, the high sampling rate reduces quantization noise (Section 4). Fourth, the effects of any nonlinearity in the A/D are limited to odd order terms, in contrast to the direct conversion receiver, which digitizes at baseband and therefore experiences terms of all orders. And fifth, the digital lowpass filters also act as matched filters, for a combined operation of adjacent and neighbouring channel rejection, noise suppression and precision signal shaping.

Immediately prior to digitization, the spectra are as shown in Figure 3a. The desired signal occupies a narrow range of frequencies of width W_d centered at f_q (480 kHz in our example). The asymmetry about f_q shown in the figure is only to aid in distinguishing the images in positive and negative frequencies, and has no physical basis. In principle, the bandwidth W_q can be almost $2f_q$ without harm to the desired signal, since filtering in the digital quadrature demodulator rejects unwanted frequencies. This greatly simplifies the design of an analog IF filter. In practice, the bandwidth W_q is limited by the computational power of the DSP, and by the dynamic range, which limits the total power of undesired signals. We have built a digital conversion receiver in which the stop band of the analog IF filter begins 175 kHz away from the 480 kHz center. Larger bandwidths are possible, if adjacent channel rejection is not required to be in the range 70-80 dB.

In a single conversion configuration (Figure 2a), the RF portion of the receiver mixes the incoming signal at f_{rf} directly down to f_q . Clearly, the bandwidth W_{rf} of the RF filter prior to the mixer cannot exceed $2f_q$ if interfering signals are not to overlap the desired signal at the IF. This poses two problems: the selectivity required of the RF filter (960 kHz in our example), and the limitation on tuning range if the RF filter has a fixed center frequency. In its favour, though, is simplicity. If we compare it to direct conversion, the facts of no splitter, one mixer instead of two, and no phase and gain imbalance compensate for the more difficult RF filter design. Moreover, increases in DSP speed will permit higher values of f_q , and consequently increases in RF bandwidth and tuning range. A pipelinable architecture has also been proposed [3] for digital quadrature demodulation, which will further increase f_q . It is easy to foresee f_q in the range 2 - 4 MHz, to the point where single conversion is sufficient for an MSAT receiver.

The double conversion configuration (Figure 2b) is a conventional superheterodyne design. Tuning range restrictions disappear, and it is the filter at f_{if} which limits the bandwidth to $2f_q$, a relatively easy design. It is more complex than single conversion, and has reduced sensitivity and dynamic range, but it retains the benefits of digital quadrature demodulation.

3 DIGITAL QUADRATURE DEMODULATOR

The digital quadrature demodulator (quad demod) provides DSP-based recovery of the complex envelope of the desired signal centered at f_q . Functionally, it appears as shown in Figure 4. Complex sampling techniques themselves are not new, of course, but we have incorporated the matched filtering operation in the quad demod. We also show how bandwidth, adjacent channel rejection and processing power are related.

Careful selection of the sampling rate f_s is necessary. If $f_s = 2f_q/L$, where L is odd, then the images due to sampling are equispaced, and the normal and conjugate images are interleaved (as required for recovery of both components of the complex envelope). We select the image at $f_{q2} = f_q/L$ for quadrature demodulation, and further restrict f_s to obtain

$$f_s = 4f_q/L, \quad f_{q2} = f_q/L, \quad f_3 = 4f_{q2} \quad (1)$$

which will simplify the down conversion. Since the image spacing is $f_s/2$, and because neighbouring images must not overlap the desired channel, the stop band of the analog IF filter preceding the A/D is defined by $f_q \pm W_q/2$, where

$$W_q/2 = (f_s - W_d)/2 = (4f_q/L - W_d)/2 \quad (2)$$

The images resulting from sampling are shown in Figure 3b.

Next, the entire spectrum is shifted left, to move the image centered at f_{q2} into the window of the lowpass filters, by multiplying with the "numeric LO" output $\exp(-j2\pi f_{q2} t)$. Since the output is sampled, it becomes

$$\begin{aligned} \exp(-j2\pi f_{q2} k/f_s) &= \exp(-j\pi k/2) \\ &= (1, j, -1, -j, 1, j, -1, -j, \dots) \end{aligned} \quad (3)$$

Therefore no multiplications are required, and down conversion becomes a matter of alternating I and Q channels and alternating the sign.

The lowpass filters, which double as matched filters, can be combined with the downconversion, forming the equivalent complex filter

$$\begin{aligned} \dots, h(-4), -jh(-3), -h(-2), jh(-1), \\ h(0), jh(1), -h(2), -jh(3), \dots \end{aligned} \quad (4)$$

where $h(k)$ is the original lowpass filter unit pulse response. In principle, 4 sets of filter

coefficients are required, one for each phase, though they are trivially related. However, their outputs can be decimated to a rate f_{s2} , since the desired channel has a much lower bandwidth than W_q . Define the decimation factor M:

$$M = f_s / f_{s2} \quad (5)$$

If M is a multiple of 4, then only one set of filter coefficients is required, and combined down conversion and filtering reduces to a single filtering operation, yielding

$$I = f_{s2} / R_s = 4 f_q / (L M R_s) \quad (6)$$

samples per symbol, where R_s is the symbol rate of the modulation.

To determine the computational load, it is easiest to consider the lowpass filters as a single real filter acting on a complex input. Since the input samples always have one component equal to zero, an N-point filter needs a computation rate of

$$C = N f_{s2} = 4 N f_q / (L M) \quad (7)$$

multiply-adds per second.

A guide to the out-of-band attenuation properties of the filter is the number of symbols spanned by its impulse response:

$$N_s = N R_s / f_s = N L R_s / (4 f_q) \quad (8)$$

The tradeoff between digital filter selectivity and analog IF filter selectivity, as limited by computation rate, can be determined by combining (2), (7) and (8):

$$N_s = R_s M C / W_q^2 \quad (9)$$

after the approximation $W_d \ll W_q$. Similarly, combining (7) and (8) gives the incoming center frequency in terms of computation rate and selectivity:

$$f_q = \frac{LM}{4} \sqrt{\frac{C R_s}{N_s}} \quad (10)$$

Our processor can supply 15.36 Mips (where an instruction is a multiply-add). We chose $L = 5$ and $M = 6$, to give the following specifications:

$$f_q = 480 \text{ kHz} \quad f_s = 384 \text{ kHz}$$

$$I = 4 \text{ samples/symbol} \quad N = 240 \text{ points}$$

$$N_s = 10 \text{ symbols} \quad (11)$$

Filter selectivity is extremely good. A Kaiser window design of the square root raised cosine matched filter gave the results in Figure 5, for a Kaiser parameter $\alpha = 4$. Attenuation is 75 dB by the middle of the adjacent channel, and is about 93 dB a few channels away.

4 SENSITIVITY AND DYNAMIC RANGE

4.1 Framework for Analysis

Two of the most common measures of receiver performance are sensitivity and dynamic range.

Here we evaluate these two parameters for the digital conversion receiver with single conversion RF. Included in the analysis is a model of an idealized bandpass A/D converter.

Sensitivity, the minimum power of the desired signal, depends on the modulation. As a design example, we assume 32 kbps QPSK, coherently detected, carrying digital speech. Threshold for digital speech usually occurs in the vicinity of a 10^{-2} BER (bit error rate). From [4], the minimum value γ_{bm} of the ratio of energy per bit to N_o , the one sided noise PSD (power spectral density), is 4 dB (factor of 2.5). In turn, N_o equals kT_{rec} , where k is Boltzmann's constant, and T_{rec} is the noise temperature of the receiver. Thus the sensitivity is related to noise temperature by

$$P_{min} = \gamma_{bm} R_b k T_{rec} \quad (12)$$

Maximum signal power P_{max} is conventionally determined by a two tone test, and is that value at which the IM products have power equal to P_{min} . The SFDR (spurious free dynamic range) is defined [5] as the ratio

$$SFDR = P_{max} / P_{min} \quad (13)$$

when expressed in dB.

4.2 Model of Ideal Bandpass A/D Converter

The output of the bandpass A/D converter is a number, not a voltage. Nevertheless, it can be characterized by noise figure, dynamic range, etc, like other RF circuit elements. First, we assign it a power gain. Normally, the high impedance input is shunted by a low impedance matching resistor R_q , which we consider part of the bandpass A/D. By convention, DSP analysis assumes a 1 ohm resistor, so that watts equals volts squared. If the A/D output is scaled to be numerically equal to the voltage at the input, then the power gain of the A/D equals its input resistance R_q .

The A/D has n bits, spanning an input voltage range $[-V_q, V_q]$. In our idealized model, we assume that it has only two effects on the input: quantization and limiting.

Quantization adds noise. As usual in quantization analysis, we assume the quantization error to be independent from sample to sample, and uniformly distributed with variance

$$\sigma_q^2 = V_q^2 / 3 \cdot 2^{2n} \quad (14)$$

at the output. If the sampling rate is f_s , then the two sided noise PSD at the input is given by

$$\frac{N_{oq}}{2} = \frac{1}{3f_s R_q} \frac{V_q^2}{2^{2n}} \quad (15)$$

and the noise temperature and noise figure are, respectively

$$T_{oq} = N_{oq} / k \quad F_q = 1 + N_{oq} / kT_o \quad (16)$$

where $T_o = 290$ K. Note that noise density decreases inversely with sampling rate, as discussed in [3]. Thus there is a benefit to the forced high rate sampling in our digital quadrature demodulator: quantization noise power at the output of a matched filter is reduced by a factor W_d/f_s , where W_d is the noise bandwidth of the filter.

The minimum detectable signal level for the quantizer alone is obtained by substituting (16) into (12):

$$P_{\min q} = \gamma_{bm} R_b N_{oq} = \frac{2\gamma_{bm} R_b}{3f_s R_q} \frac{V_q^2}{2n} \quad (17)$$

For 32 kbps, sampling at 384 kHz, and 16 bit conversion, we have

$$P_{\min q} = (V_q^2/R_q)_{dB} - 104.90 \text{ dB} \quad (18)$$

If we further assume $R_q = 50$ ohm and $V_q = 3$ volt, then the minimum detectable input signal level $P_{\min q}$ at the A/D converter is -82.3 dBm.

The SFDR depends on the IM products generated in a two-tone test. If the input power is P_q , then each tone has amplitude $\sqrt{P_q/R_q}$. An equivalent representation of the input signal is

$$\tilde{v}_q(t) = 2\sqrt{P_q/R_q} \cos(2\pi f_m t) \cos(2\pi f_c t) \quad (19)$$

where f_m is half the frequency separation of the tones, and f_c is the average frequency of the tones.

To determine IM products, we model the A/D as a bandpass limiter. From [6], the envelope nonlinearity equivalent to the limiter is

$$g(v) = \begin{cases} v, & |v| \leq V_q \\ \frac{2V_q}{\pi} \left((1 - (V_q/v)^2)^{1/2} + (v/V_q) \sin^{-1}(V_q/v) \right) \text{sgn}(v), & |v| > V_q \end{cases} \quad (20)$$

From (19), the modulation at the output of the A/D is given by

$$g(2\sqrt{P_q/R_q} \cos(2\pi f_m t)) \quad (21)$$

Expansion of the modulation in a Fourier series gives the fundamental and IM products of the two tone test. Numerical evaluation of the fundamental (at f_m) and 3rd order (at $3f_m$) components gives the results shown in Figure 6. The IM products are zero for input power P_q up to $V_q^2/4R_q$. Beyond this point, they increase dramatically.

For SFDR we need the two tone input power at which the power in IM products equals $P_{\min q}$. From Figure 6, it is clear that the maximum signal power is just $V_q^2/4R_q$, to a good approximation. From (18), therefore, the SFDR of the bandpass A/D is

$$\text{SFDR} = \frac{V_q^2}{4R_q P_{\min q}} = \frac{3 f_s}{2 R_b \gamma_{bm}} 2^{2(n-1)} \quad (22)$$

For the parameters used earlier ($f_s = 384$ kHz, $R_b = 32$ kbps, QPSK, 16 bits), we have an SFDR of 98.90 dB.

A real A/D is not a perfect limiter, of course, and slight nonlinearities further reduce the dynamic range. Nevertheless, the above analysis of an idealized A/D serves as a useful bound. In any case, we shall see below that the A/D is unlikely to be the controlling factor in dynamic range analysis.

4.3 Receiver Analysis

In this section we obtain sensitivity and dynamic range for the full digital conversion receiver in its single conversion form (Figure 2b).

Components with specifications listed in the first three columns of Table 1 are readily available. The first bandpass filter is a dielectric resonator, the mixer is commercially available, the second bandpass filter is built from discrete components, and the IF amplifier is commercially available.

The spurious free dynamic range (SFDR) of the individual components depends on their maximum allowable input powers. For an amplifier we use

$$P_{ip} = P_{1dB} + 10\text{dB} \quad (23)$$

where P_{ip} is the third order output intercept point and P_{1dB} is the 1 dB output compression point. For the mixer, the 1 dB

compression point is taken as the value at which the IF power deviates from the linear conversion loss by 1 dB. The maximum input power is then given by

$$P_{\max} = \frac{2}{3} (P_{ip} - G) + \frac{1}{3} P_{\min} \quad (24)$$

where G is the gain, P_{\min} is the minimum detectable signal level, as in (12), and all quantities are in dB. In the case of the quantizer, the table entry is the maximum power, rather than the 1 dB point. The component SFDRs, calculated as

$$\text{SFDR} = P_{\max} - P_{\min} \quad (25)$$

are listed in Table 1.

The overall receiver performance can be calculated using conventional analysis [e.g. 5]. Component noise temperatures referred to the receiver input are shown in Table 1. We obtain a receiver noise figure $NF = 6.9$ dB, with a gain of 58 dB (to the numeric output of the A/D), and a receiver sensitivity of -117.2 dBm.

To determine the dynamic range of the receiver as a whole, we approximate its maximum input power by referring all component maximum powers to the receiver input, and selecting the minimum value (see Table 1). The result is -54.0 dBm, stemming from the IF amplifier, for a receiver dynamic range of 63.2 dB.

It is the IF amplifier, rather than the A/D and digital quad demod, that limits performance. It contributes over 50% of the receiver noise (compared with 24% from quantization), and its P_{max} referred to the input is 30 dB lower than that of the A/D.

Design for a digital conversion receiver therefore centers on improving the linearity of the IF amplifier. This contrasts with conventional receivers, in which the emphasis is on the crystal filter's nonlinearity and inband ripple and delay variation. With better IF amplifiers, the digital conversion receiver could achieve an SFDR on the order of 80 dB, which is far better than the typical 60 dB when using analog circuitry with a crystal filter.

5 CONCLUSIONS

This paper has described a digital conversion receiver featuring digitization at a low intermediate frequency, followed by DSP-based extraction of the complex envelope components. It eliminates the problems of DC offset and phase and gain imbalance encountered in analog direct conversion designs. The sensitivity of the digital conversion receiver is comparable to other designs, and its dynamic range is determined by the analog IF amplifier, rather than the A/D converter and DSP.

The paper also provided a model for the bandpass A/D converter that can be included in conventional receiver design calculations.

In the future, with the increased speed of DSP chips, we would anticipate that more receiver systems will incorporate DSP-based architectures.

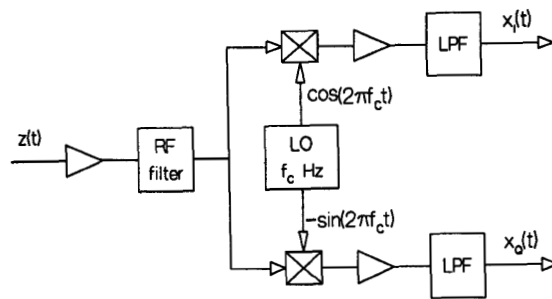


Fig 1. The Direct Conversion Receiver

ACKNOWLEDGEMENT

This work was funded by the Science Council of British Columbia.

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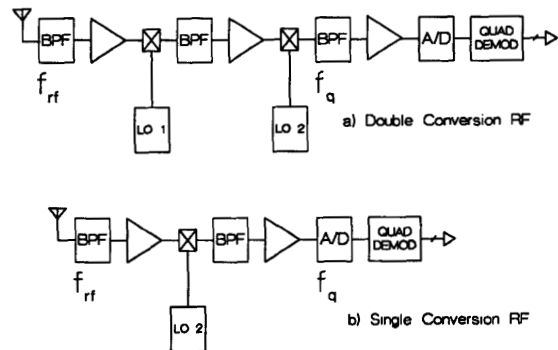


Fig 2. The Digital Conversion Receiver

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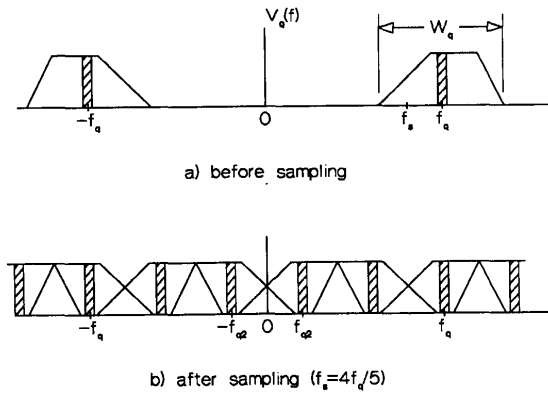


Fig 3. Images in the Quadrature Demodulator

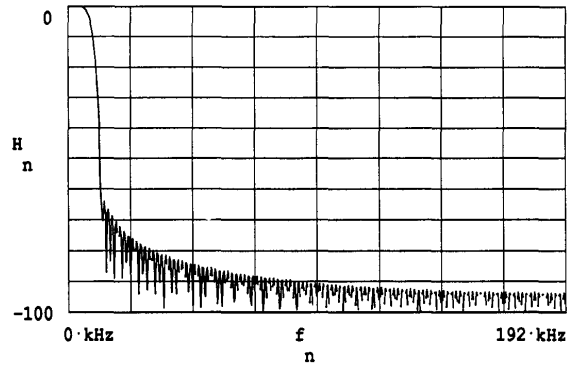


Fig 5. Adjacent Channel Rejection in Root Nyquist Filter

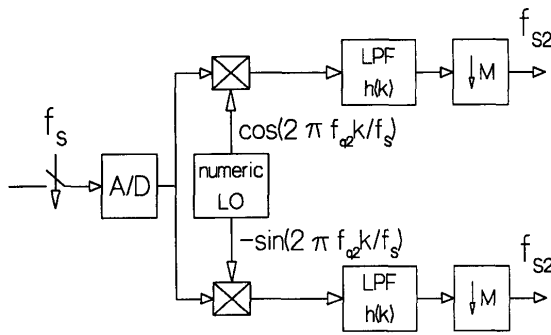


Fig 4. Inside the Digital Quad Demod

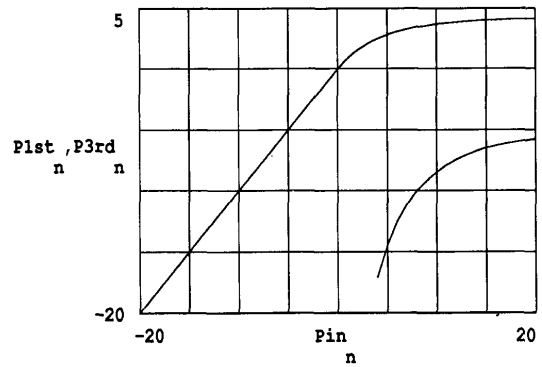


Fig 6. Two Tone Test of A/D, First and Third Order Components

	Gain (dB)	Noise Fig (dB)	Compress Pt (dBm)	Component SFDR (dB)	T at Rx input (K)	Pmax at Rx input (dBm)
RF Amp	10	2	10	91.5	170	-35.8
BPF 1	-1	1	20	107.9	7	-32.9
Mixer	-7	7	0	90.6	146	-37.3
BPF 2	-1	1	20	107.9	47	-24.9
IF Amp	40	7	10	65.9	924	-54.0
A/D	17	42.6	16.5	98.8	419	-24.5

Table 1. Component Data for Digital Conversion Receiver

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