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(54) **METHOD FOR IMPROVING SELECTIVITY OF EPI PROCESS**

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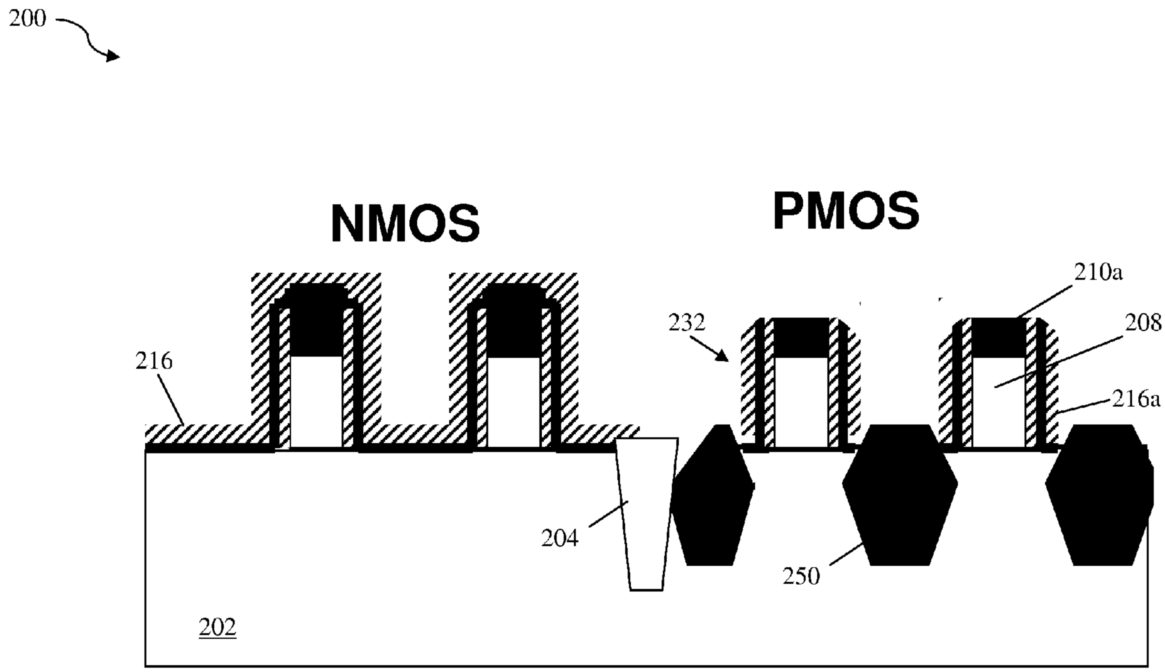
(57) **ABSTRACT**

The present disclosure provides a method of fabricating a semiconductor device that includes providing a semiconductor substrate, forming a gate structure over the substrate, forming a material layer over the substrate and the gate structure, implanting Ge, C, P, F, or B in the material layer, removing portions of the material layer overlying the substrate at either side of the gate structure, forming recesses in the substrate at either side of the gate structure, and depositing a semiconductor material in the recesses by an expitaxy process.



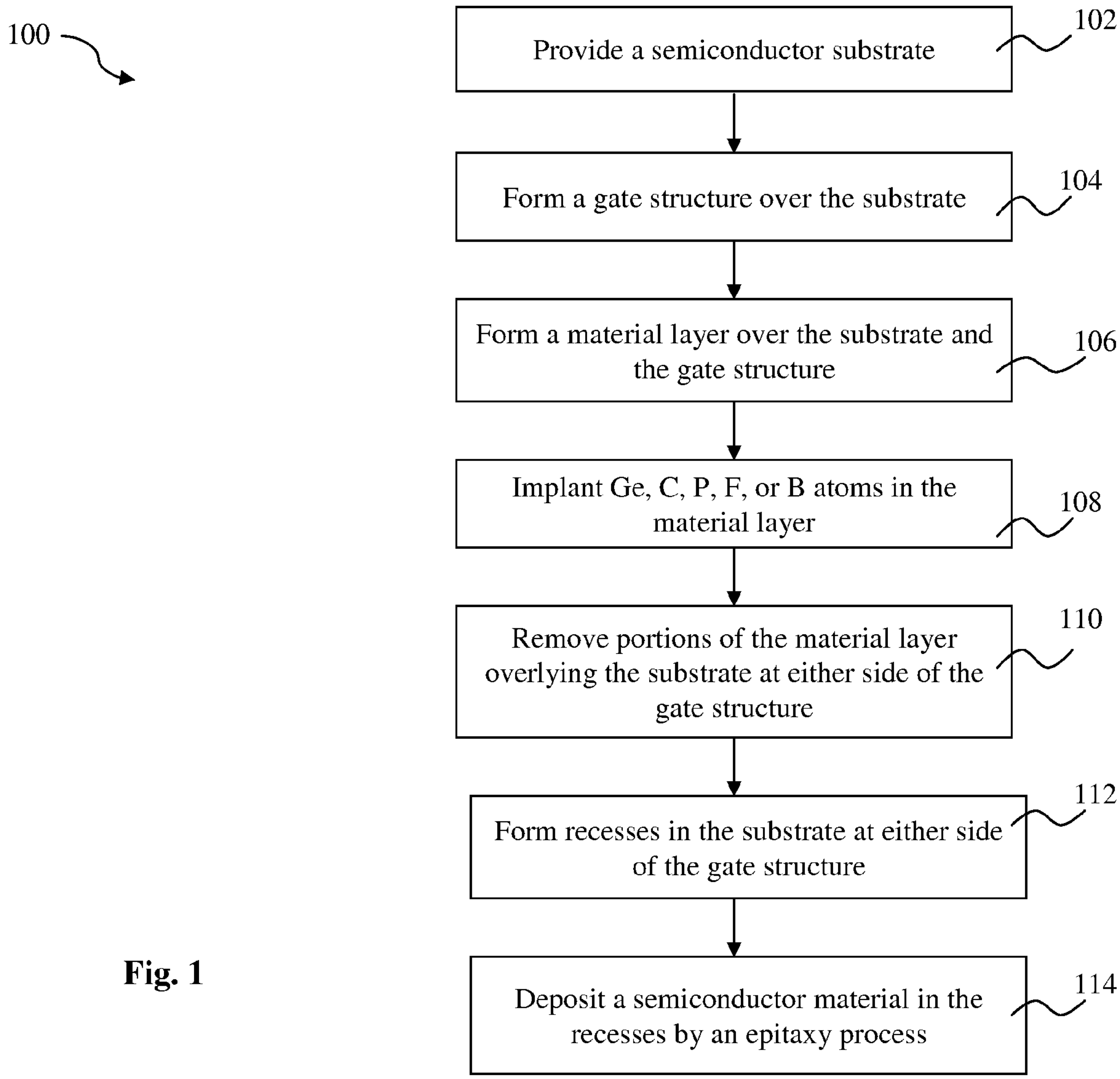

100
Provide a semiconductor substrate
102
Form a gate structure over the substrate
104
Form a material layer over the substrate and the gate structure
106
Implant Ge, C, P, F, or B atoms in the material layer
108
Remove portions of the material layer overlying the substrate at either side of the gate structure
110
Form recesses in the substrate at either side of the gate structure
112
Deposit a semiconductor material in the recesses by an epitaxy process
114

Fig. 1

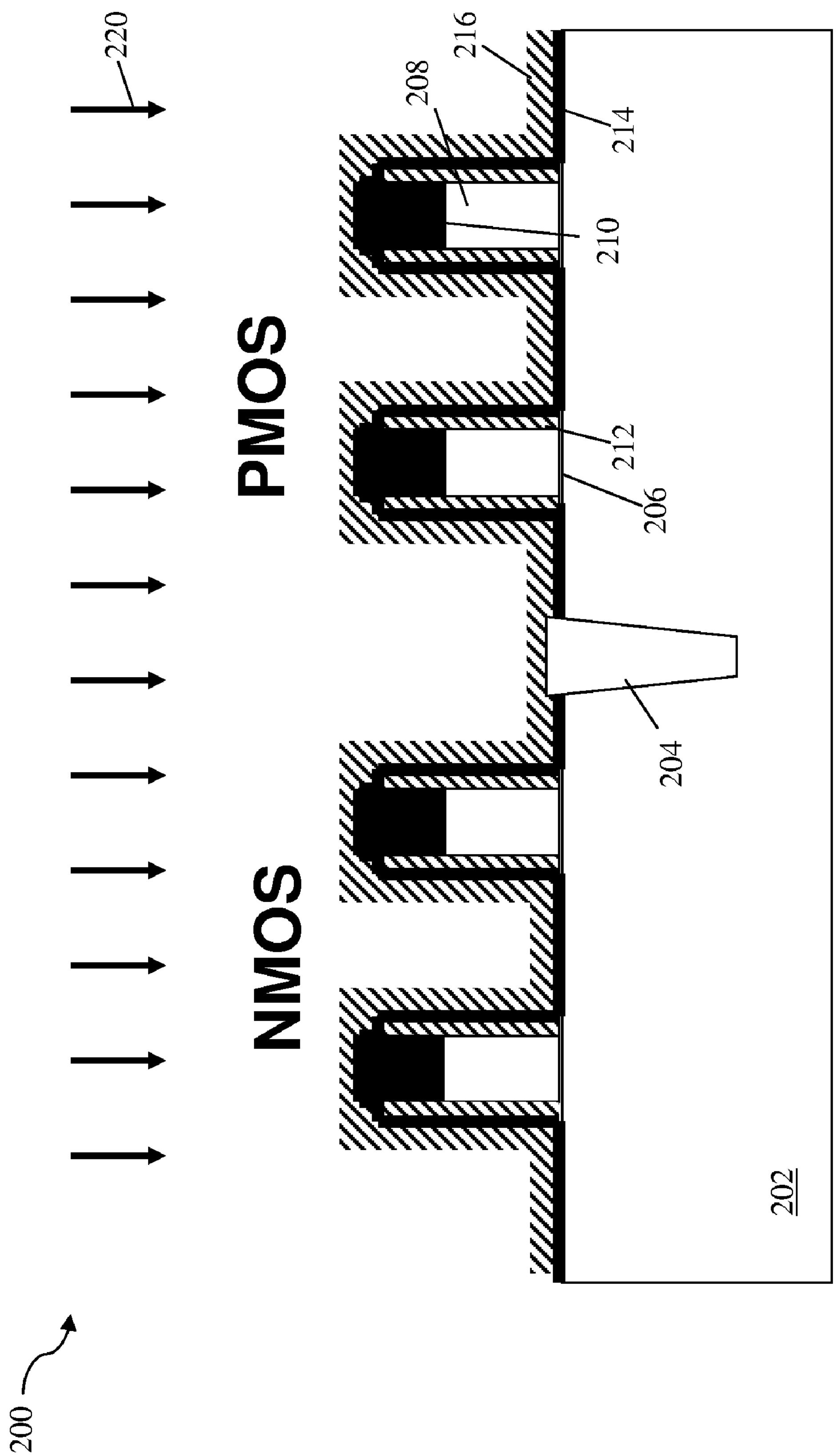


Fig. 2

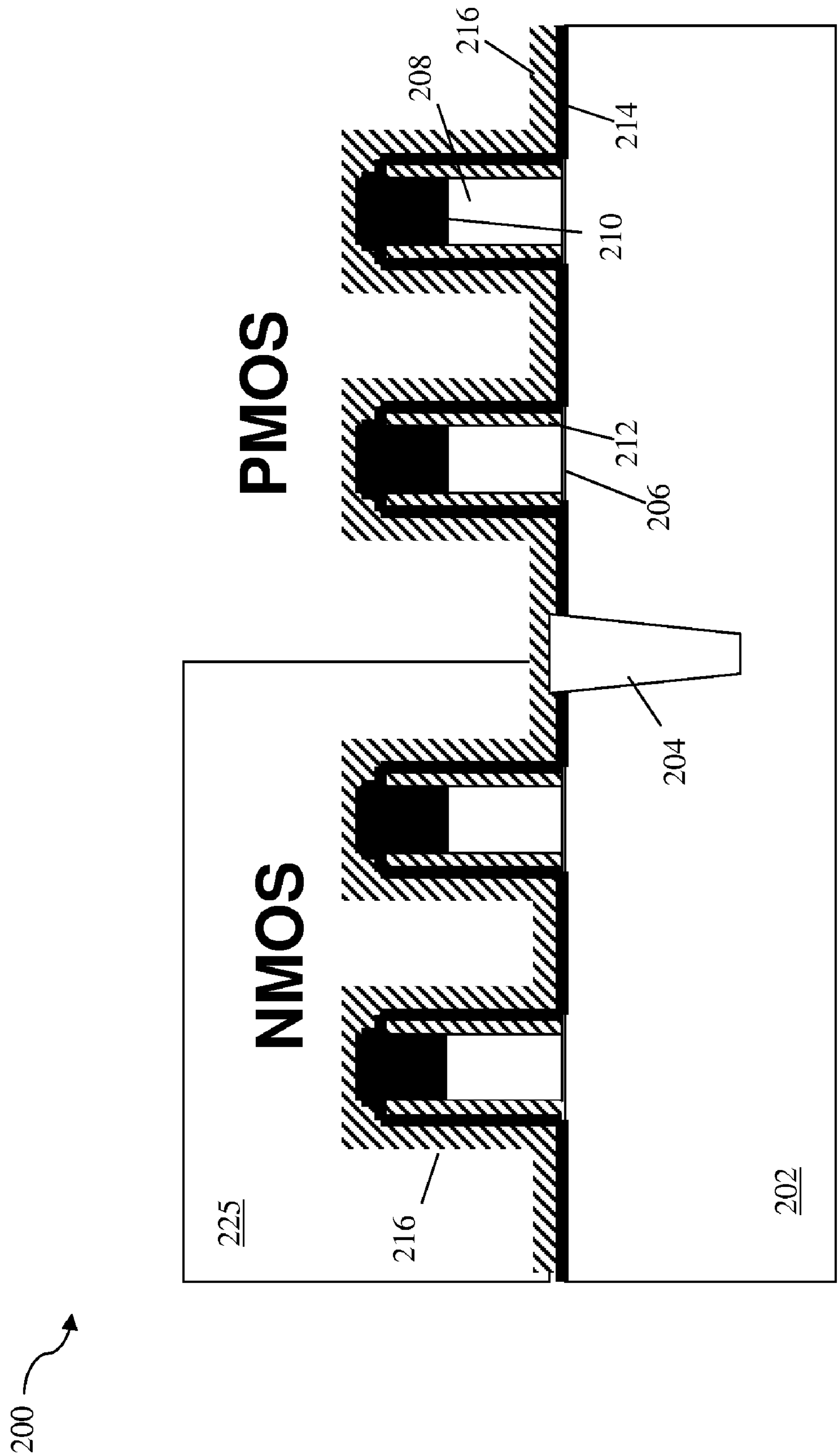


Fig. 3

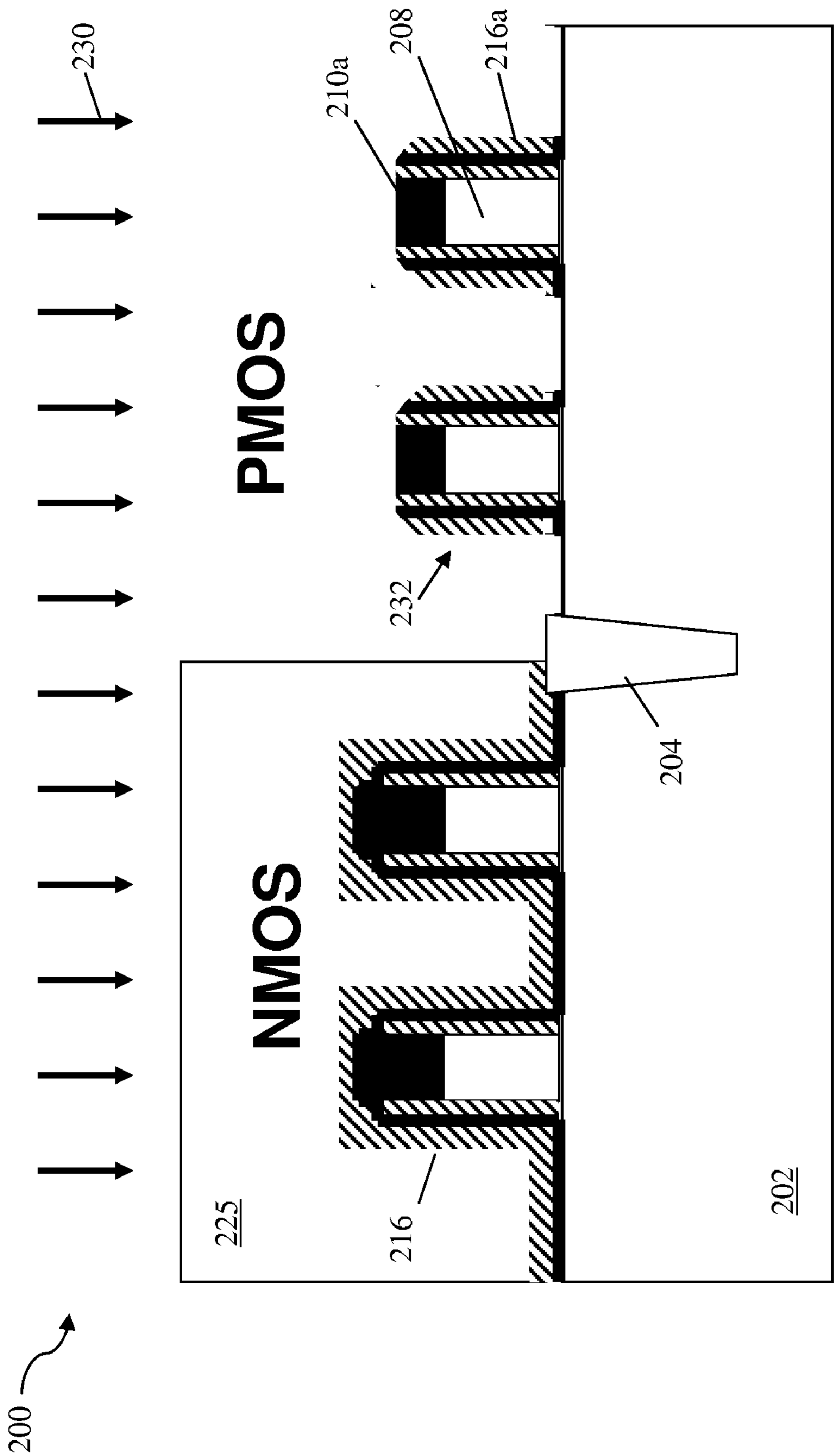


Fig. 4

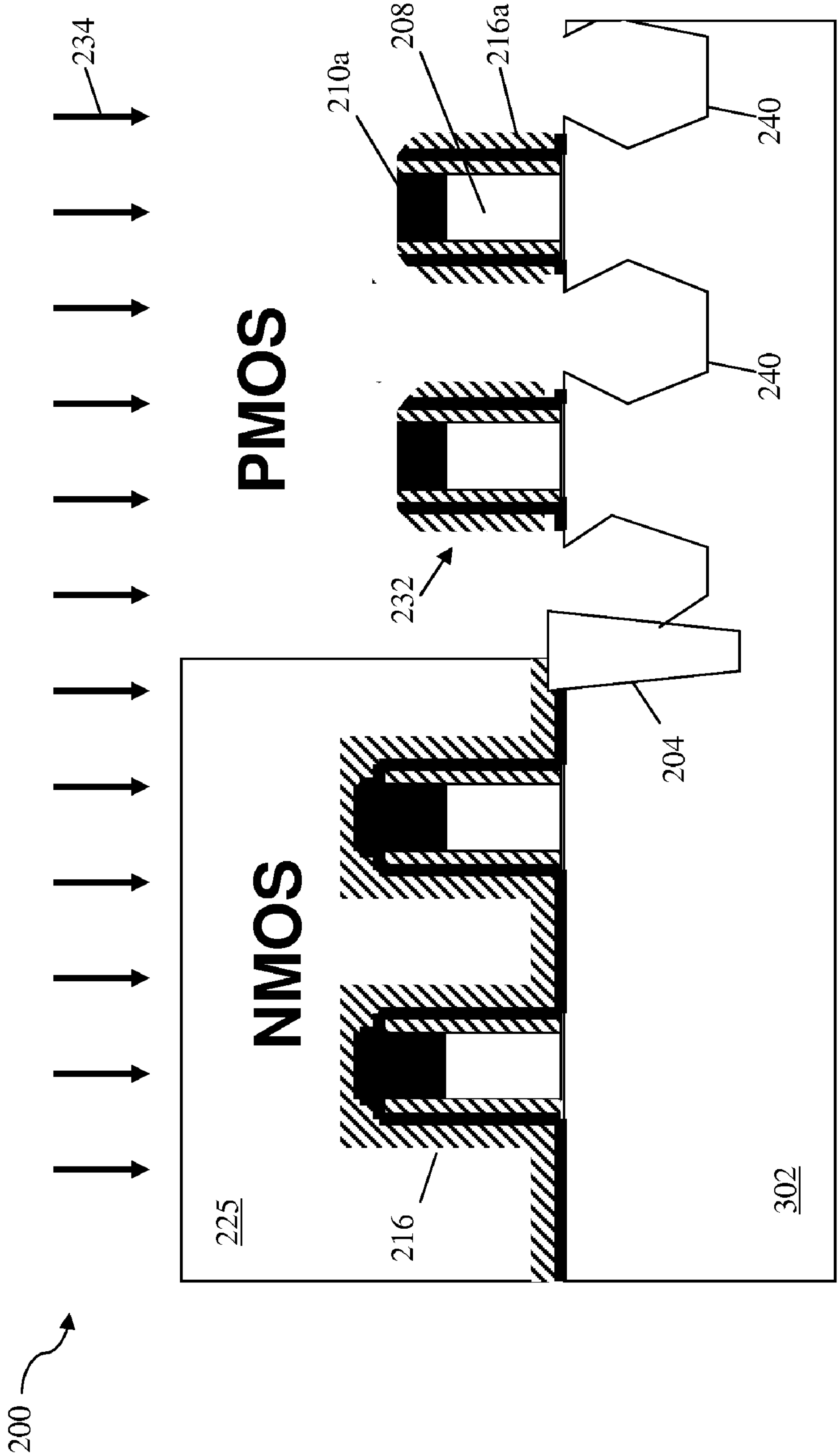


Fig. 5

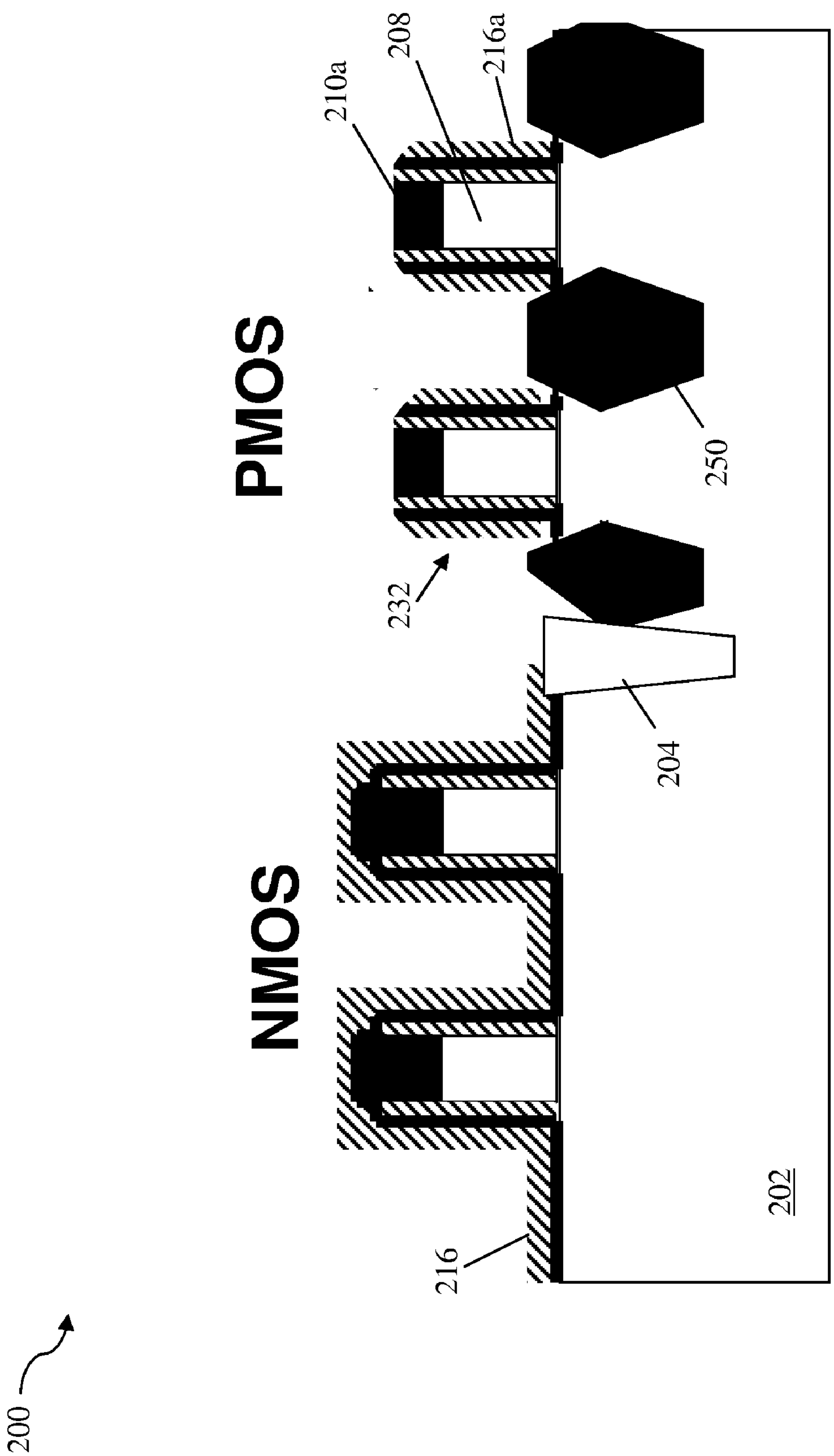


Fig. 6

METHOD FOR IMPROVING SELECTIVITY OF EPI PROCESS

BACKGROUND

[0001] When a semiconductor device such as a metal-oxide-semiconductor field-effect transistors (MOSFETs) is scaled down through various technology nodes, high-k dielectric material and metal are adopted to form a gate stack. In addition, a strained substrate using epitaxy (epi) silicon germanium (SiGe) may be used to enhance carrier mobility and improve device performance. However, current techniques to form these strained structures have not been satisfactory in all respects. For example, an etchant gas may be used with the epi process to maintain selectivity between the spacer and the substrate which can adversely impact the SiGe growth rate.

SUMMARY

[0002] One of the broader forms of an embodiment of the present invention involves a method of fabricating a semiconductor device. The method includes providing a semiconductor substrate; forming a gate structure over the substrate; forming a material layer over the substrate and the gate structure; implanting one of Ge, C, P, F, and B in the material layer; removing portions of the material layer overlying the substrate at either side of the gate structure; forming recesses in the substrate at either side of the gate structure; and depositing a semiconductor material in the recesses by an expitaxy process.

[0003] Another one of the broader forms of an embodiment of the present invention involves a method of fabricating a semiconductor device. The method includes providing a semiconductor substrate having a first region and a second region; forming first and second gate structures over the first and second regions of the substrate, respectively; forming a silicon nitride layer over the substrate and the first and second gate structures; performing an implantation process to the silicon nitride layer; protecting the silicon nitride layer overlying the first region of the substrate; removing portions of the silicon nitride layer overlying the second region of the substrate at either side of the second gate structure; forming recesses in the substrate at either side of the second gate structure; and forming a semiconductor material in the recesses, the semiconductor material being different from the semiconductor substrate.

[0004] Yet another one of the broader forms of an embodiment of the present invention involves a semiconductor device. The semiconductor device includes a semiconductor substrate; and a transistor that includes: a gate structure disposed on the substrate, the gate structure including sidewall spacers that are implanted with one of Ge, C, P, F, and B; and source and drain regions disposed in the substrate at either side of the gate structure, the source and drain regions formed of a semiconductor material different from the semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0006] FIG. **1** is a flowchart of a method of fabricating a semiconductor device with strained structures according to various aspects of the present disclosure; and

[0007] FIGS. **2-6** are cross-sectional views of a semiconductor device at various stages of fabrication according to the method of FIG. **1**.

DETAILED DESCRIPTION

[0008] It is to be understood that the following disclosure provides many different embodiments, or examples, for implementing different features of various embodiments. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed. Moreover, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed interposing the first and second features, such that the first and second features may not be in direct contact.

[0009] Referring to FIG. **1**, illustrated is a flowchart of a method **100** of fabricating a semiconductor device with strained structures according to various aspects of the present disclosure. The method **100** begins with block **102** in which a semiconductor substrate is provided. The method **100** continues with block **104** in which a gate structure is formed over the substrate. The method **100** continues with block **106** in which a material layer is formed over the substrate and the gate structure. The method continues with block **108** in which Ge, C, P, F or B atoms are implanted in the material layer. The method **100** continues with block **110** in which portions of the material layer overlying the substrate at either side of the gate structure are removed. The method **100** continues with block **112** in which recesses are formed in the substrate at either side of the gate structure. The method **100** continues with block **114** in which a semiconductor material is deposited in the recesses by an epitaxy process. The discussion that follows illustrates various embodiment of a semiconductor device that can be fabricated according to the method **100** of FIG. **1**.

[0010] Referring to FIGS. **2-6**, illustrated are cross-sectional views of a semiconductor device **200** at various stages of fabrication according to the method **100** of FIG. **1**. It is understood that FIGS. **2-6** have been simplified for the sake of clarity to better understand the inventive concepts of the present disclosure. In FIG. **2**, the semiconductor device **200** includes a substrate **202**. The substrate **202** includes a silicon substrate. In another embodiment, the semiconductor substrate **202** may include an epitaxial layer. For example, the substrate **202** may have an epitaxial layer overlying a bulk semiconductor. The substrate **202** further includes doped regions such as p-wells and n-wells. Furthermore, the substrate **202** may include a semiconductor-on-insulator (SOI) structure such as a buried dielectric layer. Alternatively, the substrate **202** may include a buried dielectric layer such as a buried oxide (BOX) layer, such as that formed by a method referred to as separation by implantation of oxygen (SIMOX) technology, wafer bonding, selective epitaxial growth (SEG), or other proper method. The semiconductor device **200** includes active regions defined in the substrate **202**.

[0011] Various shallow trench isolation (STI) structures **204** are formed in the semiconductor substrate for isolating the various active regions. The formation of STI may include etching a trench in a substrate and filling the trench by insulator materials such as silicon oxide, silicon nitride, or silicon oxynitride. The filled trench may have a multi-layer structure such as a thermal oxide liner layer with silicon nitride filling the trench. In one embodiment, the STI structure may be created using a process sequence such as: growing a pad oxide, forming a low pressure chemical vapor deposition (LPCVD) nitride layer, patterning an STI opening using photoresist and masking, etching a trench in the substrate, optionally growing a thermal oxide trench liner to improve the trench interface, filling the trench with CVD oxide, using chemical mechanical planarization (CMP) to etch back, and using nitride stripping to leave the STI structure.

[0012] One or more operational devices are formed in the active regions. The operational devices include n-type and p-type metal-oxide-semiconductor field-effect transistors (NMOS and PMOS). The operational devices are configured as an array of NMOS devices and an array of PMOS devices. The NMOS and PMOS devices may be fabricated by CMOS technology processing. Accordingly, it is understood that additional processes may be provided before, during, and after the method **100** of FIG. **1**, and that some other processes may only be briefly described herein. Each NMOS and PMOS device includes a gate structure formed on the semiconductor substrate **202**. The gate structure includes a gate dielectric **206** and a gate electrode **208**. The gate dielectric **206** may include silicon oxide, silicon nitride, high-k dielectric, or other suitable material. The high-k dielectric layer may include a binary or ternary high-k film such as HfOx. Alternatively, the high-k dielectric layer **216** may optionally include other high-k dielectrics such as LaO, AlO, ZrO, TiO, Ta2O5, Y2O3, SrTiO3 (STO), BaTiO3 (BTO), BaZrO, HfZrO, HfLaO, HfSiO, LaSiO, AlSiO, HfTaO, HfTiO, (Ba, Sr)TiO3 (BST), Al2O3, Si3N4, oxynitrides, or other suitable materials. The gate dielectric is formed by a suitable process such as an atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), thermal oxidation, UV-ozone oxidation, or combinations thereof.

[0013] The gate electrode **208** may include polysilicon (or poly). For example, silane (SiH_4) may be used as a chemical gas in a CVD process to form the poly. The poly layer may include a thickness ranging from about 400 to about 800 angstrom (A). The gate structure may further include a hard mask layer **210** formed on the gate electrode **208**. The hard mask layer **210** includes silicon oxide. Alternatively, the hard mask layer **210** may optionally silicon nitride, silicon oxynitride, and/or other suitable dielectric materials, and may be formed using a method such as CVD or PVD. The hard mask layer **210** may include a thickness ranging from about 100 to about 400 angstrom (A).

[0014] The semiconductor device **200** includes an offset spacer **212** formed on each sidewall of the gate structures. The offset spacer **212** includes silicon nitride and has a thickness ranging from about 4 to about 6 nm. The offset spacer **212** may be formed by CVD, PVD, ALD, plasma enhanced CVD (PECVD), or other suitable technique. An ion implantation process may be performed to form lightly doped source/drain regions (LDD) in the substrate **202**. The LDD regions (not shown) are aligned with the offset spacer **212**. The ion implantation process may utilize p-type dopants (e.g., B or In) for the PMOS devices and n-type dopants (P or As) for the NMOS devices.

[0015] The semiconductor device **200** further includes an oxide layer **214** formed over the substrate **202** and the gate structures. The oxide layer **214** may be formed by CVD, PVD, ALD, or other suitable technique. The oxide layer **214** includes a thickness ranging from about 2 to about 4 nm. The semiconductor device **200** further includes a cap layer **216** formed over the oxide layer **214**. The cap layer **216** may be formed of silicon nitride (Si3N4). The cap layer **216** may be formed by CVD, PVD, ALD, or other suitable technique. The cap layer **216** includes a thickness ranging from about **20** to about **30** nm. In the present embodiment, the cap layer **216** has a thickness of about 25 nm. It should be noted that the pad oxide layer **214** may be omitted in some embodiments as will be explained later.

[0016] An implantation process **220** is performed on the cap layer **214**. The implantation process **220** implants Ge, C, P, F, or B atoms in the cap layer **214**. In an embodiment, the implantation process **220** implants Ge utilizing an implant energy of about 5 KeV and a dosage of about 5E14 atoms/cm^2. In another embodiment, the implantation process **220** implants C utilizing an implant energy of about 5 KeV and a dosage of about 1E15 atoms/cm^2. In other embodiments, the implantation process **220** implants P utilizing an implant energy of about 5 KeV and a dosage of about 1E15 atoms/cm^2. In yet another embodiment, the implantation process **220** implants F utilizing an implant energy of about 5 KeV and a dosage of about 1E15 atoms/cm^2. In still another embodiment, the implantation process implants B utilizing an implant energy of about 1.5 KeV and a dosage of about 2E13 atoms/cm^2. It is noted that an annealing process is not required in conjunction with the implantation process **220**. Additionally, it has been observed that responsive to the implantation process **220**, the silicon nitride becomes oxygen rich and thus improves selectivity of a subsequent epitaxial process as will be discussed below.

[0017] In FIG. **3**, a patterned photoresist layer **225** is formed to protect the NMOS devices. The patterned photoresist layer **225** may be formed by a photolithography process. An exemplary photolithography process may include processing steps of photoresist coating, soft baking, mask aligning, exposing, post-exposure baking, developing photoresist and hard baking. The photolithography exposing process may also be implemented or replaced by other proper techniques such as maskless photolithography, electron-beam writing, ion-beam writing, and molecular imprint.

[0018] In FIG. **4**, an etching process **230** is performed to remove portions of the cap layer **216** overlying the substrate **202** at either side of the gate structures of the PMOS devices. The patterned photoresist layer **225** protects the NMOS devices during the etching process **230**. In the present embodiment, the etching process **230** includes a dry etching process. For example, the dry etching process utilizes a pressure ranging from about 5 to about 15 mTorr, a power ranging from about 300 to about 900 W, HBr having a flow rate ranging from about 100 to about 400 sccm, O2/He having a flow rate ranging from about 10 to about 40 sccm, and NF3 having a flow rate ranging from about 1 to about 20 sccm. The etching process **230** also removes the cap layer **216** overlying the hard mask layer **210**. Further, the etching process **230** continues to break through the oxide layer **214** (if present) directly overlying the substrate **202** and removes a portion of the hard mask layer **210** on the gate electrode **208**. Therefore, following the etching process **230**, sidewall spacers **232** with an outer implanted cap layer **216**a are formed on the sidewalls of the gate structures of the PMOS devices. Further, a portion of the hard mask layer **210***a* remains on the gate electrode **208**. It is understood that the etching process **230** may be performed as one etching process or multiple etching processes.

[0019] In FIG. **5**, an etching process **234** is performed to etch recesses or openings **240** in the substrate **202**. The etching process **230** includes a dry etching process, wet etching process, or combination dry and wet etching processes to remove portions of the silicon substrate **202** that are exposed. For example, the dry etching process utilizes a pressure ranging from about 5 to about 15 mTorr, a power ranging from about 300 to about 900 W, HBr having a flow rate ranging from about 100 to about 400 sccm, O2/He having a flow rate ranging from about 10 to about 40 sccm, Cl2 having a flow rate ranging from about 20 to about 60 sccm, and NF3 having a flow rate ranging from about 1 to about 20 sccm. It is noted that the hard mask layer **210***a* and spacers **232** protect the gate structures of the PMOS devices, and the patterned photoresist layer **225** protects the NMOS devices during the etching process. The recesses **240** may have a depth ranging from about 400 to about 500 angstrom (A).

[0020] In FIG. **6**, a semiconductor material is deposited in the recesses **240** to form strained structures of the semiconductor device **200**. In an embodiment, an epitaxy or epitaxial (epi) process is performed to deposit a semiconductor material in the recesses **240**. The semiconductor material is different from the substrate **202**. Accordingly, the channel region of the PMOS device is strained or stressed to enable carrier mobility of the device and enhance device performance. The patterned photoresist **225** protecting the NMOS devices is removed prior to the epi process. In the present embodiment, silicon germanium (SiGe) is deposited by an epi process in the recesses **240** of the substrate **202** to form SiGe features **250** in a crystalline state on the silicon substrate. It has been observed that the implanted cap layer **216** overlying the NMOS devices and the implanted cap layer **216***a* on the sidewalls of the gate structures of the PMOS devices do not exhibit SiGe selectivity loss. That is, the SiGe selectivity to silicon nitride is improved by the implantation process **220** such that SiGe is deposited on the silicon substrate and not on the implanted silicon nitride. Accordingly, an etchant gas such as HCl does not have to be used with the epi process to maintain the selectivity between silicon nitride and silicon substrate. It has been observed that the SiGe growth rate is adversely impacted when using an etchant gas, and a facet profile of the SiGe feature is constrained. Thus, since the embodiments disclosed herein do not require utilizing an etchant gas, through-put is increased and a larger process window is achieved.

[0021] It is noted that the SiGe features **250** do not accumulate on the hard mask **210***a*, the cap layer **216** overlying the NMOS devices, the cap layer **216***a* of the spacer **232**, and the STI **204**. Additionally, the SiGe features **250** may be deposited such that they are raised about 125 angstrom (A) above the surface of the substrate **202**. In furtherance of the present embodiment, the SiGe features **250** may be in-situ doped with p-type dopants, such as B or In, to form source and drain regions of the PMOS devices.

[0022] The semiconductor device **200** continues with processing to complete fabrication as discussed briefly below. For example, an etching process is performed to remove portions of the cap layer **216** overlying the NMOS region thereby forming sidewall spacers on the gate structures of the NMOS devices. Further, source and drain regions for the NMOS device may be formed by ion implantation of n-type dopants such as P or As. In another embodiment, silicon carbide (SiC) may be deposited by an epi process in the silicon substrate to form the source/drain regions of the NMOS devices in a similar manner as described above. Additionally, silicide features are formed on the raised source and drain regions to reduce the contact resistance. The silicide can be formed on the source and drain regions by a process including depositing a metal layer, annealing the metal layer such that the metal layer is able to react with silicon to form silicide, and then removing the non-reacted metal layer.

[0023] An inter-level dielectric (ILD) layer is formed on the substrate and a chemical mechanical polishing (CMP) process is further applied to the substrate to planarize the substrate. Further, an contact etch stop layer (CESL) is formed on top of the gate structures before forming the ILD layer. In an embodiment, the gate electrode **208** remains poly in the final device. In another embodiment, the poly is removed and replaced with a metal in a gate last or gate replacement process. In a gate last process, the CMP process on the ILD layer is continued to expose the poly of the gate structures, and an etching process is performed to remove the poly thereby forming trenches. The trenches are filled with a proper work function metal (e.g., p-type work function metal and n-type work function metal) for the PMOS devices and the NMOS devices.

[0024] A multilayer interconnection (MLI) including metal layers and inter-metal dielectric (IMD) is formed on the substrate to electrically connect various device features to form a integrated circuit. The multilayer interconnection includes vertical interconnects, such as conventional vias or contacts, and horizontal interconnects, such as metal lines. The various interconnection features may implement various conductive materials including copper, tungsten and silicide. In one example, a damascene process is used to form copper multilayer interconnection structure.

[0025] The semiconductor device **200** serves only as one example. The semiconductor device **200** may be used in various applications such as digital circuit, imaging sensor devices, a hetero-semiconductor device, dynamic random access memory (DRAM) cell, a single electron transistor (SET), and/or other microelectronic devices (collectively referred to herein as microelectronic devices). Of course, aspects of the present disclosure are also applicable and/or readily adaptable to other type of transistor, including single-gate transistors, double-gate transistors, and other multiple-gate transistors, and may be employed in many different applications, including sensor cells, memory cells, logic cells, and others.

[0026] The foregoing has outlined features of several embodiments. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A method of fabricating a semiconductor device, comprising:

providing a semiconductor substrate;

forming a gate structure over the substrate;

forming a material layer over the substrate and the gate structure;

implanting one of Ge, C, P, F, and B in the material layer;

removing portions of the material layer overlying the substrate at either side of the gate structure;

forming recesses in the substrate at either side of the gate structure; and

depositing a semiconductor material in the recesses by an expitaxy process.

2. The method of claim **1**, wherein the semiconductor material includes silicon germanium (SiGe).

3. The method of claim **1**, wherein the material layer includes silicon nitride.

4. The method of claim **1**, wherein the removing portions of the material layer includes performing an anisotropic etching that does not etch other portions of the material layer disposed on sidewalls of the gate structure.

5. The method of claim **1**, wherein the implanting Ge includes utilizing an implant energy of about 5 KeV and a dosage of about 5E14 atoms/cm^2.

6. The method of claim **1**, wherein the implanting C includes utilizing an implant energy of about 5 KeV and a dosage of about 1E15 atoms/cm^2.

7. The method of claim **1**, wherein the implanting P includes utilizing an implant energy of about 5 KeV and a dosage of about 1E15 atoms/cm^2.

8. The method of claim **1**, wherein the implanting F includes utilizing an implant energy of about 5 KeV and a dosage of about 1E15 atoms/cm^2.

9. The method of claim **1**, wherein the implanting B includes utilizing an implant energy of about 1.5 KeV and a dosage of about 2E13 atoms/cm^2.

10. A method of fabricating a semiconductor device, comprising:

providing a semiconductor substrate having a first region and a second region;

forming first and second gate structures over the first and second regions of the substrate, respectively;

forming a silicon nitride layer over the substrate and the first and second gate structures;

performing an implantation process to the silicon nitride layer;

protecting the silicon nitride layer overlying the first region of the substrate;

removing portions of the silicon nitride layer overlying the second region of the substrate at either side of the second gate structure;

forming recesses in the substrate at either side of the second gate structure; and

forming a semiconductor material in the recesses, the semiconductor material being different from the semiconductor substrate.

11. The method of claim **10**, wherein the implantation process includes implanting one of Ge, C, P, F, and B in the silicon nitride layer.

12. The method of claim **11**, wherein the implanting Ge includes utilizing an implant energy of about 5 KeV and a dosage of about 5E14 atoms/cm^2;

wherein the implanting C includes utilizing an implant energy of about 5 KeV and a dosage of about 1E15 atoms/cm^2;

wherein the implanting P includes utilizing an implant energy of about 5 KeV and a dosage of about 1E15 atoms/cm^2;

wherein the implanting F includes utilizing an implant energy of about 5 KeV and a dosage of about 1E15 atoms/cm^2;

wherein the implanting B includes utilizing an implant energy of about 1.5 KeV and a dosage of about 2E13 atoms/cm^2.

13. The method of claim **10**, wherein the forming the semiconductor layer includes epitaxially growing silicon germanium (SiGe) in the recesses.

14. The method of claim **13**, wherein the first gate structure is part of an NMOS transistor and the second gate structure is part of a PMOS transistor.

15. The method of claim **10**, wherein an annealing is not performed in conjunction with the implantation process.

16. The method of claim **10**, further comprising forming a silicon oxide layer over the substrate and the first and second gate structures, wherein the silicon nitride layer is formed on the silicon oxide layer.

17. A semiconductor device, comprising:

a semiconductor substrate; and

a transistor that includes:

a gate structure disposed on the substrate, the gate structure including sidewall spacers that are implanted with one of Ge, C, P, F, and B;

source and drain regions disposed in the substrate at either side of the gate structure, the source and drain regions formed of a semiconductor material different from the semiconductor substrate.

18. The semiconductor device of claim **17**, wherein the semiconductor material includes silicon germanium (SiGe).

19. The semiconductor device of claim **17**, wherein the sidewall spacers include silicon nitride.

20. The semiconductor device of claim **18**, wherein the silicon nitride becomes oxygen rich in response to being implanted with the one of Ge, C, P, F, and B.

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