Defects in Microelectronic Materials and Devices

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Figure on cover: Z-contrast image of a silicon-silicon dioxide-hafnium dioxide structure showing an isolated Hf atom in the SiO_2 interlayer (image courtesy of K. Van Benthem and S. J. Pennycook). The expanded image is an electron density plot for this structure (courtesy of A. G. Marinopoulos and S. T. Pantelides).

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3

Defects in Strained-Si MOSFETs

Yongke Sun and Scott E. Thompson

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3.1 Introduction

Strained-Si channel metal-oxide-semiconductor field-effect transistors (MOSFETs) are used in nearly all 90 nm and smaller commercial logic technologies. Strained channels improve the electron and hole motilities by altering the semiconductor band structure. Strained semiconductor layers are known to produce dislocation defects and have been extensively studied on blanket wafers on which several materials science review papers have recently been published [1–4]. However, much less has been published on strained-Si defects relating to manufacturing commercial production technologies which we address in this chapter. The chapter is outlined as follows: Section 3.2 briefly reviews strained-Si MOSFETs in state-of-the-art production technologies, Section 3.3 covers the yield of integrated circuits, Section 3.4 focuses on defects in strained-Si layers, Section 3.5 discusses strain relaxation, Section 3.6 describes process flow thermal cycles and manufacturing tradeoffs, and Section 3.7 briefly introduces the potential benefits and problems involving incorporating strain in alternative wafer orientations.

3.2 State of the Art: Strained-Si MOSFETs

In this section, we briefly describe techniques used in commercial 90 and 45 nm logic technologies to introduce uniaxial stress into the Si channel; more process details are published elsewhere [5,6]. The techniques in production include high stress tensile and

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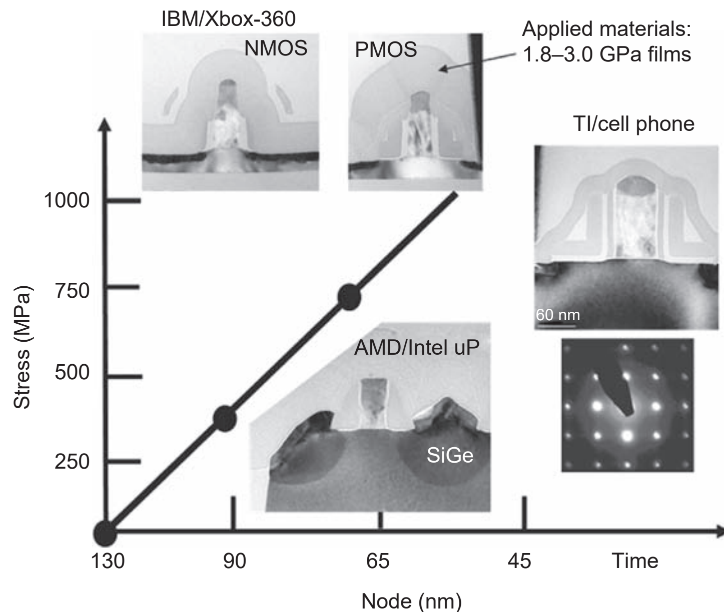

FIGURE 3.1
Various structures to introduced strain into the channel of MOSFETs, e.g., embedded SiGe in S/D, and stress liners. (From Chipworks Report. With permission.)

compressive SiN capping layers, and selective epitaxial SiGe deposited in recessed/raised sources and drains (S/D). Examples of these production techniques are shown in Figure 3.1, where the transmission electron micrographs (TEM) are obtained by Chipworks [7]. Future generations will bring the SiGe closer to the channel, increase the Ge concentration [8–11], and increase the stress in the capping layers, which is approaching 3 GPa. Other possible future techniques for process stress or mobility enhancement may include tensile shallow trench oxide, or embedded SiC [12] for nMOSFETs and hybrid orientated (110) wafers [13]. Together, these techniques are expected to lead to channel stresses of $\sim$1–2 GPa, approaching the stress level of wafer-based biaxial stress [14].

The common defects in strained layers are misfit dislocations induced by film strain relaxation. To minimize defect density, the process-induced strain, unlike wafer-based strain, is introduced late in the process flow. Epitaxial SiGe is introduced postisolation and gate formation by etching the S/D and growing selective epitaxial SiGe [8,15,16]. The high stress capping layers are introduced even later postsalicide formation. In some cases when the high stress capping layers for stress memorization are introduced before S/D anneal [17,18], they can cause drain shorting defects at S/D anneals at elevated temperatures.

3.3 Yield of Integrated Circuits

Before investigating the defects in strained-Si in Section 3.4, it is first helpful to understand how these defects alter yield. Yield is one of the key factors in determining the success of a production technology, or a technology option like strained-Si, since yield directly affects the die cost of an integrated circuit. Yield considerations have played, and will continue to

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90 nm | 65 nm | 45 nm

~100 M Transistor/chip microprocessor | ~400 M Transistor/chip | ~400 M Transistors/chip

FIGURE 3.2
Examples of logic chips fabricated with strained-Si channel MOSFETs: Intel and AMD microprocessors.

play, a key role in determining which technologies are commercially adopted. To understand chip yield, it is necessary to understand that, for a logic die to yield (i.e., be fully functional and sellable), every single logic transistor, which typically numbers in the hundreds of million per chip, needs to work. This is unlike memory chips where redundant memory blocks are added and fuses set to repair nonyielding bits, rows, columns, or even blocks. Figure 3.2 shows some typical die photos and transistor device cross sections that are fabricated using strained-Si. The chips serve the three dominant markets of computer, communication, and consumer electronics, and highlight the wide success of this technology in not only high performance but also low-cost markets.

How strained-Si defects affect yield depends on how susceptible yield is to the defects. Yield is a function of defect density and amount of critical chip area sensitive to the defects. The critical area is defined as the chip area in which, if a defect occurs, it will cause a nonfunctional device. Using the example of strained-Si, this important concept of critical area will become clearer and will help to understand the choices made for the first three generations of strained-Si. For strained-Si devices, the dominant failure modes are misfit dislocations and stacking faults. The strain field around the dislocations and stacking faults captures metal impurity atoms and increases the dopant diffusion by several orders of magnitude [19]. Stacking faults and dislocations that are contained entirely within the neutral space charge region of the S/D junctions do not impact transistor yield, while those extending from source to drain cause high leakage current (see Figures 3.3 and 3.4) and nonfunctional transistors. Some levels of dislocations and stacking faults are present and can be found in commercial chips on the market, as seen in the Chipworks report on Intel's 90 nm strained-Si technology. Figure 3.5 shows a stacking fault in the S/D on a commercial chip that does not degrade the functionality.

Defects will have a more deleterious impact on the yield as the channel length of the MOSFET is scaled. At shorter channel length, the dislocations or stacking faults are more likely to penetrate through the source to the drain and cause a nonfunctional device. Due to the deleterious nature of these defects, study of these defects is an important subject for improving the quality of strained-Si in high-volume manufacturing.

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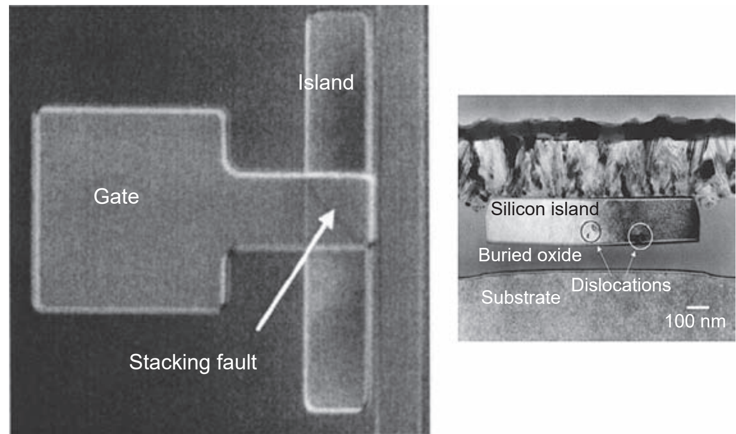

FIGURE 3.3
Examples of stacking fault and dislocation defects between source and drain of a MOSFET. (The left panel of this figure is reprinted with permission from Yang, J., Neudeck, G.W., and Denton, J.P., *Appl. Phys. Lett.*, 77, 20, 2000. The right panel of this figure is reprinted with permission from Sleight, J.W., Chuan Lin, and Gula, G.J., *IEEE Electron Devices Lett.*, 20, 5, 1999.)

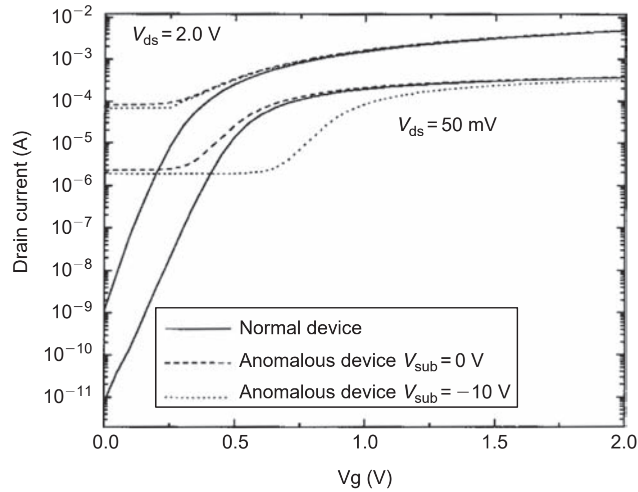

FIGURE 3.4
Current versus voltage curve for a normal and MOSFET with a source to drain defect. (Reprinted with permission from Sleight, J.W., Chuan Lin, and Gula, G.J., *IEEE Electron Device Lett.*, 20, 5, 1999.)

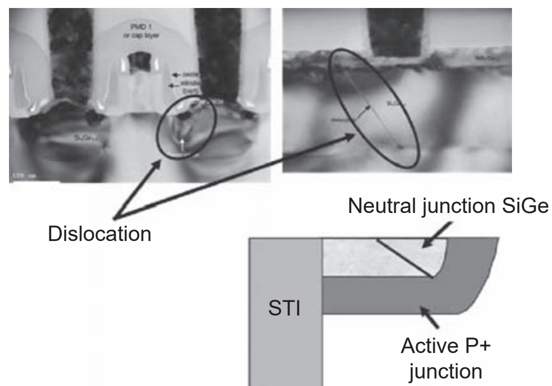

FIGURE 3.5
Examples of stacking faults in embedded SiGe source and drain. (From Pentium 4 prescott Microprocessor report, www.chip-works.com.)

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3.4 Defects in Strained Layers

Misfit dislocations and stacking faults in the S/D SiGe epitaxy can be generated during epitaxial growth and thermal processes due to strain relaxation. The misfit dislocations are one-dimensional threading defects, while the stacking faults are two-dimensional planar defects. They are different yet closely related to each other. The formation of threading dislocations and stacking faults is strongly influenced by several factors, including strain level, lattice temperature, and implantation damage. Threading dislocations are further classified into two types, edge and screw dislocations, as shown in Figure 3.6. A dislocation can be visualized by imagining cutting a crystal along a plane and slipping one half across the other by a lattice vector. The halves will fit back together without leaving a defect. But if the cut only goes part way through the crystal, the boundary of the cut will leave a dislocation. The boundary of the cut is the dislocation line; the vector of the slip is the Burgers vector. When the Burgers vector is perpendicular (parallel) to the dislocation line, the dislocation is called edge (screw) dislocation. As we will see in the following discussion, the dominant dislocation type in strained-Si is neither pure edge nor screw, but is mixed.

A mixed-type dislocation is best visualized by the concept of an edge dislocation. An edge dislocation is formed by slipping one half of the crystal in the direction perpendicular to the cutting plane. Then the defect is created as if one plane of atoms is inserted to a regular crystal and ends at the defect line as shown in Figure 3.7. Here, even though there exists one extra plane of atoms in half of the crystal, except for the nearby area of the dislocation, the atoms still maintain the stacking order of crystal. Thus, the extra half plane is not a planar defect, in contrast to the stacking fault-induced edge dislocation that will be introduced next. It is easy to see that a dislocation line cannot end inside the crystal. Dislocations either end at the surface or form a ring inside the crystal. Most dislocations in strained-Si devices terminate at both ends of the shallow trench isolation (STI) that surrounds all devices. Likewise, in the process of crystal growth, the dislocations in the substrate tend to propagate into the newly grown crystal unless techniques are used to terminate the defects on the sides [4,20].

The stacking fault, just as its name implies, is caused by wrong stacking order of atoms in the process of crystal or film growth. A face-centered cubic (FCC) crystal lattice is formed by close packing of the atoms, which are shown in Figure 3.8a and b, where the close-packed plane is the (111) plane. If we take the base plane as the A-plane, the second

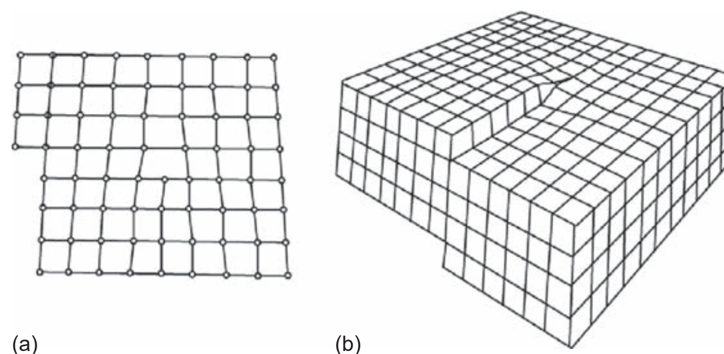

FIGURE 3.6
Two types of dislocations: (a) edge and (b) screw dislocation.

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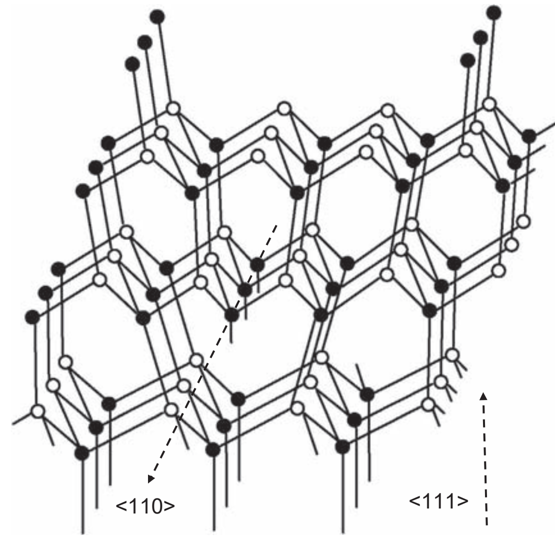
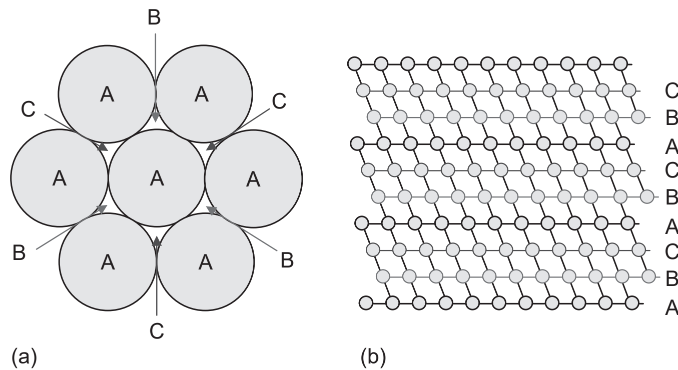


FIGURE 3.7
A 60° dislocation in Si. The dislocation is created in crystal structure along the line where the extra half plane ends.

plane as the B-plane, then the atoms can take either A or C configuration in the third plane. The ABCABC . . . sequence of atom array forms the face-centered cubic (FCC) crystal lattice. A stacking fault occurs when a whole or part of one (111) plane is absent. When this happens, the stacking sequence becomes, for example, ABCA***BA***BABC . . . or ABCA***BA-C***ABC . . . The former sequence is shown in Figure 3.8c. Normally, a stacking fault is formed by part of the absent (111) plane, and is bordered by an edge dislocation. This dislocation is different from the dislocations introduced earlier, and is a partial dislocation, since its Burgers vector is not the translation vector of the crystal lattice. However, a perfect



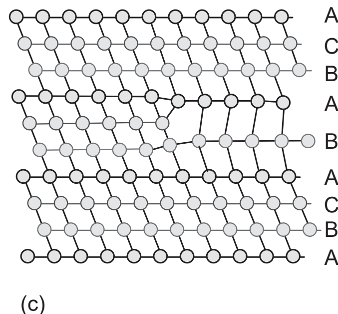


FIGURE 3.8
FCC crystal lattice and the formation of a stacking fault. (a) and (b) show the FCC stacking sequence, and (c) shows how a stacking fault forms.

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dislocation may dissociate into partial bounding stacking faults under certain circumstances. Since a stacking fault is a planar defect with broken or distorted bonds extending through a large thickness of the film, it is likely to be more deleterious to device operation than a single threading dislocation.

The dislocations and stacking faults in SiGe/Si system exhibit quite complicated characteristics. These defects normally can glide along a crystal plane. Understanding the movement of defects during thermal cycles is important to diminish the impact of these defects to yield. Because the dislocation takes place when the two halves of crystal glide over each other on one crystal plane (shear stress exceeds the yield stress of the material), the crystal structure determines in which plane the dislocations have the lowest energy to form. Si has a diamond structure, and is formed by two FCC lattices by displacing each other one quarter of the body diagonal of the cubic cell. All Si atoms have four nearest neighbors, which are positioned at the vertices of a tetrahedron and connected to the center atom by four bonds. Any two nearest atoms are along a <111> direction, and any two atoms on the vertices are along a <110> direction. By plotting the atom positions in the Si crystal along the <111> direction, we can see that the atoms in (111) plane are close packed in two layers and connected with the other double layers by one bond per atom (see Figure 3.9). The interactions within the double layer are strong and hard to break, but the interactions between double layers are relatively weak. Thus, the lowest energy glide for diamond structures is in the (111) plane. Therefore, the dislocation lines in Si are generally in the (111) plane. To determine the direction of the dislocation line, we need to inspect the directions formed by connecting atoms in the (111) plane. In any (111) plane, there exist three <110> directions. They are the connecting lines between the three atoms at the vertices of a tetrahedron in one (111) plane. Due to the two planes fitting with each other after the glide, the dislocation lines are usually along the <110> directions, which form a 60° angle to the Burgers vector. Hence, this type of dislocation is also called the 60° dislocation. The majority of observed dislocations in the compressively stressed SiGe system are found to be of the 60° type. The 60° dislocation is a mixed type of dislocation that is characteristic of both edge and screw

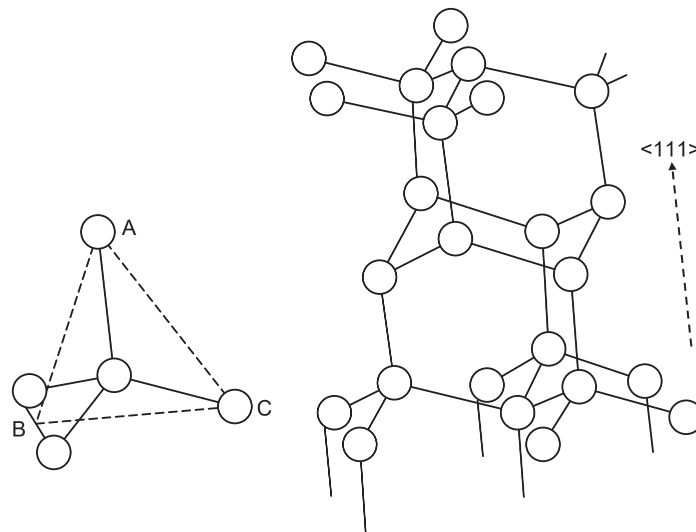

FIGURE 3.9
Atom positions in Si crystal along the <111> direction. Note there are two close layers connected with the other double layers by one bond per atom.

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dislocations. The formation of the 60° dislocation is illustrated in Figure 3.7. Another typical dislocation line is along the <112> direction in the (111) plane. The <112> directions are lines that connect atoms in different tetrahedrons. A <112> dislocation is an edge dislocation. An atom on a dislocation line has one extra electron to form a full shell, and thus form a dangling bond (see Figure 3.7).

A perfect $a/2$ <110> 60° dislocation can dissociate into two $a/6$ <112> partial dislocations, i.e., a 90° and a 30° partial dislocation. Of necessity, a stacking fault between the two partial dislocations must also be generated. This dissociation depends critically on strain and lattice temperature. For (001) orientated films under tension such as Si/SiGe, stacking faults may extend through the strained-Si film thickness, whereas most studies consider that the partials are pushed together at the interface and the dislocations are perfect 60° dislocations for compressively strained films such as SiGe/Si.

3.5 Strained-Layer Critical Thickness and Strain Relaxation

To induce and maintain high stress in the channel, the thickness of the SiGe epitaxy in the S/D usually reaches over 100 nm. This raises concerns of strain relaxation, since for the epitaxial layers grown on a substrate, there exists a critical thickness h_c, below which the lattice mismatch can be entirely accommodated by strain, and beyond which, part of the mismatch must be accommodated by dislocations. If strain is relaxed in the SiGe epitaxy and dislocations are generated in the edge of the S/D region, they probably penetrate into the channel and thus cause large leakage. For controlling the defects, the SiGe epilayers in the S/D region must be limited under the critical thickness or treated with special thermal cycles.

The equilibrium critical thickness h_c was studied by Ball and van der Merwe [21], and by Matthews and Blakeslee [22], who found that for $Si_{1-x}Ge_x$ films grown on Si, the relation between h_c (nm) and the Ge atom fraction x_c can be written as

$$x_c = \frac{0.55}{h_c} \ln\left(\frac{4h_c}{b}\right).$$

For 60° glide dislocations, the Burgers vector $b = a_0/2$ <110> ~0.4 nm for Si. Obviously, the critical thickness for SiGe film decreases with Ge content. For SiGe film containing 20% Ge, the critical thickness is about 14 nm.

The thickness for low-temperature molecular beam epitaxy (MBE) grown layers can be much larger than the critical thickness without inducing any dislocations [23,24]. Figure 3.10 shows a series of SiGe films grown at 494°C with different Ge content. The $\sigma_{exc}/\mu = 0$ line indicates the Matthews and Blakeslee criterion for absolute stability, where σ_{exc} is excess stress and μ is the shear modulus. As we can see, films with much larger thickness than the critical thickness are still fully strained. This is because normal as-grown epilayers are far from the thermodynamic equilibrium due to the low substrate temperature (e.g., $T < 0.5T_{melt}$). These layers are in metastable states. Strain relief needs excess stress, which decreases with temperature [25]. For example, in Figure 3.10, the excess stress needed at 494°C obeys $\sigma_{exc}/\mu = 0.026$. For thick SiGe epitaxy grown in the S/D region, the S/D annealing in high temperatures such as 900°C–1000°C can cause strain relaxation and create dislocations [23,24]. For epitaxial layers with thickness less than the critical thickness, annealing at high temperature such as 900°C for even 30 min does not cause observable differences [23].

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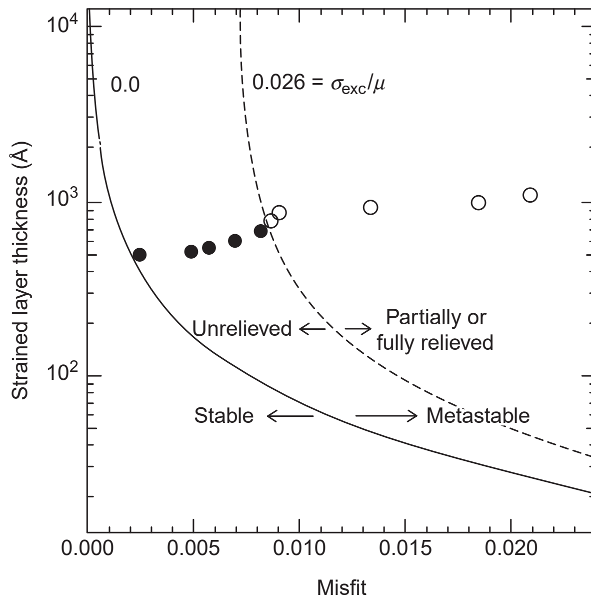

FIGURE 3.10
Thickness and misfits for a series of SiGe films grown at 494°C. Fully strained and partially strain-relieved films are represented by filled and open circles, respectively. (Reprinted with permission from Tsao, J.Y., Dodson, B.W., Picraux, S.T., and Cornelison, D.M., *Phys. Rev. Lett.*, 59, 21, 1987.)

Except for the stress that is induced intentionally in the channel, the mechanical stress induced by thermal cycles in the complementary metal-oxide-semiconductor (CMOS) process should be controlled to minimize stress-induced defects. One important thermal budget is the formation of STI, which is before the SiGe deposition. It is well known that stress is strongly concentrated at both the top and bottom corners of the STI. Inherently large mechanical stress and damage in STI, combined with the subsequent process-induced stress and defects, would generate STI dislocations. If located within the junction depletion region, the STI dislocations can cause abnormally large leakage current through the junction and transistor. The dislocation generation is closely related to the S/D annealing [26,27]. During thermal annealing, crystal defects from ion implantation, especially in heavy-dose arsenic-implanted S/D regions [28], produce STI dislocation nucleation and generate dislocations, which glide to the region of maximum stress under the combined influence of mechanical stress and high-temperature processing, and interact with others to evolve a larger dislocation. Ikeda et al. [26] proposed two-step annealing to both activate the S/D dopants and minimize the mechanical stress. Ishimaru et al. [29] and Park et al. [30] proposed the technology of diminishing the residual stress in STI through high-temperature densification and the optimized combination of trench filling tetraethoxysilane (TEOS–O_3) oxide, respectively. Damiano et al. [28] proposed additional oxidation, and Jeon et al. [31] changed the S/D anneal from rapid thermal annealing (RTA) to tube anneal; both claimed they completely eliminated the trench dislocations.

3.6 Process Flow

For the purpose of sustaining large enough strain in the channel, stress is introduced in the strained-Si process flow as late as possible to avoid high-temperature anneals and strain relaxation. A typical 130 to 45 nm front-end CMOS process flow is shown in Table 3.1. The key thermal cycles that will potentially cause device defects are the STI, S/D formation, and gate oxide formation, each of which requires ~30 s or longer thermal budgets at temperature

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TABLE 3.1

Process Modification of Strained-Si Technology to a Standard CMOS Process Flow

Typical CMOS Process Flow	Strained-Si
• Gate stack	
• Gate patterning	
• Offset spacers (optional)	
• *n*-Type LDD+halo/pocket implants	
• *p*-Type LDD+halo/pocket implants	
• Spacer deposition and etch (STI)	
←	• Recess and SiGe deposition (pMOSFETs)
• *n*-Type HDD implants	
• *p*-Type HDD implants	
• RTA	
• Silicide protection deposition and etch	
• Silicidation	
←	• High stress capping layer (nMOSFETs)

around 1000°C. Only slight modifications to a standard CMOS logic technology process flow are needed to insert the longitudinal compressive and tensile stress into the p- and nMOSFETs, respectively. For strained-Si pMOSFETs, a Si recess etch is inserted after spacer formation and followed by selective epitaxial chemical vapor deposition (CVD) of SiGe in the S/D region. The specific process flow steps are shown in Figure 3.11. Germanium concentration of 17%–35% is used, which creates a lattice spacing larger than Si. The mismatch in the SiGe to Si lattice causes the smaller lattice constant Si channel to be under compressive stress, the magnitude of which also depends on the spacing of the SiGe epitaxy to the channel in addition to the Ge concentration. A 30 nm recessed SiGe layer at the S/D location results in a 250 MPa stress in the middle of the channel; while the same SiGe layer, when present at the S/D extension location, stresses the channel to ~900 MPa. As an example, the three-dimensional finite element analysis in Figure 3.12 shows the stress distribution for a 45-nm gate length transistor after the SiGe deposition. Strain can also be engineered at other process steps like STI and silicide [32]. Integrating the SiGe layer in the S/D extension location also has a key advantage to reduce the effect of the SiGe deposition thermal budget on S/D. Furthermore, by confining the SiGe to the S/D region and introducing it late in the process flow, integration challenges, such as misfit dislocations, yield, and increased self-heating due to the low thermal conductivity of SiGe, are reduced.

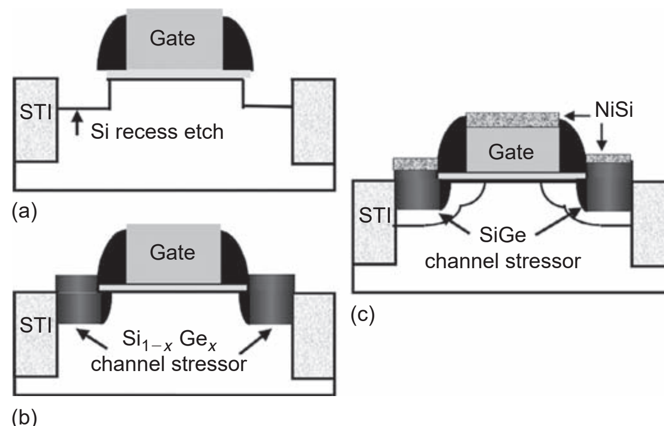

FIGURE 3.11
Strained-Si process flow.

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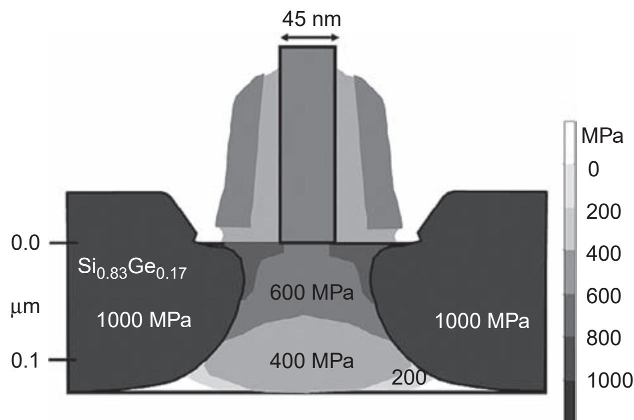

FIGURE 3.12
Stress distribution after SiGe deposition obtained by 3D finite element simulation for a 45 nm gate length transistor.

Longitudinal uniaxial tensile stress is introduced into the nMOSFETs by engineering the stress and thickness of the Si nitride-capping layer [32–35]. There are several techniques to nearly completely neutralize the capping layer strain on p-type MOSFETs; one is the use of a Ge implant and masking layer [33]. Another technique to relax the strain is to selectively remove the capping from the p-type transistors. Wafer-based strained-Si, e.g., Si channels grown on virtual SiGe substrates, also attracted a lot of attention in the last decade. However, compared to process-induced strain, the strain induced in the channel is biaxial tensile strain. This has been proven not to be as efficient as the longitudinal tensile strain for nMOSFETs [36], and even degrades the performance of the pMOSFETs [37,38]. Second, thermal annealing can easily cause strain relaxation in the strained-Si layer [39–41]. In contrast, a significant advantage of the uniaxial stress Si process flow is that, on the same wafer, compressive stress is introduced into the pMOSFETs and tensile stress in the nMOSFETs to improve both the electron and hole mobility. Since the nitride capping layer is already present to support unlanded contacts, only a few new process steps are introduced at less than a 2% wafer cost increase.

3.7 Strain and Alternative Wafer Orientation

Critical thickness and strain relaxation also relate to the wafer orientation. Although there are attempts to use wafers with different orientations, combined with epitaxial strain, to potentially enhance carrier mobility, the critical thickness for dislocation introduction is very low in non-(001) wafers, and kinetically suppressing dislocation nucleation is very difficult [42]. Diamond cubic and zinc blende structures create undesirable partial dislocation stacking in (111), (110), and (112), leading to relaxed layers with very high threading dislocation densities [43]. Thus, for CMOS technology incorporated with strain, at present, the best recommendation continues to be to use (001) wafers.

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