

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner

Case IPR2025-00683
Patent 8,907,425

**PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37
C.F.R. § 42.107 TO PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,907,425**

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EXHIBIT LIST

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EX2001	Complaint for Patent Infringement , Dkt. No. 1, <i>Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited</i> , Case No. 2:24-cv-00623, (E.D. Tex. Filed August 1, 2024)
EX2002	Complaint for Patent Infringement , Dkt. No. 1, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Case No. 2:24-cv-00730, (E.D. Tex. Filed September 6, 2024)
EX2003	Consolidation Order , Dkt. No. 12, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed December 6, 2024)
EX2004	Docket Sheet , <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Case No. 2:24-cv-00730, (E.D. Tex.) (Printed May 31, 2025)
EX2005	Docket Control Order , Dkt. No. 51, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed February 14, 2025)
EX2006	Second Docket Control Order , Dkt. No. 55, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed February 21, 2025)
EX2007	First Amended Docket Control Order , Dkt. No. 59, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed February 27, 2025)
EX2008	Third Amended Docket Control Order , Dkt. No. 83, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed April 9, 2025)
EX2009	Docket Sheet , <i>Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited</i> , Case No. 2:24-cv-00623, (E.D. Tex. Dated April 23, 2025)
EX2010	Notice of Compliance (re: P.R. 3-1 and 3-2 disclosures) , Dkt. No. 45, <i>Advanced Integrated Circuit Process LLC v. United</i>

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	<i>Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed January 30, 2025)
EX2011	Plaintiff’s Unopposed Motion for Leave to Amend Infringement Contentions , Dkt. No. 54, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed February 20, 2025)
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EX2015	Scheduling Order , Dkt. No. 28, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Case No. 2:24-cv-00730, (E.D. Tex. Filed December 11, 2024)
EX2016	Defendant TSMC’s Invalidity Contentions , <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Served May 1, 2025)
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EX2020	Joint Notice Resolving Discovery Disputes Set for Hearing (Dkt.

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	Nos. 78, 80, 89, 90), Dkt. No. 102, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed April 30, 2025)
EX2021	Defendant Taiwan Semiconductor Manufacturing Company Limited’s Motion to Stay Pending <i>Inter Partes</i> Review , Dkt. No. 99, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed April 28, 2025)
EX2022	United Microelectronics Corporation’s Motion to Dismiss Plaintiff’s Claims for Direct Infringement and Pre-Suit Indirect Infringement , Dkt. No. 15, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed December 6, 2024)
EX2023	Defendant Taiwan Semiconductor Manufacturing Company Limited’s Reply in Support of its Motion to Stay Pending <i>Inter Partes</i> Review , Dkt. No. 109, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 20, 2025)
EX2024	Plaintiff’s Opposition to Defendant Taiwan Semiconductor Manufacturing Company Limited’s Motion to Stay , Dkt. No. 108, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 12, 2025)
EX2025	USPTO Office Action , dated March 17, 2017, re: TSMC Patent Application No. 14/941,669
EX2026	TSMC Application Data Sheet , dated November 16, 2015, re: TSMC Patent Application No. 14/941,669
EX2027	Exhibit 425-08 to Defendant TSMC’s Invalidation Contentions, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Served May 1, 2025)
EX2028	Exhibit 425-16 to Defendant TSMC’s Invalidation Contentions, <i>Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Served May 1, 2025)
EX2029	Exhibit 425-19 to Defendant TSMC’s Invalidation Contentions, <i>Advanced Integrated Circuit Process LLC v. United</i>

Exhibit	Description
	<i>Microelectronics Corporation</i> , Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Served May 1, 2025)

Advanced Integrated Circuit Technology, LLC (“Patent Owner”) respectfully requests that the Board decline to institute *inter partes* review (“IPR”) on the petition (“Petition”) filed by Taiwan Semiconductor Manufacturing Company Ltd. (“Petitioner”) because it fails to show “a reasonable likelihood that the petitioner would prevail with respect to” any of the claims at issue.

I. INTRODUCTION

United States Patent No. 8,907,425 (“the ’425 patent”) is directed to very specific integrated-circuit designs that improve electron and hole mobility in NMOS and PMOS transistor channels, respectively—thereby increasing transistor speeds—by *inter alia* forming three stress-related features: (1) “a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region” wherein “an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode”; (2) “a stress insulating film . . . which causes a second stress opposite to the first stress”; and (3) “a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer.” EX1001, claim 1.

None of the Petition’s Grounds teaches the third claimed feature, much less the claimed combination of the three stress-related features. Instead, each of the Petition’s theories is based on (1) creating Frankenstein-like embodiments stitching

together cherry-picked features and then drafting self-serving graphics designed to arrive at the claimed combination; and/or (2) alleging errors in various references and then offering self-serving “corrections” that alter the teachings of those references. None of the Petition’s theories establishes obviousness; rather, each at most establishes hindsight reconstruction of the ’425 patent’s claimed invention.

II. BACKGROUND

A. *Technology Background*¹

A “MISFET” is a metal-insulator-semiconductor field effect transistor. EX1003 ¶ 49. MISFETs include source and drain regions for current input and output. *Id.* These source/drain regions are doped with either a p-type or n-type impurity. *Id.* ¶ 50. “A MISFET with *p*-type source/drain regions is called **PMOS**” and a MISFET “with *n*-type source/drain regions is called **NMOS**.” *Id.* There is a channel region located between the source and drain regions, and a gate over the channel region. *Id.* ¶ 49.

“Some NMOS [transistors] have demonstrated performance enhancement by

¹ This summary, as well as other factual statements in this Preliminary Response, is based on the evidence offered in support of the Petition. Patent Owner relies on this evidence for purposes of this Preliminary Response only and reserves the right to submit evidence to clarify or correct any facts, in the event of institution.

the introduction of tensile stress to the channel region. However, some PMOS [transistors] may suffer from decreased performance” if the channel region is exposed to tensile stress. EX1006 ¶ [0025]. “Likewise, while some PMOS [transistors] have demonstrated performance enhancement by introduction of compressive stress to the channel region, NMOS [transistors] may suffer from decreased performance” if exposed to compressive stress. *Id.*

The '425 patent teaches that “it is possible to improve the drive capability of the [NMOS] transistor by using [a] stress insulating film [] to apply a tensile stress to the channel region” of the NMOS transistor. EX1001 at 3:5–17. However, because of the tensile stress, using this type of stress insulating film to cover all the transistors in a device decreases the performance of the PMOS transistor. *Id.* The '425 patent addresses techniques for creating a device that balances the ideal stresses to improve the performance of both the NMOS and PMOS transistors.

B. The '425 Patent Invention

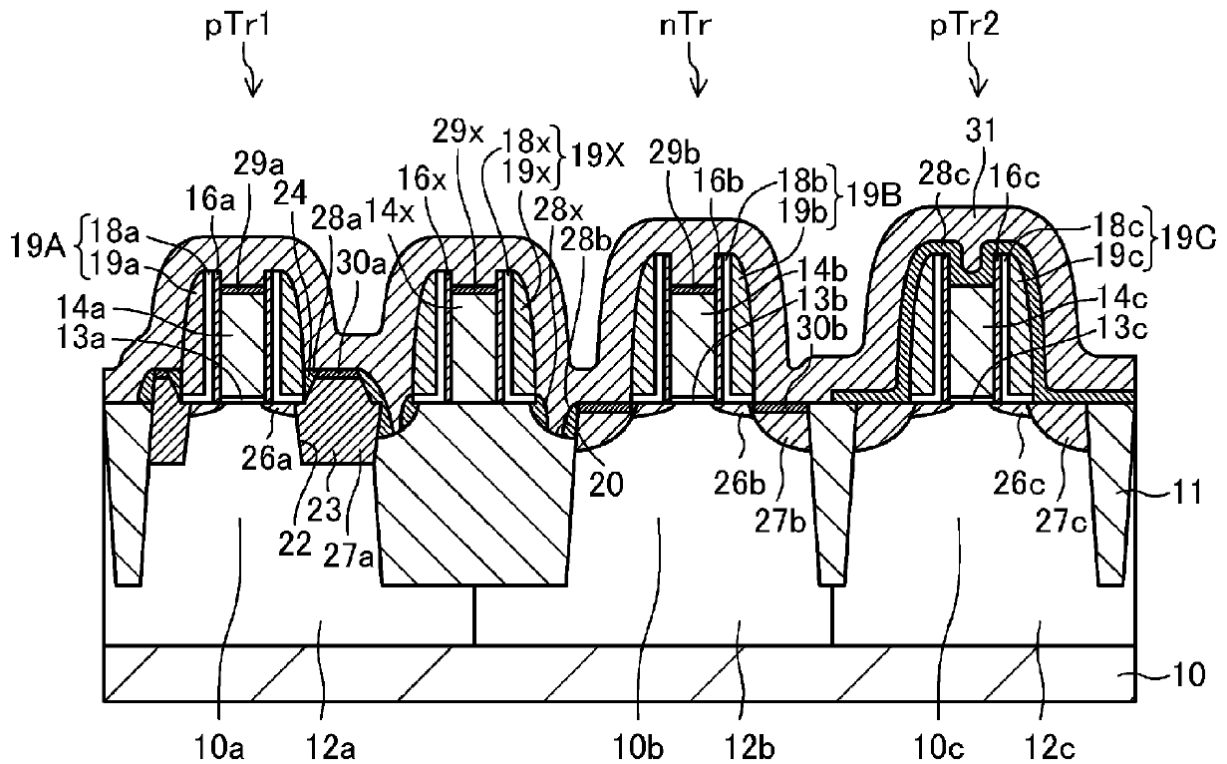
The '425 patent (EX1001) was invented and developed by Satoru Itou and Toshie Kutsunai of Panasonic Corporation, a leader and pioneer in the development and manufacture of electronic equipment including semiconductors and cameras. The '425 patent, which claims priority from a foreign application filed January 7, 2010, issued on December 9, 2014.

The '425 patent relates to “semiconductor devices which include a [MISFET] having a source/drain region including a silicon compound layer, and methods for fabricating the semiconductor devices.” EX1001 at 1:16–22. The '425 patent has fifteen claims, one of which (*i.e.*, claim 1) is an independent claim and the remainder of which (*i.e.*, claims 2–14) are dependent claims. *Id.* at 19:46–22:16. Thus, all claims in the '425 patent require the limitations of claim 1, directly or by dependency.

Although the '425 patent includes several points of novelty, for the purposes of this Preliminary Response, Patent Owner will focus on the structures that balance the compressive and tensile stresses to improve the performance of both the PMOS and NMOS transistors. Claim 1 requires “a silicon compound layer” causing a first stress in one gate length direction (*e.g.*, a compressive stress), “a stress insulating film” causing stress “opposite to the first stress” (*e.g.*, a tensile stress), and “a first stress-relief film [] formed in a space between the silicon compound layer and the first sidewall spacer.” *Id.* at 3:24–37.

Figure 6B, shown below, illustrates an embodiment of the stress-controlling benefits taught by the '425 patent. In the PMOS transistor (pTr1), a silicon compound layer 23 is deposited in a trench 22 on a lateral side of a first sidewall 19A. *Id.* at 14:24–42, Fig. 6B.

FIG.6B



EX1001, FIG. 6B

“The silicon compound layer 23 causes a compressive stress in the gate length direction of the channel region in the first active region 10a.” *Id.* at 14:43–45. This compressive stress improves the performance of the PMOS transistor. *Id.* at 16:12–25. Meanwhile, above the NMOS transistor (nTr), a stress insulating film 31 applies tensile stress to the channel region of the second active region 10b. *Id.* at 16:26–30. This tensile stress improves the performance of the NMOS transistor. *Id.*

A “stress-relief film 28a is formed in the space 24 between the silicon compound layer 23 and the first sidewall 19A” of transistor pTr1. *Id.* at 14:51–54. The location of the stress-relief film 28a and the silicon compound layer 23 separate

the stress insulating film 31 from the channel region in the first active region 10a and reduces the tensile stress applied by the stress insulating film 31 to the channel region in the first active region 10a. *Id.* at 15:65–16:9. This prevents or diminishes a “reduction in drive capability of the [PMOS] transistor pTr1 due to a decrease in the mobility of holes.” *Id.* at 16:9–11.

C. Petitioner’s Cited References

1. Ground 1

The Petition asserts obviousness (*e.g.*, of claim 1) over Wu in view of Alvarez (“Ground 1”). Petition at 16–36.

a) Wu (EX1005)

As reflected in Wu Figure 14 and the accompanying text, Wu discloses a substrate with a PMOS transistor 31 and NMOS transistor 33 wherein an epitaxial layer 58 is deposited in a trench in the active area of the PMOS transistor 31. Epitaxial layer 58 can be silicon germanium. EX1005 ¶ [0021]. Although Figure 14 shows the epitaxial layer 58 “slightly projected from the top surface of the semiconductor substrate 30,” Wu notes that it “may be substantially leveled with or lower than the top surface of semiconductor substrate 30.” *Id.* ¶ [0021]. Wu does not disclose how high above (or below) the substrate epitaxial layer 58 may rise (or recess).

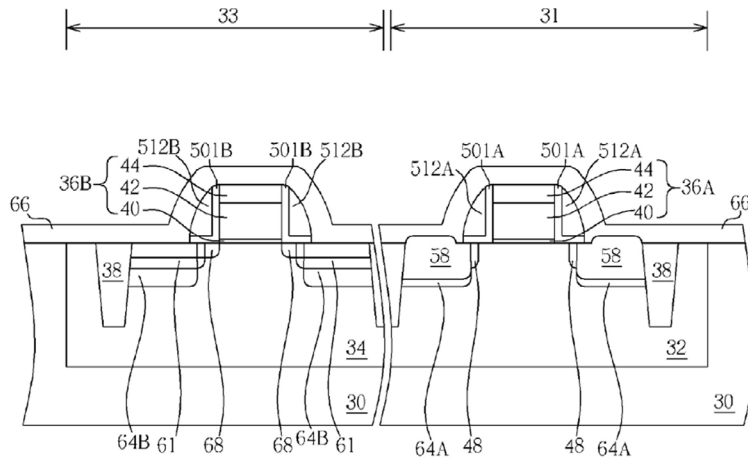
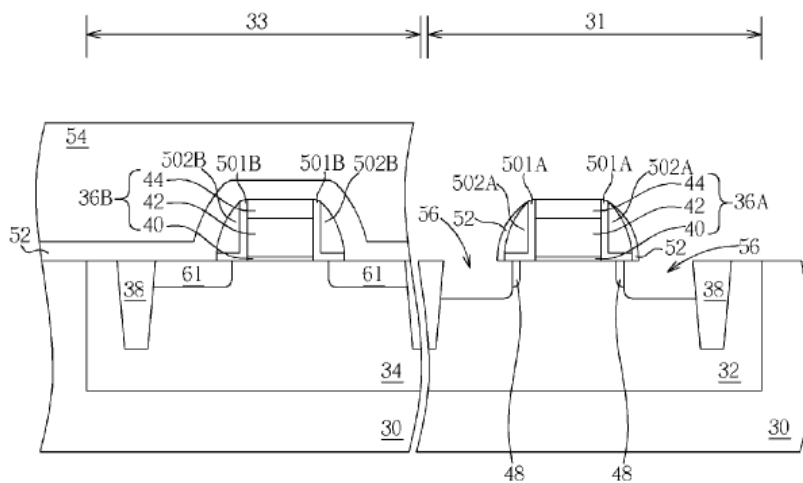


FIG. 14

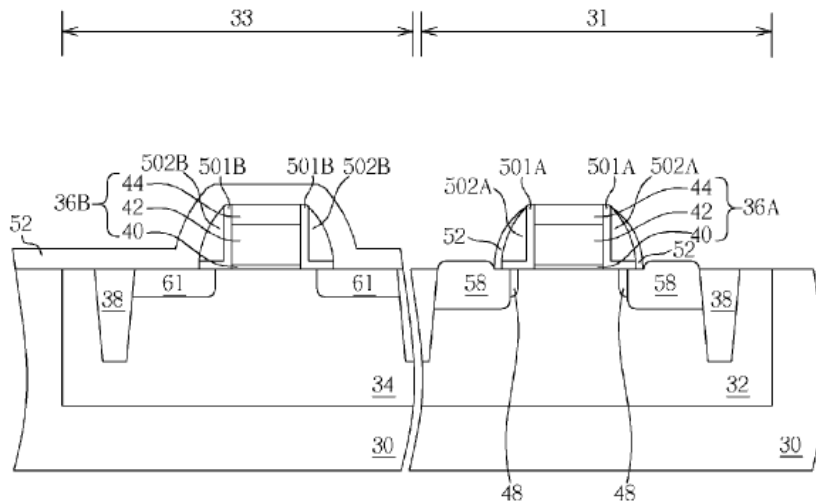
EX1005, FIG. 14

Ground 1 depends on the apparent space between spacer 501A and epitaxial layer 58 depicted in Figure 14 (reproduced above). This space is not an intentional design element of Wu's transistor—indeed, it is never discussed—but rather is only an artifact of Wu's fabrication process. More specifically, and as depicted in Figure 11 below, Wu deposits sacrificial layer 52, *id.* ¶ [0019], that protects oxide layer 501A and spacer 502A while recess 56 is etched, *id.* ¶ [0020], FIG. 11.

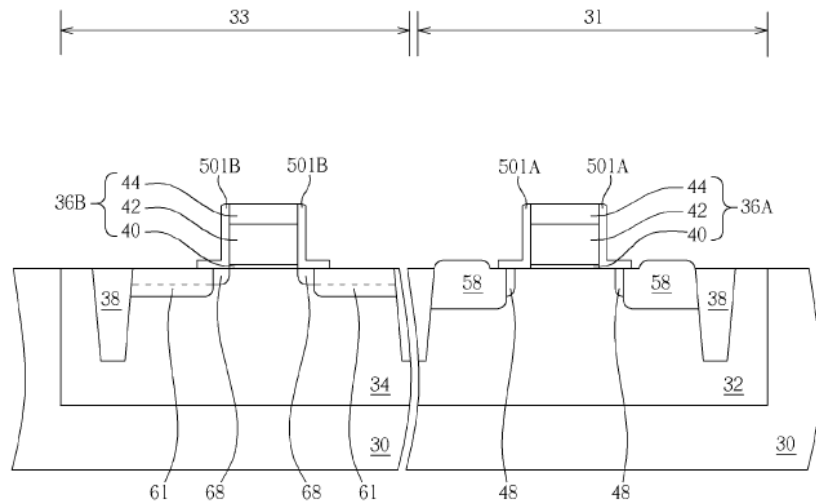


EX1005, FIG. 11

After epitaxial layer 58 is grown in the trench, *see id.*, FIG. 12, sacrificial layer 52 and spacer 502A are removed, yielding a small space between oxide layer 501A and epitaxial layer 58, *see id.* FIG. 13.



EX1005, FIG. 12



EX1005, FIG. 13

Wu does not state how thick the sacrificial layer of silicon nitride 52 is and thus does not disclose the dimensions of the space.

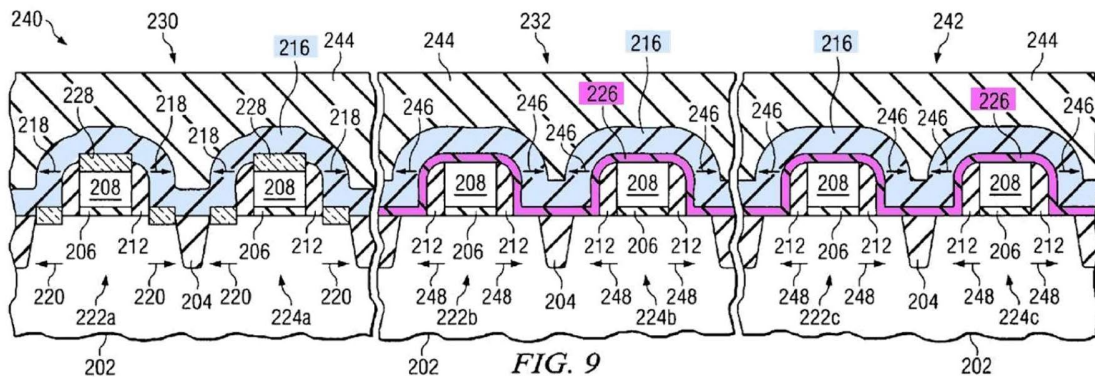
Wu further describes depositing a self-aligned silicide (*i.e.*, silicide) on the “source/drain” regions, although it explains that the self-aligned silicide is “not shown.” EX1005 ¶ [0043]. In this process, “[a] metal layer . . . is deposited. And a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B.” *Id.* ¶ [0024]. Wu does not disclose the thickness of the silicide layer.

After the deposition of silicide on the source and drains, “[a] deposition process is performed to form a CESL 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B.” *Id.* ¶ [0044]. Wu teaches that CESL can be either “a dielectric material or a strained silicon material.” *Id.* ¶ [0025]. Wu does not express a preference for a strained material. Wu is also silent about the orientation of any stress, assuming a strained silicon material is used, with respect to epitaxial layer 58.

The Petition concedes that Wu does not disclose (1) “a stress insulating film . . . which causes a second stress opposite to the first stress” caused by a silicon compound [1F]; or (2) “a first stress-relief film” at all, much less one that “is formed in a space between the silicon compound layer and the first sidewall spacer [1H].” Petition at 33, 35–36.

b) *Alvarez (EX1006)*

Alvarez discloses NMOS and PMOS transistors. EX1006 ¶ [0004]. The Petition relies upon Alvarez as teaching a “stress controlling material 226” (magenta) to reduce stress caused by “stress increasing material 216” (light blue), Petition at 10, as shown in Petitioner’s version of Alvarez Figure 9 below. *Id.* at 19–20.



Petition at 19 (annotating EX1006, FIG. 9)

Alvarez does not disclose a silicon compound layer (*e.g.*, silicon germanium) at all, much less (1) a strained silicon compound layer; (2) any relationship in stresses between a strained silicon compound layer and “stress increasing material 216”; or (3) any spatial relationship between a strained silicon compound layer, gate sidewall and “stress controlling material 226.”

2. Ground 2

The Petition asserts obviousness (*e.g.*, of claim 1) over Cheng alone or in view of Wang (“Ground 2”). Petition at 55–66, 75–77.

Focusing on Figure 4(e), relied on by the Petition, “doped source and drain regions 420a” can be selected from a variety of materials including “amorphous silicon, polysilicon, strained silicon, germanium, silicon germanium, silicon carbide, and/or other materials.” EX1008 ¶ [0065]. Consistent with this, in the text corresponding to Figure 1, Cheng explains that “[t]he source/drain regions 136 may be of conventional composition and fabrication. For example, the source/drain regions 136 may comprise doped portions of the substrate 104.” *Id.* ¶ [0022]. Also, in connection with Figure 1, Cheng explains that “the recesses 144 *may* be filled to a height above the surface 106 of the substrate 104, such that the source/drain regions 136 may be raised source/drain regions. The height of raised source/drain regions may range between about 5 nm and about 100 nm.” *Id.* ¶ [0022] (emphasis added). Importantly, although Cheng provides a range for the overall height of these regions, Cheng is silent about how high above the surface of the substrate the source/drain regions may be raised.

Regarding gate sidewall structures in transistor 401a in Figure 4(e), Cheng explains that “hard mask[] 410a . . . [is] formed over the gate electrode[] 408a.” *Id.* ¶ [0056]. Subsequently, “sidewall dielectric layers 412 and 414, and spacer material 415 are disposed over the semiconductor device(s) . . . such as by etching, to form sidewall dielectric structures 412a, 412b, 414a and 414b, and spacers 415a and 415b. . . . A dummy spacer layer 416 is formed over the semiconductor devices

401a and 401b.” *Id.* ¶ [0061]. Then, “the dummy spacer material 416 is processed to form the dummy spacers 416a and 416b. The dummy spacer material 416 may include silicon dioxide (SiO₂), silicon nitride (SiN), silicon oxy-nitride (SiON), Silicon oxy-carbide (SiOC), polymer, and/or other materials.” *Id.* ¶ [0063].

After this processing—and after the processing of transistor 401b, as reflected in Figures 4(f) to 4(i)—Cheng discloses the deposition of etch stop layer 430a over transistors 401a and 401b. *Id.* ¶ [0070]; Figure 4(j). Cheng teaches that etch stop layer 430a “may include silicon nitride (SiN), silicon dioxide (SiO₂), silicon oxy-nitride (SiON), and/or other materials.” *Id.* ¶ [0070]. Cheng also teaches that “etch stop layer 430a and 430b *may* include a stress level that *may* range between about +0.001 and about +50 GPa for tensile film and between about -0.001 and about -50 GPa for compressive film.” *Id.* (emphasis added). Cheng expresses no preference as to whether etch stop layer 430a is tensile, compressive, or unstressed.

b) Wang (EX1009)

Like Cheng, Wang also discloses MOSFET transistor designs as shown in the Petition’s colored version of Figure 9, below. Petition at 56. The Petition’s theory of obviousness under Ground 2A is predicated on Cheng alone and relies on Wang because it allegedly “helps demonstrate how a POSITA would have understood Cheng’s disclosures.” *Id.* at 55.

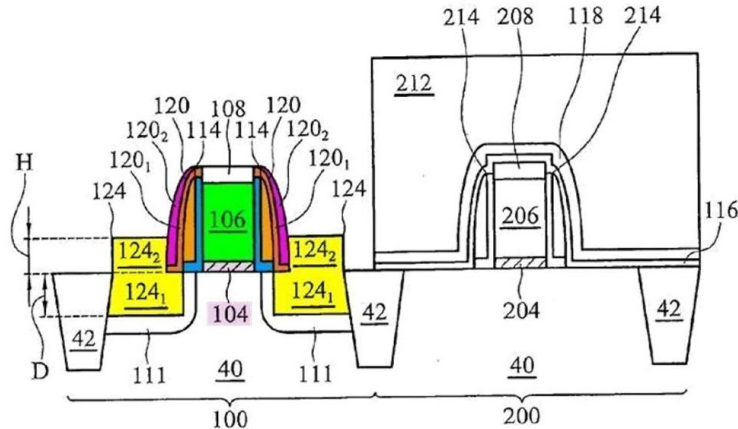


FIG. 9

EX1009, FIG. 9

3. Ground 3

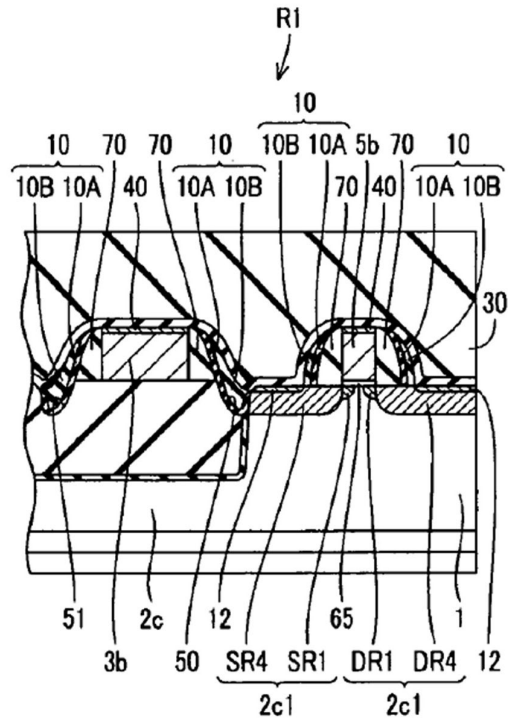
The Petition asserts obviousness (*e.g.*, of claim 1) based on Saito, in view of Fukutome and James. Petition at 79–102.

a) *Saito (EX1010)*

Unlike the Petition’s other references, Saito is directed to a type of memory device known as static random access memory (“SRAM”). EX1010 ¶¶ [0003], [0049]; Petition at 79 (“Saito discloses a textbook SRAM circuit.”). Saito provides a cross section of a portion of the device as Figure 21, shown below as the excerpt presented in the Petition. Petition at 13. Figure 21 shows (1) “sidewall (side wall oxide film) 70 which consists of a silicon oxide film,” EX1010 ¶ [0073]; (2) “insulating film 10A which consists of a silicon oxide film” that is “formed on the side surface of sidewall 70” and has a “thickness . . . about 20 nm,” *id.* ¶ [0074]; (3) “insulating film 10B from which material differs in insulating film 10A, for

example, the insulating film which consists of a silicon nitride film,” *id.*; (4) “[i]mpurity diffusion region 2c1,” which includes “impurity diffused layer SR4 and DR4,” *id.* ¶¶ [0077], [0101]; (5) “silicide film[] 12” formed on “the front surface of [] impurity diffusion region 2c1,” *id.* ¶ [0077]; (5) insulating film 13 (not numbered but immediately below interlayer insulation film 30) and (6) “interlayer insulation film 30,” *id.* ¶ [0080].² The Petition admits that “Saito is silent regarding strain in SiN layer 13.” Petition at 91.

² Although Saito’s textual description of element 5b as “polysilicon wiring formed on the upper surface of this gate insulating film 65” corresponds to the relationship between gate insulating film 65 polysilicon wiring 5b in Figure 21, the Petition nevertheless curiously asserts that “A POSITA would have recognized ‘5b’ in FIGS. 12–21 identifies the polysilicon gate of PMOS transistor P2 and thus should be labeled ‘polysilicon wiring 3c.’” Petition at 81. Solely for purposes of this Preliminary Response, Patent Owner will accept Petitioner’s correction.

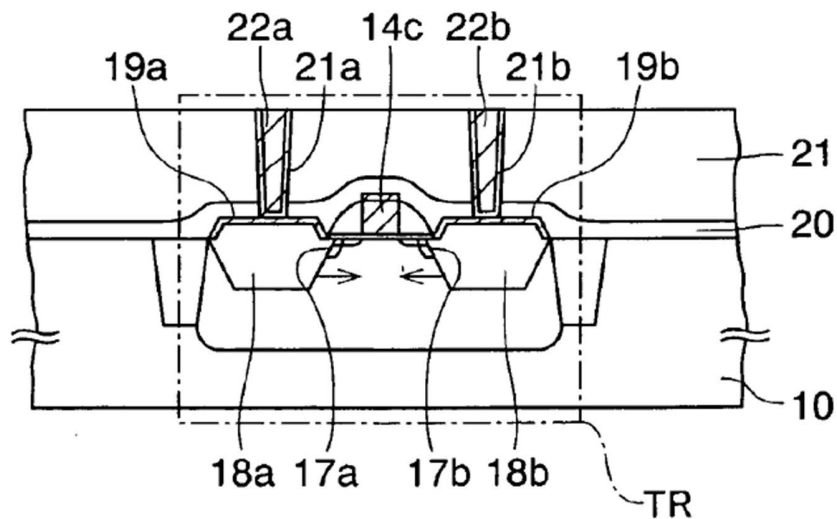


EX1010, FIG. 21 (excerpted)

The Petition concedes by omission that Saito does not teach *any* of the three stress-related limitations—namely, (1) “a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region” wherein “an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode”; (2) “a stress insulating film . . . which causes a second stress opposite to the first stress”; and (3) “a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer.” Petition at 32–35.

b) Fukutome (EX1011)

Fukutome is not directed to a memory or SRAM device, and the terms “SRAM” and “memory” are absent from the reference. The sole teaching of Fukutome on which the petition relies is “faceted ‘SiGe source/drain material layers 18a and 18b’ grown to ‘positions higher than the surface of the silicon substrate’ to suppress junction leakage and improve reliability,” Petition at 14, as shown in Fukutome Figure 5G, EX1011 at 7.



EX1011, FIG. 5G

c) James (EX1012)

James is not directed to a memory or SRAM device, and the terms “SRAM” and “memory” are absent from the reference. Rather, James is directed to various processors including a Sony graphics synthesizer, a Texas Instruments digital signal processor (“DSP”), and Intel’s Prescott processor. EX1012 at 1–2. According to the Petition, James teaches that (1) “[r]aised SiGe regions further improve PMOS

performance by reducing contact resistance,” Petition at 3; and (2) “it was also common to induce strain by applying stressed films,” Petition at 4. The Petition relies on James as teaching modifying Saito by using a “tensile silicon nitride CESL 13.” *Id.* at 92.

D. The Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art (“POSA”) “would have had at least a master’s degree in electrical engineering, physics, materials science, or a related field and at least three years of work experience in integrated circuit device design and manufacturing, including strained-channel MISFETs and fabrication thereof. Additional education could substitute for professional experience, and significant experience or training could substitute for formal education.” Petition at 8. It is unnecessary for Patent Owner to propose a competing definition at this time because, even under Petitioner’s proposed definition, Petitioner has failed to demonstrate a reasonable likelihood of success on any of the challenged claims. Patent Owner reserves the right to present evidence in support of a different definition of the level of ordinary skill in the art, if the Board institutes IPR.

III. LEGAL STANDARDS

“In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid*

Tech., Inc., 815 F.3d 1356, 1363 (Fed. Cir. 2016) (noting 35 U.S.C. § 312(a)(3) requires that petitions must identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”). To meet this burden, “[t]he petition must specify where *each element of the claim* is found in the prior art patents or printed publications relied upon.” 37 C.F.R. § 42.104(b)(4) (emphasis added). And “the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016). The burden of persuasion on the petitioner never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Applying the foregoing substantive standards and burdens, “[t]he Director may not authorize an *inter partes* review to be instituted unless the Director determines . . . that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

IV. CLAIM CONSTRUCTION

Claims are construed according to *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b). “Any prior claim construction determination concerning a term of the claim in a civil action . . . will be considered.” *Id.*

Petitioner argues that no claim terms require construction. Petition at 8. Patent Owner does not propose any claim constructions at this time because the Petition fails to demonstrate a reasonable likelihood of success.³

V. ARGUMENT

The Petition fails to show a reasonable likelihood of prevailing on any claim, under any Ground. As discussed below, Petitioner fails to meet the threshold for institution on claim 1—the sole independent claim—and this is true for every Ground of challenge. Because Petitioner’s theories on the dependent claims rely on the theories presented for claim 1, the Petition’s deficiencies with respect to claim 1 are fatal as to each Ground in its entirety.

A. *Ground 1 Fails*

Wu, in view of Alvarez, does not render obvious all the limitations of claim 1. As noted in Section II.B above, claim 1 of the ’425 patent recites several elements, including “a first sidewall spacer,” “a first source/drain region . . . which includes a silicon compound layer,” “a stress insulating film,” and “a first stress-relief film,” among others. Claim 1 further recites limitations governing the relationships of these elements to one another. For example, the “stress-relief film”

³ Patent Owner reserves the right to propose constructions in the event the Board grants institution.

must be “formed in a space between the silicon compound layer and the first sidewall spacer.” EX1001 at 20:4–5. In addition, the silicon compound layer of the first source/drain region must “caus[e] a first stress in a gate length direction of a channel region,” while the stress insulating film “causes a second stress opposite to the first stress.” *Id.* at 19:60–67.

Neither Wu nor Alvarez teaches or suggests “a stress insulating film . . . which causes a second stress opposite to [a] first stress” that is “in a gate length direction of a channel region” and caused by “a silicon compound layer,” as required by claim 1. Nor do they teach or suggest a “stress-relief film” that is “formed in a space between the silicon compound layer and the first sidewall spacer,” as claim 1 recites. Even in combination, Wu and Alvarez do not render obvious the missing limitations because, *inter alia*, Petitioner fails to identify a rationale that would lead a POSA to combine the references in the manner proposed by the Petition.

1. Wu and Alvarez Do Not Disclose or Render Obvious the Claimed Stress Relationship Between a Silicon Compound Layer and a Stress Insulating Film

Neither Wu nor Alvarez teaches or suggests the claimed relationship between opposite stresses caused by a silicon compound layer and a stress insulating film. Petitioner identifies Wu’s “epitaxial layer 58 of silicon germanium” as the silicon compound layer of claim 1. Petition at 32 (quoting EX1005 ¶ [0021]).

Petitioner further asserts that epitaxial layer 58 “compress[es] the channel.” *Id.* (quoting EX1005 ¶ [0021]) (alteration in original). The Petition then identifies Wu’s “contact etch stop layer (CESL) 66” as the alleged stress insulating film of claim 1. *Id.* at 33 (citing EX1005 ¶¶ [0025], [0044], FIGS. 7, 14).

However, to teach the claimed stress relationship, the stress from the Wu’s stress insulating film must be “opposite” of the compressive stress in epitaxial layer 58. But Wu teaches that the CESL may be strained or unstrained. EX1005 ¶ [0025] (“The material of the CESL 66 may include a dielectric material or a strained silicon material.”). And even Petitioner’s own expert admits that, if the CESL is stressed, Wu “does not specify whether the strain [in the CESL] is tensile or compressive.” EX1003 ¶ 162. As discussed below, a POSA would have understood that a tensile CESL deposited over the silicon germanium layer in Wu would negatively affect the transistor’s performance, as compared to a CESL composed of an unstrained dielectric material or compressive material. Petitioner therefore fails to show that a POSA reading Wu would have understood CESL 66 to cause a tensile stress in the channel region of the PMOS transistor of the cited embodiment.

Alvarez also does not teach or suggest a silicon compound layer of a source/drain region and a stress insulating film with opposite stresses on the channel region. Indeed, as mentioned above, Alvarez does not teach or suggest a silicon compound layer being included in the source/drain region at all. Without a silicon

compound layer causing “a first stress in [] a channel region,” Alvarez cannot possibly suggest a stress insulating film causing “a second stress *opposite to the first stress*,” EX1001 at 19:60–67 (emphasis added), because the first stress does not exist in Alvarez.

Because this limitation is absent from both Wu and Alvarez, the Petition uses the claimed invention as a guide for stitching together disparate teachings of the references into a Frankenstein’s monster—presented by the Petition as Figures A and A’. Petition at 23–24, 29–30. Petitioner argues that this hindsight-motivated combination satisfies the limitations of claim 1 that are missing from the cited art, but this argument fails for at least the following reasons.

The Petition asserts that a POSA would have combined Wu and Alvarez as proposed in Figures A and A’ to mitigate certain problems, but those problems are *created* by Petitioner’s Frankenstein-esque implementation. That problematic implementation is apparently motivated by Petitioner’s desire to challenge the ’425 patent. For example, Petitioner changes Wu’s CESL 66 from an unstrained CESL 66 to a CESL that exhibits tensile stress. Petition at 18. Then, since the CESL 66 now has tensile stress, that strained CESL would negatively affect the performance of the PMOS. *See* Section II.A, *supra*. To fix the negative effects of the stressed CESL on the PMOS, Petitioner then adds in a stress control layer 226 from Alvarez. Petition at 19–20. Petitioner fails to show any other reason, apart from its hindsight

reconstruction of the claims, why a POSA would have arrived at the proposed arrangement.

First, the Petition overstates Wu’s teachings. As noted above, Wu does not disclose that CESL 66 should be strained with tensile strain. Wu mentions that the CESL in the embodiment in Figures 1–7 “*may* include . . . a strained silicon material, i.e., silicon nitride.”⁴ EX1005 ¶ [0025]. Even assuming a strained material

⁴ There is no mention of the material used in the CESL in the embodiment of Figures 9–14. *See* EX1005 ¶ [0044]. The Petition conflates both embodiments in cobbling together Figures A and A’, *see* Petition at 17–18 (annotating FIG. 14 to identify a “[s]pace between raised SiGe and sidewall” and citing description of FIGS. 1–7 for “strained” CESL), but never attempts to justify this combination of distinct embodiments, as required for obviousness. *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) (When “combining multiple embodiments from a single reference, or selecting from large lists of elements in a single reference, there must be a motivation to make the combination and a reasonable expectation that such a combination would be successful, otherwise a skilled artisan would not arrive at the claimed combination.”). This is yet another way in which Petitioner relies on hindsight reconstruction for Ground 1.

is selected, Wu does not specify whether it would be tensile or compressive. *See id.* In fact, Petitioner concedes that a silicon nitride CESL “may provide tensile stress, compressive stress, or no stress,” depending on how it is prepared. Petition at 4. Alvarez further supports this when it teaches that stress-controlling material 226 and stress-increasing material 216 are preferably “the same material . . . deposited using different parameters” to affect the resulting stress. EX1006 ¶ [0052]; *see id.* ¶ [0054] (quantifying differences in stress between the two materials).

In the absence of any express suggestion in the art, the Petition asserts that a POSA would “implement Wu’s strained CESL 66 with tensile strain to improve *NMOS* mobility.” Petition at 20 (emphasis added). But Petitioner admits that “[a] tensile CESL near a *PMOS* channel generally applies tensile stress to the channel,” which can “*lessen[] PMOS performance improvements.*” *Id.* at 4–5 (emphasis added) (citing multiple exhibits). Thus, by Petitioner’s own admission, a POSA would have understood that applying a tensile CESL in both the PMOS and NMOS regions would sacrifice PMOS transistor performance for the benefit of NMOS transistor performance.

This understanding provides a clear motivation ***not*** to sacrifice PMOS performance by using a tensile film, based on facts alleged in the Petition itself. Specifically, the Petition acknowledges that, PMOS is intrinsically “*much slower* than NMOS.” Petition at 2 (emphasis added). Although the Petition explains that

“[s]trained-silicon technology changed that,” *id.*, it provides no explanation as to why a POSA would sacrifice speed in an intrinsically slow PMOS transistor performance solely for purposes of making a fast NMOS transistor even faster. And the Petition’s reference teaches that any ensuing benefit to the NMOS transistor would likely be marginal because “the performance of NMOS devices is relatively difficult to improve.” EX1023 ¶ [0039]. Nothing in Wu’s or Alvarez’s teachings suggests otherwise.

Petitioner nevertheless improperly assumes that a POSA seeking “to improve NMOS mobility” using a tensile CESL would have been motivated to use that same tensile CESL *in the PMOS region*. See Petition at 20 (arguing it was obvious to “mitigate the adverse effects of tensile CESL 66 on PMOS carrier mobility”). Petitioner must prove (not assume) the existence of that motivation. See, e.g., *Procter & Gamble Co. v. Teva Pharms. USA, Inc.*, 566 F.3d 989, 994 (Fed. Cir. 2009) (“A party seeking to invalidate a patent based on obviousness must demonstrate ‘by clear and convincing evidence that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.’” (quoting *Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1361 (Fed. Cir. 2007))). Petitioner failed to present any evidence or argument as to why a POSA would sacrifice the performance of the PMOS transistors for that

of the NMOS transistors.

Indeed, the cited art suggests a POSA would *not* have been motivated to modify Wu in the proposed manner. Wu and Alvarez both teach manufacturing processes in which a silicon nitride layer is selectively formed on, or selectively removed from, the NMOS region and/or the PMOS region at various points in the respective processes. *See, e.g.*, EX1005 ¶¶ [0019]–[0020], [0040], FIGS. 2, 3, 10, 11 (“sacrificial layer 52” preferably comprises “silicon nitride” and is selectively removed from “P well 34” during fabrication steps); EX1006 ¶ [0065]. In fact, Alvarez specifically discusses forming a strained silicon nitride layer over only the PMOS region or only the NMOS region. *See* EX1006 ¶ [0065]; *see also id.* ¶¶ [0043], [0052], [0063]. CESL 66 could therefore include a strained silicon nitride film causing tensile stress selectively formed over the NMOS region and a compressive or unstrained silicon nitride selectively formed over the PMOS region.

Petitioner thus fails to show that a desire “to improve NMOS mobility” would have motivated a POSA implementing Wu’s CESL to use a tensile CESL over the PMOS region of the transistor. As a consequence, Petitioner fails to show that Wu and Alvarez render obvious “a stress insulating film” that “causes a second stress opposite to the first stress,” in the manner alleged.

Petitioner therefore fails to show a reasonable likelihood of prevailing on Ground 1 as to independent claim 1, as well as the challenged dependent claims.

2. Wu and Alvarez Do Not Disclose or Render Obvious the Limitations of the “Stress-Relief Film”

Wu, even in combination with Alvarez, does not disclose or render obvious a “stress-relief film” that is “formed in a space between the silicon compound layer and the first sidewall spacer,” as recited by claim 1. This provides another independent reason why Petitioner fails to show a reasonable likelihood of prevailing on Ground 1.

First, neither reference teaches the “stress-relief film” of claim 1. Petitioner concedes that Wu does not teach or suggest a “stress-relief film” at all. *See* Petition at 35. It is therefore undisputed that Wu does not supply this element. *A fortiori*, Wu also cannot teach that the “stress-relief film” is formed in the recited space (or anywhere else). Again, this is not disputed. *Id.* Rather, Petitioner asserts that Alvarez’s “stress-controlling material” (226/326/426) constitutes the “stress-relief film” of claim 1. *Id.*

Alvarez, however, does not teach or suggest a “silicon compound layer.” The Petition relies exclusively on Wu for the “silicon compound layer” of the “first source/drain region.” *Id.* at 32. Alvarez barely even mentions “the source and drain regions” (not labeled in any of Alvarez’s Figures), but Alvarez does state that they “typically comprise silicon or polysilicon” without suggesting any silicon compound. EX1006 ¶ [0030]. Because it lacks a first source/drain region that

includes a silicon compound layer (as recited by claim 1), Alvarez cannot possibly teach forming anything in a space *between* the (nonexistent) silicon compound layer and the first sidewall spacer.

Second, as shown above, the Petition has offered no rationale why a POSA would have unnecessarily sacrificed PMOS performance by using a tensile CESL over Wu's PMOS region. Accordingly, there are no "adverse effects" from doing so that need to be "mitigate[d]." Petition at 20. In other words, if an unstressed or compressive film were used in the PMOS region, there would be no reason why a stress-relief film would be needed or desirable. Petitioner's failure to establish a motivation for using a tensile CESL over the PMOS region therefore also undermines the proffered motivation for applying Alvarez's stress-controlling layer 226/326/426 and/or 350/450 between Wu's silicon germanium 58 and CESL 66.

Even assuming a POSA would have used a tensile CESL over Wu's PMOS region, as Petitioner contends, the Petition fails to show that a POSA would have been motivated to form Alvarez's "stress controlling material" in a space between Wu's silicon germanium 58 and oxide layer 501A. First, Wu already proposes a solution for the supposed problem of mitigating any adverse stress effects from the CESL. In particular, Wu explains that "the preferred epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30" in part "to keep the silicon layer formed in the following steps" at some distance from the

source/drain interface with the channel. EX1005 ¶ [0041]. Wu also explains that the height of the epitaxial layer helps to “compress the channel.” *Id.* In other words, a POSA reading Wu would conclude that the silicon germanium that projects above the top surface of the substrate would already perform the function of compressing the channel.

Compressing the channel is the same function Alvarez describes for its “stress-controlling material,” namely “screen[ing] or control[ling] the amount of stress that a subsequently deposited stress-increasing material has on an underlying material layer, such as channel regions of the transistors.” EX1006 ¶ [0043]. Alvarez’s “stress-controlling material” (or “first material”) performs this function in two ways. It creates compressive stress to counteract part of the tensile stress created by the “second material” on top of it. *See id.* ¶ [0054] (Table 1). And it creates distance between the “second material” and the channel region, which decreases the impact of the stress created by the “second material.” *See id.* ¶ [0050] (noting that the proximity of the “first material” screens the impact of the stress from the “second material,” which is greater in regions where the “first material” is absent).

In short, a POSA looking to implement Wu’s teachings in combination with a tensile CESL would have understood that the raised epitaxial regions 58 already provide a compressive material and create distance between the unstrained CESL

66 and the channel region. Petitioner offers no rationale for why a POSA seeking to further mitigate tensile stress would have inserted a new layer composed of a completely different material—Alvarez’s “stress-controlling material”—rather than, for example, increasing the height of Wu’s silicon germanium to achieve the same effect. *See* Petition at 20. According to Petitioner’s own expert, a POSA would have been motivated to reduce costs by reducing the number of lithography steps in the manufacturing process. EX1003 ¶119. Using the additional layer of material taught by Alvarez would only increase the number of steps and resulting costs.

Second, Petitioner fails to identify any reason why it would have been obvious to use Alvarez’s “stress-controlling material” to form a stress-relief film *in a space between Wu’s epitaxial layer 58 and oxide layer 501A*. As explained *supra*, that space is an artifact of removing sacrificial layer 52 after the epitaxial growth of the raised silicon germanium. EX1005, FIGS. 11, 12. Wu never mentions that space or discloses any benefit to its existence, much less identifies any reason to fill it with a stress-relief film.⁵ *See id.* ¶¶ [0040]–[0041]. Likewise, the Petition never identifies any reason why a POSA would have been motivated to create a

⁵ Indeed, given that Wu discloses that CESL can be an unstrained dielectric material, there would be no need for a stress relief film.

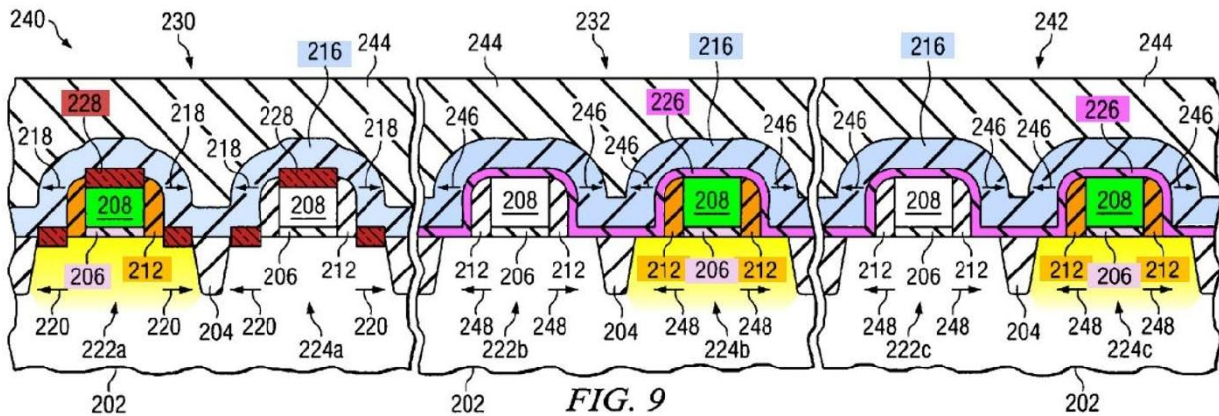
space between Wu’s epitaxial layer 58 and oxide 501A, nor any reason why that space should be filled by any particular kind of material, let alone a stress-relief film. *See* Petition at 20.

The sole suggestion anywhere in the record to form a stress-relief film in a space between a raised silicon compound layer and the sidewall of a gate electrode comes from the ’425 patent itself. *See* EX1001 at 12:59–62, 15:62–16:11. Only the ’425 patent suggests there is value in combining a raised silicon compound with a stress relief film to achieve the separation of “stress insulating film 31 . . . from the channel region.” *Id.* at 16:2–6. Moreover, the ’425 patent supports the value of this combination, despite the need for additional lithography steps to expose the upper surfaces of several components, including the “p-type source/drain region 27a” that comprises silicon compound 23. *Id.* at 12:63–13:6. As noted above, increasing the number of steps increases costs, and (according to Petitioner’s own expert) a POSA would have been motivated to reduce lithography and other processing steps. EX1003 ¶ 119.

Petitioner nevertheless attempts to reconstruct the claims without any evidence whatsoever that a POSA would have been motivated to combine the particular features of Wu and Alvarez to achieve the invention of claim 1. Instead, Petitioner just assumes a POSA would have made various choices in combining Wu and Alvarez, often without even acknowledging there is a choice to be made. These

choices are essential to Petitioner arriving at Figures A and A'. Given the absence of any other justification, the only apparent explanation for these choices is that Petitioner is using the claims as a roadmap to reconstruct the invention.

For example, the Petition assumes a POSA would select an epitaxial layer 58 made of silicon germanium and raised above the substrate for use in its stitched-together Figures. But Wu also discloses that layer 58 “may be substantially leveled with or lower than the top surface of semiconductor substrate 30.” EX1005 ¶ [0021]. If the top surface of the epitaxial layer were leveled with the top surface of the substrate, it would make the surface topography of Wu’s PMOS region similar to that of the surfaces of transistors 224*b* and 224*c* on which Alvarez applies its “stress-controlling material” 226 (magenta), as Petitioner proposes (*see* Petitioner’s annotations to Figure 9, below). This option would mean that no space would exist between Wu’s epitaxial layer 58 and oxide 501A, and thus the alleged stress-relief film could not be “formed in a space between the silicon compound layer [alleged by the Petition to be Wu’s epitaxial layer 58] and the first sidewall spacer [alleged by the Petition to be Wu’s oxide 501A],” as recited in claim 1.



Petition at 25 (annotating EX1006, FIG. 9)

Moreover, Wu discloses the formation of a salicide layer on epitaxial layer 58 to improve the electrical connection between the source and drain to the upper metallization layers. EX1005 ¶ [0021]. In Figure A' (reproduced below), Petitioner self-servingly draws that salicide layer—the red layer above epitaxial layer 58—thinly enough that a small space remains between epitaxial layer 58 and oxide 501A.

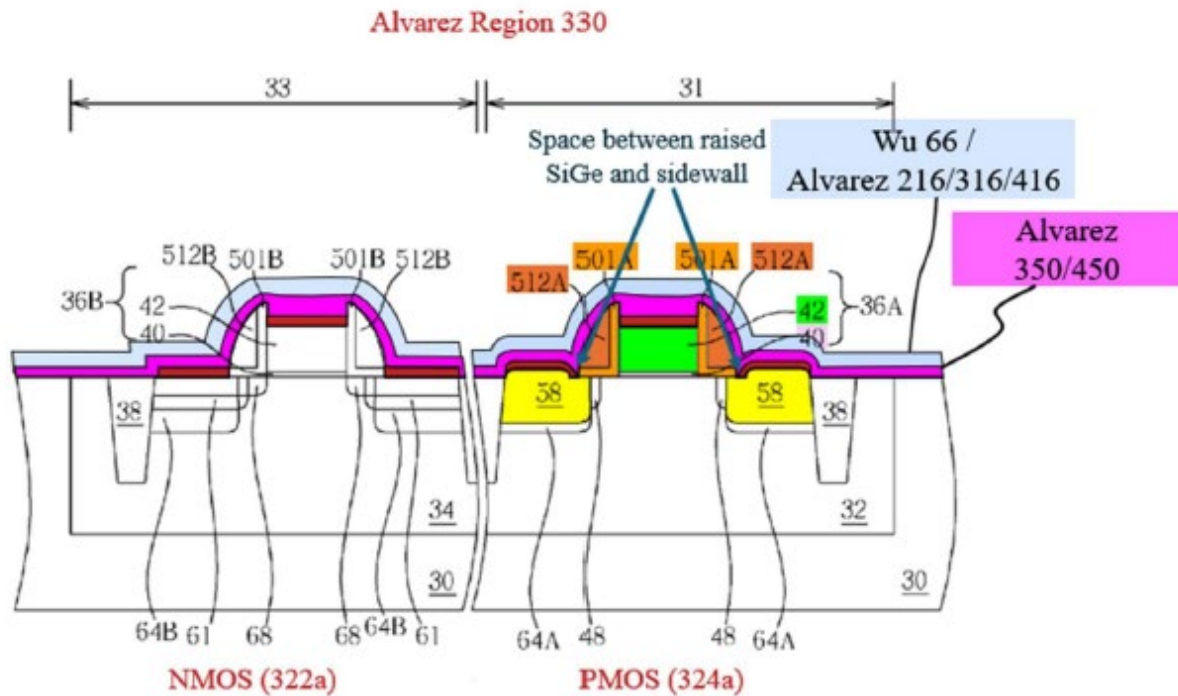


Figure A'
Petition at 37

But if the Petition had drawn Figure A' with a thicker salicide layer—e.g., the thick salicide (colored red) in annotated Alvarez Figure 9 above—no such space would exist. Given that neither Wu nor Alvarez suggests their Figures are drawn to scale, Petitioner's self-serving decision to select the dimensions of various features in its own annotations cannot be treated as evidence to support obviousness. Indeed, under Federal Circuit precedent, "it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue." *Hockerson-Halberstadt, Inc. v. Avia Grp. Int'l*, 222 F.3d 951, 956 (Fed. Cir. 2000). For that

reason, it is improper to base an argument on “an inference drawn from certain figures about the quantitative relationship between the respective widths” of depicted elements therein. *Id.*

For at least these reasons, Ground 1 fails.

B. Ground 2 Fails

Petitioner cannot establish a likelihood of prevailing on Ground 2 because Cheng, alone or in view of Wang,⁶ does not render obvious all the limitations of claim 1. First, as explained *infra*, it is undisputed that Cheng *as written* does not teach or suggest a “stress-relief film” that is “formed in a space between the silicon compound layer and the first sidewall spacer,” which Petitioner refers to as limitation [1H]. Petition at vii. Indeed, Cheng does not disclose *any space* between the alleged silicon compound layer and the alleged sidewall spacer. Instead, Petitioner fabricates this space in Cheng by making a “correction” that has no support from Cheng’s disclosure. Second, even if Petitioner’s correction had merit, the Petition presents no evidence that the structure identified as the “stress-relief film,” Cheng’s dummy spacer 416a, performs stress relief. Cheng does not

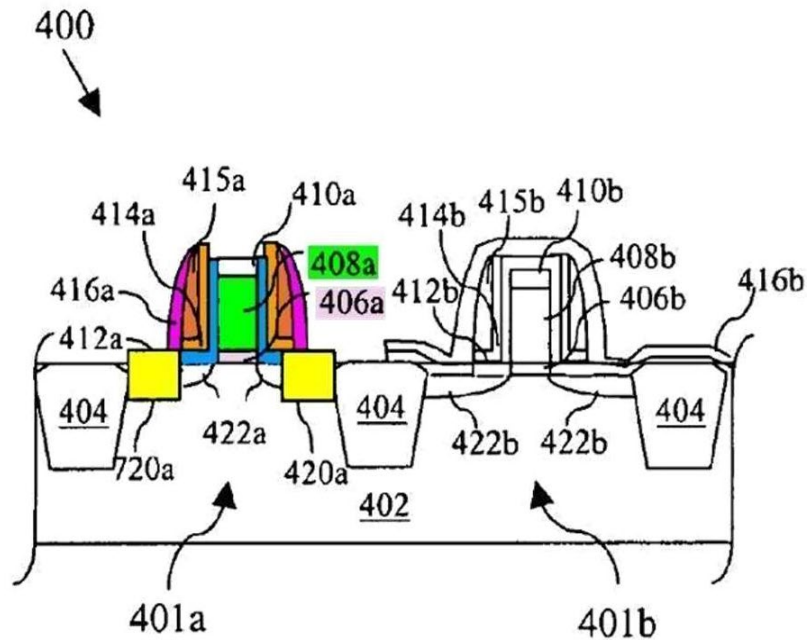
⁶ Petitioner does not otherwise rely on Wang as a substantial basis for Ground 2 against claim 1.

expressly disclose that dummy spacer 416a relieves any stress, nor is there any evidence that the dummy spacer inherently satisfies that requirement.

Petitioner does not contend that Wang cures the defects of Cheng with respect to this limitation. Rather, Petitioner relies on Wang solely to “help[] demonstrate how a POSITA would have understood Cheng’s disclosures,” referring to the purported “rendering error” in Cheng’s Figure 4e. Petition at 55, 56. As shown below, Cheng’s text does not support Petitioner’s theory that Cheng’s Figure 4e contains an error in need of “correction.” For the foregoing reasons and others as set forth below, the Petition fails to establish a reasonable likelihood of prevailing on claim 1 (or any of its dependent claims) based on Ground 2.

1. Petitioner’s Flawed “Correction” Theory Has No Support in the Cited Art

As depicted graphically in Petitioner’s annotated version of Figure 4e below, the Petition relies on (1) orange sidewall structures 414a and 415a in Cheng Figure 4e as the alleged first sidewall spacer in claim 1 of the ’425 patent, Petition at 61; (2) yellow doped source drain regions 420a in Cheng Figure 4e as the alleged silicon compound layer in claim 1 of the ’425 patent, *id.*; and (3) magenta dummy spacer 416a in Cheng Figure 4e as the alleged stress-relief film in claim 1 of the ’425 patent, *id.* at 65.

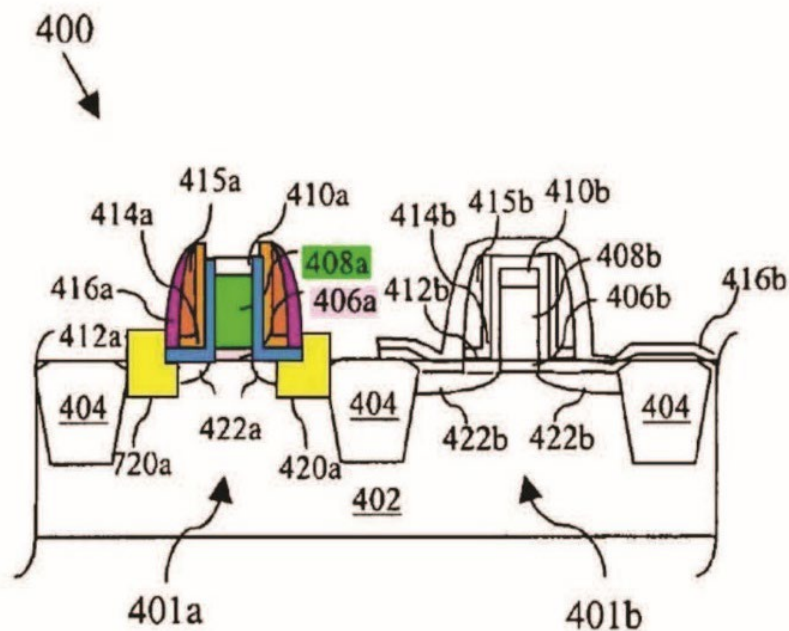


Cheng, Fig. 4e
Petition at 56

As depicted in this annotated figure, no space exists between the alleged silicon compound (*i.e.*, yellow doped source drain regions 420a) and the alleged first sidewall spacer (*i.e.*, orange structures 414a and 415b), as recited in claim 1 of the '425 patent. EX1001 at 20:4–5. And obviously, therefore, the alleged stress-relief film (*i.e.*, magenta dummy spacer 416a) is not situated in this non-existent space, as would be required to satisfy the limitation in claim 1. Note also that sidewall structure 412a (annotated blue by Petitioner) does not extend under magenta dummy spacer 416a.

In its attempt to contrive the recited “space” and locate magenta dummy spacer 416a in it, Petitioner asserts that Figure 4e needs to be “corrected,” as shown

below. Petition at 57. These purported “correct[ions]” modify the yellow doped source drain regions 720a and 420a, significantly raising their height such that they extend well above the base of the dummy spacer 416a and sidewall structures 414a and 415b. Petitioner also extends the blue sidewall structures 412a such that they extend all the way under magenta dummy spacers 416a.



Cheng, Fig. 4e (corrected)

Petition at 57

Petitioner then extrapolates from its “corrected” Figure 4e to yield a doctored version of Cheng’s Figure 4j, which Petitioner labels “Figure I” (reproduced below). The Petition’s mapping of Cheng’s features to ’425 patent claim 1’s limitations is premised on this doctored drawing.

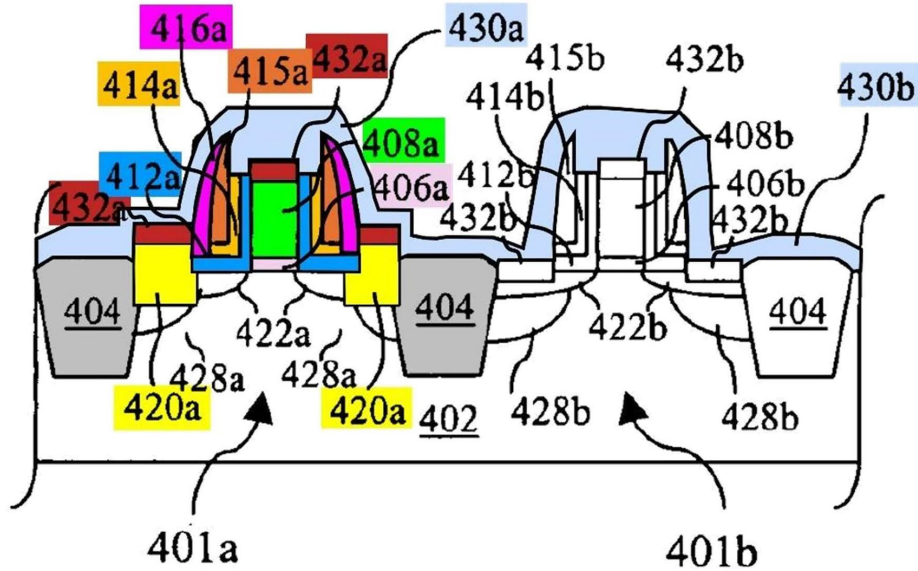


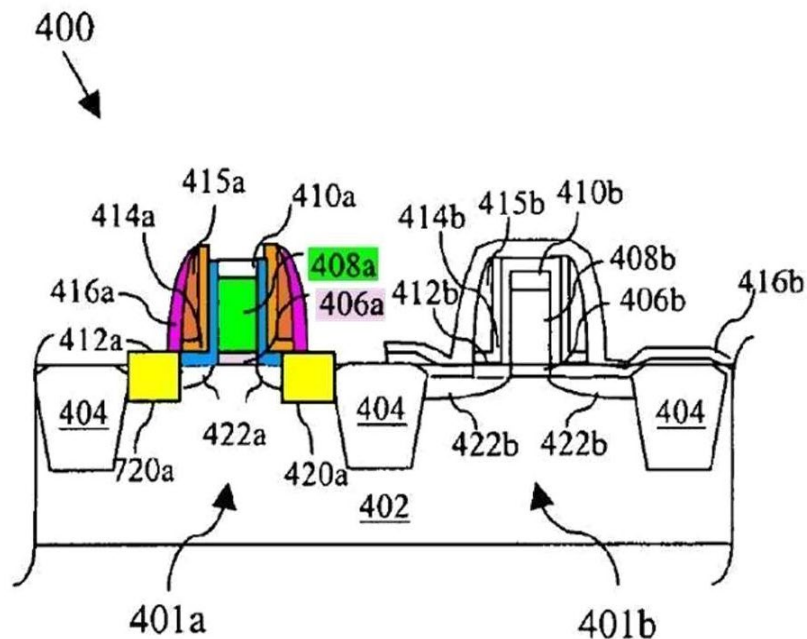
Figure I (Cheng, Fig. 4j, corrected)

Petition at 58

But the Petition’s “correction” to Cheng’s Figure 4e is unjustified.⁷ As it originally appears in Cheng, Figure 4e (below, annotated) shows the tops of yellow doped source drain regions 420a and 720a are coplanar with blue sidewall 412a. Even assuming it were proper to “correct” Figure 4e by extending blue sidewall 412a under magenta dummy spacer 416a, the coplanar relationship between the tops of yellow doped source drain regions 420a and 720a and blue sidewall 412a would create no space between the alleged silicon compound (*i.e.*, yellow doped source

⁷ Although neither of the Petition’s two “corrections” is appropriate, solely for purposes of this Preliminary Response, Patent Owner will focus on the adjustment to the height of the source drain regions 720a and 420a.

drain regions 420a and 720a) and the alleged first sidewall spacer (*i.e.*, orange structures 414a and 415b). Ground 2 therefore necessarily requires departing from the coplanar relationship between the tops of yellow doped source drain regions 420a and 720a and blue sidewall 412a by increasing the height of the yellow doped source drain regions 420a and 720a such that they extend above the top of blue sidewall 412a. But nothing in Cheng's disclosure shows that this coplanar relationship is an error in need of correcting, as Petitioner asserts.



Cheng, Fig. 4e
Petition at 56

Instead of relying on the express disclosure of Cheng to interpret Figure 4e, Petitioner relies on its expert, who engages in sleight of hand to justify increasing the height of doped source drain regions 720a and 420a. First, he compares the

disclosed “thickness” range of gate dielectric 406a with the disclosed range of the “height of raised source/drain regions” and concludes that the top of the doped source drain regions 720a and 420a must extend above the top of gate dielectric 406a. EX1003 ¶ 269. Second, he assumes that the thicknesses of gate dielectric 406a and spacer 412a are the same. *See id.* Third, he therefore concludes that the source/drain region is “substantially higher than the thickness of the gate dielectric 406a *and spacer 412a* (blue).” *Id.* (emphasis added). There are multiple flaws in his chain of logic.

First, Cheng does not disclose that the thickness of gate dielectric 406a and sidewall 412a are the same, as Petitioner’s expert erroneously assumes. His assumption is premised on their Figure 4e, which depicts them as having similar thicknesses. *Id.*; *see* EX1008, FIG. 4e. However, Cheng specifically states that the reader should not make any assumptions about the size and scale of features, which may be “arbitrarily increased or reduced for clarity of discussion.” EX1008 ¶ [0004]. Moreover, to the extent Figure 4e’s scale carries any weight—despite Cheng’s express teaching that it does not—the fact that it shows sidewall 412a and doped source-drain regions 420a and 720a are coplanar (which the Petition self-servingly discredits) is no less credible than the coplanarity of sidewall 412a and gate dielectric 406a (which the Petition self-servingly credits).

Second, Petitioner's expert's analysis of the height of the source/drain regions is flawed. He surreptitiously adds the phrase "above the substrate" when quoting Cheng's disclosure that "[t]he height of raised source/drain regions may range between about 5 nm and about 100 nm." EX1008 ¶ [0022]; EX1003 ¶ 269. This additional phrase significantly changes the meaning of Cheng's disclosure, and it is not consistent with Cheng's use of the term "height." For example, Cheng discusses the height of gate electrode 124, and then separately discusses the "combined height HP above [the] surface 106 of the substrate 104" of the gate electrode 124 and the gate dielectric layer 120. EX1008 ¶ [0019]. In other words, Cheng discusses the height of a structure "above the surface of the substrate" when intended. Thus, Cheng's disclosure of source/drain regions with a height ranging between 5 nm and 100 nm refers to the total height (including the portion in the recessed region below the surface), not just the height of the portion above the surface.

Third, the quoted height range in any event appears in the context of Cheng's description of source/drain regions 136 in Figure 1, *id.* ¶ [0022], not its description of the embodiment in Figure 4e. Cheng expressly teaches that source/drain regions 136 "may extend above the substrate surface 106." *Id.* In contrast to this disclosure and to Cheng's description of "source/drain regions 320a" in Figure 3j as "raised," Cheng make no explicit mention that source/drain regions 420a, 720a extend (or are

raised) above the substrate at all. *Compare id.* ¶¶ [0022], [0044] *with id.* ¶ [0065]. Instead, Cheng merely describes these source/drain regions being “formed or built-up *in the recessed region* 418a.” *Id.* ¶ [0065] (emphasis added).

Petitioner’s expert thus had no basis for his assumption that source/drain regions 420a and 720a in Figure 4e extend above the substrate by the maximum value (*i.e.*, 100nm) given for the *total* height of source/drain regions *in a different embodiment*. Indeed, this assumption reeks of hindsight motivation. Combined with the unwarranted assumptions about the undisclosed thickness of sidewall 412a, this is how Petitioner creates the space between the doped source drain regions (720a and 420a) and sidewall spacers (414a and 415a) needed to support its obviousness theory. But neither Cheng nor Wang suggests any benefit stemming from creating such a space, nor has Petitioner identified any benefit from doing so. The expert therefore lacked any basis for arbitrarily selecting 100 nm as the height for the portion of the doped source/drain regions 420a, 720a, much less asserting that the entirety of the 100 nm height was above the surface.

Without its unjustified “correction” to Cheng’s disclosure, Petitioner cannot show that Cheng discloses or renders obvious the alleged stress-relief film being “formed in a space between the silicon compound layer and the first sidewall spacer.” Because that limitation is missing, the Petition cannot prevail on

obviousness for claim 1 or any of the challenged dependent claims, which incorporate the limitations of claim 1.

2. Cheng Does Not Disclose a “Stress-Relief Film”

Independent of Petitioner’s defective “correction” theory, Ground 2 also fails because Cheng does not even disclose, expressly or inherently, that dummy spacers 416a are a “stress-relief film,” as the Petition argues. The entirety of the Petition’s analysis for limitation [1H] is less than one page. Petition at 65. At no point in that cursory discussion does the Petition cite any evidence that Cheng’s dummy spacers 416a would serve to relieve stress.

The Petition identifies no *express* teaching in Cheng that the dummy spacers are a “stress-relief film” or that they relieve stress in any way. To the contrary, the very term “dummy spacer” suggests that the purpose of these structures is to fill space during fabrication to control the dimension and shape of other features of the semiconductor device until the dummy spacers are later removed. For example, Cheng teaches that “portions of the dummy spacer material 416a [are] removed from the device 401a” by the process (*e.g.*, an etch) that forms the “recessed source and drain regions 418a . . . on either side of the gate structure.” EX1008 ¶ [0063]; *see, e.g., id.* ¶¶ [0045], [0081] (describing removal of dummy spacers during fabrication of other embodiments). To the extent residual dummy spacers 416a are

present in the final device 401a, Cheng does not expressly disclose that they perform any functional role—much less a stress related role—in that device.

Indeed, Petitioner does not appear to contend that Cheng expressly discloses that dummy spacers 416a perform any stress-relief function. Rather, the arguments in the Petition focus on the *position* of dummy spacers 416a in the modified version of Cheng’s device. *See* Petition at 65.

Absent express disclosure of a stress relief function, the Petition must meet the “high standard” for inherency, under which Petitioner must establish that Cheng’s dummy spacers 416a “necessarily” serve as a stress-relief film or that their stress-relief characteristic is “the natural result of the combination of elements explicitly disclosed by the prior art.” *Par Pharm., Inc. v. TWi Pharms., Inc.*, 773 F.3d 1186, 1195–96 (Fed. Cir. 2014). Neither the Petition nor Petitioner’s expert even acknowledge, much less attempt to satisfy, this exacting burden.

Instead, the Petition cites Cheng’s disclosure of “silicon dioxide (SiO₂)” as one possible material from which the dummy spacers can be made. Petition at 65 (quoting EX1008 ¶ [0063]). But Petitioner does not argue that silicon dioxide “necessarily” relieves stress, nor even that stress-relief is the “natural result” of using silicon dioxide in forming the particular dummy spacers disclosed in Cheng. *See id.* Rather, the Petition cites three references, each of which states that some particular feature *in that reference* (*i.e.*, not Cheng’s dummy spacers 416a) serves

some stress relief role in the transistor *in that reference* (i.e., not in Cheng’s transistor). *Id.* (citing EX1031 ¶ [0067]; EX1032 ¶ [0030]; and EX1029 ¶ [0034], ¶ [0042]). Petitioner also cites paragraphs 298–99 in its expert’s declaration, but its expert offers no explanation of how those other structures in the other references would have been understood by a POSA or informed a POSA’s reading of Cheng. EX1003 ¶¶ 298–99.

Petitioner’s expert merely states that “[t]he stress-relief film 28a [in the ’425 patent] is made of silicon oxide, like Cheng’s dummy spacer 416a.” EX1003 ¶ 298. That is not sufficient to meet Petitioner’s burden of proving that dummy spacers 416a *inherently* relieve stress. The fact that the ’425 patent envisions a stress-relief film formed from silicon oxide does not mean that all silicon oxide structures *necessarily* produce the same result. Indeed, Petitioner conceded that certain insulating materials used to form contact etch stop layers “may provide tensile stress, compressive stress, or no stress,” depending on how the layer is prepared. Petition at 4; *see also* EX1001 at 15:52–54 (describing “first stress-relief film” as being made of “insulating material”). Although Petitioner was referring specifically to CESLs made from silicon nitride, not silicon oxide, Cheng expressly discloses silicon nitride as another possible material for the dummy spacers 416a. EX1008 ¶ [0063].

This confirms that two materials with the same chemical formula do not necessarily have the same stress characteristics. Petitioner's comparison to the '425 patent's disclosure is therefore irrelevant to Petitioner's burden to show inherency. Moreover, unlike Cheng, the '425 patent expressly discloses that the purpose of "stress-relief film 28a" includes relieving stress from the stress insulating film 31 on the channel region. EX1001 at 16:2–9. There is accordingly no evidence that the '425 patent relies on chemical composition as the basis for the stress-relief characteristic, to the extent that is the Petition's implication.

Because there is no evidence that Cheng discloses, either expressly or inherently, that dummy spacers 416a satisfy the limitation of a "stress-relief film," the Petition fails as to Ground 2 on claim 1 (and therefore on each of the dependent claims).

C. Ground 3 Fails

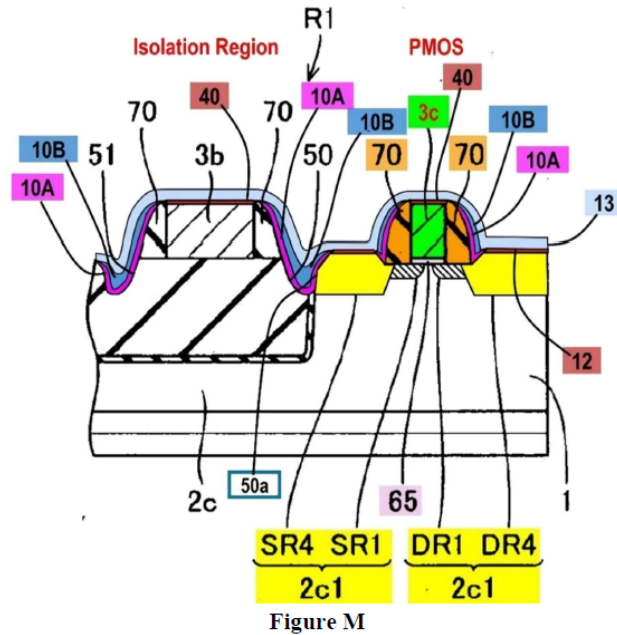
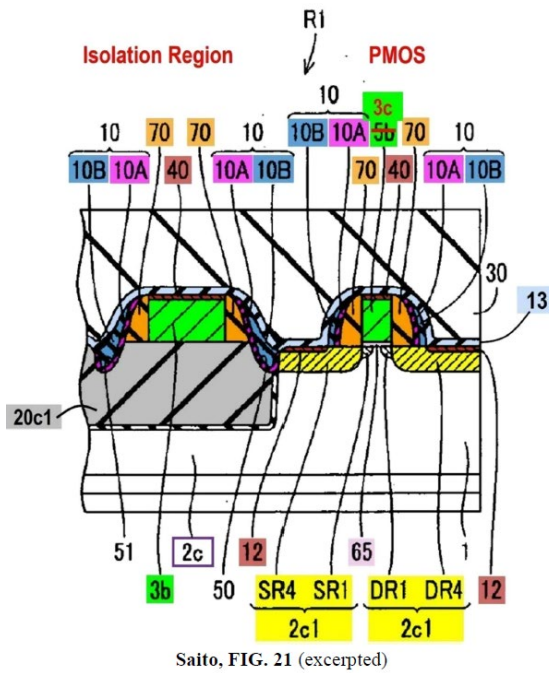
Ground 3 fails because Saito, in view of Fukutome and James, does not disclose or render obvious all the limitations of claim 1. Every claim of the '425 patent incorporates those limitations, and the Petition therefore fails to show a reasonable likelihood of prevailing on Ground 3 as to any claim.

Petitioner does not contend that the limitations of claim 1 are found in the express disclosures of the cited references. Instead, using the '425 patent's claim limitations as a roadmap, Petitioner designs them into the emergent properties of

fictional “Figure M,” another Frankenstein-esque drawing (like those fabricated in Grounds 1 and 2). This is again hindsight reconstruction of the claimed invention.

According to the Petition, Figure M is “similar to [Saito] FIG. 21.” It is not. While both are directed to a transistor,⁸ Figure 21 lacks all three elements of a novel combination of features present in the patented invention: (1) a silicon compound in the source or drain regions, much less one that exerts stress or is raised above the surface of the substrate; (2) a space between the nonexistent silicon compound and gate sidewall; and (3) a stress insulating film that exerts a stress opposite the stress from the source drain region.

⁸ Solely for purposes of this Preliminary Response, Patent Owner does not dispute that Figure 21 element 5b should be 3c.



Petition at 100 (left); Petition at 90 (right)

Ground 3 fails for three independent reasons. First, the Petition fails to establish a motivation to combine the teachings of a memory circuit like Saito with the logic circuits of the secondary references. Second, even if such a motivation existed, the Petition makes numerous unjustified (1) changes to the references' teachings, (2) cherry-picked selections from the references' teachings, and (3) assumptions about how a POSA would combine the features. Third, even assuming arguendo a POSA had a motivation to arrive at Figure M, it still does not disclose or render obvious the claimed invention.

1. Petitioner Fails to Establish a Motivation to Combine the Cited Art to Achieve the Claimed Invention

The Petition’s use of hindsight to concoct Figure M renders the entirety of Ground 3 defective because Petitioner fails to show any reason why a POSA would have combined the teachings of the cited art, which are directed to different types of circuits. This does not satisfy Petitioner’s burden to show that “a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve *the claimed invention*.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (internal quotation marks omitted) (emphasis in original).

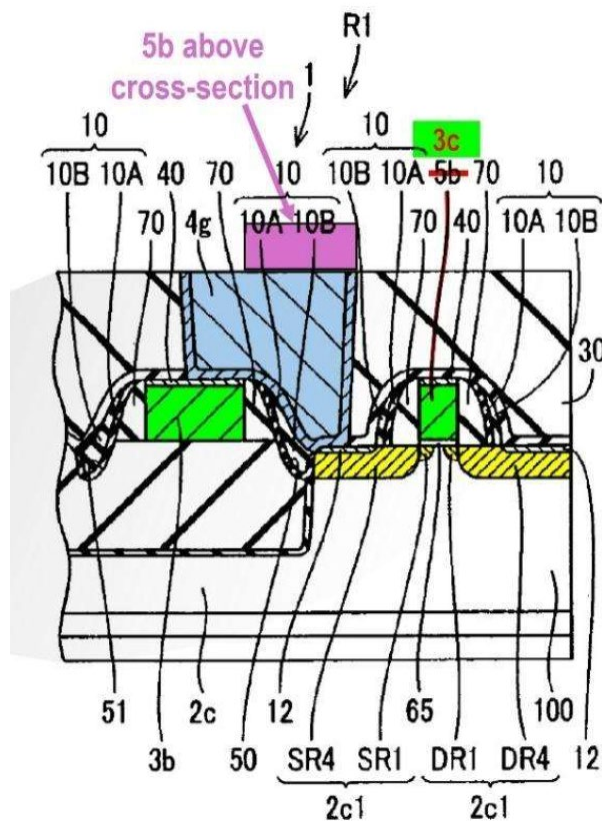
As an initial matter, the Petition offers only a conclusory reason—unspecified “performance,” Petition at 88—for using Fukutome’s epitaxially grown silicon germanium regions in a discrete SRAM memory device like Saito’s. But the Petition ignores entirely that the references are directed to very different types of circuits. Integrated circuits fall into two broad categories: those that store data (memory circuits) and those that process data (logic circuits). Logic circuits are generally manufactured using a logic process, *see, e.g.*, EX1015 at 1 (describing “the transistor structure used in a 90-nm generation CMOS *logic technology* designed for high speed and low power operation”) (emphasis added), whereas discrete memory circuits—like the standalone SRAM described in Saito—are generally manufactured with processes optimized around those devices. *See, e.g.*,

EX1046 at 8 (“SRAM designers are motivated to increase the packing density” and “the cell stability is of paramount significance.”). The Petition’s own references explain not only that “[s]trained-Si channel metal-oxide-semiconductor field-effect transistors (MOSFETs) are used in nearly all 90 nm and smaller commercial *logic* technologies,” EX1040 at 5 (emphasis added), but also that fundamental differences exist between logic processes used to fabricate logic products and memory processes used to fabricate memory products like SRAM, EX1046 at 11 (discussing “extra technological steps” in SRAM production that “are not a part of the standard CMOS logic technological process”).

The Petition never addresses the differences in how “performance” might be measured or assessed for MOS transistors in logic circuits (*e.g.*, microprocessors like Intel’s Prescott chip) versus MOS transistors in memory circuits. Indeed, Petitioner never even discloses what those key considerations are, let alone why a POSA seeking to improve an SRAM memory device would employ stressed silicon technology used in logic devices. Indeed, nowhere does the Petition identify any SRAM device in which stressed silicon germanium layers have ever been employed, much less ones raised above the surface of the substrate.

In addition, the Petition fails to address the fact that Fukutome and Saito have different layouts. Fukutome only displays a single gate, whereas Saito is directed to a PMOS directly next to an isolation gate. *See, e.g.*, EX1011, FIG. 13E; EX1010,

FIG. 12. Moreover, as the Petition acknowledges, Saito discloses a layered structure (including contact part 4g and polysilicon wiring) stacked on top of its non-raised, non-silicon compound PMOS source/drain layers. See Petition at 85 (excerpting and annotating EX1010, FIGS. 1, 12). This is highlighted by Petitioner’s own annotations to Saito’s Figure 12, shown below.



Petition at 85 (excerpting and annotating EX1010, FIG. 12)

The Petition’s generic assertion that “performance” would have motivated a POSA to “substitute Fukutome’s raised epitaxial SiGe PMOS source/drain layers for Saito’s” non-raised, non-silicon compound PMOS source/drain layers, *id.* at 87, is legally insufficient. See *ActiveVideo Networks, Inc. v. Verizon Communs., Inc.*, 694

F.3d 1312, 1328 (Fed. Cir. 2012) (finding expert testimony “insufficient” where it was “generic” and bore “no relation to any specific combination of prior art elements”).

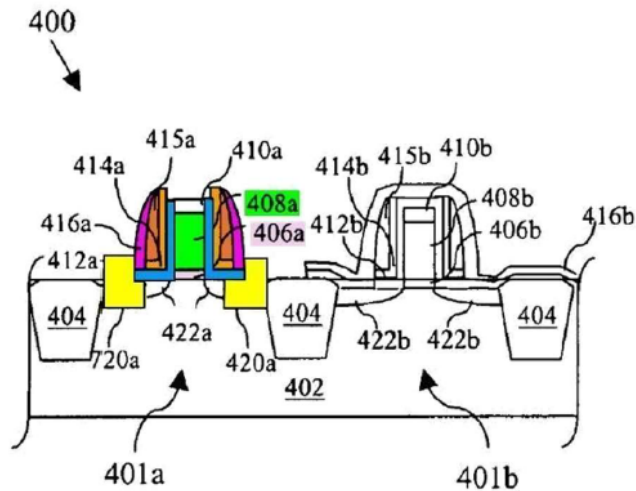
2. Even If a Motivation to Combine Existed, Figure M Does Not Result From that Motivation

Even assuming—incorrectly—that the Petition had substantiated a motivation to combine Saito with Fukutome (and James), Figure M is not the logical product of that combination. The Petition never explains why the generic desire for “performance,” Petition at 88, or the desire to “improve electron mobility in NMOS regions,” *id.* at 91, would motivate a POSA to combine James and Fukutome with Saito in the manner depicted in Frankenstein Figure M. Rather, as explained below, to arrive at Figure M from Saito’s Figure 21, the Petition makes numerous unjustified cherry-picked selections, changes to the references’ teachings, and self-serving graphical depictions. *See* Petition at 87–102. There is no evidence a POSA would have been motivated to make those choices or that Petitioner’s depictions reflect the natural result of the proposed combination.

First, the Petition “substitute[s] Fukutome’s raised epitaxial SiGe PMOS source/drain layers for Saito’s non-epitaxial PMOS source/drain layers.” *Id.* at 87. This substitution actually entails multiple changes because Saito’s source/drain layers are neither a “silicon compound” nor “located higher than a surface of the

semiconductor substrate,” as recited in claim 1. The Petition never explains how Fukutome’s raised epitaxial SiGe PMOS source/drain layers would translate to better performance in an SRAM circuit or how any allegedly better performance would justify the additional cost, processing steps, and processing time associated with epitaxial SiGe PMOS source/drain layers for an SRAM device.

Second, the Petition assumes that the raised epitaxial silicon germanium grows away from the gate structure, leaving a space between the two, without explaining why such a space would necessarily form. Although Fukutome Figure 5G does show a silicon germanium structure with slanted sides that appears to create a space between it and the gate structure, Petitioner’s “corrected” version of Cheng Figure 4e from Ground 2 (reproduced below) shows silicon germanium that is grown vertically along the gate structure.



Petition at 57 (modifying EX1008, FIG. 4e)

If the silicon germanium layer grows vertically, as shown in the Petition's modified version of Cheng's Figure 4e, no space will exist between the silicon germanium and the gate structure. And because the Petition asserts that Saito's 10A (the alleged "stress relief film") is grown after the silicon germanium epitaxial layer is created, *see* Petition at 89–90 (depicting addition of, *inter alia*, layer 10A in "Figure M"), there would be no space in which that alleged stress relief film could form, as required by claim 1. The Petition offers no explanation why a POSA would have been motivated to grow silicon germanium regions so as to leave a space to be filled later by layer 10A in Saito.

Third, the Petition assumes without explanation that insulating layer 10A and nitride layer 10B would be formed *after* the silicon germanium epitaxial layer but *before* the silicide film, *see id.* at 97 ("[L]ayers 10A/10B are . . . etched . . . for silicidation."), despite Fukutome's express teaching that the silicide is formed

immediately after the formation of the silicon germanium. More specifically, Fukutome teaches that silicide 19a and 19b are formed immediately after the formation of the silicon germanium 18a, 18b. *See* EX1011 ¶ [0103], Figs. 5E, 5F. Because the silicide in Fukutome is grown immediately after the raised silicon germanium layer is formed and implanted, the silicide layer would likely fill any space (if one existed) before Saito's 10A and 10B are deposited. In that case, the Petition's alleged stress relief film would not be "formed in a space between the silicon compound layer and the first sidewall spacer," as recited in claim 1.

To attempt to avoid this result, the Petition self-servingly disregards Fukutome's specified ordering of steps. But Petitioner offers no explanation for why a POSA would have thus departed from the teachings of the cited references, further supporting the conclusion that Figure M is the result of hindsight reconstruction. Apparently cognizant that this shortcoming eviscerates its obviousness theory, the Petition posits that "silicide film 12 forms atop the SiGe layers but not the SiGe facets (where insulating layer 10A would block silicidation)." Petition at 103. But Fukutome teaches that the silicide is formed on all of the exposed surfaces of the silicon germanium. *See* EX1011, Fig. 8C. In the absence of express teachings or some motivation to form insulating layer 10A before the silicide formation—neither of which exists here—Petitioner has the burden of showing that this ordering of the process steps is inherent, which requires

that it be the “natural result” of the combination. *Par Pharm.*, 773 F.3d at 1195–96. Petitioner makes no attempt to meet this burden.

Fourth, the Petition changes the shape of oxide layer 10A from that shown in Saito Figure 21. In Figure M, the Petition assumes that the oxide layer 10A would form in the same manner in the small crevice Petitioner concocted between the spacers 70 and the SiGe facets as the oxide layer 10A forms in the large gap in the isolation region. Petition at 100–01. But the Petition offers no evidence that materials form similarly in very small spaces and very large spaces, and Petitioner fails to present any evidence that oxide layer 10A would make the shape Petitioner drew for Figure M.

Fifth, the Petition selects a tensile nitride for film 13 in the PMOS transistor even though the Petition acknowledges that “[a] tensile CESL near a *PMOS* channel” can “*lessen[] PMOS performance improvements.*” Petition at 4–5 (emphasis added). As explained in Section V.A.2, a POSA would not sacrifice the performance of the PMOS for the performance of the NMOS. Figure M does not exist without this nonsensical choice.

3. Figure M Does Not Satisfy All the Limitations of the Claimed Invention

Even if a POSA were motivated to combine the references in the illogical manner proposed by the Petition and arrived at Frankenstein Figure M, it still would

not render the claimed invention obvious because other claim limitations are not taught by Figure M.

a) The “First-Stress Relief” Film Is Not Disclosed

The proposed combination does not teach or suggest “a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer,” as recited by claim 1. The Petition asserts that “Saito’s insulating film 10A (silicon oxide)” qualifies as the claimed “first stress-relief film.” Petition at 100. But even if insulating film 10A formed as shown in Figure M and met the spatial requirements set forth in the claim, the Petition makes no effort to show that silicon oxide film 10A is a “stress-relief film” as claimed.

The Petition identifies no express disclosure in Saito that insulating film 10A is a “stress-relief film.” Because Saito does not *expressly* disclose this functional role, the Petition must meet the “high standard” of showing that insulating film 10A inherently (*i.e.*, “necessarily”) provides stress relief. *Par Pharm.*, 773 F.3d at 1195–96 (“A party must, therefore, meet a high standard in order to rely on inherency to establish the existence of a claim limitation in the prior art in an obviousness analysis—the limitation at issue necessarily must be present, or the natural result of the combination of elements explicitly disclosed by the prior art.”). Neither the Petition nor its expert even acknowledge, much less attempt to satisfy, this burden.

The entirety of the Petition’s analysis for this limitation comprises two

paragraphs of text of text and two figures. *See* Petition at 99–101. The Petition never states or explains why insulating film 10A would *necessarily* serve to relieve stress. Instead, the Petition asserts based on its expert that “[a] POSITA would have recognized, and found obvious, that silicon oxide film 10A acts as a stress-relief film to buffer tensile strain from SiN layer 13 in PMOS active regions 2b/2c.” *Id.* at 101 (citing EX1003 ¶¶ 458–459). Petitioner’s expert, in turn, does not opine that insulating film 10A “necessarily” provides stress relief; instead, he merely asserts that “silicon dioxide layers were known to buffer stress in such a configuration.” EX1003 ¶ 458. But this assertion—even assuming it were true—would merely establish that other silicon dioxide films have *sometimes* provided stress relief in different devices, not that insulating film 10A “necessarily” provides stress relief in the Petition’s Frankenstein embodiment.

b) *“A Stress Insulating Film . . . Which Causes a Second Stress Opposite to the First Stress” Is Not Disclosed*

Limitation [1F] recites “a stress insulating film . . . which causes a second stress opposite to the first stress.” Petition at xii. No dispute exists that the silicon germanium layer posited by the Petition is compressive. Accordingly, Petitioner bears the burden of showing that Saito’s insulating film 13 would be tensile. The Petition, however, concedes that Saito is “silent regarding strain in SiN layer 13.”

Petition at 91. Despite that, the Petition asserts that a POSA would select a tensile stress to “enhance NMOS performance”:

A POSITA would have found a tensile SiN insulating film 13 obvious, as James discloses, because “[l]ocalized tensile stress is applied to the channels of NMOS devices,” which can “increase[] electron mobility” and “enhance NMOS performance” without “extra cost for either capital equipment or special substrates.” (James, 2, 5, Fig. 6; *supra* §II.B, §V.C.1.a(1)(b).) A tensile insulating film 13 would form over “[c]rystalline facets” of the “raised [SiGe] source/drains” (see Figure M). (James, 2; *see id.*, Fig. 6; Ex-1003 ¶¶448-450.)

Id. at 97–98. That argument is premised on a benefit accruing to NMOS transistors from a tensile film. But the transistor in Figure M is a PMOS transistor, not an NMOS transistor. *Id.* at 101. As the Petition concedes, “[a] tensile CESL near a **PMOS** channel generally applies tensile stress to the channel,” which can “**lessen[] PMOS performance improvements.**” *Id.* at 4–5 (emphasis added). The Petition does not explain why a POSA would disadvantage the PMOS transistor in Figure M to benefit a NMOS transistor that is not in Figure M.

VI. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board decline to institute IPR.

Dated: July 18, 2025

Respectfully submitted,

By: / Russell A. Chorush /
Russell A. Chorush (Reg. No. 55,689)
Attorney for Patent Owner
Advanced Integrated Circuit Process, LLC

CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a copy of the foregoing PATENT OWNER PRELIMINARY RESPONSE was served to counsel of record for Petitioner as follows:

Lead Counsel for Petitioner	Back-up Counsel for Petitioner
J. Preston Long, (Reg. No. 65,125) jp.long@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 901 New York Avenue NW Washington, DC 20001-4413 Tel: 202-408-4347 Fax: 202-408-4400	Kevin D. Rodkey, (Reg. No. 65,506) kevin.rodkey@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 271 17 th Street NW, Suite 1400 Atlanta, GA 30363-6209 Tel: 404-653-6484 Fax: 404-653-6444

Dated: July 18, 2025

By: / *Russell A. Chorush* /
Russell A. Chorush (Reg. No. 55,689)
Attorney for Patent Owner
Advanced Integrated Circuit Process,
LLC

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned hereby certifies that this brief complies with the type-volume limitation of 37 C.F.R. § 42.24 because this brief contains 11,810 words.

Dated: July 18, 2025

Respectfully submitted,

By: / *Russell A. Chorush* /
Russell A. Chorush (Reg. No. 55,689)
Attorney for Patent Owner
Advanced Integrated Circuit Process,
LLC