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(54) **METHOD TO ENHANCE DEVICE PERFORMANCE WITH SELECTIVE STRESS RELIEF**

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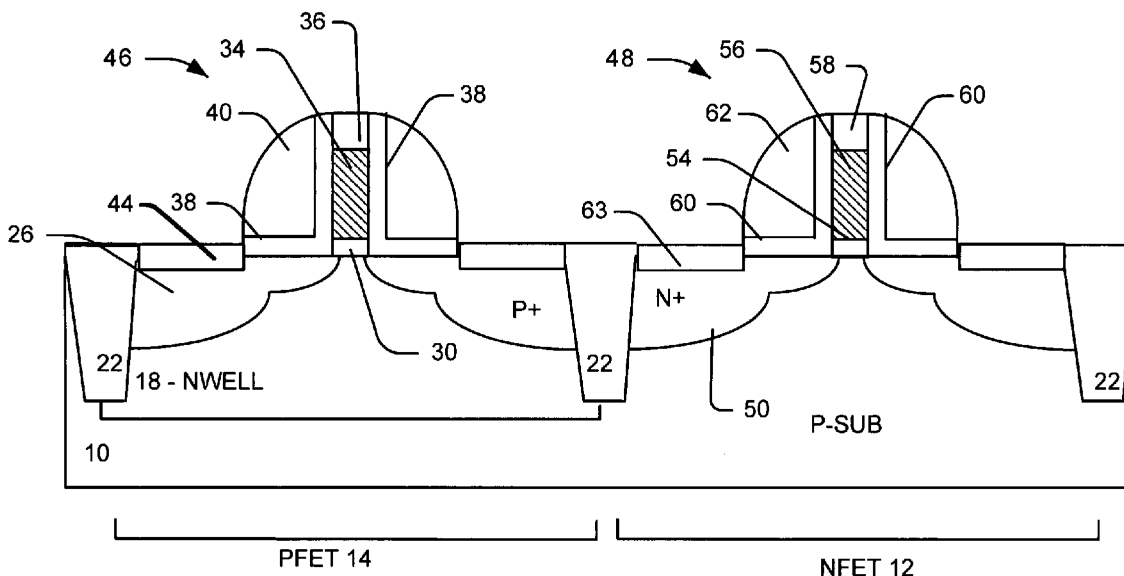
(57) **ABSTRACT**

A structure and method of fabrication of a semiconductor device having a stress relief layer under a stress layer in one region of a substrate. In a first example, a stress relief layer is formed over a first region of the substrate (e.g., PFET region) and not over a second region (e.g., NFET region). A stress layer is over the stress relief layer in the first region and over the devices and substrate/silicide in the second region. The NFET transistor performance is enhanced due to the overall tensile stress in the NFET channel while the degradation in the PFET transistor performance is reduced/eliminated due to the inclusion of the stress relief layer. In a second example embodiment, the stress relief layer is formed over the second region, but not the first region and the stress of the stress layer is reversed.



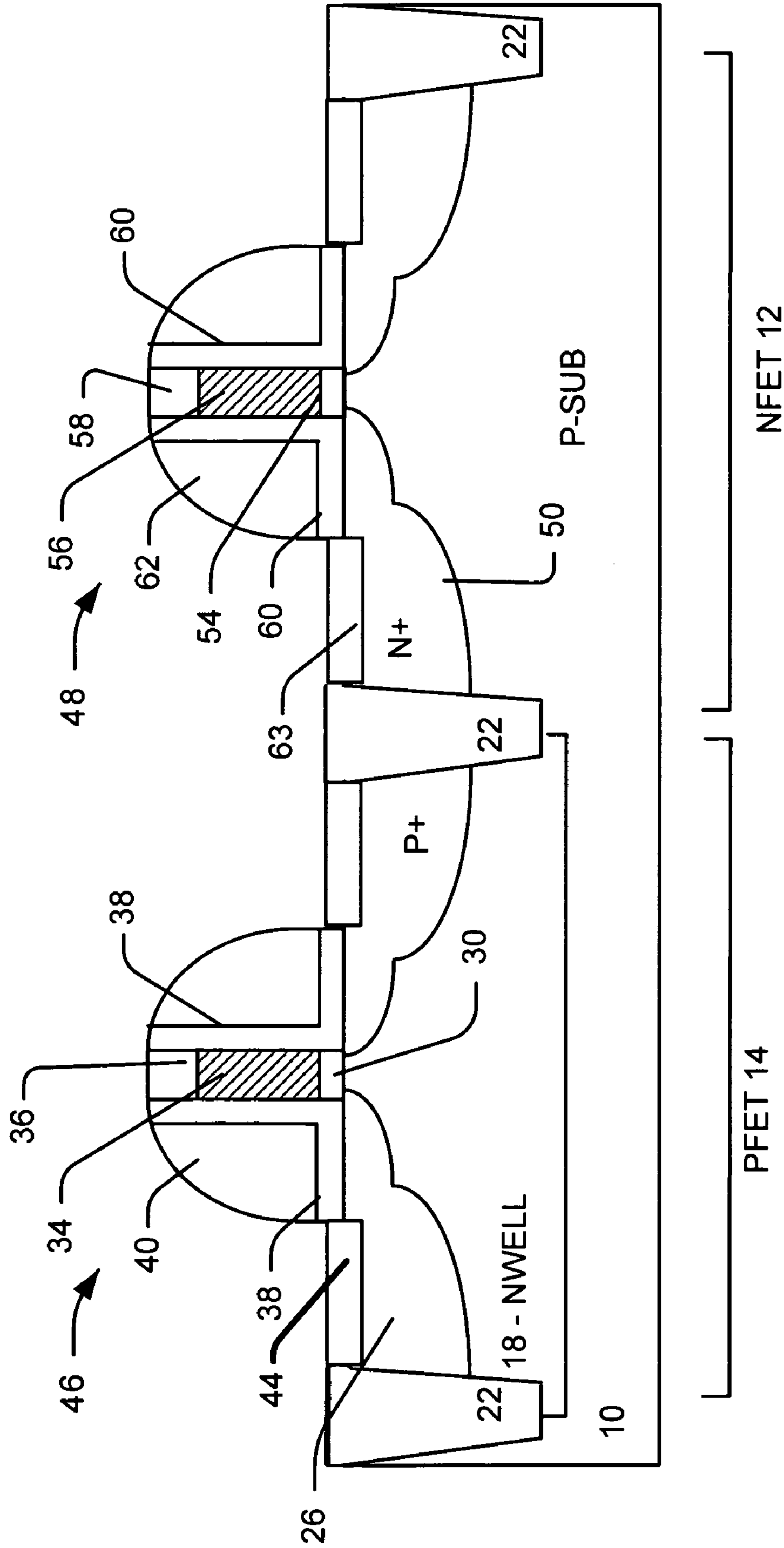


FIG. 1

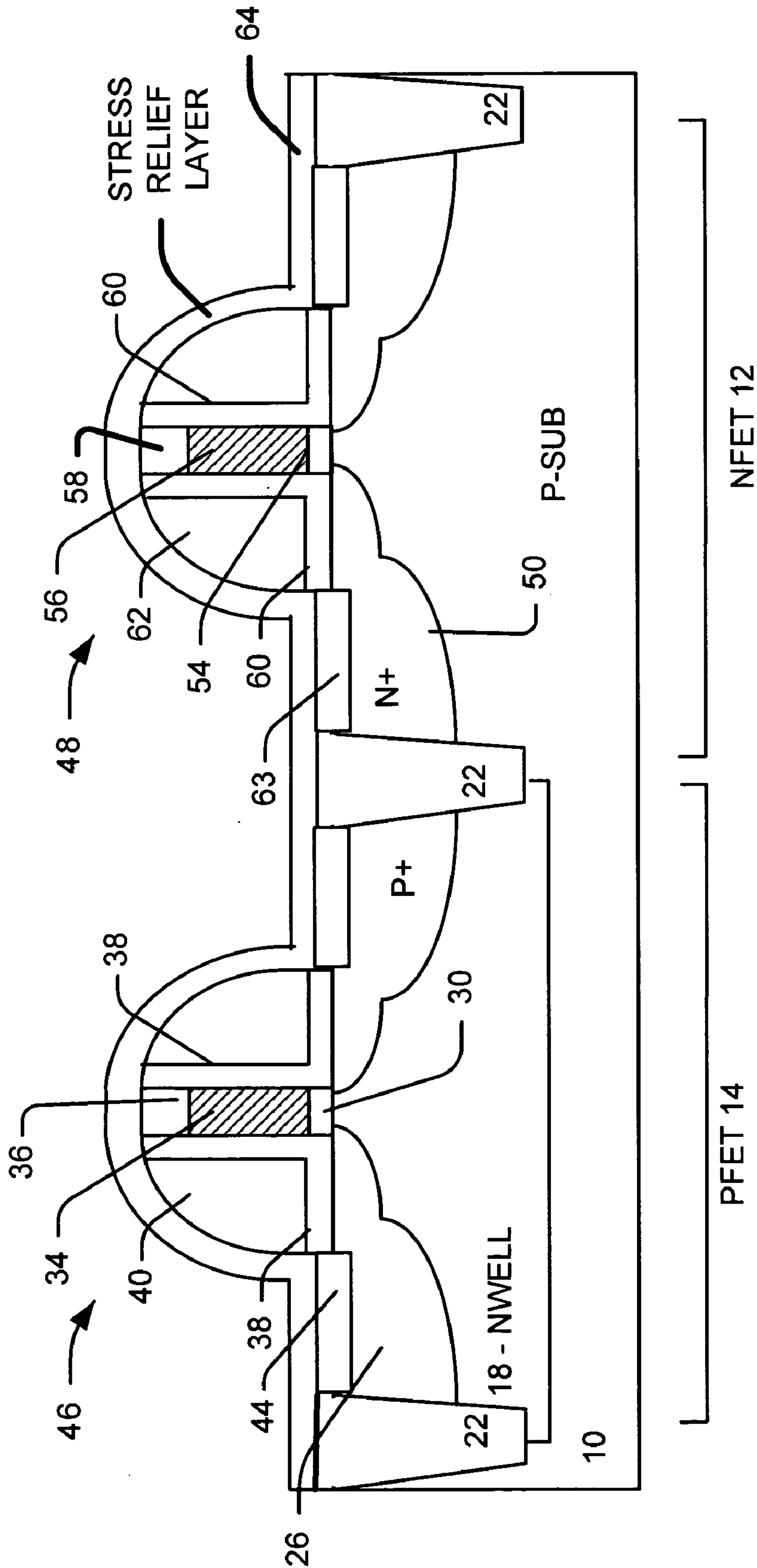


FIG. 2

FIG. 3

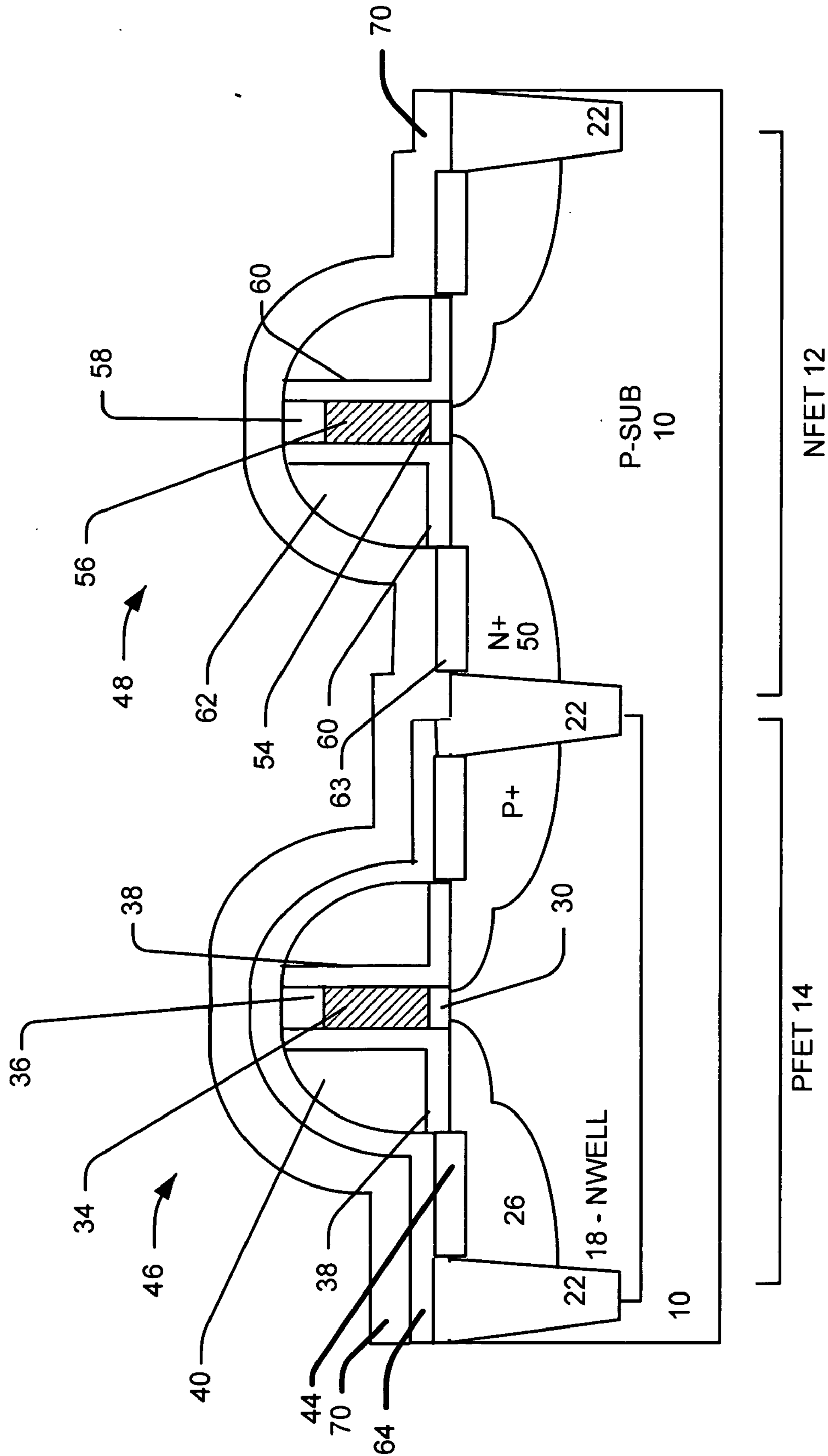


FIG. 4

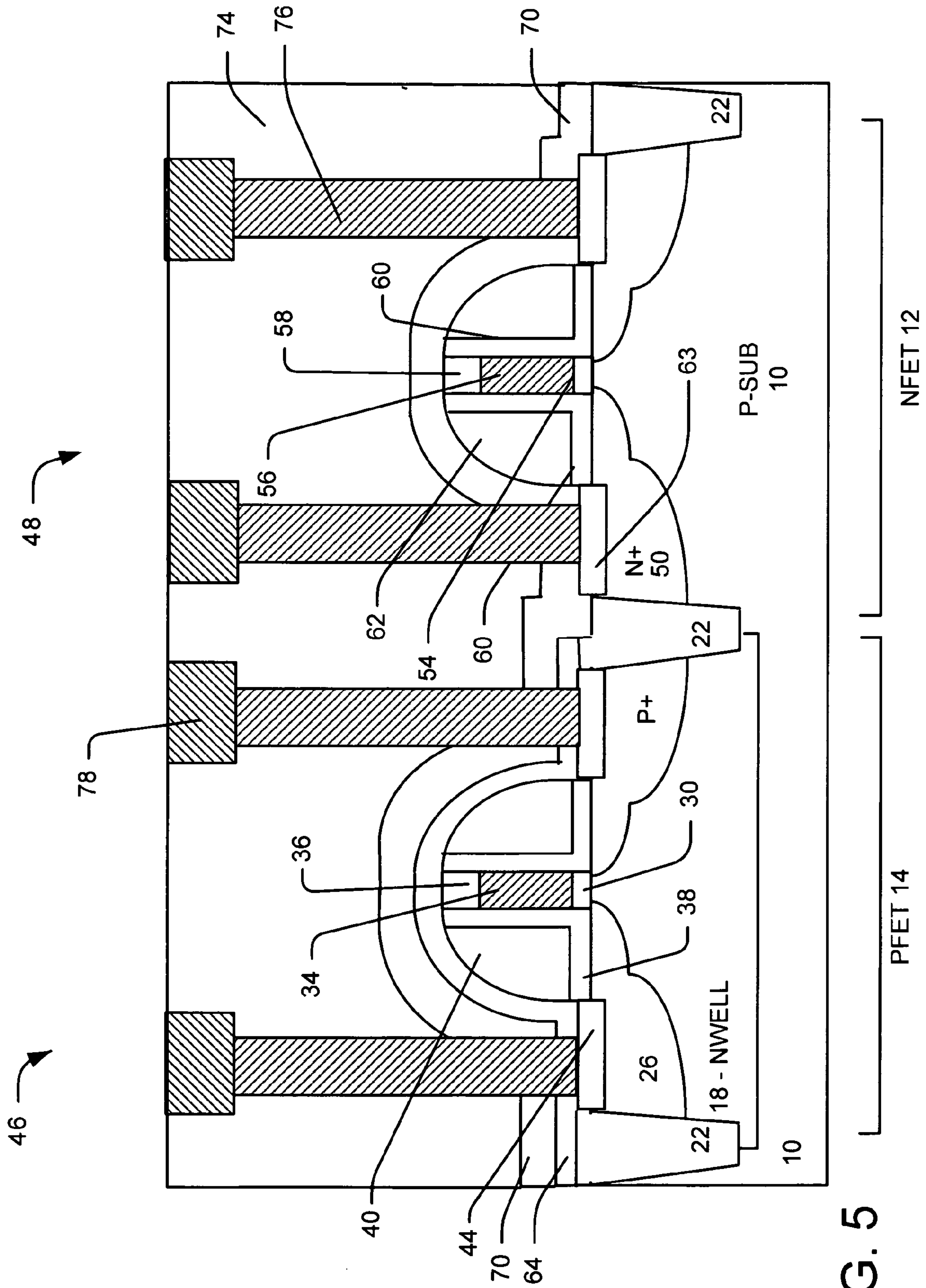


FIG. 5

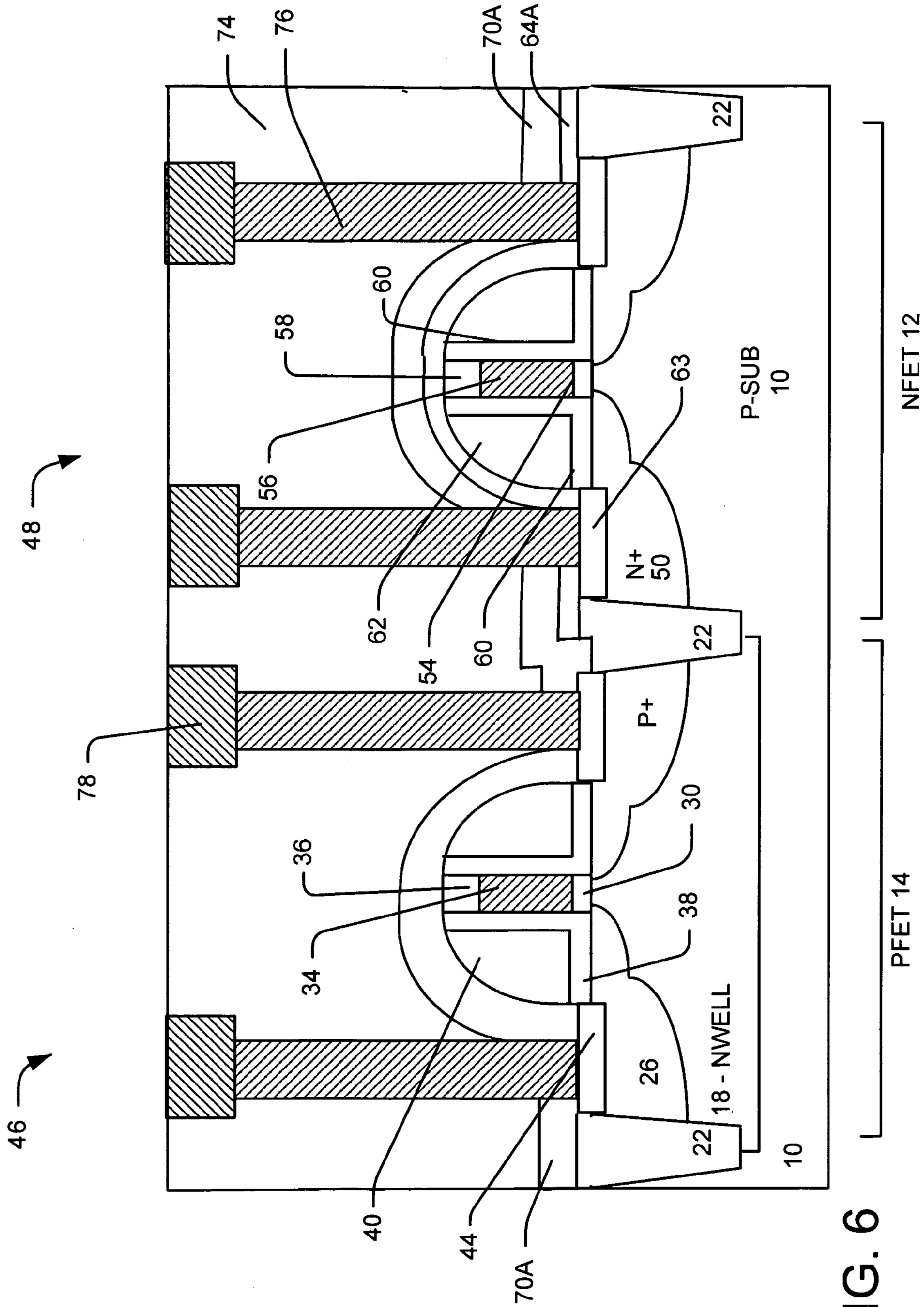


FIG. 6

METHOD TO ENHANCE DEVICE PERFORMANCE WITH SELECTIVE STRESS RELIEF

BACKGROUND OF INVENTION

[0001] 1) Field of the Invention

[0002] This invention relates generally to fabrication of semiconductor devices and more particularly to methods for selectively inducing stress in the PMOS and NMOS transistors using a overlying stress inducing layer.

[0003] 2) Description of the Prior Art

[0004] As semiconductor device speeds continue to increase and operating voltage levels continue to decrease, the performance of MOS and other types of transistors needs to be correspondingly improved. The carrier mobility in a MOS transistor has a significant impact on power consumption and switching performance, where improvement in carrier mobility allows faster switching speeds. The carrier mobility is a measure of the average speed of a carrier (e.g., holes or electrons) in a given semiconductor, given by the average drift velocity of the carrier per unit electric field. Improving carrier mobility can improve the switching speed of a MOS transistor, as well as allow operation at lower voltages.

[0005] One way of improving carrier mobility involves reducing the channel length and gate dielectric thickness in order to improve current drive and switching performance. However, this approach may increase gate tunneling current, which in turn degrades the performance of the device by increasing off state leakage. In addition, decreasing gate length generally calls for more complicated and costly lithography processing methods and systems.

[0006] Other attempts at improving carrier mobility include deposition of silicon/germanium alloy layers between upper and lower silicon layers under compressive stress, which enhances hole carrier mobility in a channel region. However, such buried silicon/germanium channel layer devices have shortcomings, including increased alloy scattering in the channel region that degrades electron mobility, a lack of favorable conduction band offset which may even mitigate the enhancement of electron mobility, and the need for large germanium concentrations to produce strain and thus enhanced mobility.

[0007] Thus, there remains a need for methods by which the carrier mobility of both NMOS and PMOS transistors may be improved, without significantly adding to the cost or complexity of the manufacturing process.

[0008] The importance of overcoming the various deficiencies noted above is evidenced by the extensive technological development directed to the subject, as documented by the relevant patent and technical literature. The closest and apparently more relevant technical developments in the patent literature can be gleaned by considering the following.

[0009] Suey Li Toh, K. P. Loh, C. B. Boothroyd, K. Li, C. H. Ang, E. Er, and L. Chan; ARTICLE: Reduction of Local Mechanical Stress in a Transistor Using Si3N4 SiOxNy Contact ESL; Electrochemical and Solid-State Letters, 8 (2) G38-G40 (2005) 1099-0062/2004/8(2)/G38/3/$7.00 © The Electrochemical Society, Inc. Found on website: www-hrem.msm.cam.ac.uk/~cbb/publications/pdf/130%20Suey%20Li.pdf

[0010] U.S. Pat. No. 6,573,172: Methods for improving carrier mobility of PMOS and NMOS devices—Fabrication of semiconductor device by forming P-channel and N-channel metal oxide semiconductor transistors in wafer, forming tensile film on P-channel transistor and forming compressive film on N-channel transistor—Inventor: En, William George; Milpitas, Calif.

[0011] U.S. Pat. No. 6,284,610: Cha—Method to reduce compressive stress in the silicon substrate during silicidation—Silicidation of source/drain junctions in the manufacture of integrated circuit, involves depositing buffer oxide layer overlying semiconductor substrate and gate electrode.

[0012] US 20040159886 A1 Lee, Sang-Eun; et al.—Method of manufacturing a semiconductor integrated circuit using a selective disposable spacer technique and semiconductor integrated circuit manufactured thereby—

[0013] U.S. Pat. No. 6,348,389: Chou et al.—Method of forming and etching a resist protect oxide layer including end-point etch—Formation and etching of resist protect oxide layer, involves forming shallow trench isolation on semiconductor substrate, and depositing and etching the resist protect oxide layer using endpoint etch mode.

[0014] US20020142606A1—Yoon—Method for forming a borderless contact of a semiconductor device—A method for forming a borderless contact of a semiconductor device includes forming a gate electrode on a field oxide of the semiconductor substrate, patterning a stacked structure of a buffer layer and an etching barrier layer on sidewalls of the gate electrode and on the field oxide, forming a silicide layer on the gate electrode and an active region exposed by the stacked structure, and forming the borderless contacts to reduce or prevent leakage current between the semiconductor device and the metal lines and degradation resulting from stresses inherent in the prior art nitride etching barrier layer by reducing abnormal oxidation associated with the buffer oxide layer under the etching barrier layer.

[0015] U.S. Pat. No. 5,252,848—Adler—Low on resistance field effect transistor.

SUMMARY OF THE INVENTION

[0016] The embodiments of the present invention provides a structure and a method of manufacturing CMOS transistors using a stress relief layer and an overlying stress layer which can be characterized as follows.

[0017] An example embodiment of a semiconductor device, comprises:

[0018] a first type MOS transistor and a second type MOS transistor on or in a substrate;

[0019] a stress relief film over the first type MOS transistor;

[0020] a stress film over stress relief film and the second type MOS transistor whereby the stress film improves the second type MOS transistor performance and whereby the stress relief film reduces the strain from the stress film.

[0021] Example embodiments comprise forming a stress relief layer over a first region (e.g., PFET or NFET region) and forming an overlying stress layer (e.g., compressive or tensile) over the at least the first region and preferably over a first and second region (e.g., both PFET and NFET regions). The stress relief layer can have a neutral stress or a stress opposite the stress of the overlying stress layer.

[0022] In a first example embodiment, a stress relief layer is formed over a PFET and a tensile stress layer is formed both PFET and NFET devices. In a second embodiment, a stress relief layer is formed over a NFET and a compressive stress layer formed both PFET and NFET devices.

[0023] Further embodiments are describe below and in the claims as presented and amended.

[0024] The above and below advantages and features are of representative embodiments only, and are not exhaustive and/or exclusive. They are presented only to assist in understanding the invention. It should be understood that they are not representative of all the inventions defined by the claims, to be considered limitations on the invention as defined by the claims, or limitations on equivalents to the claims. For instance, some of these advantages may be mutually contradictory, in that they cannot be simultaneously present in a single embodiment. Similarly, some advantages are applicable to one aspect of the invention, and inapplicable to others. Furthermore, certain aspects of the claimed invention have not been discussed herein. However, no inference should be drawn regarding those discussed herein relative to those not discussed herein other than for purposes of space and reducing repetition. Thus, this summary of features and advantages should not be considered dispositive in determining equivalence. Additional features and advantages of the invention will become apparent in the following description, from the drawings, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The features and advantages of a semiconductor device according to the present invention and further details of a process of fabricating such a semiconductor device in accordance with the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

[0026] FIGS. **1** through **5** are cross sectional views for illustrating a method for manufacturing semiconductor device according to a first example embodiment of the present invention.

[0027] FIG. **6** is cross sectional views for illustrating a method for manufacturing semiconductor device according to a second example embodiment of the present invention.

DETAILED DESCRIPTION OF THE EXAMPLE EMBODIMENTS

[0028] The example embodiments of the present invention will be described in detail with reference to the accompanying drawings. Example embodiments comprise forming a stress relief layer over a first region (e.g., PFET or NFET region) and forming an overlying stress layer (e.g., compressive or tensile) over the at least the first region and preferably over a first and second region (e.g., both PFET and NFET regions). The stress relief layer can have a neutral stress or a stress opposite the stress of the overlying stress layer.

[0029] In a first example embodiment, shown in FIGS. **1** to **5**, a stress relief layer **64** is formed over a PFET and a tensile stress layer **70** is formed both PFET and NFET devices. In a second embodiment shown in FIG. **6**, a stress relief layer **64**A is formed over a NFET and a compressive stress layer **70**A formed both PFET and NFET devices.

A. Nomenclature

Tensile Stress Layers

[0030] For a NFET, a tensile stress layer over the NFET improves NFET device performance. For a NFET, a tensile stress layer over the NFET improves NFET device performance by putting a tensile stress on the NFET channel.

Compressive Stress Layer

[0031] A compressive stress layer induces a compressive stress in the channel of a PFET.

[0032] For a PFET, a compressive stress layer over the PFET improves PFET device performance.

[0033] For a PFET, a compressive stress layer over the PFET improves PFET device performance by producing a compressive stress on the channel on the PFET channel.

[0034] Channel direction is the direction form source to drain and the direction current flows. Channel length is the distance between source and drain.

[0035] A position sign for a Strain/stress component is a tensile strain while a negative sign is a compressive strain.

II. FIRST EXAMPLE EMBODIMENT

[0036] A first example embodiment shown in FIGS. **1** to **5** shows a method of fabrication of a semiconductor device having a stress relief layer.

[0037] In this example, as shown in FIG. **5**, a stress relief layer **64** is formed over a first region of the substrate (e.g., PFET region **14**) and not over a second region (e.g., NFET region **12**). A stress layer (e.g., nitride layer) **70** is over the a stress relief layer **64** in the first region **14** and on the substrate **10**/silicide **63** in the second region **12**.

[0038] The NFET TX device **48** performance is enhanced due to the overall tensile stress (e.g., nitride **70**) while the degradation in the PFET Tx 46 performance is reduced/eliminated due to the inclusion of the stress relief layer. The stress relief layer **64** can have a neutral or opposite stress as the overlying stress layer **70**.

A. Provide a Substrate with a PFET Region and a NFET Region

[0039] We provide a substrate with first region where first type devices can be made and a second region where second type devices can be made.

[0040] For example, referring to FIG. **1**, we provide a substrate **10** with first region (e.g., PFET region **14**) where first type devices (e.g., PFET devices) can be made and a second region **12** (e.g., NFET region **12**) where second type devices (e.g., NFET devices) can be made.

[0041] The substrate can be any type of semiconductor structure, such as a wafer, or a SOI substrate and a p-doped silicon wafer.

[0042] This example description will refer to the first region as the NFET region **12** and the second region as the PFET region **14**, but the regions obviously can be interchanged, and the conductivity of the dopant reversed, and this description is not limiting.

[0043] We provide a PFET transistor **46** in the PFET region **14** and a NFET transistor **48** in the NFET region **12**. The transistors are representative and can have different structures than shown in the figs. More than one transistor can be formed in a region.

[0044] An example PFET transistor **46** can be comprised of a PFET gate dielectric layer **30**; a PFET gate electrode **34**; a PFET gate silicide layer **36** (or cap gate layer) over the PFET gate electrode **34**; a PFET spacer(s) **3840**, PFET source and drain regions **26** (e.g., S/D and SDE's) adjacent to the gate electrode **34**; PFET silicide regions **44** on the PFET source and drain regions **26**. A n-well **18** can be in the PFET region **14**.

[0045] The NFET transistor **48** can be comprised of a NFET gate dielectric layer **54**; a NFET gate electrode **56**; a NFET gate silicide layer (cap layer) **58** over the NFET gate electrode **56**; a NFET spacer **6062**, NFET source and drain regions **50** (e.g., S/D and SDE's) adjacent to the NFET gate electrode **56**; and NFET silicide regions **63** on the NFET source and drain regions **26**.

B. Form Stress Relief Layer **64**

[0046] Referring to FIGS. **2** and **3**, we form stress relief layer **64** over the substrate **10** surface in the PFET region **14** and not in the NFET region **12**.

[0047] Referring to FIG. **2**, we form a stress relief layer **64** over the substrate **10** surface.

[0048] Referring to FIG. **3**, we form a resist pattern **68** over the PFET region **14**. We then pattern the stress relief layer **64** to leave the stress relief layer **64** in the PFET region **14** over the PFET Transistor and not on the NFET region **12**. We remove the resist layer.

[0049] The stress relief layer is preferably comprised of a material with neutral stress or opposite stress relative to the subsequent first stress layer **70**. For example, (see FIG. **4**) for use with a tensile stress (SiN) layer **70**, the stress relief layer can be comprised of oxide with a thickness between 100 and 500 angstroms (~200+/−100 Å) and have a compressive stress (opposite the overlaying stress layer).

[0050] The stress relief layer **64** can comprised of a material that has a neutral stress or an opposite stress relative to the subsequently formed stress layer **70**. The amount of stress in the stress relief layer depends upon the stress in the stress layer and the amount of stress desired in the channel of the MOS transistors. Neutral can mean a stress between +1.0 and −1.0 GPa and preferably between +0.5 and −0.5 GPa and more preferably about 0 GPa.

[0051] In the first embodiment, with a (subsequently formed) tensile first stress layer **70**, the stress relief layer can have a neutral stress or a compressive stress. The compressive stress relief layer can have a compressive stress larger in magnitude than 0 and between −0.001 and −3.6 GPa. or preferably between −0.4 GP and −3.6 GPa.

[0052] The stress relief layer can be comprised of silicon oxide, silicon oxynitride, and silicon nitride. The stress relief layer and can have a thickness between 100 and 500 angstroms.

[0053] The stress relief layer **64** is preferably comprised of silicon oxide having a thickness between 100 and 300 angstroms.

C. Form a First Stress Layer

[0054] Referring to FIG. **4**, we form a first stress layer **70** (e.g., silicon nitride layer) over or on the NFET region **12** of the substrate and the stress relief layer **64** in the PFET region **14**.

[0055] The first stress layer **70** may be comprised of SiN, SiON, or SiC.

[0056] The first stress layer **70** has an internal stress that is transferred down to the substrate where the devices are located.

[0057] In the first embodiment using a tensile first stress layer **70**, the first stress layer **70** can have a tensile stress of between +0.4 GPa and +2.5 GPa and a thickness between 200 and 1200 angstroms (Å).

[0058] The stress relief layer can reduce the stress in the substrate region from the overlying first stress layer.

[0059] A compressive stress layer induces a compressive stress in the channel region of the underlying FET.

[0060] A tensile stress layer **70** induces a tensile stress in the channel region of the underlying FET. For a NFET, a tensile stress layer over the NFET improves NFET device performance by putting a tensile stress on the NFET channel. The stress layer puts a compressive stress on the S/D regions which put a tensile stress on the channel in the direction of the channel length.

[0061] For NFETS, device performance increases an overlying tensile stress layer **70** that induces a tensile (+ve) strain in the NFET channel. In contrast, NFET device performance decreases NFET channel compressive strain (−ve).

[0062] For PFETS, device performance decreases with tensile (+ve) strain in the PFET channel and device performance increases PFET channel compressive strain (−ve).

[0063] The NFET device performance is enhanced due to the overall net tensile stress from the tensile stress layer **70** on the substrate. A theory is that the substrate lattice is pulled further apart due to the tensile strain resulting in improved electron mobility.

[0064] Also, the degradation in the PFET Tx 46 performance is reduced/eliminated due to the inclusion of the stress relief layer **64** under the nitride layer **70** that reduces the tensile stress in the channel region.

D. Completing the Devices

[0065] Referring to FIG. **5**, we can form a dielectric layer **74** over the silicon first stress layer **70**. We then form interconnects (e.g., **7678**) to contact the PFET transistor **46**.

E. Review of Non-limiting Features of the First Example Embodiment

[0066] A feature of an embodiment is that one type of stress film (e.g., compressive or tensile stress) is formed over one region and a second type (e.g., opposite stress type) is formed over a second region. For example, a tensile stress layer can be formed over a NFET region and a compressive stress layer can be formed over the PFET region. The tensile stress layer increases the NFET device performance of because enhanced electron mobility.

[0067] Another feature is the stress relief layer **64** in the PFET region **14** reduces or eliminates the tensile stress from the (e.g., Nitride) stress layer **70**. The strain effects on device performance is more evident at smaller linewidths. The stress relief layer can have a neutral stress or stress opposite the stress layer **70**.

F. Second Example Embodiment—Stress Relieve Layer on NFET Region

[0068] Referring to FIG. **6**, in a second example embodiment, the stress relief layer **64**A is formed over the NFET region **12** and not over the PFET region **14** the stress relief layer **64**A can be formed over the substrate and then patterned. Then, the first stress layer **70**A having an internal compressive stress (e.g., a compressive nitride layer) **70**A is deposited over the entire substrate. The compressive stress layer **70**A improves the performance of the PFET device **46** by putting a compressive strain on the PFET channel.

[0069] Therefore the PFET (channel) region **14** has a compressive stress that increases device performance. The NFET region **12** preferably has about neutral stress caused by the stress relieve layer **64**A that underlies the compressive stress layer **70**A.

[0070] In the second embodiment, the stress relief layer **64**A can have a neutral stress or a tensile stress. A neutral stress relief layer can have stress between +0.5 and −0.5 GPa or a stress between −1.0 and +1.0. GPa. The stress relief layer with a tensile stress can have a tensile greater than 0 GPa and preferably between about 0.001 and +2.5 GPa or preferably between +0.4 GPa and +2.5 GPa (or higher).

[0071] In a second embodiment, where a compressive stress layer **70**A is formed, the stress layer **70**A can have a compressive stress between −0.4 GP and −3.6 GPa.

G. Non-limiting Example Embodiments

[0072] In the above description numerous specific details are set forth such as flow rates, pressure settings, thicknesses, etc., in order to provide a more thorough understanding of the present invention. Those skilled in the art will realize that power settings, residence times, gas flow rates are equipment specific and will vary from one brand of equipment to another. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these details. In other instances, well known process have not been described in detail in order to not unnecessarily obscure the present invention.

[0073] Given the variety of embodiments of the present invention just described, the above description and illustrations show not be taken as limiting the scope of the present invention defined by the claims.

[0074] While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention. It is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

1. A method of fabricating a semiconductor device, comprising:

forming a first type MOS transistor and a second type MOS transistor in a substrate;

forming a stress relief film over the first type MOS transistor and not over the second type MOS transistor; and

forming a stress film over said stress relief film and over the second type MOS transistor; the stress relief film having the opposite type stress as the stress film or the stress relief film having an about neutral stress; whereby the stress film improves the second type MOS transistor performance and whereby the stress relief film reduces the stress from the stress film.

2. The method of claim 1 wherein said first type MOS transistor is PMOS and the second type MOS transistor is NMOS; and said stress film is a tensile stress film.

3. The method of claim 1 wherein said first type MOS transistor is NMOS and the second type MOS transistor is PMOS; and said stress film is a compressive stress film.

4. The method of claim 1 wherein the stress relief film has the opposite type stress as the stress film.

5. A method of fabricating a semiconductor device, comprising:

forming a PMOS transistor and a NMOS transistor in a substrate;

forming a stress relief film over the PMOS transistor and not over the NMOS transistor; and

forming a tensile stress film over the stress relief film and over the NMOS transistor; said stress relief film having a neutral stress or a compressive stress; whereby the tensile stress film improves the NMOS transistor performance and whereby the stress relief film reduces the stress from the tensile stress film.

6. (Canceled)

7. The method of claim 5 wherein said stress relief film has a compressive stress and the tensile stress layer has a tensile stress.

8. The method of claim 5 wherein said stress relief film has a stress between −0.001 and −3.6 GPa and the tensile stress film has a tensile stress between +0.4 GPa and +2.5 GPa.

9. The method of claim 5 wherein said stress relief film has a stress between 0.5 and −0.5 GPa.

10. The method of claim 5 wherein the stress relief film is comprised of oxide, silicon oxynitride or SiN; and said tensile stress layer is comprised of SiN, SiON or SiC.

11. The method of claim 5 wherein the stress relief film is substantially comprised of silicon oxide.

12. A method of fabricating a semiconductor device, comprising:

forming a PMOS transistor and a NMOS transistor in a substrate;

forming a stress relief film over the NMOS transistor and not over said PMOS transistor;

forming a compressive stress film over said stress relief film and the PMOS transistor; and

said stress relief film having an about neutral stress or a tensile stress.

13. (Canceled)

14. The method of claim 12 wherein said stress relief film has a tensile stress and the compressive stress film has a compressive stress.

15. The method of claim 12 wherein said stress relief film has a tensile stress with a tensile stress between 0.4 and 2.5 GPa and the compressive stress film has a compressive stress between −0.4 GP and −3.6 GPa.

16. The method of claim 12 wherein said stress relief film has a stress between 0.5 and −0.5 GPa.

17. The method of claim 12 wherein said stress relief film is comprised of oxide, silicon oxynitride or SiN; and said compressive stress layer is comprised of SiN, SiON or SiC.

18. The method of claim 12 wherein the stress relief film is substantially comprised of oxide.

19. A method of fabrication of a semiconductor device having a stress relief layer comprising the steps of:

a) providing a substrate with a PFET region and a NFET region; providing a PFET transistor in said PFET region and a NFET transistor in said NFET region;

said substrate having a substrate surface;

(1) said PFET transistor being comprised of a PFET gate dielectric layers, a PFET gate electrode, and PFET source and drain regions adjacent to said PFET gate electrode;

(2) said NFET transistor being comprised of a NFET gate dielectric layer, a NFET gate electrode, and NFET source and drain regions adjacent to said NFET gate electrode;

b) forming a stress relief layer over the substrate surface in the PFET region and not in the NFET region; the stress relief layer having a neutral or compressive stress; and

c) forming a stress layer over the NFET region of the substrate and over the stress relief layer in the PFET region; the stress layer has a tensile stress.

20. The method of claim 19 which further includes: forming an inter level dielectric layer over the stress layer; and forming interconnects to contact said PFET transistor and said NFET transistor.

21. The method of claim 19 which further includes: the stress relief layer is comprised of a material selected from the group consisting of silicon oxide, SiON, and SiN; and the stress relief layer has a thickness between 100 and 500 angstroms.

22. The method of claim 19 which further includes: forming the stress relief layer over the substrate surface; patterning said stress relief layer to leave the stress relief layer over the PFET region and not over the NFET region.

23. (canceled)

24. (canceled)

25. (canceled)

26. (canceled)

27. The method of claim 1 wherein the step of forming the stress relief film further comprises:

forming the stress relief film over the first type MOS transistor and not over the second type MOS transistor; at least a portion of said second type MOS transistor being exposed.

28. The method of claim 1 which further comprises

the stress relief film as initially deposited over the first type MOS transistor having the opposite type stress as the stress film or the stress relief film has a neutral stress; and

after the step of forming the stress film, forming a dielectric layer over said stress relief film and said stress film; the stress relief film not being subject to an ion implant before forming said dielectric layer over said stress relief film.

29. The method of claim 1 wherein the step of forming the stress relief film further comprises:

forming the stress relief film over the first type MOS transistor and said second type MOS transistor; then

removing the stress relief film from over the second type MOS transistor.

30. The method of claim 1 wherein the step of forming the stress relief film further comprises:

forming the stress relief film over the first type MOS transistor and over said second type MOS transistor; then

removing the stress relief film from over the second type MOS transistor; and then

forming the stress film on and in contact with said stress relief film and over the second type MOS transistor.

31. The method of claim 5 wherein the step of forming the stress relief film further comprises:

forming the stress relief film over the PMOS transistor and over said NMOS transistor; and then

removing the stress relief film from over the NMOS transistor.

32. The method of claim 5 wherein the step of forming the stress relief film further comprises:

forming the stress relief film over the PMOS transistor and over said NMOS transistor; then

removing the stress relief film from over the NMOS transistor; and then

forming the stress film on said stress relief film and over the NMOS transistor.

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