A Novel 6T-SRAM Cell Technology Designed with Rectangular Patterns Scalable beyond 0.18 μm Generation and Desirable for Ultra High Speed Operation

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Abstract

A novel 6T-SRAM cell layout designed with rectangular patterns has been developed. Employing this layout, 4.13 μm^2 and 5.33 μm^2 cells with word transistor width of 0.25 μm and 0.75 μm are obtained, respectively, based on the 0.20 μm rule. Among the various layouts of 6T-SRAM cells, this layout provides minimum cell size and the smallest bit line capacitance with word transistor width over 0.75 μm for the ultra high speed operation. It is also demonstrated quantitatively that the optimized SRAM cell layout for high speed use is different from that for low power use. The cell layout proposed also provides the excellent scalability beyond 0.18 μm generation due to its highly simplified pattern design.

Introduction

In recent years, it is reported that the speed of CPU and DSP has been improved up to giga hertz operation [1]. In such situation, the most important role of SRAM for such high performance devices is the high speed operation.

Fig.1 shows contents of SRAM access time determined from our products. It mainly consists of (i) decoding delay and sensing delay, and (ii) bit line (BL) delay. Decoding delay and sensing delay are resulted from the operation in peripheral circuits of SRAM. These delays depend on gate delay of peripheral circuits. On the other hand, BL delay is resulted from the operation in the memory cell. This delay depends on memory cell current to pull down BL. Therefore, to achieve the high speed SRAM operation, (1) the reduction of gate delay in peripheral circuits and (2) the increase of memory cell current that means the increase of the word transistor (WT) size and the reduction of BL capacitance are required.

The above (1), the reduction of gate delay, has been widely studied. On the contrary, as for the memory cell technology, the cell size reduction has been reported [2-5], but the increase of WT size and the reduction of BL capacitance for the high speed operation have not been reported quantitatively. In this paper, an optimized SRAM cell layout which will satisfy these requirements consistently is proposed and is verified from experiments.

Analysis on cell design

SRAM cell designs are essentially categorized into four variations for possible combinations of two inverters as shown in Table-1. All SRAM cells reported with the sub-0.20 μm rule are categorized into type-1a, 2 and 3 as are described in Table-2 [2-5]. As a variation of WT layout of type-1a, type-1b is also proposed [6]. The smallest and secondly smallest cells previous reported were type-2 and 3. Cell size of type-1a is almost equal to that of type-2.

The disadvantages related with these conventional cells are as follows. (i) Complicated cell design results in the corner rounding and deformation of patterns. And transistor size is not constant due to the overlay shift in lithography. (ii) The spacing between each wiring pattern is designed with minimum spacing rule. Since it requires continuous improvements of resolution and NA in lithography for the further scaling, some new idea of more simplified pattern definition is desired.

A new type-1b cell is proposed as shown in Figs.2 and 3 to resolve these problems. Significant geometrical features of this cell are (i) highly simplified rectangular pattern design and (ii) wide spacing between each wiring pattern. As the result of this design, no corner rounding of patterns nor irregularity of transistor size caused by the overlay shift are achieved. These features will be important even in design rules in future.

Furthermore, the cell is 4.13 μm^2, which is comparable to the best data available for 0.2 μm generation, employing the minimum spacing not of 0.2 μm but of 0.42 μm in the active area and the poly Si layers, and of 0.69 μm in each local wiring layer. This wide spacing design is also desirable for the scaling in future.

Sample preparation and design rule verification

Proposed type-1b cell is designed with the 0.20 μm rule for electrical evaluation as shown in Figs.2, 3 and 4. Conventional type-2 and 3 cells are also designed with the same rule of 0.20 μm for the reference.

The N+/P+ spacing of 0.42 μm was achieved with the shallow trench isolation of 0.4 μm depth. Dual gate transistor of 0.18 μm gate length with insulator on the gate electrode was fabricated. CVD SiN and SiO_2 were deposited and planarized by CMP. In the type-1b cell, Vss/Vdd contacts were extended to the edge of cell using inlaid tungsten wirings. This structure enables the layout that TiN local wiring runs above Vss-N+ and Vdd-P+ contacts with the use of stacked plug interconnects which connect inlaid wirings to Vss/Vdd lines. Two pieces of local wirings were defined independently, one with a SiO_2 mask and the other with a resist mask.

DC characteristics of these three cells with WT width of 0.25 μm are measured as shown in Fig.5. The cell operation is demonstrated for the cell size from 3.40 to 4.14 μm^2. Thus the design rule and process technology we have employed are verified as equivalent to the best performances in the 0.20 μm generation as shown in Table-2.

Results and discussion

(I) Conditions of SRAM cell design

The dependence of cell stability on the size of transistor needs to be studied since the larger size WT for high speed operation will result in the worse cell stability. Fig.6 shows simulated static noise margins (SNM) with the ratio of driver / word transistor (ßDT/ßWT) as parameters. Consider-

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ing the distribution of cell stability due to the process conditions, the criterion of SNM is defined as SNM > 0.15 V at |Vth| = 0.3 V. So, the ratio ßDT / ßWT ≥ 1 is required. The correlation between the ratio of driver / load transistor (ßDT / ßLT) and simulated SNM with the ratio ßDT / ßWT = 1 in Fig.7 shows 6T-SRAM is stable in the range of 2 ≤ ßDT / ßLT ≤ 10. SRAM cells described below are designed with the ratio ßDT / ßWT = 1 and ßDT / ßLT = 6.

(II) Optimization of cell size and bit line capacitance

The memory cell size and BL capacitance are estimated as a function of WT width and shown in Figs.8 and 9.

In Fig.8, the cell size of type-1b is the smallest for the WT width of larger than 0.75 μm. With increasing WT width, the type-2 and 3 cells expand both in the bit line and the word line directions keeping ßDT / ßWT = 1, while the type-1b cell expands only in the word line direction but is constant in the bit line direction, due to the layout of WT and DT arrayed in the same direction as shown in Table-3 (a). With WT width of 0.75 μm, type-1b provides the smallest cell size of 5.33 μm^2, which is 2 % and 35 % smaller than those of type-2 and 3.

Furthermore, it is pointed out that type-3 provides the smallest cell size among these three cells for WT width of 0.25 μm, but it provides 54 % larger cell than that of type-1b for WT width of 0.75 μm. This means the optimized cell layout with large size WT is different from that with minimum size WT. Although SRAM cell layout has been evaluated in terms of the cell size with small size WT in the past, we would like to emphasize to examine the cell layout in terms of large WT width for the high speed operation.

As shown in Fig.9, BL capacitance of type-1b is the smallest and it is monotonously reduced with increasing WT width, which exhibits a sharp contrast to those of type-2 and 3. This is because the expansion of WT width for type-1b only results in the expansion of BL space while maintaining BL length constant as shown in Table-3 (b). With WT width of 0.75 μm, minimized BL capacitance is 0.37 fF/bit for type-1b.

The cell size and BL capacitance with WT width of 0.75 μm are summarized in Table-4. It is obvious that the type-1b cell provides the minimum values in the cell size and BL capacitance for WT width larger than 0.75 μm. Therefore, the type-1b layout is concluded to be desirable for the ultra high speed operation among these three cells.

Fig.10 shows the comparison of estimated access time with WT width of (a) 0.25 μm and (b) 0.75 μm. With increasing WT width, cell current is increased three times and BL capacitance is reduced 12 %, then BL delay results in the 70 % reduction. Word line capacitance is increased 2.3 times with increasing WT width, but it results in only 1 % increase in total access time. As the result, total access time is reduced 25 % with the increase of WT width. To achieve the same access time, not with the increase of WT width but with the reduction of gate delay in peripheral circuits, gate delay should be reduced 50 %. This shows the importance of SRAM cell layout with large size WT for the high speed operation.

Figs.11 and 12 show the SEM image and DC characteristics of type-1b with WT width of 0.75 μm, respectively.

Since P and N wells in type-1b are extended along BL, and they are longer than those of reference cells, the dependence of SNM on the cell array size is measured. As shown in Fig. 13, the SNM is insensitive to the well length for the array size less than 512 bit.

(III) Scalability in future

Our proposed cell layout consistently provides three advantages for future scaling. (1) The corner rounding of patterns and irregularity of transistor size caused by the overlay shift are eliminated due to the rectangular design. (2) Low NA steppers can be used due to the wide spacing of each wiring layer. (3) Narrow gate length in peripheral circuits is allowed due to the wide focus depth with the above low NA steppers.

The results of structure studies for the type-1b cell designed with the 0.18 μm rule are shown in Fig.14 where the cell size is reduced to 3.04 (1.52 x 2.00) μm^2. As shown in Fig.14, no corner rounding of patterns nor irregularity of transistor size caused by the overlay shift are observed.

The characteristics in lithography are shown in Figs.15 and 16. In Fig.15, the type-2 cell provides the focus range of only 0.4 μm with NA of 0.45, and it requires at least NA of 0.55 to obtain enough range as shown in Fig.16. For future scaling, a new stepper with higher NA is required. On the contrary, conventional low NA steppers can be used for type-1b as shown in Fig.15 due to the wide spacing of patterns.

Furthermore it is pointed out that pattern printing with lower NA in type-1b provides wider focus range of the isolated gate pattern even for narrower gate length as shown in Fig.16. Narrower gate length allowed in type-1b contributes the reduction of gate delay in peripheral circuits due to the higher drivability and lower gate capacitance.

The above three advantages demonstrate the geometrical advantage and the excellent scalability of type-1b beyond 0.18 μm generation.

Conclusion

A novel 6T-SRAM cell layout designed with rectangular patterns has been developed. Among the various layouts of 6T-SRAM cells, this layout provides minimum cell size and the smallest bit line capacitance with word transistor width over 0.75 μm for the ultra high speed operation. The cell layout proposed also provides the excellent scalability beyond 0.18 μm generation due to highly simplified pattern design.

Acknowledgement

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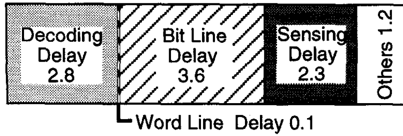

Fig.1: Contents of SRAM access time (a.u.)

Table-1: Variations of the inverter layouts and SRAM cell layouts.

	Category 1	Category 2	Category 3	Category 4
Layouts of Inverters				
Layouts of SRAM Cells	Type-1a cell Type-1b cell	Type-2 cell	Type-3 cell	Type-4 cell

Description of Symbols: Vss, Vdd, Strage Node, Gate Electrode

Table-2: Recent reported SRAM cells with 0.20 μm rule and the beyond.

Author	Sambon -sugi & c. 98VLSI [2]	Noda & c. 97IEDM [3]	Woo & c. 98VLSI [4]	Takao & c. 97VLSI [5]
Cell Layout	Type-2	Type-3	Type-1a	Type-1a
Design Rule (μm)	0.13	0.18	0.20	0.20
Cell Size (μm²)	2.49	2.91	3.97	4.08

	This work	This work	This work	
Cell Layout	Type-2	Type-3	Type-1b	
Design Rule (μm)	0.20	0.20	0.20	
Cell Size (μm²)	4.14	3.40	4.13	

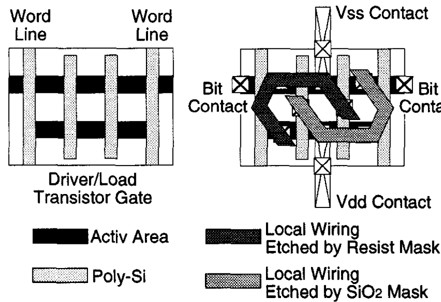

Fig.2: Layouts of proposed type-1b SRAM cell.

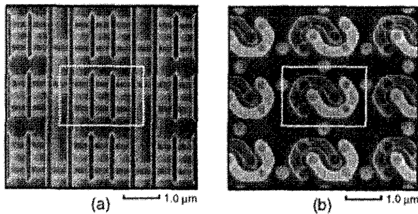

Fig.3: SEM images of proposed type-1b SRAM cell;
(a) after poly Si fabrication,
(b) after local wiring fabrication.

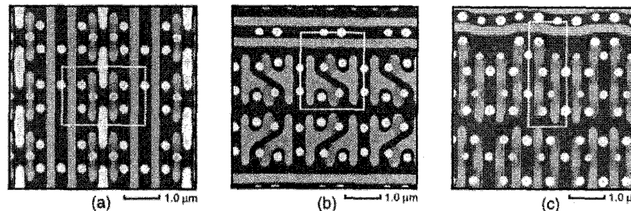

Fig.4: SEM images of SRAM cells after 1st contact fabrication;
(a) type-1b cell (1.72 x 2.40 = 4.13 μm²), (b) type-2 cell
(1.84 x 2.25 = 4.14 μm²), (c) type-3 cell (1.08 x 3.15 = 3.40 μm²).

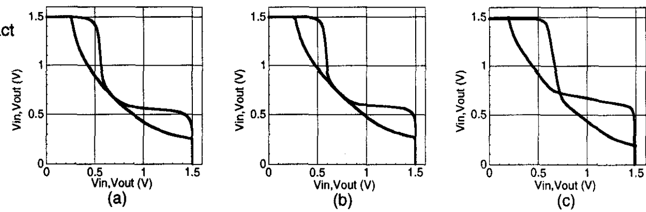

Fig.5: DC characteristics of SRAM cells at Vcc = 1.5 V;
(a) type-1b cell, (b) type-2 cell, (c) type-3 cell.

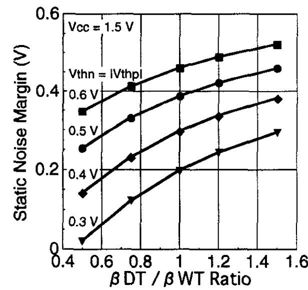

Fig.6: DT and WT size dependence
of the cell stabilty with βDT/βLT = 6.

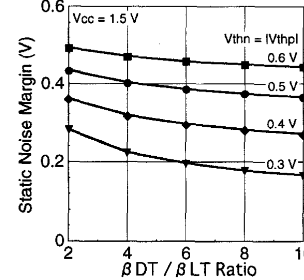

Fig.7: DT,WT and LT size dependence
of the cell stability with βDT/βWT = 1.

8.2.3

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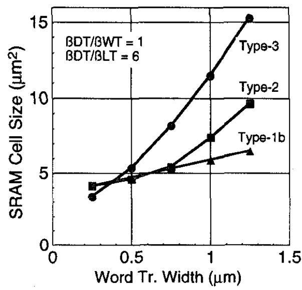


Fig.8: Cell size of each SRAM cell layout as a function of WT size.

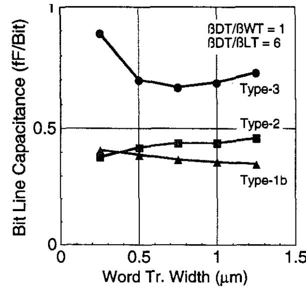


Fig.9: BL capacitance of each SRAM cell layout as a function of WT size.

Table-3: WT size dependence of cell transistor layouts and bit line layouts.

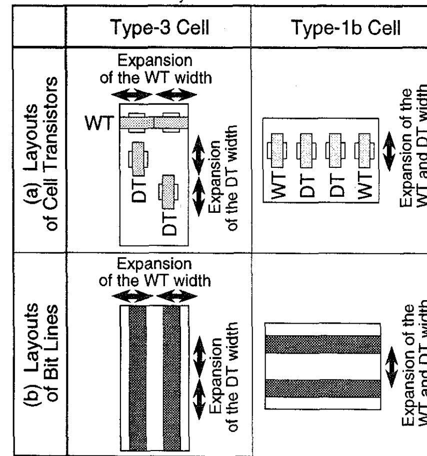


Table-4 : Comparison of cell size and bit line capacitance of each SRAM cell layout.

Cell Layout	WT width = 0.25 μm	WT width = 0.75 μm	
	Cell Size (μm²/Bit)	Cell Size (μm²/Bit)	BL Capacitance (fF/Bit)
Type-1b	4.13 [1.72x2.40]	5.33 [2.22x2.40]	0.37
Type-2	4.14 [1.84x2.25]	5.45 [1.98x2.75]	0.44
Type-3	3.4 [1.08x3.15]	8.22 [1.98x4.15]	0.67

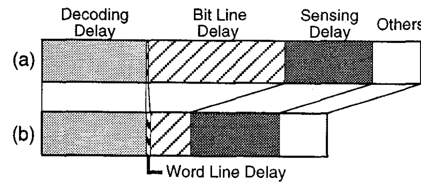


Fig.10: Comparison of the access time; (a) reference and (b) BL delay reduction.

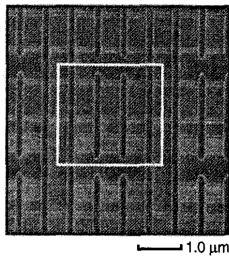


Fig.11: SEM image of type-1b cell with WT width of 0.75 μm after poly Si fabrication.

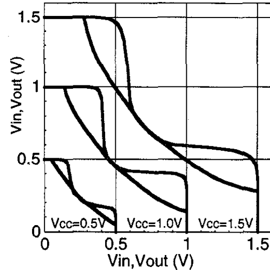


Fig.12: DC characteristics of type-1b cell with WT width of 0.75 μm.

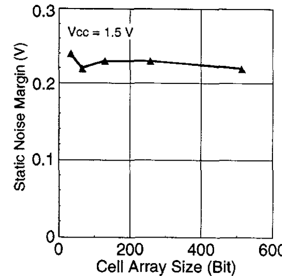


Fig.13: Cell array size dependence of the cell stability.

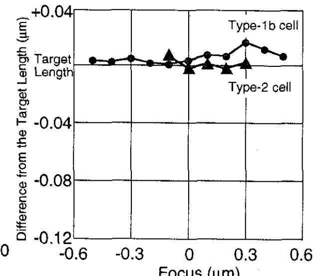
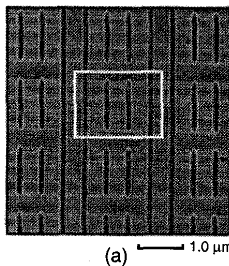
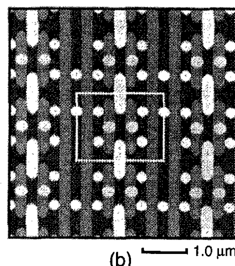


Fig.15: Focus depth dependence of the gate length of the memory cell transistor. Round plot is of type-1b cell, and triangle plot is of type-2 cell. Both plots are with NA of 0.45.





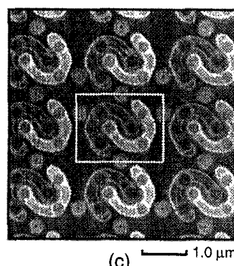


Fig.14: SEM images of type-1b cell designed with 0.18 μm rule; (a) after poly Si fabrication, (b) after 1st contact fabrication. (c) after local wiring fabrication. Cell size = 3.04 (1.52x2.00) μm².

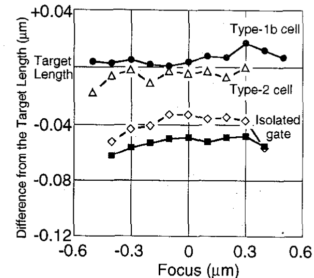


Fig.16: Focus depth dependence of the gate length of the memory cell transistor and the isolated transistor. Vacant plot is with NA of 0.55, and occupied plot is with NA of 0.45.