

## Source/Drain Extension Scaling for 0.1 $\mu$ m and Below Channel Length MOSFETS

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### Abstract

In this paper, we investigate the scaling of source/drain extension (SDE) depth and SDE to gate overlap for 0.1 $\mu$ m and below MOSFETs. We show for the first time that a minimum SDE to gate overlap of 15-20 nm is needed to prevent drive current ( $I_{DSAT}$ ) degradation. We also show for the first time that scaling SDE vertical depths below 30-40 nm results in little to no performance benefit for 0.1 $\mu$ m devices and beyond since any improvement in short channel effects due to reduced charge sharing is offset by a large increase in external resistance and poor gate coupling between the channel and extensions.

### I. Introduction

Since the 1970's silicon MOSFET gate dimensions have been reduced from 10 $\mu$ m to sub-0.1 $\mu$ m through a combination of gate oxide thickness and junction depth scaling. Recently, very short gate length transistors with shallow SDE junctions and small gate overlap have been reported[1,2]. Many of these transistors have lower than expected drive currents given the extremely short channel lengths. We propose that these low drive currents result from an SDE which is too shallow leading to a high external resistance and poor gate to SDE coupling. In this work we look at the tradeoffs involved with SDE scaling for 0.1 $\mu$ m MOSFETs and below. The SIA roadmap predicts SDE junction depths as low as 10 nm for these deep submicron devices (Fig. 1).

### II. Minimum Source/Drain Extension Overlap

We use the test structure in Fig. 2 to evaluate the effect of SDE to gate overlap on  $I_{DSAT}$ . In this test structure, the SDE implant is performed after the formation of a thin offset spacer. By varying the thickness of the offset spacer, the SDE to gate overlap and vertical junction depth can be independently varied. The transistor data presented are measured on devices with a process flow similar to our 0.25 $\mu$ m technology[3]: complementary doped poly-Si gates, retrograde n/p-wells, 4.5nm thermal gate oxides, low energy implants for SDE formation, low Dt spacer formation, rapid thermal anneal for gate and source/drain formation and activation and selectively formed TiSi<sub>2</sub>. We also include data on transistors with gate length, gate oxide, and power supply scaled by 0.7 and (0.7)<sup>2</sup> from our 1.8V 0.25 $\mu$ m technology. All transistors have controlled sub-threshold slopes of less than 85mV/decade, 1nA/ $\mu$ m off state leakage, and electrical channel lengths ( $L_E$ ) between 0.06 and 0.14 $\mu$ m.

With the above test structure fabricated for a range of poly-Si gate lengths, we measured transistor saturation drive current versus SDE overlap for both fixed vertical SDE depth and for fixed source to drain extension metallurgical spacing (Fig. 2). The SDE metallurgical spacing is kept constant by adjusting the poly-Si gate length to maintain 1nA/ $\mu$ m off state leakage. Figure 3 shows the vertical SIMS profile of an SDE junction used in the experiment (1.0e15cm<sup>-2</sup>, 5keV arsenic implant RTA annealed). Figure 4 shows the effect of spacer offset on overlap capacitance and  $I_{DSAT}$ . For spacer offsets greater than 40 nm,

there is a flattening in overlap capacitance implying minimal SDE to gate overlap. A degradation in  $I_{DSAT}$  is also clearly observed for offset spacer widths greater than 20nm. The lateral diffusion of the SDE junction under the gate edge is estimated to be 0.6-0.7 times the vertical depth minus the offset spacer width. This estimate is obtained from process simulations and junction staining measurements. Experimentally the offset spacer width is varied from 0 to 40nm and is used to modulate the SDE to gate overlap from approximately 40 to 0nm. Figures 5 and 6 show  $I_{DSAT}$  versus SDE overlap for both NMOS and PMOS 0.25 $\mu$ m devices as well as 0.7 and (0.7)<sup>2</sup> scaled devices. Figures 5 and 6 show that independent of process technology feature size, a degradation in  $I_{DSAT}$  is observed if the overlap is less than 15-20nm.

### III. Source/Drain Extension Depth

We now investigate optimal SDE vertical depth. For this set of experiments, the offset spacer width is zero. Figure 7 shows the N and PMOS drive current versus SDE depth for devices with 1nA/ $\mu$ m of off state leakage. The SDE depths were adjusted by varying the implant energy (500eV - 40KeV) and the RTA temperature. In Fig. 7 we see that a maximum in the  $I_{DSAT}$  occurs when the vertical junction depth is 35-40nm. For an SDE deeper than 35-40nm, short channel effects degrade due to increased charge sharing resulting in a larger channel length needed to meet the off state criteria and a loss in  $I_{DSAT}$ . SDE depths shallower than 35-40nm results in degraded  $I_{DSAT}$  due to increased external resistance and poor SDE to gate coupling.

Simulation results for the above experiment are shown in Fig. 8 where we quantify external resistance and short channel behavior (defined by source to drain metallurgical distance at 1nA/ $\mu$ m off state leakage) versus SDE junction depth. The simulation results in Fig. 8 support the conclusion that the observed drive current maximum at 35-40nm junction depth results from tradeoffs in short channel effects, external resistance and SDE to gate coupling. Note that these conclusions implicitly assume that the maximum SDE concentration is solid solubility limited.

### IV. Conclusions

We show for the first time that scaling SDE vertical depths below 30-40nm results in little to no performance benefit for 0.1 $\mu$ m devices and beyond since any improvement in short channel effects due to reduced charge sharing is offset by a large increase in external resistance and poor SDE to gate coupling. This implies at the minimum channel length limit of ~30.0nm [4], the physical gate length (minimum metallurgical spacing plus 2x the SDE to gate overlap) will need to be at least 60-70nm, in order to prevent  $I_{DSAT}$  degradation.

### References

- [1] M. Ono et. al., IEDM Tech. Dig., p119-122 1993.
- [2] A. Hori et. al., IEDM Tech. Dig., p485-488 1994.
- [3] M. Bohr et. al., IEDM Tech. Dig., p847-850 1996.
- [4] D.J. Frank et. al., IEDM Tech. Dig., p553-556 1992.

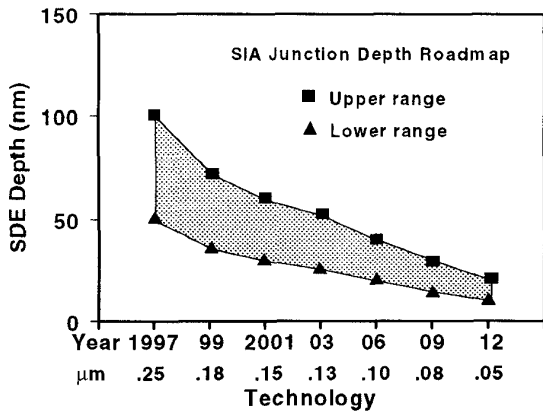


Figure 1: SIA roadmap for junction depth.

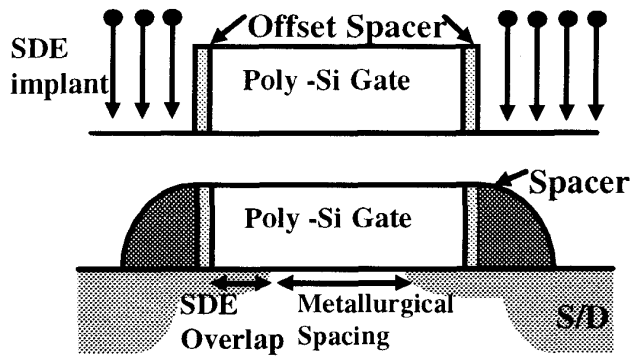


Figure 2: Test structure to evaluate minimum SDE to gate overlap.

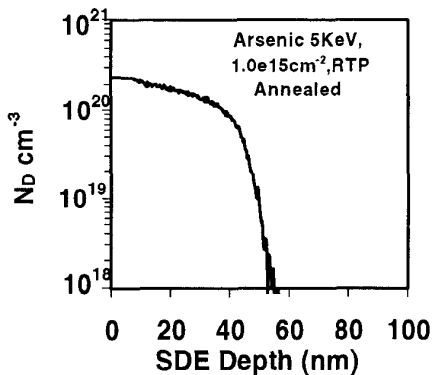


Figure 3: Vertical SIMS profile of Arsenic SDE.

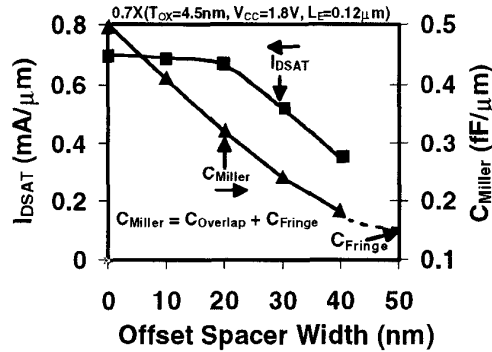


Figure 4:  $I_{DSAT}$  and  $C_{Miller}$  versus spacer offset.

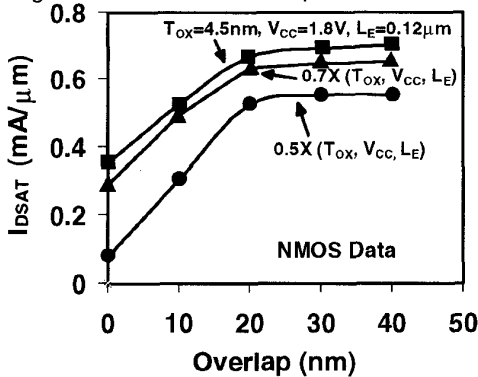


Figure 5:  $I_{DSAT}$  versus SDE overlap (NMOS).

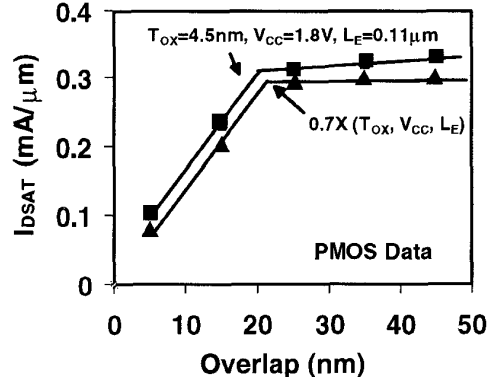


Figure 6:  $I_{DSAT}$  versus SDE overlap (PMOS).

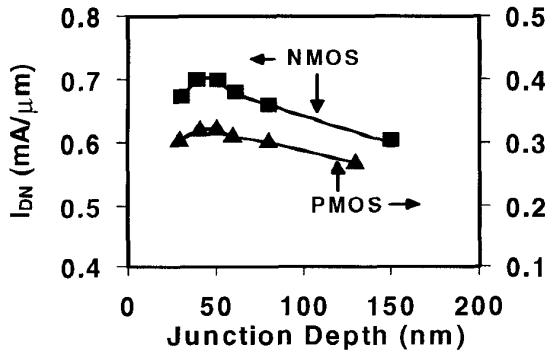


Figure 7:  $I_{DSAT}$  versus SDE depth.

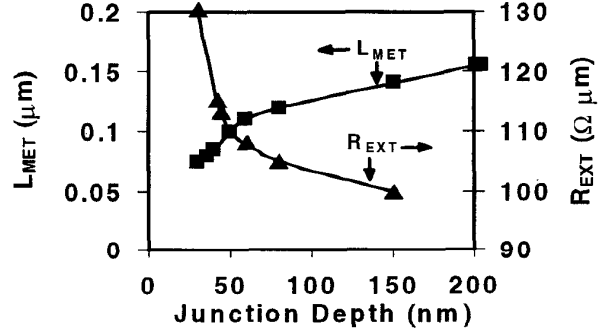


Figure 8: Simulation data quantifying  $R_{EXT}$  and  $L_{MET}$  versus junction depth.