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Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
14/941,669 11/16/2015 Austin Hsu 59507-US-PA 6649

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
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EXAMINER

NGUYEN, SOPHIA T

ART UNIT PAPER NUMBER

2822

NOTIFICATION DATE DELIVERY MODE

03/17/2017

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM
Belinda@JCIPGROUP.COM

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DETAILED ACTION

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Response to Amendment

2. Applicant's amendment dated 12/23/2016, in which claims 1, 7 were amended, claims 5, 9 were withdrawn, claims 12-20 were cancelled, claims 21-28 were added, has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

(a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

3. Claim(s) 1-4, 6 are rejected under 35 U.S.C. 102(a)(1)/(a)(2) as being anticipated by Chen et al. (US Pub. 20130207166).

Regarding claim 1, Chen et al. discloses in Fig. 1, Fig. 5, paragraph [0015]-[0017], paragraph [0033] a field effect transistor, comprising:

a substrate [21] having isolation structures [11] and recesses [23];

at least one gate structure [13], disposed on the substrate [21] and between the recesses [23]

and the isolation structures [11] ;

spacers [17 and 19], disposed on sidewalls of the at least one gate structure [13]; and

strained source and drain regions [22 and 24], disposed in the recesses [23] and located on

opposite sides of the at least one gate structure [13], wherein top edges of the strained source and drain

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regions [22 and 24] extends beyond and below the spacers [17 and 19] and are located beside the sidewalls of the at least one gate structure [13], and portions of the strained source and drain regions [22 and 24] adjacent to the isolation structures [11] have top surfaces coplanar with and levelled with a top surface of the substrate [21].

Regarding claim 2, Chen et al. further discloses in Fig. 1 and Fig. 5, paragraph [0015], paragraph [0031]-0033] the transistor comprising capping layers [37] or [45] located on the strained source and drain regions [22 and 24].

Regarding claim 3, Chen et al. further discloses in paragraph [0015], paragraph [0026], paragraph [0031] wherein a material of the strained source and drain regions [22 and 24] comprises boron-doped silicon germanium and a material of the capping layers [45] comprises a silicon-containing material doped with boron [boron-doped SiGe].

Regarding claim 4, Chen et al. further discloses in Fig. 1 and Fig. 5 wherein at least one of the strained source and drain regions [22 and 24] has a bucket-shaped profile, and a top dimension of the at least one of the strained source and drain regions [22 and 24] is smaller than a width of the at least one of the strained source and drain regions [22 and 24].

Regarding claim 6, Chen et al. further discloses in paragraph [0019]-0020] wherein the at least one gate structure [13] is a polysilicon gate structure or a replacement metal gate structure.

4. Claim(s) 1, 4 and 6 are rejected under 35 U.S.C. 102(a)(1)/(a)(2) as being anticipated by Montanini et al. (US Pub. 20140353741)

Regarding claim 1, Montanini et al. discloses in Fig. 3E, Fig. 3F, a field effect transistor, comprising:

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a substrate [210] having isolation structures [220] and recesses [350][paragraph [0019], paragraph [0029], paragraph [0036]; paragraph [0042], paragraph [0045]],

at least one gate structure [110], disposed on the substrate [210] and between the recesses [350] and the isolation structures [220][paragraph [0019]-[0020], paragraph [0029]];

spacers [335 and 345], disposed on sidewalls of the at least one gate structure [110][paragraph [0034], lines 17-19]; and

strained source and drain regions [240], disposed in the recesses [350] and located on opposite sides of the at least one gate structure [110], wherein top edges of the strained source and drain regions [240] extends beyond and below the spacers [335 and 345] and are located beside the sidewalls of the at least one gate structure [110], and portions of the strained source and drain regions [240] adjacent to the isolation structures [220] have top surfaces coplanar with and levelled with a top surface of the substrate [210][paragraph [0049]-[0050]].

Regarding claim 4, Montanini et al. further discloses in Fig. 3F wherein at least one of the strained source and drain regions [240] has a bucket-shaped profile, and a top dimension of the at least one of the strained source and drain regions [240] is smaller than a width of the at least one of the strained source and drain regions [240].

Regarding claim 6, Montanini et al. further discloses in paragraph [0029] wherein the at least one gate structure [110] is a polysilicon gate structure or a replacement metal gate structure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

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5. Claims 2-3 are rejected under 35 U.S.C. 103 as being unpatentable over Montanini et al. (US Pub. 20140353741) in view of Chen et al. (US Pub. 20130207166)

Regarding claims 2 and 3, Montanini et al. fails to disclose the transistor further comprising capping layers located on the strained source and drain regions; wherein a material of the strained source and drain regions comprises boron-doped silicon germanium and a material of the capping layers comprises a silicon-containing material doped with boron.

Chen et al. discloses in Fig. 5

capping layers [45] located on the strained source and drain regions [22 and 24][paragraph [0031]];

wherein a material of the strained source and drain regions [22 and 24] comprises boron-doped silicon germanium and a material of the capping layers [45] comprises a silicon-containing material doped with boron [boron-doped SiGe][paragraph [0015], paragraph [0026], paragraph [0031]].

It would have been obvious to one of ordinary skill in the art at the time of the effective filing date of the invention to incorporate the teachings of Chen et al. into the method of Montanini et al. to include capping layers located on the strained source and drain regions. The ordinary artisan would have been motivated to modify Montanini et al. in the above manner for the purpose of providing a solution to both the junction leakage and the adverse SCE effects; lowering the sheet resistance of the SiGe/the strained source and drain regions to provide excellent contact characteristics for a contact to be formed to the source and drain regions [paragraph [0031] and paragraph [0033] of Chen et al.].

6. Claims 7-8, 10-11, 21-28 are rejected under 35 U.S.C. 103 as being unpatentable over Harley et al. (US Pat. 9412843) in view of Chen et al. (US Pub. 20130207166)

Regarding claim 7, Harley et al. discloses in Fig. 6- Fig. 7 a field effect transistor, comprising: a substrate [100] having isolation structures [200] column 3, lines 34-44, column 5, lines 30-48]; gate structures [120 and 130], disposed on the substrate [100] and between the isolation structures [200][column 3, lines 55-67 and column 4, lines 1-38];

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spacers [140 and 160] disposed on sidewalls of the gate structures [120][column 4, lines 39-46 and column 5, lines 8-21];

strained source and drain regions [170], disposed within recesses [165] of the substrate [100] and located on opposite sides of the gate structures [120], wherein the spacers [140 and 160] cover top edges of the strained source and drain regions [170] beneath the spacers [140 and 160], portions of the strained source and drain regions [170] adjacent to the isolation structures [200] have top surfaces coplanar with and levelled with a top surface of the substrate [100][column 6, lines 8-29].

Harley et al. fails to disclose

capping layers located on the strained source and drain regions.

Chen et al. discloses in Fig. 5 and paragraph [0031]

capping layers [45] located on the strained source and drain regions [22 and 24].

It would have been obvious to one of ordinary skill in the art at the time of the effective filing date of the invention to incorporate the teachings of Chen et al. into the method of Harley et al. to include capping layers located on the strained source and drain regions. The ordinary artisan would have been motivated to modify Harley et al. in the above manner for the purpose of lowering the sheet resistance of the SiGe/the strained source and drain regions to provide excellent contact characteristics for a contact to be formed to the source and drain regions [paragraph [0031] of Chen et al.].

Regarding claim 8, Harley et al. and Chen et al. discloses wherein at least one of the strained source and drain regions has a bucket-shaped profile, and a top dimension of the at least one of the strained source and drain regions is smaller than a width of the at least one of the strained source and drain regions measuring from a widest portion thereof [Fig. 7, column 5, lines 30-49 of Harley et al., Fig. 1, Fig. 5 of Chen et al.].

Harley et al. discloses in Fig. 7 wherein the width of the at least one of the strained source and drain regions [170] measuring from the widest portion thereof is substantially equivalent to a spacing of the gate structures [120 and 130] measuring from the sidewalls of two most adjacent gate structures [120].

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Therefore, the combination of Harley et al. and Chen et al. discloses “wherein at least one of the strained source and drain regions has a bucket-shaped profile, and a top dimension of the at least one of the strained source and drain regions is smaller than a width of the at least one of the strained source and drain regions, and the width of the at least one of the strained source and drain regions is substantially equivalent to a spacing of the gate structures.”

Further, one of ordinary skill in the art would have recognized the finite number of predictable solutions for the relationship of the width of the at least one of the strained source and drain regions measuring from the widest portion thereof with respect to a spacing of the gate structures measuring from the sidewalls of two most adjacent gate structures: the width of the at least one of the strained source and drain regions measuring from the widest portion thereof is less/equal/or greater than a spacing of the gate structures measuring from the sidewalls of two most adjacent gate structures. Absent unexpected results, it would have been obvious to try different width of the at least one of the strained source and drain regions measuring from the widest portion thereof with respect to a spacing of the gate structures measuring from the sidewalls of two most adjacent gate structures to yield a device having desired performance.

Regarding claims 10 and 22, Harley et al. and Chen et al. discloses wherein a material of the strained source and drain regions comprises boron-doped silicon germanium and a material of the capping layers comprises silicon doped with boron; wherein a material of the strained source and drain regions comprises boron-doped silicon germanium and a material of the contact terminals comprises a silicon-containing material doped with boron [paragraph [0015], paragraph [0026] and paragraph [0031] of Chen et al., column 6, lines 8-20 of Harley et al.].

Regarding claim 11, Harley et al. further discloses in Fig. 7, column 3, lines 55-67 and column 4, lines 1-38 wherein the gate structure [120 and 130] comprises:

a gate dielectric strip disposed on the substrate [100];

a gate electrode strip disposed on the gate dielectric strip; and

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a hard mask strip [130] disposed on the gate electrode strip.

Regarding claim 21, Harley et al. discloses in Fig. 6- Fig. 7 a field effect transistor, comprising:

a substrate [100] having isolation structures [200] and recesses [165] located between the isolation structures [200][column 3, lines 34-44, column 5, lines 30-48];

gate structures [120 and 130], disposed on the substrate [100] and between the isolation structures [200][column 3, lines 55-67 and column 4, lines 1-38];

spacers [140 and 160] disposed on sidewalls of the gate structures [120][column 4, lines 39-46 and column 5, lines 8-21];

strained source and drain regions [170], disposed on opposite sides of the gate structures [120], disposed in the recesses [165] of the substrate [100] and located between the isolation structures [200], wherein portions of the strained source and drain regions [170] are located right beneath the spacers [140 and 160] and are in contact with the spacers [170], and portions of the strained source and drain regions [170] adjacent to the isolation structures [200] have top surfaces coplanar with and levelled with a top surface of the substrate [100][column 6, lines 8-29]; and

Harley et al. fails to disclose

contact terminals located on the strained source and drain regions.

Chen et al. discloses in Fig. 5 and paragraph [0031]

contact terminals [45] located on the strained source and drain regions [22 and 24].

It would have been obvious to one of ordinary skill in the art at the time of the effective filing date of the invention to incorporate the teachings of Chen et al. into the method of Harley et al. to include contact terminals located on the strained source and drain regions. The ordinary artisan would have been motivated to modify Harley et al. in the above manner for the purpose of lowering the sheet resistance of the SiGe/the strained source and drain regions to provide excellent contact characteristics for a contact to be formed to the source and drain regions [paragraph [0031] of Chen et al.].

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Regarding claim 23, Harley et al. and Chen et al. discloses wherein at least one of the strained source and drain regions has a bucket-shaped profile, and a top dimension of the at least one of the strained source and drain regions is smaller than a width of the at least one of the strained source and drain regions measuring from a widest portion thereof [Fig. 7, column 5, lines 30-49 of Harley et al., Fig. 1, Fig. 5 of Chen et al.].

Regarding claim 24, Harley et al. discloses in Fig. 7 wherein the width of the at least one of the strained source and drain regions [170] measuring from the widest portion thereof is substantially equivalent to a spacing of the gate structures [120 and 130] measuring from the sidewalls of two most adjacent gate structures [120].

Regarding claim 25, Harley et al. fails to explicitly disclose wherein the width of the at least one of the strained source and drain regions measuring from the widest portion thereof is less than a spacing of the gate structures measuring from the sidewalls of two most adjacent gate structures.

However, Harley et al. discloses in column 5, lines 34-44 that “[p]recise placement of the angled recessed region 167 may be beneficial to device performance, as small (0.1 nm) changes could lead to relatively large changes in voltage across the channel. By precisely defining the undercut recess 162, anisotropically etching the source/drain recesses 165 can lead to a predictable and repeatable placement of the angled recessed region 167. The substrate 100 may be etched to form the angled recessed corner 167 beneath the first spacers 140. In some embodiments, the angled recessed region 167 may extend beneath the gate 110.” Harley et al. further discloses in column 6, lines 53-65 that “precise placement of the source/drain recesses 165 may be beneficial because the predictability of placement may allow the angled recessed corner 167 to be placed in a predetermined and repeatable position for each gate on a semiconductor chip, and between each semiconductor chip. This may lead to better device performance, as the position for the angled recessed corner 167 may be placed in an optimal position without fear that variability will inhibit device performance. Such placement may allow for control of where sharp material gradients are located, which may allow improved control of strain across the channel, as well as control

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for the amount of resistance in the source/drain regions.” Thus, Harley et al. suggests that the width of the at least one of the strained source and drain regions [170] measuring from the widest portion thereof can be adjusted and optimized by placing the position for the angled recessed corner in an optimal position to allow improved control of strain across the channel, as well as to control for the amount of resistance in the source/drain regions. Thus, it would have been obvious to one of ordinary skill in the art at the time of the effective filing date of the invention to modify the method of Harley et al. to include wherein the width of the at least one of the strained source and drain regions measuring from the widest portion thereof is less/equal/or greater than a spacing of the gate structures measuring from the sidewalls of two most adjacent gate structures. The ordinary artisan would have been motivated to modify Harley et al. in the above manner for the purpose of placing the position for the angled recessed corner in an optimal position to allow improved control of strain across the channel, as well as to control for the amount of resistance in the source/drain regions and thus providing a device having desired performance. Further, one of ordinary skill in the art would have recognized the finite number of predictable solutions for the relationship of the width of the at least one of the strained source and drain regions measuring from the widest portion thereof with respect to a spacing of the gate structures measuring from the sidewalls of two most adjacent gate structures: the width of the at least one of the strained source and drain regions measuring from the widest portion thereof is less/equal/or greater than a spacing of the gate structures measuring from the sidewalls of two most adjacent gate structures. Absent unexpected results, it would have been obvious to try different width of the at least one of the strained source and drain regions measuring from the widest portion thereof with respect to a spacing of the gate structures measuring from the sidewalls of two most adjacent gate structures to yield a device having desired performance.

Regarding claim 26, Harley et al. and Chen et al. further discloses wherein the gate structures are polysilicon gate structures or replacement metal gate structures [column 3, lines 55-62, column 4, lines 19-29 of Harley et al., paragraph [0019] of Chen et al.].

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Regarding claim 27, Harley et al. and Chen et al. further discloses wherein the isolation structures are trench isolation structures [paragraph [0017] of Chen, column 3, lines 51-54 of Harley et al.].

Regarding claim 28, Harley et al. further discloses in Fig. 7 wherein the spacers [140 and 160] are multi-layered structures.

Response to Arguments

7. Applicant's arguments with respect to claims 1-4, 6-8, 10-11, 21-28 have been considered but are moot in view of the new ground of rejection and because the arguments do not apply to the new references being used in the current rejection.

Overall, Applicant's arguments are not persuasive. The claims stand rejected and the Action is made FINAL.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA NGUYEN whose telephone number is (571)272-1686. The examiner can normally be reached on Monday/Friday: 7:30am- 5:00pm.

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Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BRETT A. FEENEY can be reached on (571)2705484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. N./
Examiner, Art Unit 2822

/BRETT FEENEY/
Supervisory Patent Examiner, Art Unit 2822

Notice of References Cited	Application/Control No. 14/941,669	Applicant(s)/Patent Under Reexamination HSU ET AL.	
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*	D	US-2015/0200299 A1	07-2015	CHEN; I-Chih	H01L29/7848	257/192
*	E	US-2015/0311341 A1	10-2015	Hur; Sung Gi	H01L21/02532	257/190
*	F	US-2016/0005863 A1	01-2016	KUANG; SHIN-JIUN	H01L21/30604	257/190
*	G	US-9,287,398 B2	03-2016	Kwok; Tsz-Mei	H01L29/7848	1/1
*	H	US-2016/0126146 A1	05-2016	HOENTSCHEL; Jan	H01L21/823864	257/336
*	I	US-9,412,843 B2	08-2016	Harley; Eric C.	H01L29/66636	1/1
	J	US-				
	K	US-				
	L	US-				
	M	US-				


FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims 	Application/Control No. 14941669	Applicant(s)/Patent Under Reexamination HSU ET AL.
	Examiner SOPHIA NGUYEN	Art Unit 2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
 R.1.47

CLAIM		DATE							
Final	Original	07/13/2016	09/17/2016	03/08/2017					
	1	÷	✓	✓					
	2	÷	✓	✓					
	3	÷	✓	✓					
	4	÷	✓	✓					
	5	÷	N	N					
	6	÷	✓	✓					
	7	÷	✓	✓					
	8	÷	✓	✓					
	9	÷	N	N					
	10	÷	✓	✓					
	11	÷	✓	✓					
	12	÷	N	N					
	13	÷	N	N					
	14	÷	N	N					
	15	÷	N	N					
	16	÷	N	N					
	17	÷	N	N					
	18	÷	N	N					
	19	÷	N	N					
	20	÷	N	N					

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S38	80	(isolation or STI) same gate same recess same (strained or stressed) same source same drain same spacer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 09:37
S39	107	(isolation or STI) same gate same (recess or opening or groove) same (strained or stressed) same source same drain same spacer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 09:39
S40	27	S39 not S38	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 09:39
S41	343	(isolation or STI) same gate same (recess\$3 or opening\$1 or groov\$3) same (strain\$3 or stress\$3) same source same spacer\$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 09:42
S42	236	S41 not S39 not S38	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 09:42
S43	15	("20030040158" "20030080361" "20050218455" "20060186557" "20080029834" "20080064157" "20080099786" "20090026551" "20090065807" "20090267119" "20110039379" "20110147852" "6281562" "6621131" "6797556").PN. OR ("8907425").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2017/03/08 09:48
S44	8	("20090065867" "7402872" "7719060" "7776697").PN. OR ("8877581").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2017/03/08 09:51
S45	0	"14941669"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 10:21
S46	343	(isolation or STI) same gate same (recess\$3 or opening\$1 or groov\$3) same	US-PGPUB;	ADJ	ON	2017/03/08 10:22


		(strain\$3 or stress\$3) same source same spacer\$1	USPAT; USOCR; EPO; JPO; DERWENT			
S47	95110	((H01L29/7848 OR H01L29/66636 OR H01L21/823807 OR H01L21/823814 OR H01L29/665 OR H01L21/02532 OR H01L29/66628 OR H01L29/78 OR H01L21/823412 OR H01L21/823878 OR H01L29/1054 OR H01L29/0653 OR H01L21/823425 OR H01L29/0847 OR H01L21/26586 OR H01L29/7846 OR H01L21/30604 OR H01L21/3065 OR H01L21/31116 OR H01L21/76232 OR H01L21/02381 OR H01L29/0856 OR H01L29/0873 OR H01L29/41725 OR H01L29/41783).CPC.)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 10:26
S48	445	S47 and ((isolation or STI or insulation) same gate same (recess\$3 or opening\$1 or groov\$3) same source same spacer\$1 same (under or below))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 10:27
S49	355	S48 not S41	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 10:27
S50	26	S47 and ((isolation or STI or insulation) same gate same (recess\$3 or opening\$1 or groov\$3) same source same rais\$3 same spacer\$1 same (silicon germanium or SiGe))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 10:36
S51	32	S47 and ((isolation or STI or insulation) same gate same (recess\$3 or opening\$1 or groov\$3) same source same rais\$3 same strain\$3)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 10:38
S52	0	S47 and ((isolation or STI or insulation) same gate same (recess\$3 or opening\$1 or groov\$3) same source ame strain\$3)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 10:40
S53	327	S47 and ((isolation or STI or insulation) same gate same (recess\$3 or opening\$1 or groov\$3) same source same strain\$3)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 10:40
S54	3703	S47 and ((isolation or STI or insulation) same source same (recess\$3 or opening\$1 or groov\$3) same gate)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 10:45
S55	1398	S47 and ((isolation or STI or insulation) same source same (recess\$3 or opening\$1	US- PGPUB;	ADJ	ON	2017/03/08 10:45

		or groov\$3) same gate same spacer)	USPAT; USOCR; EPO; JPO; DERWENT			
S56	1342	S47 and ((isolation or STI or insulation) same source same drain same (recess\$3 or opening\$1 or groov\$3) same gate same spacer)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 10:45
S57	189	S47 and ((isolation or STI or insulation) same source same drain same (recess\$3 or opening\$1 or groov\$3) same gate same spacer same strain\$3)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 10:46
S58	89	S47 and ((isolation or STI or insulation) same raised same source same drain same (recess\$3 or opening\$1 or groov\$3) same gate same spacer)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 10:46
S59	64	S47 and ((isolation or STI or insulation) same raised same source same drain same (recess\$3 or opening\$1 or groov\$3) same (strain\$3 or stress\$3))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 10:50
S60	8	("20050148147" "20060138398" "20070249168" "20070281493" "20080001182" "20110024801" "7195985").PN. OR ("8455859").URPN.	US- PGPUB; USPAT; USOCR	ADJ	ON	2017/03/08 10:51
S61	25	("20060115949" "20060138398" "20060231877" "20080237634" "20090174002" "20090191679" "20110316046" "20120132957" "5500869" "6303447" "6348384" "6605498" "6921913" "7071065" "7238561" "7253086" "7413958" "7553717" "7601983" "7700452" "7791064" "8253204" "8455324" "8455859" "8558289").PN. OR ("9293537").URPN.	US- PGPUB; USPAT; USOCR	ADJ	ON	2017/03/08 10:53
S62	10	("20060076622" "20070012913" "20070235802" "20080128746" "20080246057" "20100193876" "6946350" "7335959" "7494858").PN. OR ("8558289").URPN.	US- PGPUB; USPAT; USOCR	ADJ	ON	2017/03/08 10:55
S63	36	("20030098479" "20040092114" "20040262683" "20050118793" "20050148147" "20060088968" "20060115949" "20060240630" "20070023847" "20070072353" "20070105331" "20070249168" "20080242032" "5559053" "5858857" "6165870" "6562696").PN. OR ("7553717").URPN.	US- PGPUB; USPAT; USOCR	ADJ	ON	2017/03/08 10:56
S64	14	("20070161216" "20080237634" "20090032880" "20120064686" "20120086056" "20120132957" "20120135576" "20140127893"	US- PGPUB; USPAT; USOCR	ADJ	ON	2017/03/08 10:57

		"5681768" "7553717" "7569848" "8357573" "8460980" "8507386").PN. OR ("9412843").URPN.				
S65	64	S47 and ((isolation or STI or insulation) same raised same source same drain same (recess\$3 or opening\$1 or groov\$3 or cavit\$3) same (strain\$3 or stress\$3))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/08 11:00
S66	25	("20040173815" "20050184345" "20050285203" "20060166492" "20070004123" "20120153387" "20130069172" "20130109144" "20130207166" "20140175556" "20140335674" "20150236157" "4145703" "4173765" "4214312" "4222062" "4222063" "4407058" "4794283" "7544577" "7553717" "7608515" "7821044" "8012820" "8450165").PN. OR ("9287398").URPN.	US- PGPUB; USPAT; USOCR	ADJ	ON	2017/03/08 11:00

3/ 10/ 2017 2:30:33 PM

C:\Users\snguyen8\Documents\EAST\Workspaces\14941669.wsp

Search Notes 	Application/Control No. 14941669	Applicant(s)/Patent Under Reexamination HSU ET AL.
	Examiner SOPHIA NGUYEN	Art Unit 2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/7848,66636,66628,665,41783;H01L21/823814,823418	09/17/2016	SN
H01L29/7848,66636,665,66628,78,1054,0653,0847,7846,0856,0873,41725,41783;H01L21/823807,823814,02532,823412,823878,823425,26586,30604,3065,31116,76232,02381	03/08/2017	SN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST	09/17/2016	SN
EAST	03/08/2017	SN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/S.N./ Examiner.Art Unit 2822	
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