

IPR2025-00639
Patent No. 9,122,965

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., and
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

v.

ICASHE, INC.,

Patent Owner.

Case IPR2025-00639

Patent No. 9,122,965

DECLARATION OF MARC E. LEVITT, Ph.D.

I, Marc E. Levitt, Ph.D., of San Jose, California, declare that:

I. ASSIGNMENT

1. I have been retained by Robins Kaplan LLP on behalf of Patent Owner iCashe, Inc. (“iCashe”) as an expert with regard to this matter. I understand that Petitioners are requesting that the Patent Trial and Appeal Board (“Board”) institute inter partes review (IPR) of U.S. Pat. No. 9,122,965 (“’965 patent”) (Ex. 1001).

2. In my capacity as an expert, I have been asked to provide my independent analysis and opinions regarding the ’965 patent, the prosecution history of the ’965 patent and related applications as applicable, the alleged prior art relied upon by Petitioner, the meaning of various claim terms from the ’965 patent from the perspective of a person of ordinary skill in the art (“POSITA”), and the opinions offered by Petitioners’ expert, Dr. Emmanouil Tentzeris, in his declaration (“Tentzeris Declaration”) (Ex. 1003). My opinions and conclusions are fully discussed in later sections of this declaration.

3. I am an independent consultant, and I am not, and have never been, an employee of iCashe or Samsung. I received no compensation for this declaration beyond my normal hourly compensation based on my time actually spent analyzing the ’965 patent, the prosecution history of the ’965 patent and related applications, the prior art publications relied upon by Petitioners, the Declaration of Dr. Tentzeris,

and other related materials. I will not receive any added compensation based on the outcome of any IPR or other proceedings involving the '965 patent.

II. BACKGROUND QUALIFICATIONS

4. I am an independent high technology consultant with over 30 years of experience in the areas of executive leadership, business development, technology, technology development, and intellectual property. I have extensive technical and business experience in computer architecture, networking, mobile, semiconductor design, semiconductor manufacturing, systems-on-a-chip, systems architecture, technical software, embedded software, enterprise software, algorithms, and computational finance.

5. I graduated from Lehigh University in 1986 with a Bachelor of Science degree with High Honors in Computer Engineering, and later obtained my Master's degree and PhD in Electrical Engineering from the University of Illinois in Urbana-Champaign, Illinois. I completed my studies in 1990, and wrote my doctoral thesis on time-based strategies for semiconductor manufacturing and test under the supervision of Dr. Jacob A. Abraham. During my education, I conducted VLSI testing research at Hewlett-Packard and EDA software development at Digital Equipment Corporation.

6. After receiving my PhD, I worked at Sun Microsystems (Sun) rising to the dual position of Senior Hardware Manager and Senior Staff Engineer. While at

Sun I worked on multiprocessor server systems, high performance workstation systems, microprocessors and related chipsets/ASICs. At Sun I was responsible for, among other things, the test and design-for-test strategy for all SPARC microprocessors and related ASICs, JAVA processors, processor modules, and SPARC reference platform designs. I also worked with issues related to power management, clocking, reset, test, design-for-test, and debug issues throughout numerous departments at Sun Microsystems. I was a key member of the VLSI Design Review team, and reviewed and signed off on every circuit design used inside Sun's custom chips. Additionally, I developed or architected CAD tools to aid in the design, test, manufacture, and debug of integrated circuits and computer systems within Sun.

7. I later brought my extensive architecture expertise and expertise in circuit design, development, and manufacturing to positions I held at Sonics Inc. and Transmeta Corp. At Sonics Inc. I was the Director of Silicon Development, in which capacity I was in charge of in-house deep sub-micron design projects in 0.18um CMOS, and was also responsible for developing, planning and executing product ideas, system-on-chip platforms, and OEM silicon based on the Sonics Integration Architecture. At Sonics Inc. I also designed the OC-12 network processor (MIPS based) and assisted in the design and development of two VoIP chipsets.

8. At Transmeta Corp., I was the Director of VLSI. In this position I managed and architected the Northbridge and Southbridge for the Efficeon TM8xxx and the TM6000 1GHz x86 Low Power System on a Chip project, for which I was responsible for the logic, verification, and circuit design teams on this unique project that integrated a 1GHz x86 processor, north bridge, south bridge, video processing, and graphics engine in 130nm/90nm technology. My responsibilities included all hardware product management, scheduling, resource planning, and lab prototype work, including managing interactions with software engineering (CMS, BIOS, and drivers), systems engineering, packaging, foundry, and operations requirements for the project. Additionally, I was a key interface with consumer electronics companies in developing solutions for set-top-boxes for smart video delivery and processing.

9. I later became a Vice President and General Manager at Cadence Design Systems, where I ran Cadence's Design for Manufacturing (DFM) Business Unit, which is responsible for enterprise class technical software used in semiconductor design, analysis, and manufacturing including mixed signal and RF circuit design and analysis. I oversaw a \$130+ million per year business and approximately 240 worldwide employees in R&D, operations, marketing, sales, and application engineering with teams in Japan, Taiwan, Russia, India and the United States.

10. Since my work at Cadence Design Systems, I have principally acted as a professional consultant in the areas of technology development, intellectual property, and business development in the areas of software, networking hardware, and semiconductors. My consulting clients included CNEX LABS where I helped develop the clocking, power management, and PCIe capabilities of their NVMe PCIe SSD controller ASIC.

11. As a result of my extensive industry experience, I have expertise in, among other things, computer architecture, VLSI design, VLSI manufacturing, software, and systems. This expertise and background extends to at least the following areas:

- Computer Architecture: RISC, CISC, DSP, memory hierarchies, memory systems, pipelining, clock design, power management, low power design, microcode, microarchitecture, multicore, 2d & 3d graphics, SPARC, x86, MIPS, ARM, USB, GPU, VGA, LPC, PCI, PCI-X, Hypertransport, PCIe, NVMe, SoCs, AGP, Ethernet, cache, FPU, TLB, DDR, DRAM, and SRAM;
- VLSI Design: All aspects of front to back design process and methodologies for digital, analog, and mixed signal designs, including RTL (Verilog & VHDL), logic, circuit, physical design, layout, verification, PLL, RAM, TLB/CAM, IO, PHY, scan, DFT, BIST, LCDs;

- VLSI Manufacturing: CMOS, mask making, OPC, testing, packaging, yield enhancement, debug, failure analysis, and production ramp;
- Software: Computer aided design (CAD), drivers, BIOS, operating systems (Windows, Linux, Unix, Android, etc.), mobile software, embedded software, JSRs, client-server software, enterprise software, applications, large web based systems (Google, Facebook, AWS etc.), algorithms, and computational finance. I have expertise in the following exemplary languages: Fortran, C, C++, Perl, Python, Pascal, Java, and ASM; and
- Systems: Systems-on-a-Chip, VoIP, networking, multiprocessors, servers, PCs, parallel processing, distributed computing, mobile phone, tablets, settop-boxes, TV, digital camera/camcorders, encryption/security, power management, ACPI, LCD, OLED, GSM, EDGE, WCDMA, 3GPP, CDMA, IEEE 802.x/Ethernet, switching, routing, RFID, Bluetooth.

12. I am also a named inventor on at least 15 issued U.S. patents relating to, among other things, circuit design, logic design, memory design, hardware testing, software, diagnosis, and formal verification. I have published as author or co-author over 30 journal articles, conference publications, and book chapters.

13. I was also the recipient of the Sun Microelectronics Engineering Excellence Award in 1996. I am a member of Tau Beta Pi and Eta Kappa Nu

Engineering Honor Societies and, from January to March of 1997, I was the guest editor of IEEE Design & Test of Computers magazine for a special issue on microprocessors.

14. My curriculum vitae, which is attached to this declaration as Appendix A, sets forth the details of my background and experience in the relevant field.

III. BASIS FOR OPINIONS

15. I believe that I am qualified to render opinions regarding the technology described and claimed in the '965 patent, based on my experience and education. Based on my expertise and qualifications, I believe that I am qualified to provide opinions as to the state of the art and what a POSITA would have understood, known, or concluded as of the conception of the inventions of the '965 patent. I was working in the integrated circuit and system design field in the 2008 timeframe, worked closely with many others in the field, companies designing RF circuits, and participated in various industry organizations.

16. In reaching my opinions and conclusions, I have relied upon my education, my work experience in the relevant field, and my training, and considered and relied upon my review and analysis of the following materials:

- The Petition;
- The '156 patent (Ex. 1001);
- The prosecution history of the '156 patent (Ex. 1002);

- The Dreifus Declaration (Ex. 1003);
- Ex. 1004, U.S. Patent App. Pub. No. 2010/0112941 (“Bangs”);
- Ex. 1005, U.S. Patent App. Pub. No. 2009/0040022 (“Finkenzeller”);
- Ex. 1006, U.S. Patent App. Pub. No. 2009/0215489 (“Kerdraon”);
- Ex. 1007, U.S. Patent App. Pub. No. 2008/0073426 (“Koh”);
- Ex. 1008, U.S. Patent App. Pub. No. 2007/0156436 (“Fisher”);
- Ex. 1009, File History for U.S. Patent Application No. 12/188,346 (“’346 Application File History”);
- Ex. 1011, File History for U.S. Patent No. 9,483,722 (“’722 File History”);
- Ex. 1014, Plaintiff iCash’s Infringement Contentions, Including Exhibit B;
- Ex. 1015, Dachs, C., NFC — The Intuitive Contactless Technology Becomes Reality, 122 E&I Elektrotechnik und Informationstechnik 466 (Dec. 1, 2005) (“Dachs”);
- Ex. 1017, U.S. Patent App. Pub. No. 2005/0224589 (“Park”);
- Ex. 1018, U.S. Patent No. 8,260,199 (“Kowalski”);
- Ex. 1023, U.S. Patent No. 5,943,624 (“Fox”);
- Ex. 1026, U.S. Patent App. Pub. No. 2008/0235796 (“Buhr”);
- Ex. 1027, Finkenzeller, K., RFID Handbook, First Edition (“Finkenzeller-RFID”);

- Ex. 1028, Goldweber Declaration for Ex. 1027;
- Ex. 1031, U.S. Patent App. Pub. No. 2004/0133787 (“Doughty”); and
- Ex. 1036, Mayes, K. et al., Smart Cards, Tokens, Security and Applications (December 11, 2007).
- Ex. 2032, P5CN072 Secure Dual Interface PKI Smart Card Controller – Short Form Specification, Rev. 1.0 (Mar. 9, 2005) (“P5CN072 Specification”) Ex. 2033, (PN532/C1 Near Field Communication (NFC) controller – Product short data sheet, Rev. 3.2 (Sept. 20, 2012); and
- Ex. 2033, PN532/C1 Near Field Communication (NFC) controller – Product short data sheet, Rev. 3.2 (Sept. 20, 2012)

IV. LEVEL OF SKILL IN THE ART AND BASIS FOR OPINIONS

17. For purposes of this declaration, I do not dispute the following opinions of Dr. Tentzeris:

- That the patent claims and prior art should be considered “through the eyes of a person of ordinary skill in the art at the time of the alleged invention,” and the various factors that contribute to that consideration as listed in Ex. 1003, ¶ 56;
- That “a person having ordinary skill in the art in this matter would have had a Bachelor’s degree in computer science, computer engineering, electrical

engineering, or a similar field, with 2-3 years” of professional experience,” where [a]dditional graduate education could substitute for professional experience or significant experience in the field could substitute for formal education.” Ex. 1003, ¶ 57.

18. I disagree with Dr. Tentzeris that a POSITA in this matter necessarily must have specific experience in “smartcards and contactless communications” rather than electronic devices more generally. *Id.* The technology at issue in this matter and the state of the art at the time of the ’965 patent’s priority date would be understood by a person who has the qualifications I list above, even without specific experiences with “smartcards and contactless communications.”

19. Based on my experience, and whether under Dr. Tentzeris’s definition or my own, I am qualified to render opinions regarding the technology claimed and described in the ’965 patent. Based on my expertise and qualifications, I am qualified to provide an opinion as to what a POSITA would have understood, known, or concluded as of the 2008 timeframe.

V. RELEVANT LEGAL PRINCIPLES

20. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. I have applied these legal principles in rendering my opinions below.

A. Claim Construction

21. I understand that the ordinary and customary meaning of a claim term is the meaning that the term would have to a POSITA at the time of the invention.

22. In the absence of an express intent on the part of the inventor to give a special meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by a POSITA.

23. I understand that it is the use of the words in the context of the written description, and as customarily used by those skilled in the relevant art, that accurately reflects both the ordinary and the customary meaning of the terms in the claims.

24. I understand that the basis for a term's ordinary and customary meaning may be derived from a variety of sources, including the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art at the time of the invention.

25. I have been instructed that dictionary definitions or definitions from technical references can be used to inform or confirm the ordinary and customary meaning of words found in a claim, but that in construing claim terms, the general meanings gleaned from reference sources, such as dictionaries, must always be compared against the use of the terms in the context of the claim itself.

26. I understand that a patent applicant is entitled to be his or her own lexicographer (in other words, provide his or her own meaning to a word or phrase) and may rebut the presumption that claim terms are to be given their plain and ordinary meaning. To do so, the applicant must clearly set forth a definition of the term that is different from its ordinary and customary meaning. Where the applicant provides an explicit definition for a term, that definition will control interpretation of the term as it is used in the claim in which it appears. I understand that the specification can also be relied on for more than just explicit lexicography to determine the meaning of a claim term. For example, I understand that the meaning of a particular claim term may also be determined by implication, that is, according to the usage of the term in the context of the specification.

B. Anticipation

27. I understand that under U.S. Patent Law, 35 U.S.C. § 102, a claim is invalid as anticipated only if each and every element as set forth in the claim is actually disclosed, either expressly or inherently, in a single prior art reference.

28. I am informed that a reference is anticipatory if it contains the claim elements in the same order as claimed, regardless of whether the prior art and the claimed invention are directed to achieving the same purpose.

29. I am informed that a prior art reference may anticipate a claim without expressly disclosing a feature of the claimed invention if that missing feature is necessarily present, or inherent, in the single anticipating reference.

30. I am informed that inherency requires more than the probability or possibility that a claimed feature is present in the prior art, but rather that the feature or characteristic is a necessary part of the prior art. I also am informed that recognition of the inherency by a POSITA— at the time— is not required.

C. Obviousness

31. I understand that under U.S. patent law, 35 U.S.C. §103, a claim is invalid as obvious if the differences sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

32. I am informed that an obviousness analysis requires an assessment of the scope and content of the prior art, the differences between the art and the claims at issue, and the level of ordinary skill in the art. I am told that it is against this backdrop that obviousness is assessed.

33. I am informed that a POSITA is a hypothetical person who is presumed to be aware of all the pertinent prior art. I am also informed that an obvious analysis may take account of the inferences and creative steps that a POSITA would employ.

VI. BACKGROUND OF THE '965 PATENT

A. State of the art at the time of invention

34. Devices that communicate using RF communications, such as near field communication (NFC) devices, traditionally operate in either a passive mode or an active mode. Ex. 1001 at 1:13-14.

35. A passive RF device is characterized by the fact that it does not generate its own RF field; it relies instead upon an interrogating RF field generated by an active device. Ex. 1001 at 1:22-24. To communicate with the active device, the passive device modulates and reflects back the signal received from the active device. Ex. 1001 at 1:22-27. Passive devices are typically not powered. Ex. 1001 at 1:22. Instead, the passive device builds a charge from the active device's signal in order to modulate and return the active device's signal. Ex. 1001 at 1:22-27.

36. In contrast to passive devices, active devices are typically connected to a power source and generate an RF signal. Ex. 1001 at 1:12-15. An active device communicates by transmitting its own generated signal to another device, rather than modulating a received signal. Ex. 1001 at 1:14-16.

37. Active and passive RF device communicate differently. When a passive device communicates with an active device, the active device continuously generates an RF signal and the passive device modulates and reflects back the same signal. When two active devices communicate, the devices must alternate their

transmissions, such that one device receives while the other device transmits. A device cannot both listen and transmit simultaneously.

B. Overview of the '965 patent

38. The inventors of the '965 patent claims created a new mechanism for contactless, secure payments that would interface with existing smartcard infrastructure and allow consumers to make smartcard payments using their mobile phones. Inventors Dr. Narendra, Mr. Tadepalli, and Mr. Chakraborty sought to incorporate smartcard functionality into a mobile phone, thereby allowing users to make contactless radio frequency (RF)-based payments without the need to carry a separate smartcard. They achieved this by developing “performance enhancement circuits” that would allow the phone to operate as an active RF device, but to interface with existing smartcard point-of-sale infrastructure by appearing to the point-of-sale reader as a passive RF device.

39. The inventions claimed in the '965 patent improved the process of effectuating smartcard transactions by integrating a smartcard controller into a mobile device, together with a small form factor antenna, by using performance enhancement circuits coupled between the smartcard controller and the antenna. *See* Ex. 1001 at Abstract, 2:42-45, 19:11-21.

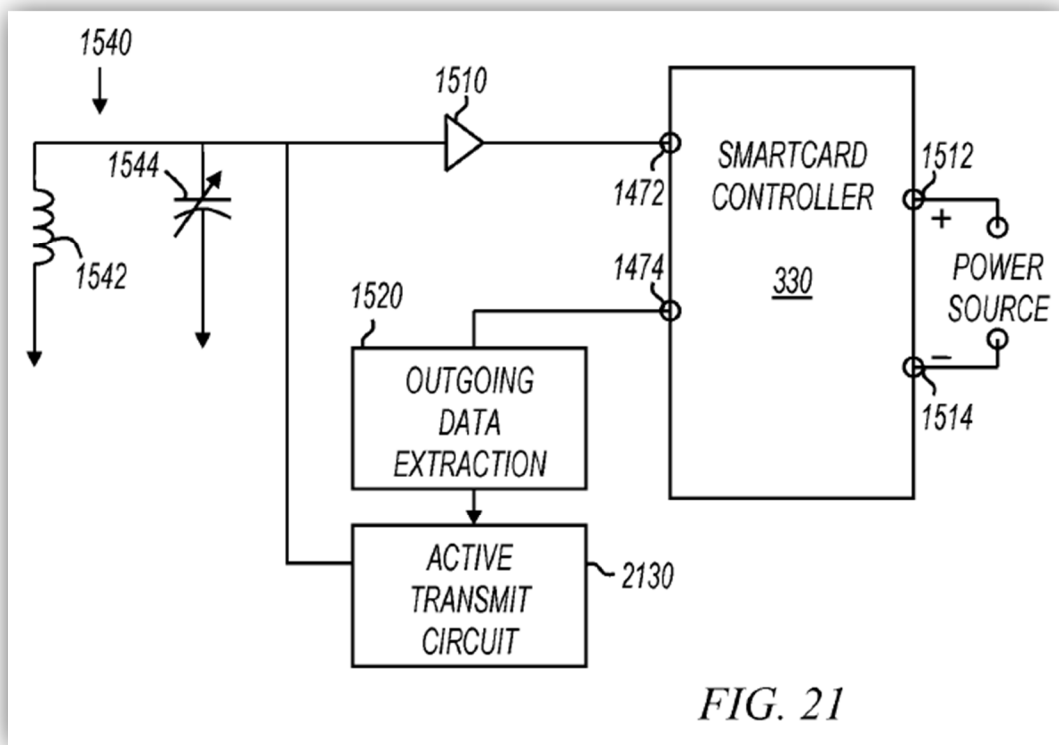
40. In developing this improvement, the '965 patent inventors sought to design a system that would interface with existing smartcard infrastructure. Ex. 1001

at 2:42-45. Conventional point-of-sale smartcard readers are active devices that are configured to communicate with passive devices, such as conventional smartcards in the form of, e.g., credit cards. Therefore, the '965 patent inventors sought to incorporate smartcard circuitry into a mobile phone in a manner that could communicate in a passive mode with conventional smartcard readers. Ex. 1001 at 2:42-45.

41. The '965 patent inventors faced unique challenges in implementing smartcard circuitry into a mobile phone. For example, mobile phones require a relatively small form factor, such that the antennas of traditional passive smartcards were too large. Ex. 1001 at 2:4-6. As the specification of the '965 patent describes, prior to the '965 patent, “[t]here ha[d] been attempts to implement passive [RFID] tags into smaller mobile devices,” such as mobile phones. Ex. 1001 at 2:4-6. But those attempts were “met with limited success due in part to the size of the loop antenna” required. *Id.* at 2:4-12.

42. To overcome this problem, the '965 patent inventors created a device that modulates a received signal to communicate in a passive mode, but that does so by drawing upon an internal power source to *actively*, rather than *passively*, load modulate the received signal. Ex. 1001 at 8:63-65, 9:7-10, 10:10-14. By relying on an internal power source and using active load modulation, the '965 patent device can operate with a smaller antenna than those of traditional passive smartcards.

43. The '965 patent device achieves this using performance enhancement circuits arranged within the phone between the smartcard controller and the antenna. Ex. 1001 at 15:6-10. The performance enhancement circuits include an amplifier and load modulation circuitry, as shown for example in Figures 21 and 25, below. Ex. 1001 at 16:32-46, 17:4-10.



Ex. 1001, Fig. 21.

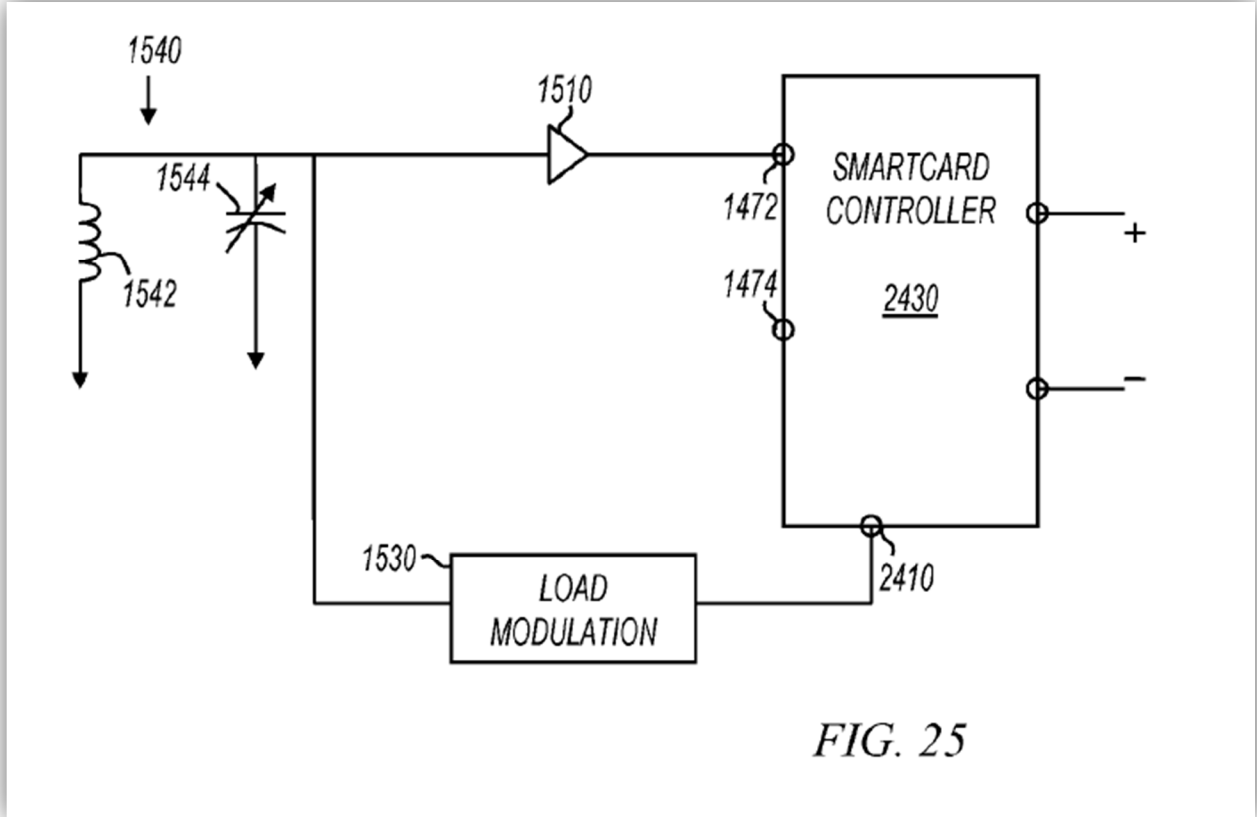


FIG. 25

Ex. 1001, Fig. 25.

44. The amplifier, such as amplifier 1510 shown above in Figure 25, “amplifies the voltage received at antenna 1542, and the amplified voltage is provided to the smartcard controller.” *Id.* at 15:8-10. The amplifier thereby “increases the maximum distance at which the RFID card can operate while receiving data.” *Id.* at 15:10-12.

45. Additionally, performance enhancement circuits include an “active transmit driver circuit” or “active transmit circuit,” as shown above in Figure 21, which includes “circuits to actively transmit a signal rather than simply load

modulate tuned circuit 1540.” Ex. 1001 at 16:32-44. Additionally, performance enhancement circuits include a load modulating circuit, such as load modulation driver circuit 1530 shown in Figure 25. Load modulation driver circuit 1530 “modulates the impedance of the tuned circuit 1540 to form the outgoing data path.” Ex. 1001 at 15:25-27.

46. Load modulation may be passive or active. As the '965 patent describes, passive load modulation is “generally well known, and may be as simple as a switched transistor that adds and removes a reactive element” from the tuned circuit. Ex. 1001 at 15:42-45. However, the '965 patent further discloses an active circuit for actively transmitting data. In particular, the '965 patent describes that performance enhancement circuits may include an active transmit driver circuit. Ex. 1001 at 16:37-40, 19:35-20:3 (claim 7), 20:26-27 (claim 15). “Active transmit driver circuit 2130 may include circuits to actively transmit a signal rather than simply load modulate” a tuned circuit. *Id.* at 16:37-40. That is, rather than responding passively by modulating a received signal, the active transmit driver circuit 2130 actively generates a signal for communicating with another device. Ex. 1001 at 16:40-44.

47. For example, Figure 16 illustrates a waveform of an interrogating RF signal, such as a signal produced by a point-of-sale device. The waveform includes both a carrier frequency 1620 and two sidebands 1610 about the carrier frequency. Ex. 1001 at 15:29-32. The '965 patent describes that, in responding to an

interrogating signal, such as that shown in Figure 16, rather than passively load modulating the received signal or actively generating a responsive signal, the active transmit driver circuit “*form[s] a signal that mimics the sidebands 1610*” of the interrogating frequency “*as if the interrogating RF field experienced load modulation.*” *Id.* at 16:40-44 (emphasis added).

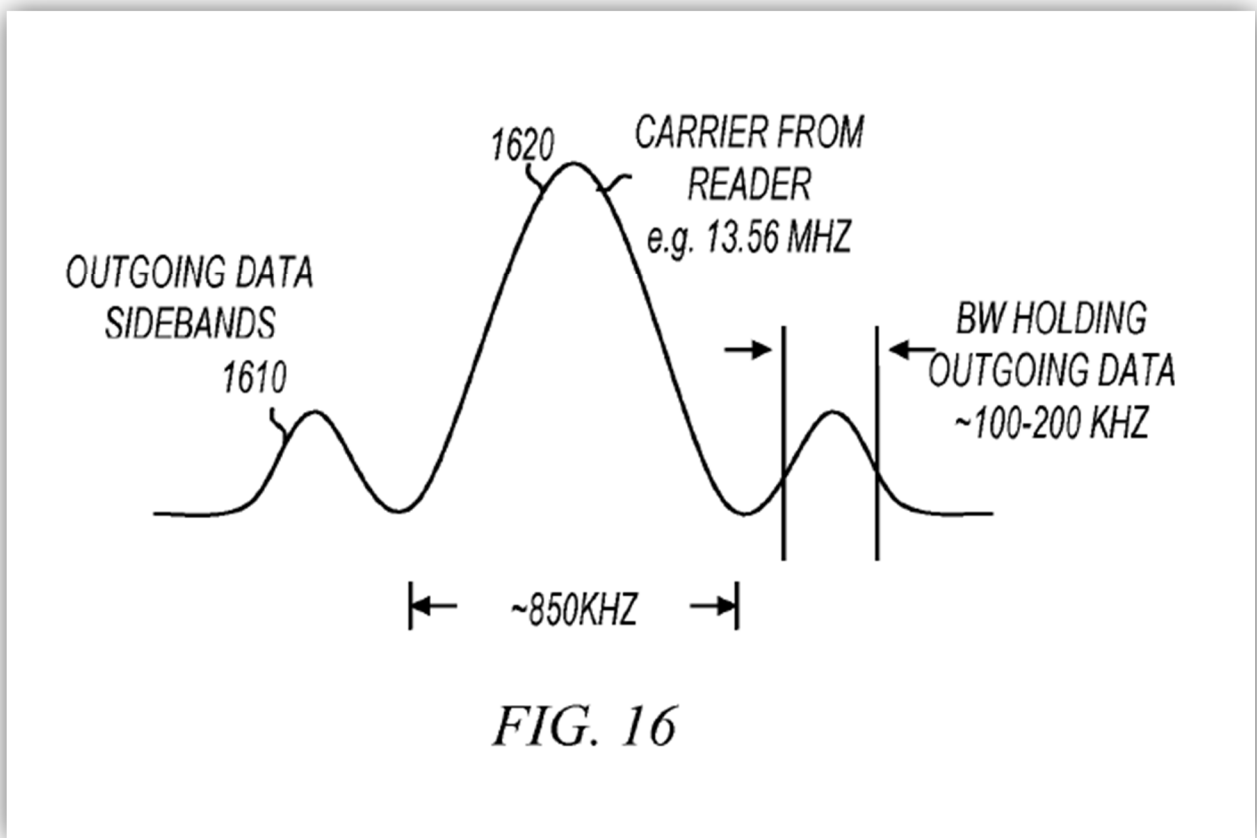


FIG. 16

48. Thus, the active transmit driver circuit performs an active transmission but, by *mimicking the sidebands of the interrogating frequency*, the transmission *appears* to other devices like a passive transmission. By mimicking the sidebands and appearing to operate as a passive smartcard, the claimed mobile device of the

'965 patent could readily interface with then-existing smartcard reader infrastructure, such as point-of-sale devices.

49. The '965 patent further describes that the smartcard controller and performance enhancement circuits draw power directly from the device's own power source. Ex. 1001 at 8:63-65, 9:7-10. By relying on an internal power source, the smartcard controller and performance enhancement circuits can operate without requiring a conventionally large loop antenna that would otherwise be needed to build a high enough charge to power the components. Ex. 1001 at 8:63-65, 9:7-10, 10:10-14. And thus, the circuitry can be provided in a small enough form factor for use in a mobile phone. Ex. 1001 at 9:20-26; *see also* Ex. 1001 at 16:44-46 ("Active transmission can make use of power available on the RFID card and can further increase the usable distance when smartcard controller 330 is transmitting.").

50. Claim 1 of the '965 patent claims as follows:

1[pre] A mobile device comprising:

1[a] a smartcard controller;

1[b] an antenna; and

1[c] performance enhancement circuits coupled between the smartcard controller and the antenna, wherein the performance enhancement circuits include an amplifier and a load modulation circuit, and wherein the amplifier is coupled to

amplify a signal received from the antenna and to provide an amplified signal to the smartcard controller. Ex. 1001, 19:11-21.

51. Claim 7 of the '965 patent claims as follows:

7[pre] A mobile device comprising:

7[a] a smartcard controller;

7[b] an antenna; and

7[c] performance enhancement circuits coupled between the smartcard controller and the antenna, wherein the performance enhancement circuits include an amplifier and an active transmit driver circuit, and wherein the amplifier is coupled to amplify a signal received from the antenna and to provide an amplified signal to the smartcard controller. Ex. 1001, 19:34-20:3.

52. Claim 13 of the '965 patent claims as follows:

13[pre] A mobile device comprising:

13[a] a smartcard controller;

13[b] an antenna;

13[c] an amplifier coupled to amplify signals received at the antenna and drive the smartcard controller; and

13[d] a driver circuit to drive the antenna with data provided by the smartcard controller. Ex. 1001, 20:17-23.

VII. PRIORITY DATE OF THE '965 PATENT

53. I understand that Dr. Tentzeris disputes the priority date of the '965 patent. Dr. Tentzeris asserts that the Challenged Claims are not entitled to the benefit of the August 8, 2008, the date on which U.S. Patent Application No. 12/188,346 was filed. I disagree with Dr. Tentzeris's assertion. I reserve any right that I may have to address this issue in detail should inter partes review be instituted.

VIII. ANALYSIS OF BANGS

54. Dr. Tentzeris opines that claim 1-20 of the '965 patent are either anticipated by or rendered obvious by Bangs (Ground 1). I disagree with Dr. Tentzeris's conclusions regarding Bangs, for the reasons discussed below.

A. Overview of Bangs

55. Bangs is directed to an antenna circuit for an NFC communicator that "reduce[s] the voltage to which circuitry of the NFC communicator is subjected by a received RF H field." Ex. 1004 at Abstract. As Bangs explains, NFC communicators are vulnerable to unpredictable and excess voltage fluctuations that can be caused by a number of variables. Ex. 1004, [0012]-[0014].

56. For example, an NFC communicator may communicate with a variety of devices that "will almost certainly have different antenna spatial envelopes, different dimensions, shapes, footprints or sizes (form factors)," all of which will

affect the RF fields produced by those devices and thus the voltage experienced by the receiving NFC communicator. *Id.* at [0013].

57. Bangs explains that “size or environmental constraints,” which limit the “size and/or topology of the antenna circuit,” may in turn affect the voltage developed across the NFC communicator’s antenna circuit during communication. *Id.* at [0015]. Even items that the user of an NFC communicator is wearing or carrying may influence the voltage experienced by the communicator. *Id.* at [0013].

58. As Bangs states, there is simply “no way of accurately predicting the electromagnetic influences in the environment or environments within which the NFC communicator will operate or how those electromagnetic influences may change with time.” *Id.* at [0013]. Therefore, Bangs seeks to protect NFC functionality “from over-voltage resulting from received high strength RF H fields.” Ex. 1004 at [0090]; *see also id.* at [0014], [0015].

59. Bangs addresses this problem by providing an improved antenna circuit arranged between the antenna and NFC circuitry of an NFC communicator. *Id.* at Abstract, Figs. 3-6. In particular, Bangs incorporates first and second capacitors into the antenna circuit “to reduce the voltage to which circuitry of the NFC communicator is subjected by a received RF H field.” *Id.* at Abstract, [0057]-[0065], Fig. 3. Bangs also discloses reducing voltage on the NFC communicator circuitry by

coupling receive circuitry of the NFC communicator to “only a portion of the antenna coil.” *Id.* at Abstract, [0078]-[0080], Fig. 5

B. Bangs Does Not Disclose Various '965 Patent Claim Limitations

a. “a smartcard controller”

60. All challenged claims include a limitation “a smartcard controller” Ex. 1001, 19:12-21 (claim 1), 19:35-20:3 (claim 7), 20:17-23 (claim 13).

61. Indeed, Bangs does not disclose smartcard functionality, does not contemplate any ability to effectuate secure transactions, and does not provide any teaching that a smartcard controller could be implemented into the circuitry of Bangs.

62. The Petition asserts that “controller 107” of the Bangs “NFC communicator” is a “smartcard controller.” Pet. at 31. This bare assertion is based on controller 107’s control over the NFC communicator, which operates in accordance with standards such as ISO/IEC 14443. *Id.* (citing Ex. 1004 (Bangs) at [0051], [0052], [0005]). The Petition states, “[f]or example, Bangs discloses that ‘controller 107 is coupled to the data store 108 which is provided to store data (information and/or control data) to be transmitted from and/or data received by the NFC communications enabled device,’ and that ‘[s]ome areas of application are payment systems, ticketing systems,’ etc.” *Id.* (citing Ex. 1004 at [0051], [0005]-[0006]; Tentzeris ¶¶ 77-79) (Petitioners’ alterations).

63. The Petition asserts that controller 107 satisfies the “smartcard controller” limitation based on how Petitioners suggest the “smartcard controller” term is used in the ’965 patent. Specifically, the Petition states, “The use of a controller that supports the ISO 14443 standard is consistent with the ’965 specification and prosecution of the related ’722 patent.” Pet. at 31-32 n.3 (citing Ex. 1001 (’965) at 8:50-53). The Petition references a portion of the ’965 specification describing smartcard controllers, emphasized below, within the broader context of the ’965 patent’s discussion of smartcard controllers:

Smartcard controller 330 is a dual interface smartcard controller with one of the interfaces including RFID functionality. In some embodiments, smartcard controller 330 is compatible with passive RFID tag readers in NFC applications. For example, *smartcard controller 330 may be a device capable of implementing all or part of the ISO 14443 standard for contactless NFC devices*. Also for example, smartcard controller 330 may be a dual interface smartcard controller capable of implementing both ISO 7816 and ISO 14443 standards for contact/contactless requirements. The “SmartMX” family of controllers available from NXP Semiconductors N.V. of The Netherlands are examples of suitable dual interface smartcard controllers.

Ex. 1001 at 8:44-56 (emphasis added); Pet. at 31-32 n.3.

64. The language emphasized above and cited in the Petition does not support the Petition's argument that Bangs's controller 107, which is an *NFC controller*, is a smartcard controller. In the cited portion of the '965 specification, the patent is describing the characteristics of a smartcard controller—among them, support for ISO 14443. Ex. 1001 at 8:44-56. But even if a “smartcard controller 330 may be a device capable of implementing all or part of the ISO 14443 standard for contactless NFC devices,” Ex. 1001 at 8:48-50, that does not mean that *any device* implementing the ISO 14443 standard is a smartcard controller. In other words, based on the discussion in the '965 specification, having ISO 14443 capability is a necessary but not a sufficient condition for a device being a smartcard controller.

65. Contrary to the assertions in the Petition, a POSITA would understand that not every controller operating with contactless communication protocols is a “smartcard controller.” NFC is merely a short-range wireless communication technology for exchanging data between two peer devices or an NFC tag (a subset of RFID tags) and a reader. *Id.* It is built on top of ISO 14443 as a protocol. *Id.* Thus, NFC is just another wireless protocol, like WiFi, to exchange data, which is exactly the use described within Bangs. Ex 1004 at [0040]. Use of such protocols does not imply smartcard-specific functionality.

66. The '965 patent identifies specific examples of smartcard controllers, i.e., “the ‘SmartMX’ controllers sold by NXP Semiconductors N.V. of Eindhoven, The Netherlands.” Ex. 1001 at 2:39-41; 8:53-56 (“The ‘SmartMX’ family of controllers available from NXP Semiconductors N.V. of The Netherlands are examples of suitable dual interface smartcard controllers.”). A POSITA would have understood that a “smartcard controller,” generally and as described in the '965 specification, comprises *smartcard functionality*—and more than just communications functionality, like NFC.

67. Consistent with the discussion of smartcard controllers in the '965 specification, a POSITA would understand that a smartcard controller, such as SmartMX smartcard controllers as described in the specification of the '965 patent, include functionality in accordance with certain smartcard standards in existence at the time of the invention. At the time of the inventions claimed in the '965 patent, smartcard standards such as ISO 7816, GlobalPlatform, and JavaCard governed the use and manufacture of smartcards. *Id.*

68. The '965 patent makes frequent reference to ISO 7816—an international standard identifying uniform physical characteristics, electrical interfaces, transmission protocols, security comments, and other specifics for smartcards, specified across 15 parts of the standard. *See, e.g.*, Ex. 1001 at 8:50-53 (“smartcard controller 330 may be a dual interface smartcard controller capable of

implementing both ISO 7816 and ISO 14443 standards for contact/contactless requirements”); 5:23-24 (“Electrical contacts 122 may also be compliant with a smartcard ‘contact’ interface (e.g., ISO 7816)”); 6:15-17 (“Mobile computing device 110 may also communicate with RFID card 120 using a ISO 7816 compatible interface or the like.”). Smartcard standards like ISO 7816 set specifications for secure transaction execution, secure key storage, or EMV-style applet processing. Smartcard functionalities include, e.g., a secure element providing the capabilities to securely store and process sensitive data that is considered tamper proof.

69. The Petition fails to establish that the controller disclosed by Bangs is a “smartcard controller.” Indeed, a POSITA would understand that the controller disclosed by Bangs is not a smartcard controller for the reasons discussed above. Bangs does not disclose that its controller 107 is capable of performing any *smartcard* functionality, such as secure transaction execution, secure key storage, or EMV-style applet processing. It is not, for example, ISO 7816 compliant. *Id.* A POSITA would understand that smartcard controllers include a secure element for securely processing and storing sensitive data in accordance with certain smartcard standards in existence at the time of the invention. Ex. 2032 (*P5CN072 Secure Dual Interface PKI Smart Card Controller – Short Form Specification*, Rev. 1.0 (Mar. 9, 2005) (“P5CN072 Specification”) at 8 (showing secure element, i.e., Secure_MX51 CPU).

70. Nor does Bangs provide any indication that its controller 107 meets any *smartcard* specification. Bangs only identifies the controller 107 as operating in accordance with RF communications standards, which are simply contactless communication protocols. Ex. 1004 at [0005] (“Examples of near field RF communicators are defined in various standards for example ISO/IEC 18092, ISO/IEC 14443, ISO/IEC 15693[,] ISO/IEC 21481. Examples of NFC communicators can be found in ISO/IEC 18092 and ISO/IEC 21481 in particular.”), [0052] (describing compatibility with these standards).

C. “wherein the antenna comprises an inductive element too small to draw enough power sufficient to operate the smartcard controller from an interrogating radio frequency (RF) field”

71. Claims 3, 9, and 19 of the '965 patent require “wherein the antenna comprises an inductive element too small to draw enough power sufficient to operate the smartcard controller from an interrogating radio frequency (RF) field.” Ex. 1004, 19:24-27 (claim 3), 20:6-11 (claim 9), 20:35-38 (claim 19).

72. As described above, the '965 patent describes that the smartcard controller and performance enhancement circuits draw power directly from the device's own power source. Ex. 1001 at 8:63-65, 9:7-10, 10:10-14. By relying on an internal power source, the smartcard controller and performance enhancement circuits can operate without requiring a conventionally large loop antenna that would otherwise be needed to build a high enough charge to power the components. Ex.

1001 at 8:63-65, 9:7-10, 10:10-14. Indeed, the smartcard controller and performance enhancement circuits can operate with an antenna so small that it would not, itself, be sufficient to power the smartcard controller by drawing power from an interrogating frequency. Ex. 1001 at 8:63-65, 9:7-10, 10:10-14. This allows the claimed circuitry to be provided in a small enough form factor for use in a mobile phone. Ex. 1001 at 9:20-26.

73. Dr. Tentzeris opines that a POSITA “would have understood” or “found it obvious” that the antenna disclosed by Bangs is too small to draw enough power from an interrogating field to operate the Bangs controller. Ex. 1003 at ¶ 109. Dr. Tentzeris goes on: “Bangs’ antenna does not need to be large enough to power components in the device.” *Id.* Dr. Tentzeris does not support extrinsic evidence for these assertions. I disagree with Dr. Tentzeris’s assertions as they contradict the stated purpose of Bangs.

74. Bangs describes a need in the field of NFC devices to protect NFC circuitry from “large voltage fluctuations” that can occur with existing antenna designs. Ex. 1004, ¶ [0012]. To address that problem, Bangs and his co-inventors provide a circuit design to “limit[] or reduce[]” the voltage from the antenna coil that is “experienced by the remainder of the NFC communicator.” *Id.* at ¶ [0022]. Thus, Bangs discloses an antenna so large that it will generate voltage high enough that other NFC circuitry must be protected.

IX. ANALYSIS OF THE COMBINATION OF BANGS AND KERDRAON

75. Dr. Tentzeris opines that claims 1-20 of the '956 patent are obvious in view of the combination of Bangs and Kerdraon (Ground 2). I disagree with Dr. Tentzeris's conclusions regarding the combination of Bangs and Kerdraon, for the reasons discussed below.

D. Overview of Kerdraon

76. Kerdraon relates to methods and systems for managing applications stored on a mobile terminal, such as a mobile phone. Ex. 1006, abstract, [0002], [0007]. Kerdraon does not disclose, or even relate to, effectuating contactless payments by implementing a smartcard controller into a phone to interface with existing point-of-sale infrastructure.

77. Kerdraon discloses a system containing a "Smart MX card component 33," an NFC module 29, and an antenna 31. Ex. 1006, [0038], [0069], [0070], Fig. 4. Dr. Tentzeris relies on Kerdraon solely for its disclosure of a smartcard controller. Ex. 1003, ¶¶ 177-187. (citing, e.g., Ex. 1006 at [0070]-[0071]). But Kerdraon provides no disclosure regarding smartcard controller communications. Kerdraon does not disclose, or even relate to, effectuating contactless payments by implementing a smartcard controller in a phone to interface with existing point-of-sale infrastructure.

E. A POSITA Would Not Have Either A Reason to Combine Bangs and Kerdraon or an Expectation of Success from the Combination

78. Dr. Tentzeris contends, “Because Bangs already teaches controller 107 accesses and manages stored data (Bangs [0049], [0067]), implementing Kerdraon’s smartcard controller teachings in Bangs’ NFC-enabled mobile phone would have been a straightforward modification.” Ex. 1003 at 187. Dr. Tentzeris further opines that “[a] person of ordinary skill in the art would have understood that Bangs’ controller 107 may be implemented with application specific smartcard functions, as taught by Kerdraon.” *Id.* “Thus,” he concludes, “a person of ordinary skill in the art would have found it straightforward and advantageous to apply Kerdraon’s smartcard controller teaching to Bangs’ NFC-enabled mobile phone, and would have known such a combination (yielding the claimed limitations) would predictably work and provide the expected functionality.” *Id.* I disagree with Dr. Tentzeris’s assertions.

79. At the most basic level, combining Bangs with Kerdraon would entail integrating two discrete components, i.e., Bangs’s NFC controller, i.e., controller 107, with Kerdraon’s “smart card controller,” i.e., “Smart MX card component 33.” A POSITA would recognize that integrating these two components would not be a simple exercise. *Id.* A POSITA would also recognize that integrating the two discrete components would result in a system with particular characteristics. *Id.* Practically,

a POSITA would recognize that, e.g., the SmartMX controller of Kerdraon, integrated with an NFC controller, would use a standard interface such as NFC-WI/S²C for NFC transmission.

80. As a real-world example, technical documentation for an example NXP NFC controller, the PN532, indicates that “[a] complete secure card functionality is only possible in combination with a secure IC using the NFC-WI/S²C interface,” as shown below.

In card emulation mode, the CIU is able to answer to a Reader/Writer command either according to the FeliCa or ISO/IEC 14443A/MIFARE card interface scheme. The CIU generates the load modulation signals, either from its transmitter or from the LOADMOD pin driving an external active circuit. A complete secure card functionality is only possible in combination with a secure IC using the NFC-WI/S²C interface.

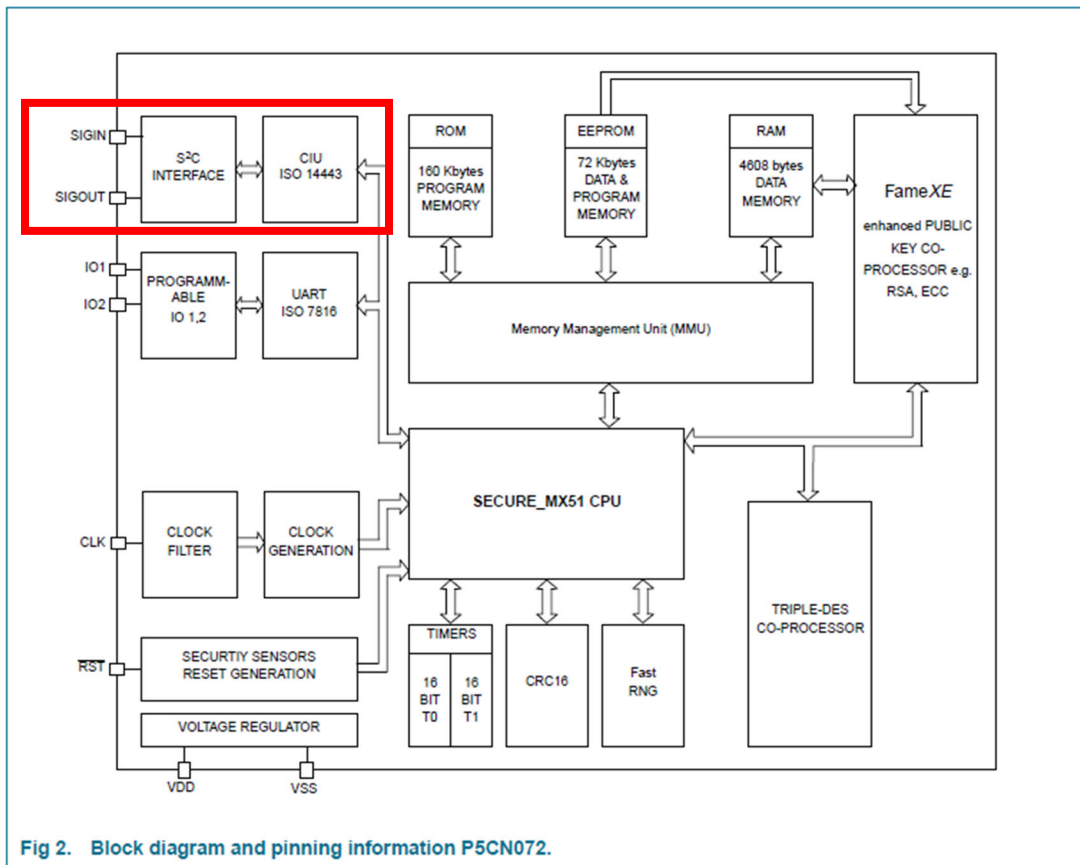
Ex. 2033 (*PN532/C1 Near Field Communication (NFC) controller – Product short data sheet*, Rev. 3.2 (Sept. 20, 2012) (“PN532 Data Sheet”) at 6 (emphasis added).

81. Consistent with the NFC-WI/S²C interface identified in documentation for the NXP PN532 NFC controller, the NXP SmartMX smartcard controller, would also use the NFC-WI /S²C interface. As a real-world example, technical documentation for an example NXP smartcard controller from the time period, the P5CN072 SmartMX smartcard controller, indicates that the SmartMX smartcard controller can be integrated with a compatible NFC IC (e.g., the PN532); such a configuration would use the S²C interface unit, as shown below.

2.1 Product Specific Features

- 72 Kbytes EEPROM (including 192 bytes reserved manufacturer/security area)
- 160 Kbytes User ROM
- 4608 bytes RAM
 - ◆ 256 bytes + 3 Kbytes CXRAM
 - ◆ 1280 bytes FXRAM usable for FameXE
- **Memory Management and Protection Unit (MMU)**
 - ◆ for more details see 2.2. Security Features
- **S²C Interface Unit**
 - ◆ compatible with ISO/IEC14443A-3 via a NFC IC
 - ◆ fully supports the T=CL protocol acc. ISO/IEC14443-4
 - ◆ Data Transfer rates supported (106 Kbit/s)

Ex. 2032 (P5CN072 Specification) at 1 (emphasis added).



Ex. 2032 (P5CN072 Specification) at 8 (annotations added).

82. As these examples illustrate, and as a POSITA would recognize, smartcard controllers such as the SmartMX controllers disclosed in the '053 patent, as well as Kerdraon (*see* Ex. 1006 at [0070]-[0071]), would use, e.g., the NFC-WI/S²C interface. A POSITA would also recognize that use of the NFC-WI/S²C interface to integrate the NFC controller and the SmartMX smartcard controller would result in a device with a *passive interface*, and that would communicate with an NFC transceiver via the NFC-WI standard, which is a passive mode, as discussed below. *Id.* Specifically, as discussed below, and as disclosed in NXP documentation, when a smartcard controller is interfaced to an NFC transceiver device, for compatibility and security reasons, the resulting communication is entirely passive. It would thus not involve any performance enhancing circuits as disclosed in the '053 patent, as discussed below.

83. For example, Philips/NXP documentation regarding the PN532 NFC controller demonstrates this passive communication. When the PN532 NFC controller solution is used to support secure smartcard capabilities through a device such as a SmartMX smartcard controller, through the integration described above, it must do so over the NFC-WI/S²C interface (i.e., SIGIN and SIGOUT) and use the LOADMOD pin to drive the external circuit.

In card emulation mode, the CIU is able to answer to a Reader/Writer command either according to the FeliCa or ISO/IEC 14443A/MIFARE card interface scheme. The CIU generates the load modulation signals, either from its transmitter or from the **LOADMOD** pin driving an external active circuit. A complete secure card functionality is only possible in combination with a secure IC using the NFC-WI/S²C interface.

Ex. 2033 (PN532 Data Sheet) at 6 (emphasis added).

84. The interface and operations based on the S²C interface and LOADMOD described in the PN532 Data Sheet do not use the circuits and functionality disclosed in the challenged claims of the '053 patent, including at least the “amplifier” and “active transmit driver circuit” limitations. As illustrated below, the use of SIGIN, SIGOUT, and LOADMOD renders the transmit drivers (TX1, TX2) and amplifiers (I-channel Amplifier, Q-channel Amplifier) unused.

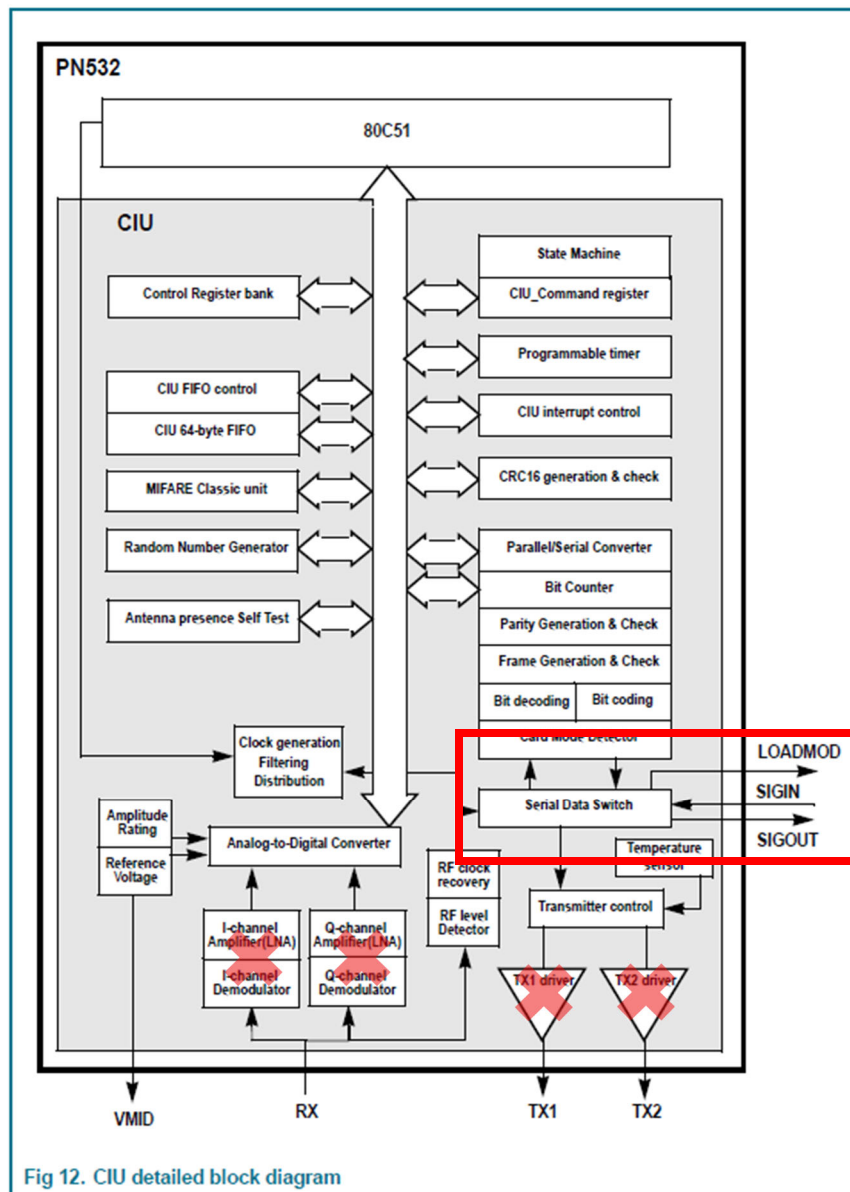


Fig 12. CIU detailed block diagram

Ex. 2033 (PN532 Data Sheet) at 19 (annotations added).

85. Because these limitations of the combined system would have been apparent to a POSITA, a POSITA would not have been motivated to combine Bangs and Kerdraon. Neither the Petition nor Dr. Tentzeris addresses any of these readily apparent technical issues with combining Bangs's NFC controller with a smartcard

controller like Kerdraon's. Instead, the Petition sets forth a number of purported reasons why it would be beneficial for Bangs to include a smartcard controller. *See* Pet. at 63-65. But the Petition does not begin to explain how Kerdraon's smartcard controller could be integrated into Bangs's system, with Bangs's controller 107.

86. For the reasons set forth above, it would not have been obvious to a POSITA to combine a smartcard controller, like that of Kerdraon, with Bangs.

X. ANALYSIS OF THE COMBINATION OF BANGS AND KOH

87. Dr. Tentzeris opines that claims 1-20 of the '956 patent are obvious in view of the combination of Bangs and Koh (Ground 3). I disagree with Dr. Tentzeris's conclusions regarding the combination of Bangs and Koh, for the reasons discussed below.

F. Overview of Koh

88. U.S. Patent Publication No. 2008/0073426 to Koh et al. (Ex. 1007 or "Koh") is entitled "Method and apparatus for Providing Electronic Purse." Koh was published March 27, 2008. The Petition fails to demonstrate that one of ordinary skill in the art would have been motivated to combine Koh with Bangs and would have had an expectation of success in doing so, as discussed below.

89. Koh discloses "a mechanism provided to devices, especially portable devices, functioning as an electronic purse (e-purse) to be able to conduct transactions over an open network with a payment server without compromising

security.” Ex. 1007 at [0007]. Koh further discloses “a near field communication (NFC) enabled cellphone that includes a Smart MX (SMX) module.” Ex. 1007 at [0033].

G. The Petition Does Not Establish that a POSITA Would Have Either a Reason to Combine Bangs and Koh or an Expectation of Success from the Combination

90. Dr. Tentzeris contends, “Because Bangs already teaches that controller 107 performs generic controller functions, including “processing” requests received from another component and accessing “store[d] data” to provide a “response” (Bangs [0049]–[0051]), it would have been straightforward to apply Koh’s smartcard controller teachings to Bangs’ mobile device.” Ex. 1003 at 195. Dr. Tentzeris further opines that “[a] person of ordinary skill in the art would have understood, and at a minimum found it obvious, to implement Bangs’ controller 107 with application specific smartcard functions, as taught by Koh.” *Id.* “As such,” he concludes, “person of ordinary skill in the art would have found it straightforward and advantageous to apply Koh’s smartcard controller teachings to Bangs’ NFC-enabled mobile phone and would have known such a combination (yielding the claimed limitations) would predictably work and provide the expected functionality.” *Id.* I disagree with Dr. Tentzeris’s assertions.

91. Because the combination of Bangs and Koh would entail the same combination of a SmartMX smartcard controller into Bangs’s system as is discussed

above regarding Kerdraon, the same analysis applies to the combination of Bangs and Koh.

H. A POSITA Would Have Neither Reason to Combine Bangs and Koh or an Expectation of Success from the Combination

92. Here, Petitioners cannot articulate any basis for combining Bangs with Koh. Because the combination of Bangs and Koh would entail the same combination of a SmartMX smartcard controller into Bangs's system as is discussed above regarding Kerdraon, the same analysis applies to the combination of Bangs and Koh.

XI. ADDITIONAL REMARKS

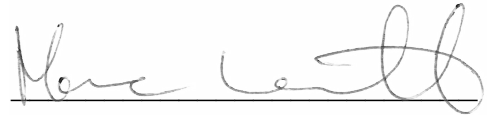
93. I reserve any right that I may have to supplement this declaration if further information becomes available or if I am asked to consider additional information or to submit an additional declaration if *inter partes* review is instituted. Furthermore, I reserve any right that I may have to consider and comment on any additional expert statements and testimony of Petitioner's experts in this matter.

94. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false

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statements may jeopardize the validity of the application, or any patents issued thereon.

Dated: July 16, 2025

A handwritten signature in black ink, appearing to read "Marc Levitt", written over a horizontal line.

Marc E. Levitt, Ph.D.

APPENDIX A

MARC E. LEVITT, PH.D.

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Technology Development ■ Patent/IP Consulting ■ Business Development Startup Ventures, Hardware, Software and Systems

Independent consultant with 30+ years of experience in the areas of executive leadership, business development, technology, technology development, and intellectual property. Broad technical and business depth in computer architecture, networking, mobile, semiconductor design, semiconductor manufacturing, systems-on-a-chip, systems architecture, technical software, embedded software, enterprise software, algorithms, and computational finance. Experience in negotiating IP/patent related issues as part of technology sharing agreements, licensing, and M&A. Strong track record in turn around management and developing new strategic markets through internal development, start-ups, and M&A.

AREAS OF EXPERTISE

Computer Architecture: RISC, CISC, DSP, GPU, memory hierarchies, pipelining, clock design, power management, low power design, microcode, microarchitecture, multicore, memory controllers, 2d & 3d graphics, interconnects/NoC, PCI, PCIe, USB2, USB3, UFS, SDIO, MIPI DSI.

VLSI Design: All aspects of front to back design process and methodologies for digital, analog, and mixed signal designs. Includes RTL (Verilog & VHDL), logic, circuit, physical design, layout, verification. Tapeouts to: IBM, TSMC, UMC, TI, NEC, LSI Logic, & Mitsubishi.

VLSI Manufacturing: CMOS, mask making, OPC, testing, packaging, yield enhancement, debug, failure analysis, and production ramp.

Software: Computer aided design (CAD), drivers, BIOS, operating systems (Windows, Linux, Unix, Android, etc), mobile software, embedded software, JSRs, client-server software, enterprise software, applications, large web based systems (Google, Facebook, AWS etc), algorithms, video streaming, and computational finance.

Systems: Systems-on-a-Chip, VoIP, networking, multiprocessors, servers, PCs, parallel processing, distributed computing, mobile phone, tablets, set-top-boxes, DTV, digital camera/camcorders, automotive, encryption/security, power management, video streaming, MPEG, H264, H265, IEEE 802.x/Ethernet, switching, routing, Bluetooth.

Video: DASH, HLS, Dash.js, ExoPlayer, PlayReady DRM, Widevine DRM, MPEG, H264, H265, VP9, AV1, ffmpeg, GStreamer, CAMF, CENC, BMFF, encoding pipelines, decoding, packaging, all SoC hardware.

Business Development. Product development teams, software product lines, and semiconductor product development projects. Includes strategy, execution, division P&L, margin improvement, and cost management. New product introduction in both large companies and start-ups. Market and technology roadmap development and execution.

PROFESSIONAL EXPERIENCE

Consultant Levitt Technologies

2007 - Present

Independent consultant in the areas of: technology development, intellectual property, and business development/strategy.

Clients in business strategy and technology development include start-ups, VCs, Private Equity firms, and public companies in areas of software, networking hardware, and semiconductors. Partial list of former clients: PhysWare/Nimbic (sold to Mentor Graphics Q2'14), PwrLite Software (sold to Xilinx Q3'09), Proficient Design, and Credence Test Systems.

Intellectual property consulting clients are IP investors, patent brokers, public & private corporations, law firms and their clients in the semiconductor, communications, software, and systems areas. Experience at District Court, ITC, and PTAB including expert reports and being deposed.

Complete list available upon request.

Girasole Imports LLC **2014 – Present**
Managing Member
Italian wine importer and distributor for California.

Commodity Trading Advisor **1999 – Present**
Registered Commodity Trading Advisor with NFA ID 0311607

LongRun Technologies LLC **2010 – 2022**
MEMBER
LongRun Technologies LLC owns and administers former Transmeta LongRun Technology licensing agreements with five (5) major semiconductor and systems companies.

Video Over Cellular Innovations LLC **2010 – 2011**
CHIEF TECHNICAL OFFICER
Responsible for technical positioning and analysis to support the sale of this Emmy Award winning mobile video technology, IP, and associated patents. Worked with potential purchasers and bankers on due diligence. Helped successfully support sale to Samsung October 2011. Patents were part of Apple-Samsung litigation.

Cadence Design Systems, San Jose, California **2002 – 2007**
VICE PRESIDENT & GENERAL MANAGER
Ran Cadence's Design for Manufacturing (DFM) Business Unit. This unit is responsible for enterprise class technical software used in semiconductor design, analysis, and manufacturing. Profit/loss responsibility for ~\$130M/year business worldwide and ~240 worldwide employees in R&D, operations, marketing, sales, and AE teams. Locations in Taiwan, Japan, Russia, India, along with three primary locations in the United States (CA, NJ, NC).

- Lead business partner in creating the corporate partnerships between Cadence and ASML, Cadence and Applied Materials, Cadence and Hitachi HiTech, and Cadence and IBM. Included all IP rights and patent issues.
- Initiated and negotiated M&A activity in support of business unit and company's strategic objectives. Drove the purchase of two start-ups by Cadence for DFM BU. Experience in evaluating and developing business models, financial models, sources of value calculations, synergies, due diligence.
- Present at IEEE conferences such as DAC and ISQED. Participation ranges from technical papers, panel sessions, to keynote addresses.
- Analyst Day team member. Help represent Cadence to Wall Street by presenting Yield and DFM strategy to analysts and fund managers during the event.
- Turned around business unit and drove margins from negative territory to top quartile companywide. Maintained and improved morale, expanded product line, technically overtook competition in key sectors, and improved customer relationships.

Transmeta Corp, Santa Clara, CA **2000 – 2002**
DIRECTOR VLSI
Product manager and architect in charge of running the TM6000 1GHz x86 Low Power System on a Chip project. Responsible for the logic, verification, and circuit design teams on this unique project that integrated a 1GHz x86 processor, north bridge, south bridge, and graphics engine in 130nm/90nm technology. Duties include all hardware product management responsibilities, scheduling, resource planning, and lab prototype work. Interaction with software engineering (CMS, BIOS, and drivers), systems engineering, packaging, foundry, and operations. Coordinate and drive all teams (hw, sw, system) to deliver on commitments.

Sonics Inc, Mountain View, CA **1998 – 2000**
DIRECTOR SILICON DEVELOPMENT
In charge of in-house deep sub-micron design projects in 0.18um CMOS. Responsible for developing, planning and executing product ideas, SoC platforms, and OEM silicon based on the Sonics' Integration Architecture. Ownership encompassed product definition, project planning, resource development, resource allocation, packaging, and test. Designed OC-12 network processor (MIPS based) and assisted in two VoIP chipsets for clients.

Independent

1997 – 1998

CONSULTANT

Clients included Transmeta and Raycer Graphics (now Apple). Worked in the areas of clocks, reset, design-for-test, design-for-debug, and power management. Consulted with management, design teams and product engineering teams on foundry, debug, yield, quality and test issues.

High Frequency Finance, Sunnyvale, CA

1996 – 1998

FOUNDER

Company started to develop and deliver a new generation of decision support tools to professional traders and treasury professionals with emphasis on FX. Extensive work in nonlinear statistics, quantitative finance, and real-time software. Realtime streaming software development for Reuters and Bloomberg. Worked with leading money managers and hedge funds.

Sun Microsystems, Mountain View, CA

1990 – 1997

SR HW MANAGER & SR STAFF ENGINEER

- Significant operational experience performing design, management, and product ramp related tasks.
- Responsible for the test and design-for-test strategy for all SPARC microprocessors and related ASICs, JAVA processors, processor modules, and SPARC reference platform designs.
- Corporate wide consultant on power management, clocking, reset, test, design-for-test, and debug issues.
- Key member of VLSI Design Review team – reviewed and signed off on every circuit design used inside Sun's custom chips.
- Member of ATE selection committee and key interface to test and product engineering organization both inside and outside of Sun.
- Staff Engineer working on the UltraSPARC-I processor. Developed the power management, clocking, test strategy and methodology used for the project at the chip, module, and system level. This strategy and methodology was adopted as a division wide standard used by UltraSPARC-I+, UltraSPARC-II, UltraSPARC-IIi, and UltraSPARC-III.
- Responsible for the evaluation CAD tools. Worked closely with tool vendors to specify new features and functionality. Responsible for specification and some implementation of in-house CAD tools that were directly tied to our advanced design practices.
- Developed, specified, and patented a methodology for fast synchronous SRAM testing that was adopted as a JEDEC standard.

ADDITIONAL EMPLOYMENT

VLSI Testing Research, Hewlett-Packard, 1989

EDA Software Development, Digital Equipment Corporation 1988

PUBLICATIONS, HONORS, AWARDS

Sixteen patents awarded in the areas of circuit design, logic design, hardware testing, software, diagnosis, and formal verification

Over 30 journal, conference publications, and book chapters

Sun Microelectronics Engineering Excellence Award 1996.

Member of Tau Beta Pi and Eta Kappa Nu Engineering Honor Societies

Guest editor of *IEEE Design & Test of Computers* magazine for a special issue on microprocessors January-March 1997.**EDUCATION**

MS and PhD in Electrical Engineering, University of Illinois, Urbana, IL, 1986-1990

BS with High Honors Computer Engineering, Lehigh University, Bethlehem, PA, 1982-1986

PUBLICATIONS LIST

JOURNALS AND CONFERENCES

1. "Moving Manufacturing More Effectively Into Design," *DesignCon 2007*.
2. "The Impact of DFM in the Design Phase below 90 Nanometers," *DesignCon 2006*
3. "Making the (Yield) Difference: DFY/DFM," *Proceedings 24th VLSI Test Symposium*, 2006.
4. "Using yield-focused design methodologies to speed time-to-market," *Proceedings of the SPIE Design and Process Integration for Microelectronic Manufacturing III*, 2005.
5. "What Is Design for Yield, and How Do We Get There?" *DesignCon 2005*.
6. "Collaborating Effectively on the Rocky Road to DFM" *FSA Suppliers Expo & Conference 2005*
7. "Using Yield-Focused Design Methodologies to Speed Time-to-Market," *DesignCon 2005*.
8. "Design for manufacturing? Design for yield!!!," *Proceedings 5th International Symposium on Quality Electronic Design*, 2004.
9. "When IC yield misses the target, who is at fault?," *Proceedings 41st Design Automation Conference*, 2004
10. "SOC Testing - Throwing the Baby out with the Bath Water!" *IEEE BAST Workshop*, 2000.
11. "FXYP: A Foreign Exchange Yield Investing Index," *Proceedings of Forecasting Financial Markets and Computational Finance*, 2000.
12. "System-on-Chip Debug and Test," *IEEE BAST Workshop*, 1999
13. "Market Time Data™ Improving Technical Analysis and Technical Trading," *Proceedings of Forecasting Financial Markets*, 1998.
14. "Microprocessors Lead The Way In Complex Design," *IEEE Design & Test of Computers*, vol.14, no.1, Jan-Mar 1997
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16. "A fault diagnosis methodology for the UltraSPARC-I microprocessor," *Proceedings European Design and Test Conference*, 1997.
17. "Formal verification of the UltraSPARC family of Processors via ATPG Methods," *International Test Conference*, 1996.
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21. "A 64b microprocessor with multimedia support," *Digest of Technical Papers IEEE International Solid-State Circuits Conference*, 1995.
22. "UltraSPARC: The next generation superscalar 64-bit SPARC," *Digest of Papers Compcon '95. Technologies for the Information Superhighway*, 1995
23. "Practicing DFT: The Good, The Bad, and The Ugly" *IEEE BAST Workshop*, 1995
24. "Exploitation of Market Inefficiencies via Nonlinear Prediction," *Proceedings of Neural Networks in the Capital Markets*, 1994.
25. "BiCMOS logic testing," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Jun 1994
26. "Microprocessor Testing: Which technique is best?" *Proceedings 31st Design Automation Conference*, 1994.
27. "SPARCcenter 2000: Multiprocessing for the 90's," *Digest of Papers Compcon Spring '93*, 1993
28. "Economic and productivity considerations in ASIC test and design-for-test," *Digest of Papers Compcon Spring '92*, 1992
29. "ASIC testing upgraded," *IEEE Spectrum*, vol.29, no.5, May 1992
30. "The effect of multiple charge-discharge paths on testing of BiCMOS logic circuits," *Proceedings 3rd European Conference on Design Automation*, 1992.
31. "Test considerations for BiCMOS logic families," *Proceedings of the Custom Integrated Circuits Conference*, 1991
32. "Physical design of testable VLSI: Techniques and experiments," *IEEE Journal of Solid-State Circuits*, Apr 1990
33. "BiCMOS fault models: Is stuck-at adequate?," *Proceedings International Conference on Computer Design: VLSI in Computers and Processors*, 1990.
34. "Just-in-time methods for semiconductor manufacturing," *Proceedings Advanced Semiconductor Manufacturing Conference and Workshop*, 1990.
35. "Physical design of testable VLSI: Techniques and experiments," *Proceedings of the IEEE Custom Integrated Circuits Conference*, 1989.

36. "The economics of scan design," *Proceedings International Test Conference*, 1989.

BOOK CHAPTERS

1. *Market Time and Short-Term Forecasting of Foreign Exchange Rates*, in **Decision Technologies for Financial Engineering**, A. Weigend, Y. Abu-Mostafa, and P. Refenes eds., World Scientific, Singapore, 1997.
 2. *Machine Learning for Foreign Exchange Trading*, in **Neural Networks in the Capital Markets**, P. Refenes ed., John Wiley & Sons, Chichester, UK, 1995.
 3. *BiCMOS Testing*, in **BiCMOS Technology and Applications 2nd Edition**, A.R. Alvarez ed., Kluwer Academic Publishers, Boston, MA, 1993.
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PATENT LIST

1. US5341382 "Method and apparatus for improving fault coverage of system logic of an integrated circuit with embedded memory arrays", 1994
2. US5379303 "Maximizing improvement to fault coverage of system logic of an integrated circuit with embedded memory arrays", 1995
3. US5513186 "Method and apparatus for interconnect testing without speed degradation", 1996
4. US5528165 "Logic signal validity verification apparatus", 1996
5. US5570376 "Method and apparatus for identifying faults within a system", 1996
6. US5774474 "Pipelined scan enable for fast scan testing", 1998
7. US5787012 "Integrated circuit with identification signal writing circuitry distributed on multiple metal layers", 1998
8. US5850150 "Final stage clock buffer in a clock distribution network", 1998.
9. US5864564 "Control circuit for deterministic stopping of an integrated circuit internal clock", 1999
10. US5870408 "Method and apparatus for on die testing", 1999
11. US5872796 "Method for interfacing boundary-scan circuitry with linearized impedance control type output drivers", 1999
12. US5892778 "Boundary-scan circuit for use with linearized impedance control type output drivers", 1999
13. US5898702 "Mutual exclusivity circuit for use in test pattern application scan architecture circuits", 1999
14. US5900757 "Clock stopping schemes for data buffer", 1999
15. US6081913 "Method for ensuring mutual exclusivity of selected signals during application of test patterns", 2000
16. US8549339 "Processor core communication in multi-core processor", 2013.

Addendum to CV for Marc E Levitt, Ph.D.

The following is a list of consulting relationships not disclosed in my public CV.

Active Consulting Assignments – All Areas

Robins Kaplan / DivX

- Dates: September 2024 – present
- Area/activities: Technical expert supporting litigation in video streaming technologies – device, server, DRM, encode, & decode.
- Case: v. Amazon 3:22-cv-00687 Eastern District of Virginia
- Testimony: None.

Robins Kaplan / DivX

- Dates: September 2024 – present
- Area/activities: Technical expert supporting litigation in video streaming technologies – device, server, DRM, encode, & decode.
- Cases: v. Netflix 2:19-cv-1602 Central District California
- Testimony: None

Mintz Levin PC / Onesta

- Dates: July 2024 – present
- Area/activities: Technical expert in computer architecture, memory controllers, GPU, power management, SoC, and AI hardware.

Troutman Pepper / VideoLabs

- Dates: April 2024 – present
- Area/activities: Non-testifying technical expert supporting litigation in power management technologies.
- Cases:
 - v. ASUSTeK Computer, Inc. 6:22-cv-00720 Western District of Texas
 - v. HP Inc. 6:23-cv-00641 Western District of Texas
 - v. HP Inc. 6:22-cv-01086 Western District of Texas

Robins Kaplan LLP / iCashe

- Dates: December 2022 – present
- Area/activities: Technical expert regarding NFC technologies.
- Cases: v. Samsung 2:24-cv-00429 Eastern District of Texas
- Testimony: None

Keker, Van Nest, & Peters / Real Intent

- Dates: June 2020 - present

- Area/activities: Technical expert supporting copyright and patent infringement analysis in the EDA software space.
- Case: Synopsys v Real Intent 5:20-cv-02819-EJD N.D. Cal
- Testimony: Expert reports on invalidity, non-infringement, and copyright filed. Deposed on all reports. Declaration in support of opposition to permanent injunction.
- Favorable jury verdict to client.

Robins Kaplan LLP / Corel Software LLC

- Dates: June 2015 – present (stayed 2019 - mid 2023)
- Area/activities: Technical expert supporting litigation in office automation and productivity software.
- Case: v Microsoft Corp. 2:15-cv-00528-JNP Utah Central
- Testimony: Declaration on source code operation, deposed on source code operation. Expert report filed on source code operation. Deposed on source code operation expert report.

Closed Consulting Assignments – Litigation

Winstead / MOSAID Technologies

- Dates: June 2023 – November 2024
- Area/activities: Technical expert supporting litigation in power management technologies.
- Cases: v. MediaTek, Inc. et al. No. 2:23-cv-00129-JRG Eastern District of Texas
- Testimony: Declaration for claim construction and deposition. Infringement report submitted.
- Case settled

TensegrityLaw Group / DivX

- Dates: June 2022 – September 2024
- Area/activities: Technical expert supporting litigation in video streaming technologies – device, server, DRM, encode, & decode.
- Cases:
 - v. Amazon (3:22-cv-00687) Eastern District of Virginia
 - International Trade Commission (337-TA-1343)
- Testimony: Declarations for ITC petition and Markman. Expert reports on infringement and validity, testified at ITC hearing.

TensegrityLaw Group / DivX

- Dates: January 2022 – September 2024
- Area/activities: Technical expert supporting litigation in video streaming technologies – device, server, DRM, encode, & decode.
- Cases: v. Netflix 2:19-cv-1602 Central District California
- Testimony: None

BCLG / Universal Connectivity Technologies

- Dates: January 2024 – September 2024
- Area/activities: Technical expert supporting litigation in interconnect technologies.
- Cases:

- v. Dell Inc. 1:23-CV-01506-RP Western District of Texas
- v. HP Inc 1:23-CV-01177-RP Western District of Texas
- v. Lenovo Group Ltd. 2:23-cv-00449-JRG Eastern District of Texas
- Testimony: None

Mintz Levin PC / Daedalus

- Dates: January 2022 – January 2024
- Area/activities: SoC Power management technology
- Cases: International Trade Commission (337-TA-1355)
- Testimony: Rebuttal report on validity, deposed on expert report, testified at ITC hearing.

Mintz Levin PC / AMD

- Dates: August 2021 – July 2023.
- Area/activities: Technical expert supporting litigation involving SoCs and graphics capabilities.
- Case: Certain Graphics Systems, Components Thereof, and Digital Televisions Containing the Same (Inv. No. 337-TA-1318)
- Testimony: Initial expert report on domestic industry and infringement, rebuttal expert report, deposed on expert reports, testified at ITC hearing.

Nixon Peabody / Network Systems Technologies

- Dates: July 2022 – June 2023
- Area/activities: SoC interconnect technology
- Cases:
 - v Lenovo, Samsung Electronics Co et. al. (2:22-cv-00481) ED Texas
 - v Texas Instruments et al (2:22-cv-00482) ED Texas
 - v Arteris, Qualcomm (1:22-cv-01331) WD Texas
- Testimony: None

Carter Arnett / Bench Walk Lighting

- Dates: October 2019 – June 2023
- Area/activities: LED design and packaging.
- Case: v. Everlight Electronics Co Ltd (1:20-cv-00049) D. Del.
- Testimony: Claim Construction Declaration

Kilpatrick Townsend / DivX

- Dates: October 2021 – December 2022
- Area/activities: Technical expert supporting arbitration involving video playback devices that are DivX capable.
- Case: DivX LLC v Konka Group Co, Ltd, Arbitration before JAMS
- Testimony: Initial expert report

Robins Kaplan LLP / ACQIS

- Dates: September 2020 – September 2022
- Area/activities: Technical expert supporting litigation involving high performance serial interfaces including PCI Express and USB.
- Cases:

- v. Samsung Electronics Co., Ltd., et al. (2:20-cv-00295) Eastern District of Texas
- v. Acer Inc. (2:21-cv-275) Eastern District of Texas
- Testimony
 - Samsung: Numerous Declarations, Expert Report Infringement, Rebuttal Expert Report Validity, Deposed on both reports.
 - Acer: Expert Report Infringement, Rebuttal Expert Report Validity, Deposed on both reports.

DiMuro Ginsberg / Heavy Duty Lighting

- Dates: April 2021 – August 2022
- Area/activities: LED design and packaging.
- Case: v. Acuity Brands Lighting (1:20-cv-03648-SCJ) Northern District of Georgia
- Testimony: Claim Construction Declaration, Deposed on Declaration

Mintz Levin PC / DivX

- Dates: December 2021 – April 2022
- Area/activities: Technical expert supporting litigation involving smart TV devices.
- Case: Certain Video Processing Devices, Components Thereof, and Digital Smart Televisions Containing the Same II (Inv. No. 337-TA-1297)

Mintz Levin PC / DivX

- Dates: June 2019 – April 2022
- Area/activities: Technical expert supporting litigation involving smart TV devices.
- Case: Certain Video Processing Devices, Components Thereof, and Digital Smart Televisions Containing the Same (Inv. No. 337-TA-1222)
- Testimony: Filed Expert Report, Deposed on Expert Report, ITC Hearing.

Robins Kaplan LLP / DivX

- Dates: June 2018 – December 2021
- Area/activities: Technical expert supporting litigation in video streaming technologies – device, server, DRM, encode, & decode.
- Cases: DivX v.
 - Hulu (2:19-cv-1606) Central District California
 - Netflix (2:19-cv-1602) Central District California

Hill, Kertscher, & Wharton LLP / Light Speed Microelectronics LLC

- Dates: January 2020 – October 2021
- Area/activities: Technical expert supporting litigation in hardware based fast pattern matching technologies.
- Cases: Light Speed Microelectronics v. NXP Semiconductors (6:21-cv-00066) Western District Texas

Jeffrey W. Salmon Law LLC / Sockeye Licensing TX LLC

- Dates: July 2021 – August 2021
- Area/activities: Technical expert on the operation of Goggle Cast technology based on publicly available documents.

- Cases: v. Skyworth Group Limited (6:21-cv-00220) Western District Texas

Robins Kaplan LLP / ACQIS

- Dates: June 2021 – August 2021
- Area/activities: Technical expert supporting POPR with respect to the following IPRs
 - IPR2021-00666 US\$9,529,768
 - IPR2021-00667 US\$8,977,797
 - IPR2021-00668 US\$9,703,750
 - IPR2021-00669 US\$44,654
 - IPR2021-00670 US\$45,140
- Testimony: Declaration for the POPR for each IPR.

Mintz Levin PC / Philips

- Dates: August 2020 – March 2021
- Area/activities: Technical expert supporting litigation in video content protection and authentication.
- Cases: Certain Digital Video-Capable Devices and Components Thereof (Inv. No. 337-TA-1224)

DiNovo Price / Infinity Computer Products

- Dates: August 2018 – June 2021
- Area/activities: Technical expert supporting litigation in the multifunction peripheral product space.
- Case: Infinity Computer Products v
 - Toshiba American Business Solutions (2:12-cv-6796-NIQA, lead case)
 - Oki Data (18-463 (LPS))
 - Lexmark International (5:18-cv-198-JMH-REW)
- Venue: Eastern District Pennsylvania, Delaware, New York, Kentucky
- Testimony: Declaration in support of claim construction brief, deposed numerous times.

Mintz Levin PC / Netlist

- Dates: December 2016 – February 2021
- Area/activities: Technical expert supporting litigation in the semiconductor and memory systems space. Patents involve Registered and Load Reduced DIMM architecture and testing.
- Cases:
 - Certain Memory Modules and Components Thereof (Inv. No. 337-TA-1089)
 - Certain Memory Modules and Components Thereof, and Products Containing Same (Inv. No. 337-TA-1023)
 - Netlist Inc v. SK Hynix Inc. et al (8:17-cv-01030) California Central District
- Testimony: Expert report filed, deposed for ITC case, witness statement, & testified at ITC hearing.

Lee Sullivan Shea & Smith LLP/ Sonos

- Dates: March 2020 – December 2020
- Area/activities: Technical expert supporting litigation audio players and music streaming.
- Case: CERTAIN AUDIO PLAYERS AND CONTROLLERS, COMPONENTS THEREOF, AND PRODUCTS CONTAINING THE SAME (Inv. No. 337-TA-1191)
- Testimony: None – was an alternate / backup expert due to Covid 19 concerns.

Matrox Graphics Inc.

- Dates: January 2017 – September 2019
- Area/activities: Technical expert supporting litigation in the EEPROM semiconductor memory space. Involves determining if part was properly designed and manufactured to specification and industry standards. Additionally, did STMicro withhold information regarding the quality level of the part before withdrawing the design from the market.
- Cases: Matrox Graphics Inc. c. STMicroelectronics Inc (500-05-070786-023 and 500-17-015647-038)
- Venue: Quebec Superior Court
- Testimony: First expert report filed.

Closed Consulting Assignments – Non-Litigation

Robins Kaplan LLP

- Dates: November 2021 – present
- Area/activities: Technical expert regarding VLIW compilers.
- Cases: None

Robins Kaplan LLP / DivX

- Dates: February 2022 – June 2022
- Area/activities: Technical expert in video streaming technologies – device, server, DRM, encode, & decode.

Mintz Levin PC / IV

- Dates: February 2022 – April 2022
- Area/activities: Patent consulting.

Mintz Levin PC / Philips

- Dates: August 2021 – July 2022
- Area/activities: Patent consulting.

Mintz Levin PC / Global Foundries

- Dates: February 2020 – September 2020
- Area/activities: Technical expert supporting patent consulting.

Mintz Levin PC / Philips

- Dates: November 2019
- Area/activities: Technical expert supporting patent consulting.

Robins Kaplan LLP / AMD

- Dates: September 2019 – October 2019
- Area/activities: Technical expert in dynamic binary translation and compilation techniques for x86 and ARM ISA.