

ROBERT P. COLWELL

3594 NW BRONSON CREST LOOP
PORTLAND, OR 97229
503-629-9638
BOB.COLWELL@GMAIL.COM

PROFESSIONAL EXPERIENCE

- **Director**, Microsystems Technology Office, DARPA Arlington VA 2012-2014
- **Deputy Director**, Microsystems Technology Office, DARPA 2011-2012
Led office of 17 program managers, budget ~\$600M/yr, funding research on computer systems, nanophotonics, bioengineering, radar, comms, lasers, IR imaging, and much more.
- **Consultant**, Portland, OR 2001-2011, 2014 - present
General computer HW/SW consulting to industry and academia (Safeware, the University of Pittsburgh, Intel, Qualcomm, venture capital companies, many startups, expert witness engagements, Lawrence Berkeley National Lab, US DoD)
- Named an **Intel Fellow** (27 Fellows in Intel's employee population of ~80,000) in 1997; winner of 2005 **Eckert-Mauchly Award**, highest award in field of computer architecture, for “outstanding achievements in the design and implementation of industry-changing microarchitectures, and for significant contributions to the RISC/CISC architecture debate”; elected to **IEEE Fellow** and **the National Academy of Engineering** in 2006 (the highest recognition in field of engineering) for “contributions to turning novel computer architecture concepts into viable, cutting-edge commercial processors.” Inducted into the **American Academy of Arts and Sciences**, 2012. Winner of **IEEE Bob Rau Award**, 2015. Three alumni awards from Pitt and CMU.
- **Chief IA-32 Architect**, Intel Corporation, Hillsboro OR, 1992-2001
Lead IA32 architect, responsible for all of Intel's x86 Pentium CPU architecture efforts (direct management included 40 – 110 people): Pentium Pro, Pentium II, III, 4; Initiated and led Intel's Pentium 4 CPU development
- **Senior CPU Architect**, Intel Corporation, Hillsboro OR, 1990-1992
One of three senior architects responsible for conceiving Intel's P6 microarchitecture, the core of the company's Pentium II, Pentium III, Celeron, Xeon, and Centrino families
- **Hardware Architect**, Multiflow Computer, New Haven, CT 1985-1990
One of seven hardware engineers who created the world's first VLIW (very long instruction word) scientific supercomputer under direction of Josh Fisher
- **Hardware Engineer** (part-time) Perq Systems, Pittsburgh PA, 1980 - 1984
Hardware design engineer working on graphics display hardware for first generation bit-slice-based engineering workstations
- **Member of Technical Staff**, Bell Telephone Laboratories, Holmdel, NJ, 1977-1980
Hardware design engineer working on 8 and 32-bit microprocessors

EDUCATION

- **PhD in Computer Engineering**, Carnegie-Mellon University, 1985
- **MSEE** in Computer Engineering, Carnegie-Mellon University, 1978

- **BSEE** in Electrical Engineering, University of Pittsburgh, 1977

PUBLICATIONS

Wrote foreword to “Weaving High Performance Multi-Core Processor Fabric: Essential Insights to the Intel Quickpath Architecture”, Maddox, Singh, Safranek, Intel Press 2009

National Research Council, The Future of Computing Performance: Game Over or Next Level?, Washington, D.C.: The National Academies Press, 2010.

VLIW: The Unlikeliest Architecture, IEEE Solid State Circuits News, 2009

Wrote intro to DE Shaw’s article on the Anton molecular folding engine in CACM, July 2008

Contributed parameterized chapter 2 problem sets to Hennessy & Patterson’s “Computer Architecture: A Quantitative Approach, 4th Edition” 2006

The Pentium Chronicles, IEEE/Wiley, December 2005

IEEE Computer Magazine, 48 columns for “At Random” column 2002-2005

Wrote foreword to Josh Fisher’s book “Embedded Computing: A VLIW Approach to Architecture, Compilers and Tools”, Morgan-Kaufman 2005

We May Need A New Box, IEEE Computer March 2004

Superscalar Processor Design, P6 chapter, Shen & Lipasti, McGraw-Hill 2003

Embedded Everywhere, National Academy of Science, October 2001

Intel's College Hiring Methods and Recent Results, Microelectronics Systems Education Conference, Robert Colwell, Gary Brown, Frank See, July 1999

Microprocessor, Wiley & Son Technical Encyclopedia, 1999

Challenges and Trends in Processor Design, roundtable discussion in IEEE Computer, January 1998

A 0.6um BiCMOS Processor with Dynamic Execution, Robert P. Colwell, Randy L. Steck, 1995 IEEE International Solid State Circuits Conference, pp. 176-177 (won best paper award)

Latent Design Faults in the Development of Multiflow's TRACE/200, 22nd Annual International Symposium on Fault-Tolerant Computing, Boston MA, July 1992

Architecture and Implementation of a VLIW Supercomputer, Robert P. Colwell, W. Eric Hall, Chandra S. Joshi, David B. Papworth, Paul K. Rodman, James E. Tornes, Proceedings of Supercomputing '90, New York, November 1990

A VLIW Architecture for a Trace Scheduling Compiler, Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman, IEEE Trans. on Comp., V. 37, N. 8, Aug.1988

A VLIW Architecture for a Trace Scheduling Compiler, Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman, Proceedings of the 2nd Int'l Conf. on Architectural

Support for Programming Languages and Operating Systems, Oct. 1987, Palo Alto CA (2021 Winner of Influential Paper Award from ASPLOS Conference)

Fast Object-Oriented Procedure Calls: Lessons from the Intel 432, Edward F. Gehringer, Robert P. Colwell, ISCA 13, June 1986, pp. 92-101

The Performance Effects of Architectural Complexity in the Intel 432, Robert P. Colwell, Edward F. Gehringer, E. Douglas Jensen, ACM Transactions on Computer Systems, Aug. 1988, V. 6, N. 3

A Display Architecture for Driving Two Different Bitmapped Displays from One Frame Buffer, Robert P. Colwell, 1st Int'l Conference on Computer Workstations, San Jose CA, November 1985

Computers, Complexity, and Controversy, R.P. Colwell, C.Y. Hitchcock III, E.D. Jensen, H.M. Brinkley Sprunt, C.P. Kollar, IEEE Computer, September, 1985, pp. 8-19

The Performance Effects of Function Migration and Architectural Complexity in Object-Oriented Systems, Robert P. Colwell, PhD thesis, Carnegie-Mellon University, Pittsburgh, PA, August 1985

Peering Through The RISC/CISC Fog: An Outline Of Research, Computer Architecture News, Vol. 11, No. 1, March 1983 pp. 44-50

A Perspective on the Processor Complexity Controversy, Proceedings of the International Conference on Computer Design, 1983, pp. 613-616

The Origin of Intel's Micro-ops, invited paper, IEEE Micro 2021

LECTURES AND INVITED TALKS

P6: Myths and Pipelined Realities, MP Forum '95 in Santa Clara

Evolution of Slot 1 and Slot 2, MP Forum '97 in Santa Clara

Micro '30 keynote speaker, 1997, San Jose

HPCA2 keynote speaker, Santa Clara, 1996

Talks on computing futures at CMU and Oregon Graduate Institute, Intel's Design Test and Technology Conference 1997-1998 (best presentation DTTC), invited keynote DTTC '04

LCPC (Languages and Compilers for Parallel Computing) keynote speaker, San Jose 1996

Intel Research Forum invited speaker, Hillsboro '96, Santa Clara '99

Intel Distinguished Lecture Series talks on the Pentium Pro at BYU, MIT, UCB, Stanford, CMU, Illinois, Wisconsin, Univ of Washington, OGI, UCLA

Distinguished Lectures: UC Davis May 2003; Carnegie-Mellon Univ Nov. 2003; USC April 2004

Microprocessor Report dinner speaker on Pentium Pro, March '95

Neural Networks for Computing Conference, Snowbird Utah, April 1994

IEEE Winter VLSI Workshop 1995

DARPA Winter PI conference, Pasadena CA, January 1994

International Applications Conference, San Diego CA, June 1994

Nature's Paradigm and the Challenge of Validation, Intel Validation Summit 1998, invited talk

Validation Lessons from Elsewhere, Intel Validation Summit 1999, invited talk

ISCA keynote, Anchorage Alaska, June 2002

ECE380 Seminar invited talk, Stanford Univ. February 2004

Invited speaker, Technology Management Lecture Series, PSU May 2004

Invited speaker, CSE Division Wide Seminar, University of Michigan, January 2005

Invited keynote speaker, IEEE Int'l Symp. on Async Circuits and Systems, NYC, March 2005

Invited speaker, IEEE Management Series, Portland OR, April 2005

Eckert-Mauchly Award acceptance speech, ISCA, Madison Wisconsin, June 2005

Invited keynote, International Multiconference on Computer Science and Computer Engineering, Las Vegas NV, June 2005

Invited speaker: Google, Sun Labs, Portland State University 2005

Invited speaker: Cadence, Carnegie-Mellon Univ. CS, Univ. of Rochester, Walla Walla College 2006

Invited keynote, PICMET, Portland Oregon, August 2005

Distinguished lecture, Univ. of Utah, March 2006

Invited speaker: Computer Science Symposium, St. Petersburg, Russia 2006

Invited speaker, IEEE-CS 60th anniversary meeting, Santiago Chile, San Diego CA 2006

Invited speaker, National Academies "Distinguished Voices" lecture series, April 2007, Irvine CA

Invited speaker, FCRC "Future Of Computer Architecture 2007", June, San Diego CA

Invited keynote speaker, ASAP 2007 conference, July, Montreal Canada 2007

Invited speaker, UC Irvine, "How To Be a Successful Engineer", Feb. 2008

Invited speaker, US Naval Workshop on Ship Design, Williamsburg, VA May 2008

Invited speaker, DARPA DSRC summer session, Santa Cruz CA July 2008

Distinguished Hopeman Lecture, Grove City College, April 2009

Many invited talks as DARPA MTO spokesperson on the end of Moore's Law 2011-2014

Invited speaker, Microsoft Research 20th Anniversary Symposium, Sept. 2011

Invited speaker, Computer Science and Telecommunications Board (CSTB), Sept. 2011

Invited speaker, Secretary of Defense Corporate Fellows, July 2012, 2013

Invited speaker after-dinner talk, Salishan Conference on High Performance Computing, April 2013

Invited speaker, Industrial Physics Forum, Baltimore MD, March 2013

Invited speaker, Computing Community Consortium (CCC), Pgh PA, March 2013

Invited speaker, National Defense University College, Wash. DC, May 2013

Invited speaker, Design Automation Conference, Austin TX, June 2013

Invited keynote, Hot Chips Conference, Stanford, August 2013

Invited speaker, Gov't Forum on Moore's Law, Wash. DC, November 2013

Invited talks at UT Austin, seminar & computer architecture lecture, November 2013

Invited speaker, Rebooting Computing, Wash. DC, December 2013

Invited speaker, Dartmouth College, January 2014

Invited speaker, MIT Annual Research Conference (MARC), January 2014

Invited speaker, Virginia Tech Univ., February 2014

Invited speaker, Univ. of Rochester, March 2014

Invited speaker, IEEE Technology Time Machine conf, October 2014

Invited speaker, DARPA HAPTIX kickoff meeting, Arlington VA, Nov. 2014

Invited speaker, CSTB Continuing Innovation in IT workshop, Washington DC, Mar. 2015

Invited keynote, Stanford SystemX "Headlights" Workshop, April 2015

Invited keynote, Berkeley Energy Efficient Electronics Systems Symposium, Oct. 2015

Invited speaker, University of Washington, Nov. 2015

Invited speaker, Arizona State University, Feb. 2016

Invited keynote, DoE Extreme Heterogeneity workshop, January 2018

Invited keynote, DARPA NICE workshop, Feb. 2018 (Neuro-Inspired Computing Elements), Oregon

Invited keynote, ModSim workshop, Seattle, August 2018, 2023

ECE Commencement speaker, Portland State University, June 2019

Member, National Academy of Engineering review panel for NIST (National Institute of Standards and Technology) Nanotechnology Division, June 2021

Invited keynote, ModSim workshop, Seattle, August 2023

Invited talk, University of Pittsburgh ECE dept. Oct. 2024

Invited talk, Carnegie-Mellon University ECE dept. Oct. 2024

PANEL SESSIONS

DAC '91 panel session panelist; DAC '92 CAD tools workshop instructor

ICCD '91 moderator/organizer of panel session, San Jose CA

ICCAD-94, panel session panelist, November 1994, San Jose CA

Micro 26 '93, moderator/organizer of panel session, Portland OR

ISCA workshop talk, Santa Margherita Ligure, Italy 1995, panelist Phila. PA 1996

PAID 97 Workshop talk on "accidental performance decisions" with Dave Papworth

FPGA panel session panelist, November 1996, Monterey CA

ASPLOS-VII panel session panelist, October 1998, San Jose CA

IEEE Workshop on Low-Power design panel session, San Diego, CA 1999

Four panel sessions in 2000 at various conferences

Computer Research Assoc. "Grand Challenges" conference, Santa Cruz CA, Dec. 2005

DARPA MTO Exposition, Arlington VA July 2014

NSF Future Computing evaluation panel April 2018

ModSim 2018 panelist, Seattle WA

CONFERENCE COMMITTEES

ICCD 1990, 1991, 1992, 1993, 1994, 1995

IEEE Micro 24, 26, 27, 30, 31, 32, general co-chair 37, 39, 40, 41

ISCA 1999, 2000, 2008, 2009, 2010, 2015

Supercomputing 2013, 2014

TECHNICAL EXPERT LEGAL CASES WORKED

Intergraph v. Intel, 1998-2000, deposed twice

Techsearch v. Intel, 1999, deposed once

LGE v. Elonex, Morgan Lewis, ChathamLaw, Tom Nelson, 2002

Technical advice on PCI, memory system design

Intergraph v. Dell, Jones Day, Mark Ziegelbein, 2003-2004

Deposed, technical advice on buses, CPUs

Intergraph v. HP, Irell-Manella, Flavio Rose, 2004

Barbara Sales v. Intel, Brown Bain, Dan Bagatell, 2004

Fujitsu v. LG Electronics, Morrison Foerster, Alex Chartove, 2004

Opti v. NVIDIA, Cooley Godward, Tim Teter, 2004-2006

Expert reports for claims construction, invalidity/non-infringement

MEC/Acacia v. NVIDIA, Cooley Godward, Tim Teter, 2005

Kyocera v. Nokia, Jones Day, Keith Davis, 2005

Expert report for claim construction

HP v. Gateway, DLA Piper Rudnick Gray Cary, Alan Limbach, 2005

Expert report for claim construction, infringement contentions

Broadcom v. Qualcomm, Howrey, Vinay Joshi; DLA Piper, Dave Wiggins 2006

Expert reports for claim construction and non-infringement/invalidity, deposed twice, testified at trial, Orange County, Judge J. Selna

UniRAM v. Monolithic System Tech., Townsend & Townsend, George Schwab, 2006

EVE-USA v. Mentor Graphics, Cooley Godward, Brian Mitchell, Bill Galiani, 2006

Intergraph v. Toshiba, Foley Lardner, Stephen Lobbin, John Feldhaus, 2006-2007

Declaration re: Markman brief, expert report, deposed

MicroUnity v. Sony, Finnegan Henderson, Lei Mei, 2006-2007

Tech Property Limited v. NEC, Toshiba, Matsushita, Baker Botts, Michael Hawes, 2006-2007

Samsung v. Wistron, DLA Piper, Greg Lundell, Sal Lim, 2008 – settled

Expert reports for claim construction, infringement, rebuttals, deposed

Freescale v. ProMOS, Jones Day, Drexel Feeling, 2008 – settled

Expert report for infringement

ProMOS v. Freescale, Jones Day, Brent Ray, 2008 – settled

Expert report on non-infringement

Opti v. Nintendo, Cooley Godward, Tim Teter, 2008 – settled

SuperSpeed v. IBM, Jones Day, Mark Ziegelbein, 2008 – settled

Expert reports on non-infringement and invalidity, deposed twice

Saxon v. Nintendo, Cooley Godward, Matt Brigham, 2008

MOSAid v. NVIDIA, NVIDIA, Richard Calderwood, 2008

Opti v. Apple, Cooley Godward, Tim Teter, 2009

Expert reports on non-infringement and invalidity, deposed twice, testified at trial, Marshall Texas, Judge Everingham

Network-1 v. Cisco, Wilmer Hale, Joe Haag, 2009 – settled at trial July 2010

Claim construction declaration, expert report, deposed twice, testified at trial July 2010, Tyler, Texas; Judge L. Davis

Also represented Extreme Networks, Foundry, 3Com, Enterasys, and Adtran (all settled)

Samsung/LGE v. Kodak, Wilmer Hale, Joe Haag, 2009 expert report – settled

WARF v. Intel, Wilmer Hale, Jonathan Andron, James Quarles, 2009 – deposed; settled

ACQIS v. Sun/Oracle, DLA Piper, Alan Limbach, 2009

Expert report on non-infringement, deposed, settled January 2011

Xpoint v. Qualcomm, McDermott Will & Emery, Dave Dolkas – settled

Nokia v. Apple, Wilmer Hale, Joe Haag – settled

Alliacense v. SnapOn, McDonnell Boehnen Hulbert Berghoff, Brad Hulbert

Withdrew from case due to full time employment at DARPA 2011

Toshiba v. Wistron, Knobbe Martens Olson Bear, Reza Mirzaie – settled

Expert report on infringement, invalidity rebuttal, deposed

Panasonic v. Freescale, Jones Day, David Witcoff – settled

WARF v. Apple, Wilmer Hale, Bill Lee, Lauren Fletcher, Andrew Danford, 2014-2015

Invalidity expert report, damages expert report, deposed, testified at trial (7 hours), Madison WI, Judge William Conley

AVM v. Intel, Wilmer Hale, Lauren Fletcher, 2015-2017

Damages expert report, deposed, trial Wilmington DE May 2017

AST v. Texas Instruments, Covington Burling, Anupam Sharma, Hyun Byun, 2016
Invalidity expert report, case settled

AST v. Renesas, Foley Lardner, John Feldhaus, Pavan Agarwal, 2016
Invalidity expert report, case settled

PUMA v. Apple, Haynes Boone, David O'Brien, 2016
Invalidity expert reports, deposed twice, case settled

Futurelink v. Intel, Kirkland Ellis, Eric Cheng, 2014-2017
Invalidity, non-infringement expert reports, deposed 3 times, case settled 8/17/2023

Broadcom v. Renesas, Morrison Foerster, Fahd Patel, Daniel Muino, 2018-2020
Invalidity, non-infringement expert reports, deposed twice, testified at ITC hearing

Semcon v. Amazon, Sidley Austin, Tung Nguyen, Cal Butcher, 2019
Invalidity expert report, deposed 8/15/19, case settled

VLSI Tech. v. Intel, Wilmer Hale, Christine Duh, George Manley, Jordan Hirsch, 2017-2021
Damages expert report, Rebuttal report, deposed twice

CCO (Computer Circuit Operations) v Marvell, Sheppard Mullin, Wendy Cheung, 2020
Declaration filed, case settled August 2020

Pact v. Intel, Kirkland Ellis, Kevin Bendix, 2019 - 2022
Invalidity report

ACQIS v. Samsung, DLA Piper, Gianni Minutoli, 2021
Claim Construction declaration June 2021, expert report on noninfringing alternatives Sept. 2021, deposed twice, case settled Dec. 2021

ACQIS v. Inventec, BlankRome, Greg Hermann, 2022
My role: damages & apportionment, case settled May 2022

Apple Inc. v. Future Link Systems, Inter Partes Review, EriseIP, Adam Seitz
IPR declaration filed, case settled April 2022

Apple Inc. v. Future Link Systems, Fish Richardson, John Brinkmann
Work on claim construction, case settled April 2022

ACQIS v. Microsoft, DLA Piper, Gianni Minutoli, 2022

Claim Construction declaration May 2023, case settled June 2023

Rex Computing v. Cerebras, Quinn Emmanuel, Ron Hagiz, 2021 - present

3 Reports filed, deposed, testified at hearing Wilmington DE judge Noreika

Network System Technology v. Texas Instruments, Covington Burling, Hyun Byun, 2023 - present

3 Reports filed, deposed, case settled June 2024

Arm v. Qualcomm, Morrison Foerster, Daniel Muino, 2023 - 2024

4 Reports filed, deposed, testified at trial, Wilmington DE judge Noreika

Have served as confidential technical consultant on many other patent litigation matters involved CPUs, chipsets, buses, memories, electronics, design tools, video and other technologies.

OTHER

Selected as member of ISAT (Information Systems Advanced Technology) panel for DARPA, 2006-2009, co-chaired Machine Learning on Multicore 2009 with Carlos Guestrin and Greg Morrisett

Panelist, Dept of Defense Summer Study on Future Technology, summer 1999, Washington DC

CSTB Panelist, National Academy of Science, Networks of Embedded Processors, 1999-2000, Wash. DC

CSTB Panelist, National Academy of Science, Sustaining Growth in Computing Performance, 2006-2011, Wash. DC

IEEE Computer Magazine editor for High Performance Computing, 1995 to 1999

IEEE Computer Magazine editorial board member, Perspectives editor, 1999-2016

Reviewer of dozens of technical books for Morgan Kaufmann, Mindshare, Addison-Wesley

Committee member on NSF funding for computer arch futures, Philadelphia, 1996

Intel Innovator's Day finalist '93, judge '95, judge '97

IEEE Senior Reviewer status in 1994, 1995, 1996 (conference papers, books, magazine articles)

Intel P6 public spokesman at dozens of radio, TV, and magazine interviews

Intel Divisional Award 1993 for DFA performance modeling tool

Intel Achievement Award 1996 for Pentium Pro Microarchitecture

CMU Alumni Merit Award, 1996, for technical leadership on Pentium Pro development

ACM Eckert-Mauchly award committee member, 1998-2001

Univ. of Pgh. Distinguished Alumni Award, 2000, for technical leadership on Intel's microprocessors

Univ. of Pgh. University Achievement Award, 2001, for accomplishments in field of Computing

Carnegie-Mellon Distinguished Alumni Fellows Award 2001

PICMET "Medal of Excellence" 2005

Judge for CSIDC (Computer Society Int'l Design Competition) 2005, 2006

Instructor ECE570, Adv. Computer Arch., Oregon State Univ., winter semesters 2000, 2003

Inventor or co-inventor on 40 patents