An Experimental 4-Mbit CMOS EEPROM with a NAND-Structured Cell

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Abstract —A 5-V-only high-density (512K×8 bit) electrically erasable and programmable read-only memory (EEPROM) has been designed and fabricated by using a NAND-structured cell with 1.0-μm design rules. The average cell area per bit is 12.9 μm². Block erasing, successive programming, and random reading are achieved using a newly developed NAND-cell control circuit. Typical erasing time is 1.0 ms and page-programming time is 4.0 ms, equivalent to 1.0 μs/bit. A dynamic sensing system is introduced to sense the small cell current. Typical read access time is 1.6 μs. The die size is 10.7×15.3 mm².

I. Introduction

The MEMORY capacity of conventional (FLOTOX) EEPROM has been steadily increasing. Several 256-kbit EEPROM's are being rushed into development [1]–[4] and a manufacturable 1-Mbit EEPROM has been reported recently [5]. Full function EEPROM's have many advantages including byte erase, byte program, and random access read capabilities. However, it is inherently difficult to achieve higher levels of integration because the memory cell of these devices consists of two transistors per bit: a memory transistor and a select transistor. This results in a very large cell size. Thus, conventional EEPROM's are expensive.

In order to obtain high-density and low-cost EEPROM's, a flash-EEPROM cell has been proposed [6]. Flash EEPROM's are different from EEPROM's due to the fact that the entire flash memory array can be erased simultaneously. This type of flash EEPROM has been extensively studied and developed recently [6]–[11]. By eliminating the select transistor, a smaller cell size than that of conventional EEPROM's has been achieved.

The conventional and flash EEPROM's are essentially a NOR-structured cell, in which memory cells are connected to a bit line in parallel. Therefore each memory cell has one-half contact hole and one-half source line. The next way to obtain a smaller cell is to reduce the area occupied by both the contact hole and the source line. The key to obtaining a smaller EEPROM cell is to simplify the structure. Therefore, a new cell concept has been proposed, called a NAND-structured cell, that dramatically reduces the number of cell components as well as the cell size [12]. It is well known that mask ROM utilizes a NAND-type cell and obtains a high level of integration up to 16 Mbits [17]. However, no one has ever tried to design the EEPROM by using a NAND-structured cell because the operating method has yet to be established. We have now established the operating method for the NAND-structured cell: block erasing, successive programming, and reading [12]–[16]. This new structure makes it possible to fabricate high-density EEPROM's by utilizing the same manufacturing process used for conventional EEPROM's. Through this new cell structure, an experimental 4-Mbit EEPROM has been developed by using 1.0-μm design rules, which are currently applied in the fabrication of 1-Mbit DRAM's.

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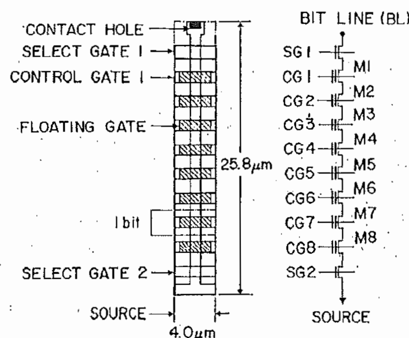

Fig. 1. Top view and equivalent circuit of NAND-structured cell.

II. NAND-Cell Structure

Fig. 1 shows the layout and the equivalent circuit of the NAND-structured cell. As shown in the figure, the NAND-structured cell has eight memory transistors in series sandwiched between two select gates: select gate 1 ($SG1$) and select gate 2 ($SG2$). The first gate ($SG1$) ensures selectivity and the second ($SG2$) prevents the cell current from

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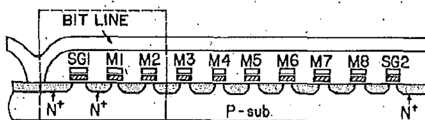

Fig. 2. Cross-sectional view of NAND-structured cell.

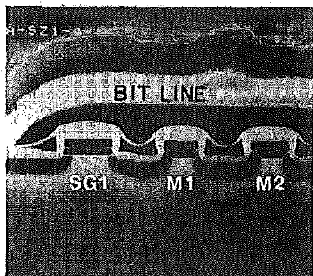

Fig. 3. Cross-sectional SEM photograph of NAND-structured cell.

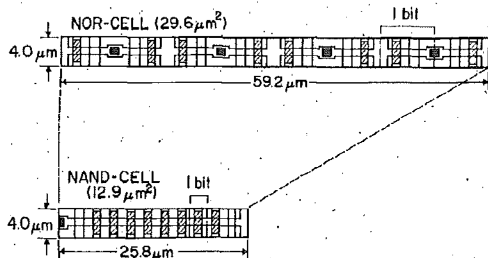

Fig. 4. Comparison of conventional NOR-structured cell with NAND-structured cell.

passing during the programming operation. The bit line consists of aluminum and n^+ diffusion layers.

Fig. 2 shows a cross-sectional view of the NAND-structured cell. The memory cell transistors are made in a self-aligned double-polysilicon, floating-gate, n-channel process. The floating gates are made of first- (lower) level polysilicon. The control gates, which are word lines in an array, are made of the second-level polysilicon. Both the channel length and the width of the memory cell transistors are 1.0 μm.

The tunnel-oxide thickness under the floating gate is around 100 Å. The dielectric between the floating gate and the control gate is an oxide–nitride–oxide (ONO) stack with a capacitive equivalent oxide thickness of 250 Å. This structure has a higher breakdown voltage [18] and lower defect density [19] than an oxide monolayer. Fig. 3 shows an SEM photograph of the NAND cells which have been successfully fabricated.

Fig. 4 shows how the cell size can be reduced by using a NAND-structured cell as compared to the current cell (NOR-structured cell). By using 1.0-μm design rules, eight memory transistors of both NOR- and NAND-structured cells are illustrated. The conventional cell consists of one-half contact hole, one select transistor, one memory transistor, and one-half source line per bit. Thus, the cell size per bit is 29.6 μm^2. However, the NAND-structured cell has only two select transistors per 8 bits, therefore it has only 1/16 contact hole, 1/4 select transistor, one memory transistor, and 1/8 source line per bit. Thus the NAND-structured cell can realize a smaller cell area than the conventional cell. The dimensions of the eight-NAND structure are 4×25.9 μm^2, yielding a 12.9-μm^2 cell size which is only 44 percent of the area required by a NOR-structured, full-function EEPROM cell.

III. Cell Operation

Fig. 5 shows the control signals for read operation of the NAND-structured cell. If a cell is selected, 0 V is applied to the control gate of the selected cell while 5 V is applied to the control gates of the unselected cells. In this condition, all unselected cells can act as pass transistors, because the threshold voltage of a ONE programmed cell is around 2 V, and the threshold voltage of a ZERO programmed cell is around -3 V. By utilizing this method, which is the same method used for the read operation of mask ROM, any cell can be randomly selected. If the selected cell is a ZERO programmed cell, cell current flows. On the other hand, if the selected cell is a ONE programmed cell, no cell current flows at all. About 40 μA of cell current typically flows (worst-case current is 20 μA) if the cell is a ZERO programmed cell.

The key programming process for the NAND-structured cell is block erasing and successive programming. Fig. 6 shows the voltage waveforms applied to the control gates, select gates, and bit lines of NAND structured cells. One block of the NAND cell array is 32 kbits; in other words, 4-kbit NAND cell units. One erase/program cycle consists of one block-erase and eight program cycles. Block erase is accomplished by applying 17 V to all control gates and 0 V to the bit lines. Electrons are injected into all the floating gates of the cells ($M1-M8$). The threshold voltage of the erased cell ($M1-M8$) becomes the enhancement mode at approximately 2 V. All cells in a block are erased simultaneously. The program cycle starts from the source-side cell ($M8$) to the bit-line side cell ($M1$) successively in order to prevent interference between selected and unselected cells. At first, programming starts at the source-side cell ($M8$). Zero volts is applied to the control gate of the selected cell ($M8$), and 22 V is applied to the control gates of the unselected cells ($M1-M7$). These unselected cells act as pass transistors. If the bit lines are applied to an intermediate voltage of 11 V, no erasing occurs and the threshold voltage of $M8$ remains at 2 V. No tunneling current flows because the voltage difference between the control gate (22 V) and the source/drain (11 V) is insufficient to initiate tunneling current. It should be noted that no erasing occurs in the unselected cells. Therefore, the ONE logic state is programmed in $M8$. On the other hand, if the bit lines are raised to 22 V, the threshold voltage of the selected cell is pushed into the depletion mode of approximately -3 V due to the tunneling current, which flows from the floating gate to the drain. Therefore the ZERO logic state is programmed. After programming the $M8$ cell,

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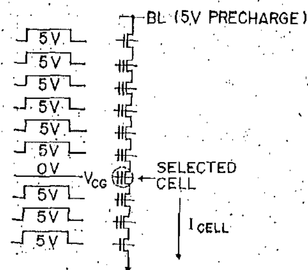

Fig. 5. Control voltages for read operation.

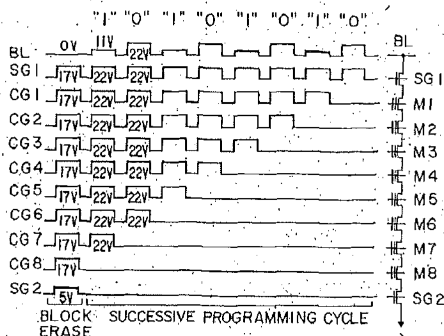

Fig. 6. Control voltages for erase/program operation.

programming of $M7$ starts. Zero volts is applied to the control gate of the selected cell ($M7$), and 22 V is applied to the control gates of the unselected cells. Subsequently, programming continues from the source-side cell to the bit-line side cell successively. The typical erase time is 1 ms and program time is 2 ms. The erase/program pulses are automatically generated by an internal address counter and timer control.

IV. Circuit Design

Row decoders are placed at center of the core area. Sense-amplifier circuits, column decoders, and bit-line control circuits are also located at the center of the chip, to divide the bit lines. Consequently, the cell array is divided into four planes, each of which has 1-Mbit (1024 × 1024) cells. NAND-cell control circuits, on-chip high-voltage generators, address and I/O buffer circuits are placed in the peripheral area.

A. Successive-Programming Circuitry

Fig. 7 shows the new circuitry to achieve the block erasing, successive programming, and random reading. The circuitry consists of pre-row decoder and successive-programming circuitry. The latter circuitry utilizes clocked-CMOS (C^2MOS) inverters. Input signals for this circuitry are three address data ($A0$, $A1$, $A2$). Output signals ($CG1'$–$CG8'$) are decoded by the main-row decoder as shown in Fig. 8, and applied to the control gates ($CG1$–$CG8$) of the NAND structured cells.

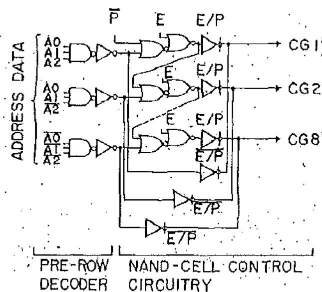

Fig. 7. Pre-row decoder and NAND-cell control circuitry.

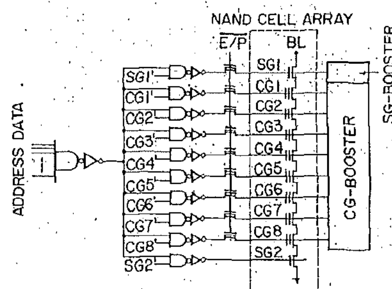

Fig. 8. Row decoder for NAND-structured cell.

TABLE I
Internal Clock Generators for NAND-Cell Control Circuitry

MODE	ERASE	PROGRAM		READ
CELL	M1~M8	M8--M2	M1	M2
CG1	17V	22V-22V	(0V)	5V
CG2	17V	22V--(0V)	0V	(0V)
⋮	⋮	⋮	⋮	⋮
CG8	17V	(0V)--0V	0V	5V
E/P	5V	5V		0V
E	5V	0V		0V
P̄	5V	0V		5V

The three kinds of operations, erase, program, and read, are selected by three kinds of internal clock generators E/P, E, and P-bar (Table I). If E/P, E, and P-bar are high, the circuitry generates signals for a block-erase mode, and eight control gates ($CG1$–$CG8$) are raised to 17 V by the control-gate booster. If E/P is high and both E and P-bar are low, it generates successive control signals from the source-side cell ($M8$) to the bit-line side cell ($M1$) for a program mode. In this mode, the control gate of the selected cell is kept at 0 V while the control gates of the unselected cells are boosted to 22 V. The control gates of the previously programmed cells are always kept at 0 V in order to prevent programmed cells from a soft erasure. If both E/P and E are low and P-bar is high, the circuitry generates signals for the read mode. For example, if the second cell is selected, the control gate ($CG2$) becomes 0 V, and the other unselected gates ($CG1$ and $CG3$–$CG8$) become 5 V. As a result, block erase, eight successive programs, and read are performed by using this circuitry.

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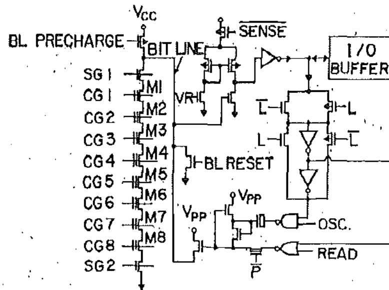

Fig. 9. Sense-amplifier and bit-line control circuitry.

B. Sense-Amplifier and Bit-Line Control Circuitry

Fig. 9 shows the sense-amplifier and bit-line control circuitry. In this 4-Mbit EEPROM design, a dynamic sensing system was adopted in order to ensure sensing against the small worst-case cell current. Before sensing the NAND-structured cells, bit lines are precharged to 5 V. Read is accomplished by applying 0 V to a control gate of the selected cell while 5 V is applied to the unselected cells, as described in Section III.

Bit-line control circuitry consists of data latch circuitry and charge pumping circuitry. In order to obtain high-speed programming, a page-program mode is adopted. One page length is 4 kbits. In the data-load sequence of the page programming, input data are stored in the latch circuitry. The stored data are boosted by the charge pumping circuit and transferred to the bit lines.

C. On-Chip High-Voltage Generator

Because both erase and program are performed by Fowler–Nordheim tunneling, the power consumption is low. Therefore, high voltages can be easily generated on the chip from a 5-V external power supply. Three kinds of high-voltage generators (V_{PP1}, V_{PP2}, and V_{PP3}) are implemented in the peripheral area. The erase voltage of 17 V and the program voltage of 22 V for control gates are generated from V_{PP1}. These voltages are selected by a voltage limiter. The intermediate voltage of 11 V for bit lines is generated from V_{PP2}. The programming voltage of 22 V for bit lines is generated from V_{PP3}.

V. Device Characteristics

The memory cells are fabricated by a 1-μm double-poly-silicon, single-aluminum process. The peripheral circuitry is fabricated from a 2-μm triple polysilicon n-well CMOS process. The average memory size is 12.9 μm^2/bit. The measured erase/program cycle exhibits over 10 000 cycles [16], which proved that oxide integrity is excellent. A chip microphotograph of 4-Mbit EEPROM is shown in Fig. 10. The chip organization is 512K×8 bit with the memory cells divided into four planes. Fig. 11 shows the observed operating waveforms. Typical read access time is 1.6 μs. Design characteristics are summarized in Table II.

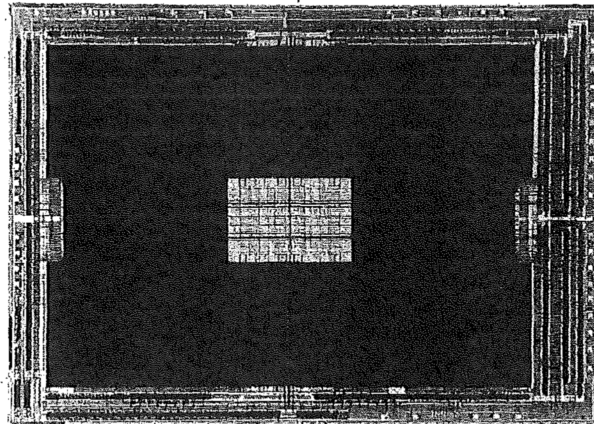

Fig. 10. Chip microphotograph of 4-Mbit EEPROM.

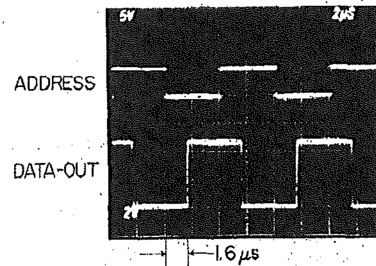

Fig. 11. Observed operating waveforms.

TABLE II
SUMMARY OF DESIGN CHARACTERISTICS

ORGANIZATION		512K x 8b	
		4Kb-PAGE PROGRAM MODE	
TECHNOLOGY		N-WELL CMOS	
		TRIPLE-LEVEL POLYSILICON	
		SINGLE ALUMINUM LAYER	
PROCESS PARAMETERS			
	CELL	GATE LENGTH	1.0μm
		TUNNEL OXIDE	100A
		INTER-POLY OXIDE	250A
	PERIPHERAL	GATE LENGTH(NMOS)	2.0μm
		GATE LENGTH(PMOS)	2.5μm
		GATE OXIDE	400A
CELL SIZE(1bit)		12.9μm²	
NAND CELL SIZE(8bit)		4 x 25.9μm²	
CHIP SIZE		10.7 x 15.3mm²	
ACCESS TIME		1.6μsec	
POWER CONSUMPTION		100mW	
STANDBY POWER		50uW	

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VI. Conclusion

A 5-V-only CMOS 4-Mbit EEPROM has been realized by using a NAND-structured cell. Employing a newly developed NAND-cell control circuitry, block erasing, successive programming, and random reading operations are successfully realized. In a read operation, a dynamic sensing scheme is adopted to ensure sensing against the small cell current. On-chip high-voltage generators are implemented and the high voltages for erase/program are generated from an external 5-V supply.

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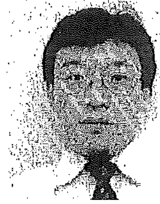

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