# A High-Density NAND EEPROM with Block-Page Programming for Microcomputer Applications

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*Abstract* —A 5-V-only CMOS 4-Mb NAND EEPROM with high-speed block-page programming circuits and on-chip test circuits for evaluating the NAND-structured cell is described. This high-density EEPROM has successfully demonstrated the applicability of these techniques for microcomputer applications, which require a large nonvolatile memory system with low power consumption.

## I. INTRODUCTION

MOST modern computer systems have CPU registers, a random access main memory, and a sequential access secondary memory to achieve high performance and low cost per bit. The necessary features of the secondary memory are large capacity, nonvolatility, and low cost per bit. The rotating magnetic disk, in its variations, is the most popular secondary memory device and has been in existence for some time. Because the magnetic disk needs a rotating mechanism (e.g., electronic motor) and a position sensing mechanism, the computer system with the magnetic disk systems is large and heavy.

High-density EEPROM's are attracting much interest in systems designers who wish to eliminate the rotating magnetic disks in portable computers and battery-powered laptops. Since the conventional EEPROM cell occupies a large area, the EEPROM's cost per bit is high and its capacity is not enough to be used as secondary memory.

Because the NAND EEPROM has a very small cell area, it can realize high density and low cost. The NAND EEPROM is the most promising candidate to replace the magnetic disk system [1]–[3].

At first, this paper introduces the NAND-structured cell and 4-Mb NAND EEPROM and describes the novel circuit techniques used in this EEPROM, which are a block-page mode for high-speed programming and several test modes to realize a highly reliable NAND EEPROM [4]–[7].

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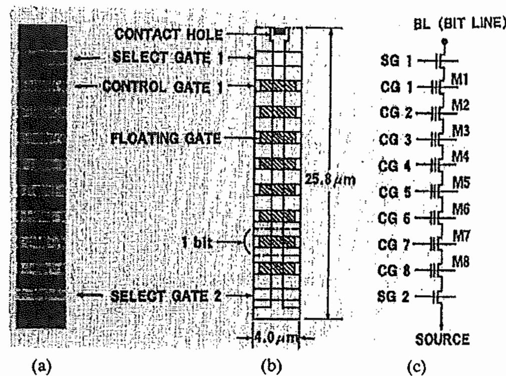


Fig. 1. Top view of the NAND-structured cell. (a) SEM micrograph. (b) Layout. (c) Equivalent circuit.

## II. 4-Mb NAND EEPROM

### A. NAND Structured Cell

Fig. 1(a)–(c) shows an SEM micrograph, the layout, and the equivalent circuit of the NAND-structured cell for the 4-Mb NAND EEPROM, respectively. As shown in this figure, this NAND-structured cell arranges eight elemental memory cells in series sandwiched between two select gate transistors. Select gate 1 (*SG*1) ensures selectivity and select gate 2 (*SG*2) prevents the cell current from passing during a programming operation. The memory cell transistors are made in a self-aligned double-polysilicon technology. The floating gates are made of first- (lower) layer polysilicon. The control gates are made of second- (upper) layer polysilicon. Both the channel length and width of the memory cell transistors are 1.0 μm.

Fig. 2 shows how the cell size can be reduced by using a NAND-structured cell as compared to the conventional cell (NOR-structured cell). By using 1.0-μm design rules, the memory transistors of both NOR- and NAND-structured cells are illustrated. The NAND-structured cell can realize a

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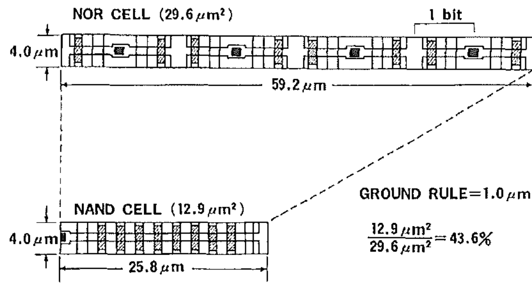



Fig. 2. Comparison of conventional NOR-structured cell with the NAND-structured cell.

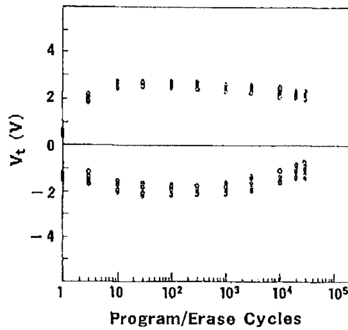



Fig. 3. Endurance characteristic of elemental memory cells of one NAND-structured cell.

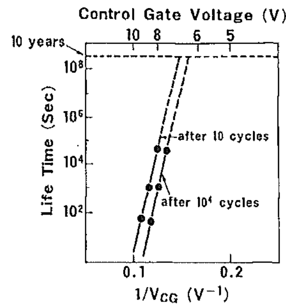
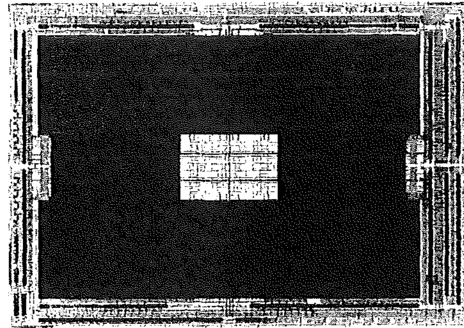


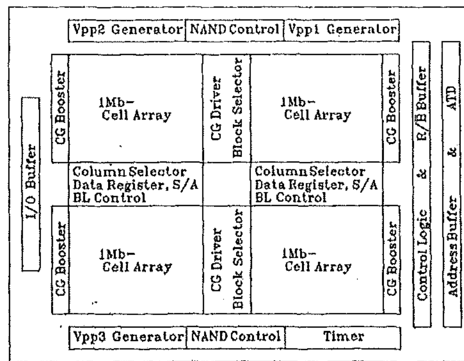

Fig. 4. READ retention characteristic of a elemental memory cell of a NAND-structured cell.

smaller cell area than that of the conventional cell. The whole area of eight NAND-structured cells is 4.0 $\mu$m$\times$25.8 $\mu$m and the cell area per bit is 12.9 $\mu m^2$. This is only 44% of the area required by a NOR-structured cell.

The endurance of the NAND-structured cell is shown in Fig. 3. Eight elemental memory cells of one NAND-structured cell are measured. The threshold voltage of each elemental memory cell after erasing/programming is independent of the location in the NAND structure. The difference between the threshold voltage of the cell after the tenth erase/program cycle and that of the cell after the 10000th erase/program cycle is very small. But the difference between the threshold voltage of the cell after the first cycle and that after the tenth cycle is not small. The warm-up of ten erase/program cycles is needed. The read retention after the 10000th erase/program cycle can be guaranteed for more than ten years in cases where the control gate voltage is below 6.5 V, as shown in Fig. 4.



(a)




(b)

Fig. 5. 4-Mb NAND EEPROM. (a) Photograph. (b) Layout.

### *B. 4-Mb NAND EEPROM*

Fig. 5 shows a photograph and the schematic layout of the 4-Mb NAND EEPROM chip. The chip size achieved is 10.7 mm $\times$15.3 mm. The organization is 512K$\times$8 b.

The memory cells are divided into four planes. Each plane has 1-Mb (1024$\times$1024) cells, in other words 128K NAND-structured cells. The memory cells are divided into 512 blocks for the block-page mode.

The circuit techniques of the 4-Mb NAND EEPROM are described briefly. On-chip high-voltage generators can realize 5-V-only erase/program operations, because erase and program are performed by Fowler–Nordheim tunneling. The block selector drives one pair of 512 pairs of $SG1$ and $SG2$. The $CG$ driver applies 5 V/0 V and $V_{GH}/V_{GL}$ to the control gates in the normal and test modes, respectively. $CG$ boosters raise the control gates of the selected NAND unit to erase/program voltages, which are generated by an on-chip high-voltage generator. The sense amplifier of the

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TABLE I
SUMMARY OF KEY ORGANIZATION, TECHNOLOGY, PHYSICAL, AND PERFORMANCE PARAMETERS

| | | | |
|---|---|---|---|
| ORGANIZATION | | 512K×8b | |
| | | 1Kbyte BLOCK-PAGE MODE | |
| TECHNOLOGY | | N-WELL CMOS | |
| | | TRIPLE-LEVEL POLYSILICON | |
| | | SINGLE ALUMINAM LAYER | |
| PROCESS PARAMETERS | | | |
| | CELL | GATE LENGTH | 1.0μm |
| | | TUNNEL OXIDE THICKNESS | 100A |
| | | INTER-POLY THICKNESS | 250A |
| | | (capative equivalent oxide thickness) | |
| | PERIPHERAL | GATE LENGTH(NMOS) | 2.0μm |
| | | GATE LENGTH(PMOS) | 2.5μm |
| | | GATE OXIDE THICKNESS | 400A |
| CELL SIZE | | $12.9\mu m^2$ | |
| NAND CELL SIZE(8bit) | | $4 \times 25.8\mu m^2$ | |
| CHIP SIZE | | $10.7 \times 15.3mm^2$ | |
| ACCESS TIME | | 1.6μsec | |
| POWER CONSUMPTION | | 100mW | |
| STANDBY POWER | | 50μW | |

dynamic sensing scheme ensures sensing against the small worst-case READ current. The address transient detector (ATD) generates the trigger signal of the dynamic sensing operation. Each bit line has a data register and a bit-line control circuit for block-page programming. Timers and an address buffer, which includes an address latch, can realize a self-timed erase/program cycle which frees the CPU to perform other tasks during erasing/programming. The $R/\bar{B}$ buffer is the output circuit of the $R/\bar{B}$ page signal for indicating one erase/program period and of the $R/\bar{B}$ block signal for indicating the whole block-page mode period.

### *C. Process and Device Technologies*

The memory cells are fabricated by a 1-μm self-aligned double-polysilicon technology. The tunnel-oxide thickness is around 100 Å. The inter-polysilicon dielectric is an oxide–nitride–oxide (ONO) stack with a capacitive equivalent oxide thickness of 250 Å.

The peripheral circuits are fabricated by a 2-μm triple-polysilicon n-well CMOS process. The gate oxide thickness is 400 Å. The gate lengths of NMOS and PMOS are 2.0 and 2.5 μm, respectively.

The main device parameters are shown in Table I.

## III. BLOCK-PAGE MODE

Fig. 6 shows a block diagram of the 4-Mb NAND EEPROM. The 4-Mb cells are split into 512 blocks. One block consists of 1024 NAND cell units. One block is the least unit for erasing/programming.

One block-page cycle consists of one block simultaneous erase cycle and eight successive page program cycles. Fig. 7 shows one block cell array and its control circuits. At first, all cells in the selected block are erased at once by applying 17 V to all control gates of the selected block and 0 V to the 1024 bit lines. Electrons are injected into all the floating gates of the cells. The threshold voltage of the erased cell becomes the enhancement mode of approximately 2 V. All cells in the block are erased simultaneously.

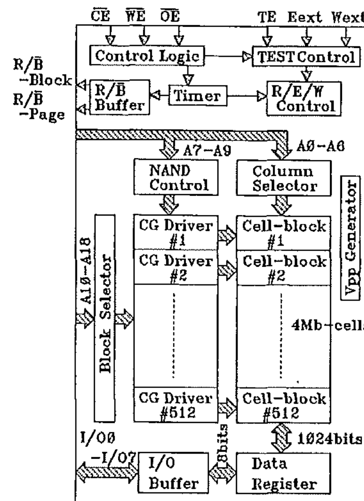


Fig. 6. Block diagram of the 4-Mb NAND EEPROM.

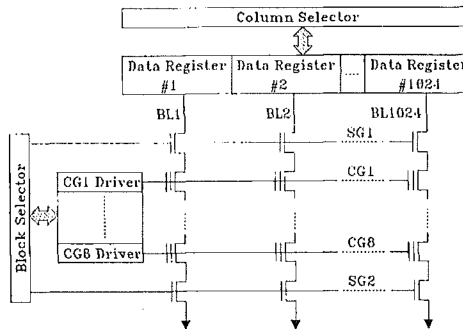


Fig. 7. One block cell array and its control circuits.

After the block erase operation is accomplished, the page programming starts from the source side cells, which are connected with the *CG*8 line, to the bit-line side cells, which are connected with the *CG*1 line, successively, in order to prevent interference between programmed cells and cells being programmed. One page-program cycle consists of a 1024-b data load sequence followed by a page program sequence. After the data load sequence, each of the bit lines is raised to programming voltages in accordance with the logic state of its data register.

At first, the programming starts at the source side cells which are connected with *CG*8. Zero volts are applied to the control gate of the selected cells (*CG*8) while 22 V are applied to the control gates of the unselected cells

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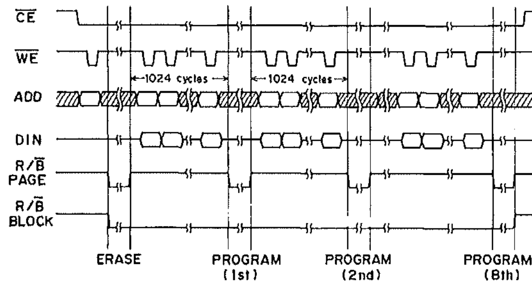


Fig. 8. Switching waveforms of block-page mode.

($CG1-CG7$), which are closer to the bit line than the selected cells. These unselected cells act as pass transistors.

In the case of ZERO programming, the bit line is raised to 22 V and electrons are emitted from the floating gate to the bit line by the electric field between the bit line and the floating gate of the selected cell. The threshold voltage of the selected cell is pushed into the depletion mode of approximately $-3$ V.

In the case of ONE programming, the bit line is raised to 11 V. But no electrons are emitted from the floating gate to the bit line, because the electric field between the bit line and the floating gate of the selected cell is insufficient to initiate tunneling. The threshold voltage of the selected cell remains at 2 V.

After programming the cells connected with $CG8$, the programming of the cells connected with $CG7$ starts. Zero volts are applied to the control gate of the selected cell ($CG7$) and the control gate of the unselected cell ($CG8$), which is closer to the source line than the selected cell ($CG7$). Twenty two volts are applied to the control gates of the unselected cells ($CG1-CG6$), which are closer to the bit line than the selected cell ($CG7$). The bit line is raised to 22 V in the case of ZERO programming, and 11 V in the case of ONE programming.

Subsequently, the programming continues from the source side cell to the bit-line side cell successively. Typical erasing time per block is 1 ms. Typical programming time per page, including the data load sequence, is 1 ms. As a result, the total programming time of one block page is 9 ms.

Fig. 8 shows the switching waveforms of the block-page mode.

After $\overline{CE}$ goes down to "low," first $\overline{WE}$ toggle triggers a block erase operation. Following the erase operation, eight page program operations are performed. Input data are stored in data registers corresponding to $\overline{WE}$ toggles. After $\overline{WE}$ stays at "high" level for around 1 ms, this EEPROM interprets that the data load sequence has finished. Each of the stored data is transferred to each of the bit lines; 1024 bits of data are programmed to the selected 1024 cells.

This EEPROM has the data registers, address input latch circuits, and timer circuit for self-timed erase/program. The EEPROM also has two extra output signals: the $R/\overline{B}$ page output signal indicates one erase/program period and the $R/\overline{B}$ block output signal indicates the whole block-page period.

If the CPU host monitors these signals, the CPU is free of controlling this EEPROM except for the data load sequence. The data registers, address input latch circuits, timer, and $R/\overline{B}$ output signals make interface circuits simple and raise CPU efficiency.

## IV. Test Mode

Tests for a EEPROM cell, for example, the endurance test and the data retention test, are important for realizing a highly reliable EEPROM. But these tests are time-consuming.

This 4-Mb NAND EEPROM has several test modes for shortening test time and raising test efficiency. When the $TE$ of the extra control input is "high," this EEPROM is in a test mode.

### A. Chip Erase and all Block-Page Program

When address input $A0$ is raised to $V_{HH}$ for a positive voltage between 9 and 15 V while $TE$ is "high," the chip erase mode is initiated and 4-Mb cells are all erased at once.

The all block-page mode is identical to the one block-page mode except that address input $A13$ is raised to $V_{HH}$ while $TE$ is "high." Then, 512 blocks are block-page programmed at the same time.

The chip erase mode and the all block-page mode are used to shorten the test time when carrying out tests that require a large number of erase/program cycles, such as the device endurance test.

### B. Cell Threshold Voltage Measure Mode

In the NAND EEPROM, the unselected cell acts as a pass transistor in READ/program operation. So, the threshold voltage of the ONE programmed cell must be controlled in the range between 1 and 3 V. In this section, the technique of measuring the threshold voltage of a ONE programmed cell is described.

Fig. 9 shows the typical READ current as a function of the control gate voltage of the selected elemental memory cell of the NAND-structured cell. In this case, the control gate voltage of the unselected elemental memory cells of the NAND-structured cell are 5 V. The threshold voltage of the ONE programmed cell is around 2 V. The threshold voltage of the ZERO programmed cell is around $-3$ V.

In the normal READ operation, the control gate voltage of the selected cell is 0 V, and that of the unselected cell is 5 V. So, the unselected cell can act as a pass transistor even if this cell is ONE programmed. If a ZERO programmed cell is selected, the selected NAND-structured cell generates READ current. If a ONE programmed cell is selected, the NAND-structured cell does not generate READ current.

Now, in the test READ mode, a control gate voltage can be externally applied. $V_{GL}$ is applied to the control gate of

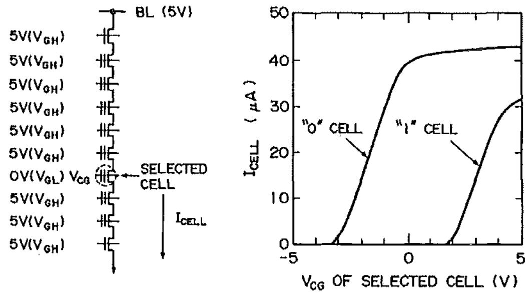


Fig. 9. Cell current as a function of the control gate voltage on the selected cell of the NAND cell.

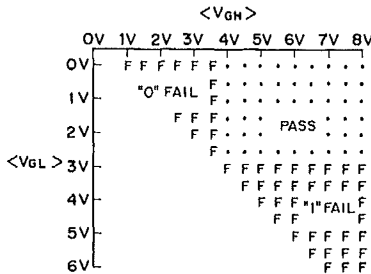


Fig. 10. Schmoo plot of test READ mode.

the selected cell. $V_{GH}$ is applied to the control gates of the unselected cells.

$V_{GL}$ is applied over 2 V. So, the NAND-structured cell generates READ current even if the ONE programmed cell is selected. If $V_{GH}$ is below 2 V, the unselected ONE programmed cell does not act as a pass transistor. So the NAND-structured cell does not generate READ current even if the ZERO programmed cell is selected.

Fig. 10 shows a schmoo plot in the test READ mode. The ZERO fail area shows that $V_{GH}$ is smaller than the threshold voltage of the unselected ONE programmed cell. So cell current does not flow in spite of the ZERO programmed cell selected. The ONE fail area shows that $V_{GL}$ is larger than the threshold voltage of the selected ONE programmed cell. So cell current flows in spite of the ONE programmed cell selected.

Thus, the threshold voltage of a ONE programmed cell can be easily evaluated from this schmoo plot. In this case, the threshold voltage of the ONE programmed cell is about 3 V.

By using this mode, the deviation in threshold voltage of a ONE programmed cell, between the initial state and the post-stressed state, can be measured. Fig. 11 shows the distribution of the threshold voltage of the ONE programmed cell in the 4-Mb NAND EEPROM. The distribution of the threshold voltage after ten erase/program cycles is between 1.6 and 3.2 V. The distribution after 10000 erase/program cycles is between 1.2 and 2.8 V. The deviation between the 10th and 10000th cycles is so small

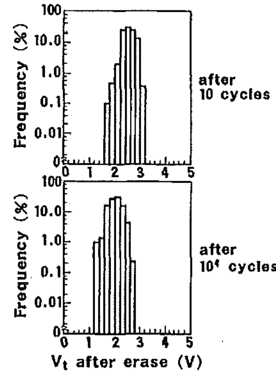


Fig. 11. Distribution of ONE programmed cell of the 4-Mb NAND EEPROM.

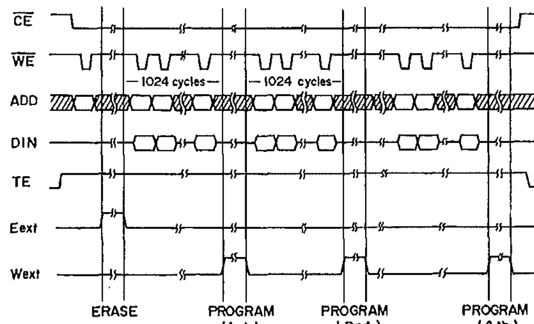


Fig. 12. Switching waveforms of test erase/program mode.

that this 4-Mb EEPROM reliably performs after 10000 erase/program cycles.

### C. External Timer and External Erase/Program Voltage

This NAND EEPROM has two extra control inputs for evaluating the NAND-structured cell. While $TE$ is "high," erase time and program time are controlled by the $E_{ext}$ and $W_{ext}$ inputs, respectively. If $\overline{CE}$ transits from "low" to "high" during an erase/program cycle in a block-page mode, the next program cycle cannot be initiated in the same block-page mode cycle.

Switching waveforms of the test erase/program mode are shown in Fig. 12.

On-chip high-voltage generators have output pads. From these output pads, erase/program voltages can be externally applied variably.

The features of the NAND-structured cell about erase/program can be evaluated by using these modes.

## V. Application

Fig. 13 shows floppy disks attached to a typical computer system and Fig. 14 illustrates NAND EEPROM's attached to a similar system. The system with floppy disks needs a floppy disk drive (FDD) that has a rotating

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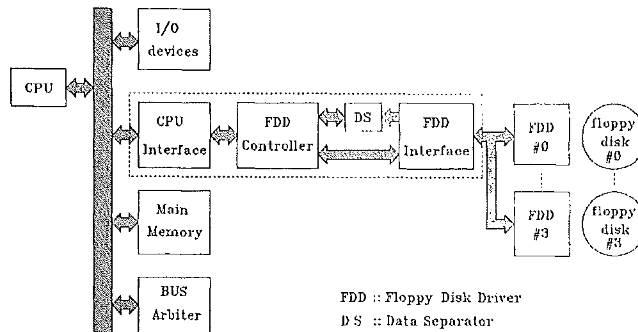


Fig. 13. Block diagram of computer system with floppy disks.

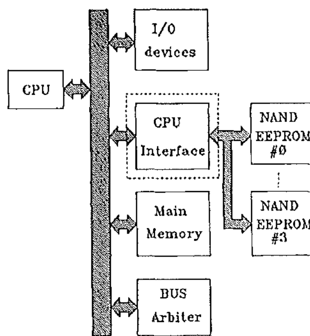


Fig. 14. Block diagram of computer system with NAND EEPROM's.

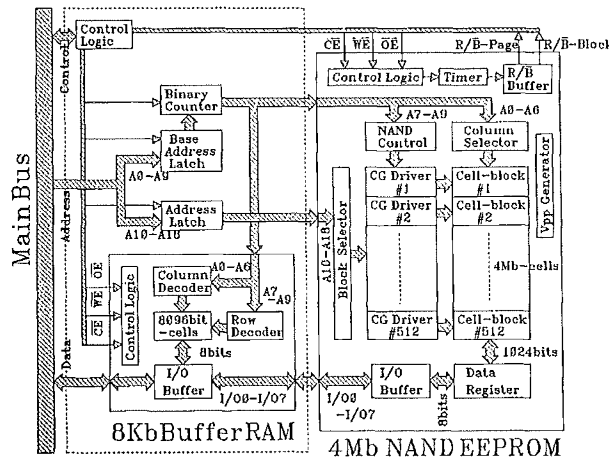


Fig. 15. Block diagram of the NAND EEPROM's and interface.

mechanism and a position sensing mechanism. An interface unit consists of FDD interface, a data separator (DS), an FDD controller, and CPU interface. DS extracts valid data from output signals of FDD. CPU interface contains a parallel–serial converter. Thus, this interface unit is complex.

On the other hand, the NAND EEPROM is a tiny semiconductor chip. The NAND EEPROM requires no extra control unit except for the CPU. The system with the NAND EEPROM is simpler, lighter, and less power-consuming than the system with magnetic media for a secondary memory device. Also, the access time per bit or

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program time per bit is 1/1000th shorter than that of the magnetic media including the seek time.

To further raise the CPU utilization on this system, a 1-kilobyte buffer RAM and a controller unit are needed for interface to the NAND EEPROM's. The buffer RAM is used for temporary storage of one block data. The controller has an address register for temporary storage of a selected block address and a binary counter for generating page and NAND-control address. By supporting these circuits, the CPU only carries out 1-kilobyte data loading to the buffer RAM during one block-page mode (as shown in Fig. 15).

The NAND EEPROM needs no power to retain its storage data. The EEPROM needs only 5-V power supply. Therefore, the NAND EEPROM is suitable for compact microcomputer applications, which are off-line systems with large storage. The memory card is an especially good application for the NAND EEPROM, whose characteristics are large capacity and nonvolatility with no power supply. This card can be used for personal cards of hospitals and banks, for an electronic camera, for the data cartridge of an electronic musical instrument, and for navigation systems.

## VI. Summary

A high-density, 5-V-only CMOS EEPROM with a NAND-structured cell using Fowler–Nordheim tunneling for programming has been realized. The block-page mode is adopted for high-speed programming and easy microprocessor interface. On-chip test circuits for test-time shortening and for cell characteristic evaluation realize highly reliable EEPROM's. The NAND EEPROM has many applications for microcomputer systems that require small size and large nonvolatile storage systems with low power consumption.

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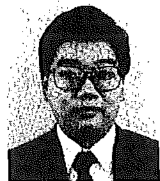

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He joined the Toshiba Research and Development Center, Kawasaki, Japan, in 1987. Since then he has been engaged in the research and development of high-density EEPROM's at the Toshiba ULSI Research Center.

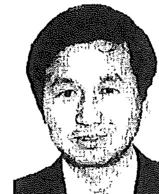
**Riichiro Shirota** was born in Hyogo, Japan, on February 22, 1954. He received the B.E., M.E., and Ph.D. degrees in physics in 1977, 1979, and 1982, respectively, from Nagoya University.

In 1982 he joined the Toshiba Corporation, Kawasaki, Japan. Since then he has been engaged in the research and development of high-density DRAM's and EEPROM's at the Toshiba ULSI Research Center.

**Kazunori Ohuchi** was born in Tochigi, Japan, on June 7, 1947. He received the B.E. degree in electronic engineering from Tohoku University, Sendai, Japan, in 1970.

In 1970 he joined the Toshiba Research and Development Center, Kawasaki, Japan. Since then he has been working on the circuit and device design of MOS memories, including EEPROM, EPROM, MROM, SRAM, and DRAM. His current interests are in the advanced device structure and circuits for 16-Mb DRAM's and beyond.

Mr. Ohuchi is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



**Fujio Masuoka** (A'88) was born in Takasaki, Japan, on May 8, 1943. He received the B.E., M.E., and Ph.D. degrees in electric engineering from Tohoku University, Sendai, Japan, in 1966, 1968, and 1971, respectively.

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Dr. Masuoka received the Watanabe Award and the National Invention Award in 1977 and 1978, respectively. He is a member of the Institute of Electronics, Information and Communication Engineers of Japan.