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High-Voltage Regulation and Process Considerations for High-Density 5 V-Only E²PROM's

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Abstract—A high-density 5 V-only HMOS I FLOTOX [1] E²-PROM technology has been developed through the use of stepper lithography and dry etching techniques. A 1.5 μm minimum feature size and 0.5 μm registration result in a FLOTOX cell with an area of 270 μm^2 . This represents a 50 percent reduction of the original cell size. Equivalent endurance (10K cycles) and data retention (10 years) have been obtained. Improved critical dimension control has increased the uniformity of the new cell within the array. Junction leakage has been reduced by using an extended low-temperature anneal cycle. Circuit techniques have been developed to ensure full temperature range (-55 – 125°C) operation. A capacitive voltage divider in a feedback loop, an E² trimmable voltage reference, and a switched-capacitor RC network are employed to produce a temperature-stable programming pulse with a rising edge time constant of ~ 600 μs . The programming voltage can be trimmed with an accuracy of ± 0.5 V over a typical range of 19–24 V in order to match the requirements of the array. 16K and 64K 5 V-only E²PROM's with respective die sizes of 128 \times 182 mil (15.1 mm^2) and 223 \times 278 mil (40.0 mm^2) have been fabricated.

I. INTRODUCTION

THE field of nonvolatile memories has grown tremendously over the past few years. In particular, the area of electrically erasable programmable read only memories (E²PROM) has seen several fundamentally different technologies emerge [1]–[4]. A difficulty common to all of these approaches is that of limited erase/write cycling.

This problem is a direct result of the high-voltage stresses

that are applied to the memory cell during normal programming operations. Thus, the use of a fixed programming voltage with a large tolerance (typically 21 ± 1 V) can place severe constraints on the process in order to avoid programming yield and reliability problems. On-chip generation of the programming pulse can relax some of these constraints if adequate control of the programming waveform is possible. A combination of technology and circuit enhancements that address this issue will be discussed.

The process developed is a high-density 5 V-only HMOS I FLOTOX E²PROM technology. Stepper lithography and dry etching techniques have reduced the minimum feature size to 1.5 μm . The improved critical dimension control and a new cell structure results in a 50 percent reduction in cell size over the original FLOTOX cell and better cell uniformity across the memory array. An extended low-temperature anneal cycle has been incorporated to reduce the junction leakage component of the high-voltage loading.

5 V-only operation has been achieved through the use of an on-chip voltage multiplier [5] and the elimination of dc programming current in the decoding circuitry. A capacitive voltage divider technique has been developed that allows the voltage multiplication (charge pump) circuits to be regulated with a feedback network. A trimmable voltage reference and a switched-capacitor RC network provide the control voltage for the feedback system.

16K and 64K 5 V-only E²PROM's have been fabricated using this technology. Both feature on-chip high-voltage regu-

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lation circuitry which provides rise time control and allows the programming voltage to be optimized for each die. Functionality has been demonstrated over the full military temperature range (-55-125°C).

II. THE TECHNOLOGY

The primary goal of the new process is to reduce the size of the E² cell without adversely affecting programming or reliability characteristics. It is important to note that a large percentage of the FLOTOX cell is taken up by a poly-to-poly capacitor. This capacitance must be large enough to couple the floating gate up to a sufficient voltage to induce tunneling, while the parasitic capacitance of the Fowler-Nordheim diode acts to degrade the coupling. Since the tunnel oxide is so thin (less than 200 Å), this parasitic capacitance is a strong function of the area of the structure. A smaller tunnel oxide area allows the size of the poly-to-poly coupling capacitor to be reduced while still maintaining acceptable programmability. Thus, the key to reducing the overall E² cell area is to reduce the tunnel oxide area.

There are three principal features that have allowed the tunnel oxide area to decrease from ~4 to ~2 μm². First, the tunnel oxide region is now defined by the intersection of the first poly layer and an oxide etch mask. In the original cell, the tunnel oxide region was effectively defined by the intersection of the first poly and diffusion layers. Difficulties associated with oxi-beak uniformity and oxi-edge junction quality are eliminated with the new cell design.

The most significant factor in this effort is the increased resolution and registration of direct-step-on-wafer lithography. Registration errors of less than 0.5 μm can be readily achieved. This is a substantial improvement over the 1.5 μm registration error typically achieved with conventional full wafer projection printing techniques. The improved resolution of the wafer stepper allows the tunnel oxide area to be reduced while actually improving control of the critical dimensions that define that region.

Finally, to fully exploit the capabilities of the wafer steppers, plasma etching has been employed on critical layers. This is necessary in order to produce minimum geometries while maintaining the desired critical dimension control. This combination of wafer steppers and dry etching techniques is capable of producing 1.5 μm geometries in a production environment.

These improvements allow the poly-poly capacitor in the new cell to be made smaller while still maintaining an acceptable top-poly-to-floating-poly voltage coupling ratio. The result is a 50 percent reduction in cell size, from 545 to 270 μm² (Fig. 1). Erase/write cycling data (Fig. 2) show that the new cell has programming and endurance characteristics which are nearly equivalent to the old cell. In addition, the improved critical dimension control results in a tighter distribution of programming thresholds (Fig. 3). The effect of this tighter control becomes significant as the number of bits in the array increases.

While considering the performance of the new E² cell, it is appropriate to discuss the programming conditions that maximize reliability and yield. As expected, cycling and bake experiments conducted on the original FLOTOX cell showed

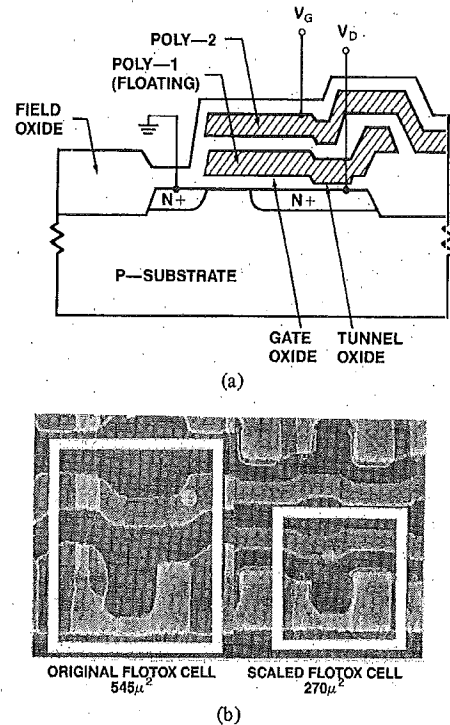


Fig. 1. (a) Cross section of the basic FLOTOX device, (b) cell size comparison.

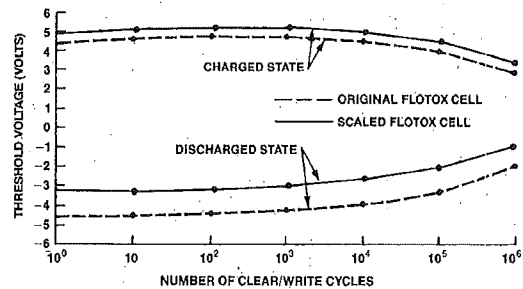


Fig. 2. Cell threshold voltage versus clear/write cycles.

that its endurance and data retention are directly related to the voltage used during programming. Too low a programming voltage resulted in failures due to insufficient program margin. Using too high a voltage resulted in failures due to overstress. Obviously, the optimum is somewhere in between the extremes, but the main complication is that this optimum programming voltage is process dependent.

In addition to the voltage level influences on programmability, it was found that FLOTOX cell performance is also dependent on the risetime of the programming pulse. Fig. 4 shows the difference in the electric field in the Fowler-Nordheim diode for a 600 μs RC and a 50 μs linear ramp. Since the Fowler-Nordheim expression has an exponential dependence on the electric field, the peak tunneling current during programming with a 600 μs RC can be orders of magnitude less than in the case of a "square" pulse.

An important process goal was to do as much as possible to accommodate a 5 V-only periphery. Specifically, at high temperature, the diffusion connected to the high-voltage node can

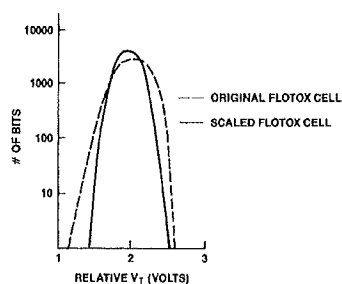


Fig. 3. Distribution of programming thresholds.

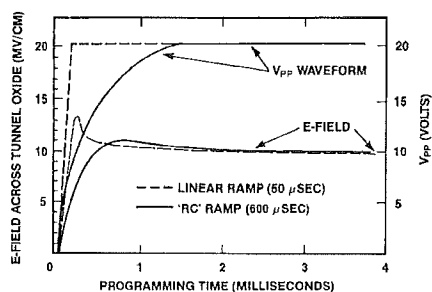
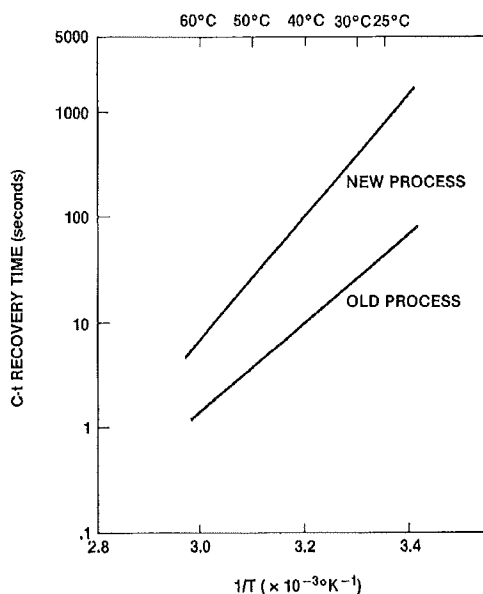
Fig. 4. Tunnel oxide electric field during programming as a function of V_{pp} risetime.

Fig. 5. Capacitance recovery time as a function of temperature.

have a substantial junction leakage current. In order to keep the size of the charge pump at a minimum, particular attention was placed on minimizing source-drain junction leakage. An extended low-temperature anneal was employed to reduce the contamination-related component of the leakage current. Fig. 5 shows a 2-5X increase in minority carrier lifetime (as measured by capacitance recovery time) for the new process.

III. CIRCUIT CONSIDERATIONS

Component operation with a single power supply has always been a desirable feature from a system design viewpoint. Until

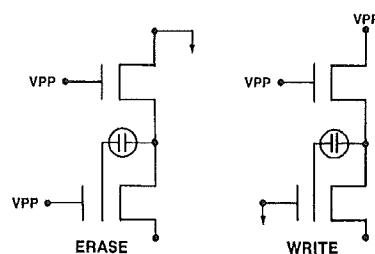


Fig. 6. Voltage conditions required for programming. Allowing the source to float during write eliminates dc programming current.

recently, E^2 PROM's required an additional high-voltage supply in order to modify the data in the memory array. Several devices have been described that utilize capacitive voltage multipliers to generate the high-programming voltage on the chip. However, manufacturing experience on 21 V E^2 PROM's has shown that yield and reliability are critically dependent on both the voltage and the risetime of the programming pulse [6]. After examining some of the key cell and decoding issues, the discussion will turn to the application of feedback, trimming, and switched-capacitor techniques to control the programming waveform.

Since the amount of current that can be generated by a charge pump circuit is limited, it is absolutely essential that the required programming current be minimal. The E^2 cell and the decoding circuitry are the main parts of the chip that must be connected to the charge pump. The two-transistor FLOTOX cell is shown schematically in Fig. 6. In the ERASE mode, the top gate of the sense transistor is taken to V_{pp} while the drain of the cell is taken to ground. Electrons tunnel to the floating gate, thereby shifting the threshold of the sense transistor in the positive direction. The loading on V_{pp} due to the cell in this case is a poly-poly capacitance. In the WRITE mode, the top gate is grounded while the drain and the select gate are taken to V_{pp} . An important point to note is that the source of the cell is allowed to float. If this were not done, then as electrons tunnel from the floating gate (and the threshold of the sense transistor becomes negative), current would be drawn from V_{pp} . However, with a floating source, there is no dc path from V_{pp} . In this mode, the loading on V_{pp} not only includes the capacitance due to the tunnel oxide structure, but also the capacitance and junction leakage of the diffusion in the cell.

The select lines of the array must be able to switch between V_{pp} and ground during programming. Traditionally, this is done by using a depletion load to V_{pp} . Unfortunately, the charge pump output is so limited that it cannot maintain the necessary high voltage while supplying the current required by all of the depletion devices on the unselected wordlines. This problem can be eliminated by using the circuit shown in Fig. 7.

Using a high-voltage switching technique that can be traced back to an OE/V_{pp} multiplexing circuit used on some varieties of 32 K EPROM's, this circuit is simple enough to replace the depletion device to V_{pp} on each wordline without paying too large an area penalty. When the output is to go high, the output node is precharged to V_{cc} . $T3$ serves as a transfer device to charge the clocked capacitor $T2$. $T1$ directs the current

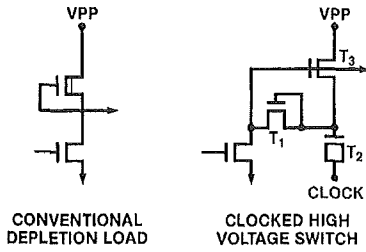


Fig. 7. Clocked high-voltage switch (T_1 - T_3) minimizes the dc current load on V_{pp} as compared to a standard depletion device.

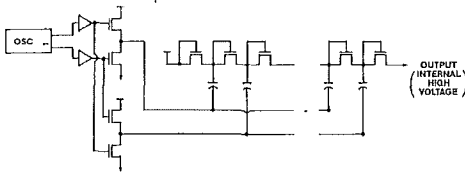


Fig. 8. Typical charge pump configuration.

from T_2 onto the output node. With each clock cycle, the output node voltage rises until it is a threshold (V_{t3}) above V_{pp} . The pumped output voltage is used to eliminate the effects of threshold drops both in the decoding circuitry and in the E² cell itself. The fact that the output node limits itself to a threshold above V_{pp} also reduces the chance of overstress in the peripheral circuitry. When the output is held low, T_3 is turned off and no current is drawn from V_{pp} .

IV. CHARGE PUMP REGULATION

As suggested in the earlier discussion of FLOTOX cell characteristics, the shape of the programming pulse can have a significant effect on both yield and reliability. Specifically, it was pointed out that there is an optimal programming voltage that will change with process variations. The fact that the programming voltage is to be generated on-chip (and does not have to meet a data sheet specification) means that a trimming scheme can be implemented. This will allow the programming voltage to be optimized for each chip.

The basic structure of a charge pump (or capacitive voltage multiplier) is shown in Fig. 8. A high-frequency oscillator (10 MHz) feeds a clock driver which produces two nonoverlapping clock signals. These clock signals are used to drive a chain of diode-connected transistors and capacitors. The open circuit output voltage of such a system can easily exceed 20 V. The actual voltage obtained is a function of the number of diode/capacitor stages, the threshold drops in the diodes, the amplitude of the clock, and the load current.

The difficulties with such a simple implementation become apparent when the load current requirements are examined. As discussed before, a fundamental requirement of the FLOTOX cell is that the risetime of the programming pulse be limited to a 600 μ s RC. This could be achieved by utilizing a charge pump whose current output is low enough to attain the desired rise time using the capacitance on the high-voltage node as the only load.

However, this approach does not compensate for junction

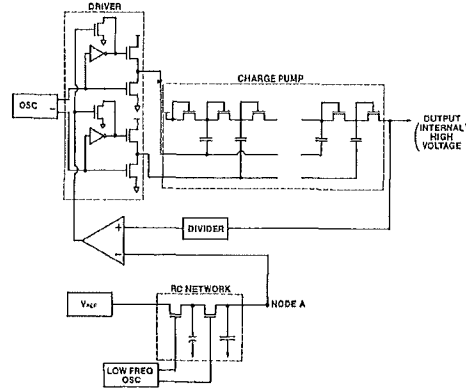


Fig. 9. Simplified schematic of the high-voltage regulation circuit.

leakage. This is significant because one of the design goals was to obtain full temperature range operation. As the temperature increases, the charge pump output will decrease and the junction leakage will increase. This will cause the risetime to push out. At some point, the charge pump may even fail to achieve the desired final voltage. This problem is even worse for the case in which both word and chip functions are to be supported because the capacitive load will also be varying.

All of the difficulties that have been discussed are characteristic of an open loop system. Thus, the approach taken to solve these problems is to introduce a feedback network to close the loop. The system that results is shown in Fig. 9. The feedback loop is made up of a clock driver (whose output swing is controllable), the diode-capacitor chain, a voltage divider, and a differential amplifier.

The negative feedback forces the output voltage to be equal to the voltage applied at node A multiplied by the reciprocal of the divider ratio. The voltage at node A is generated by an RC network that is allowed to charge up to V_{ref} . By making the time constant of the RC network equal to 600 μ s and setting V_{ref} equal to the optimal programming voltage multiplied by the divider ratio, the desired programming pulse can be produced.

The feedback loop allows the basic charge pump to be designed to work in the worst-case corner (chip erase with slow processing, high temperature, and low V_{cc}) without fear of overstress in the best-care corner (word function with fast processing, low temperature, and high V_{cc}). However, in order to achieve the desired voltage control (± 0.5 V) and the long 600 μ s time constant, special circuit techniques were required.

The most critical part of the feedback loop is the voltage divider. Again, the crucial factor turns out to be the limited output capability of the charge pump. Anything connected to the output node must be operating at a very low bias current (microamps). In addition, the output voltage is quite high (>18 V), so that a device connected to the output node will either have a high V_{ds} or a high source bias. The net effect is to make it very difficult to build an accurate temperature stable voltage divider from MOS devices.

An approach that gets around all of these problems is to exploit the inherent charge retention characteristics of the floating gate technology and build a capacitive voltage divider. First of all, there is no dc loading on the charge pump. The

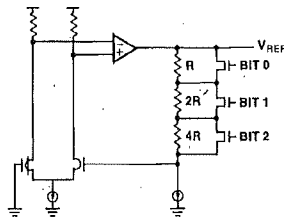


Fig. 10. Trimmable voltage reference based on enhancement and depletion device thresholds.

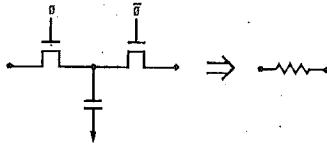


Fig. 11. Basic switched-capacitor equivalent of a resistor.

divider ratio is very stable with temperature [8]. By making all of the capacitors in the divider of the same oxide layer, the divider ratio becomes almost process independent.

The nature of the voltage divider places the majority of the output stability burden on the voltage reference (V_{ref}). Fig. 10 shows a reference that is based on the well-established technique of taking the difference of enhancement and depletion thresholds [7]. This provides a very temperature-stable reference voltage. Depletion devices operating in the linear region and a bias current source form a 3 bit binary weighted DAC whose voltage is added directly to the normal output of the reference. The three controlling bits are set by additional E^2 cells in the periphery.

Realizing a $600 \mu s$ RC network was the final design challenge. As a calibration point on the magnitude of this time constant, given a typical 30 pF capacitor, the required R would be 20 $M\Omega$. The maximum charging current in the resistor would be less than $0.25 \mu A$. If the resistor were replaced by a current source, it would be difficult to make the current stable with temperature.

Taking an idea that has long been applied to analog filter circuits [9], [10], the switched-capacitor equivalent of a resistor, shown in Fig. 11, has been used to effectively implement a $600 \mu s$ RC on-chip. The two phase nonoverlapping clocks applied to $M1$ and $M2$ alternately connect the capacitor from one node to the other. The time averaged effect is to transport an amount of charge between the two nodes that is proportional to the difference in node voltages.

This switched-capacitor technique has several advantages. Since the capacitance in the "resistor" will track the timing capacitor, the time constant is determined to the first order by the clock frequency. In general, the oscillator frequency is easier to control than a submicroamp current.

The programming pulse that is produced by the feedback controlled charge pump is presented in Fig. 12. The leading edge of the pulse rises very slowly. The effect of the trimming circuitry can also be seen. The combination of the capacitive voltage divider and the E^2 trimmable voltage reference allows

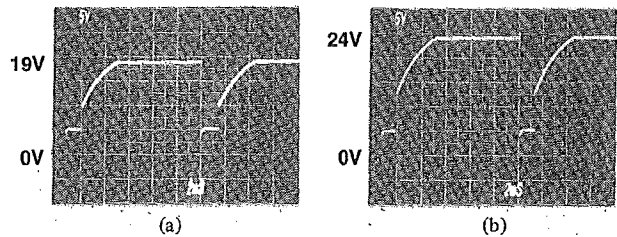


Fig. 12. Output waveform of the regulated charge pump, (a) untrimmed, (b) trimmed.

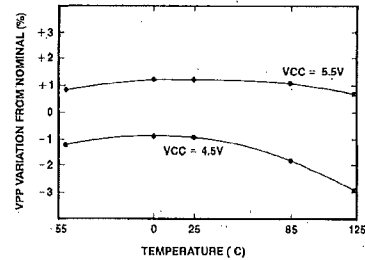


Fig. 13. Variation of the programming voltage as a function of temperature and V_{CC} .

the programming voltage to be adjusted to within ± 0.5 V of the target value. The typical voltage trim range is from 19-24 V. The graph in Fig. 13 shows the stability of the charge pump output as a function of the temperature and V_{CC} while doing a chip erase on a 16K array.

V. CONCLUSION

An advanced process technology and innovative circuit design techniques have been made to complement each other with the common goal of improving the yield and reliability of 5 V-only E^2 PROM's. The use of wafer steppers and dry etching techniques have reduced the FLOTOX cell size sufficiently to make a 64K E^2 PROM possible without degrading endurance or retention characteristics. Although the new cell is 50 percent smaller than the original cell, the new cell is observed to have a tighter distribution of programming thresholds. An extended low-temperature anneal was implemented to reduce charge pump loading at high temperature due to junction leakage.

On-chip generation of the programming voltage (5 V-only operation) is a necessity, with control of the programming pulse being critical. The waveform should be well-behaved to avoid yield loss and reliability problems. The application of feedback to the charge pump solves several of the regulation problems. A controlled rise time on the programming pulse is possible with a switched-capacitor network. The feedback loop forces the programming voltage to be a direct multiple of a trimmable temperature-stable voltage reference.

The results of this work are 16K and 64K 5 V-only E^2 PROM's which have die sizes of 128×182 mil (15.1 mm^2) and 223×278 mil (40.0 mm^2), respectively. These parts are capable of 10K erase/write cycles with 10 year data retention (see Table I). The internally generated programming pulse has a con-

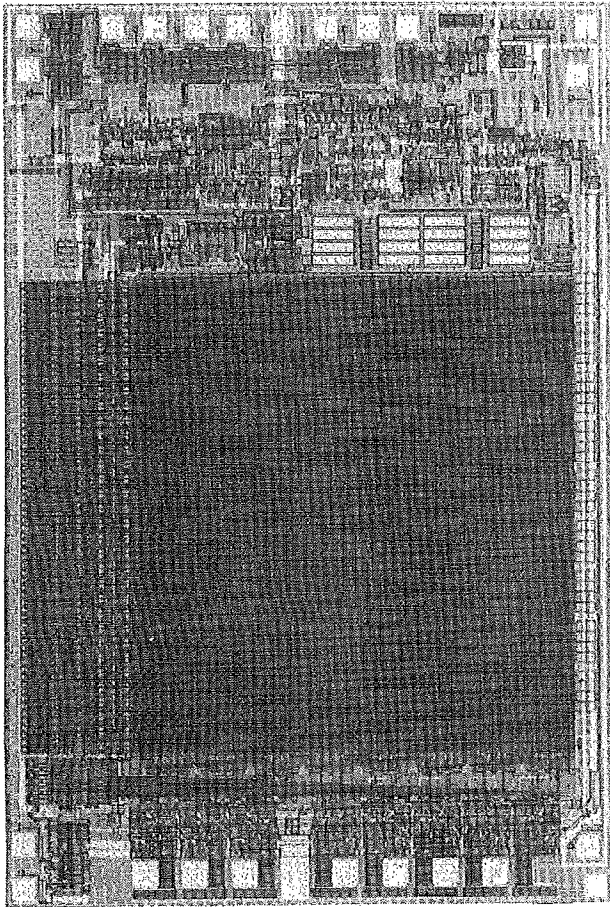


Fig. 14. Die photograph of the 5 V-only 16K E²PROM.

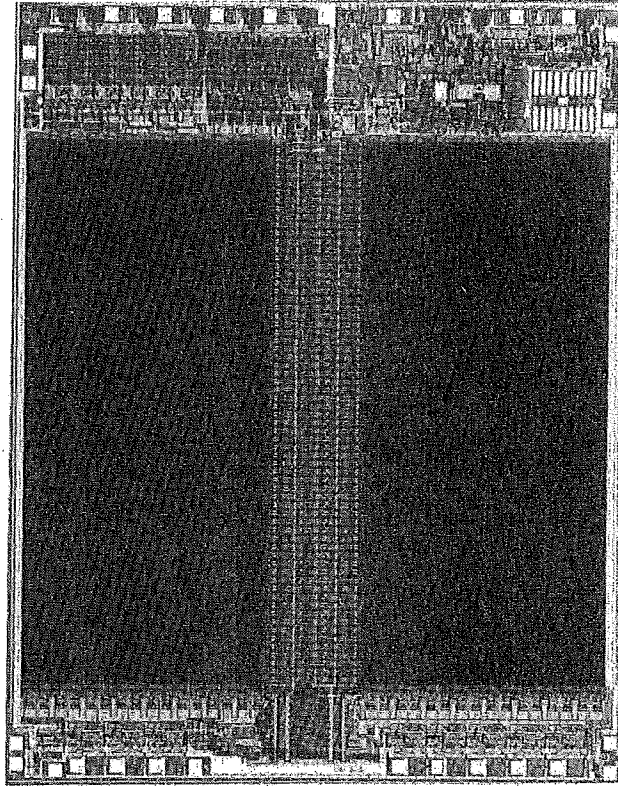


Fig. 15. Die photograph of the 5 V-only 64K E²PROM.

TABLE I
PERFORMANCE CHARACTERISTICS

PHYSICAL CHARACTERISTICS	16K E ² PROM	64K E ² PROM
CELL SIZE	270μ ²	270μ ²
DIE SIZE	23400 MIL ²	62000 MIL ²
ORGANIZATION	2KX8	8KX8
PACKAGE	24 PIN	28 PIN
CELL CHARACTERISTICS		
DATA RETENTION	>10 YRS.	>10 YRS.
C/W ENDURANCE	>10 ⁴	>10 ⁴
READ ACCESS	UNLIMITED	UNLIMITED
ELECTRICAL CHARACTERISTICS		
READ		
POWER SUPPLY	+5V	+5V
ACCESS TIME	150 NSEC	200 NSEC
WRITE/CLEAR		
POWER SUPPLY	+5V	+5V
WRITE/CLEAR TIME/WORD	10 MSEC	10 MSEC
CHIP CLEAR TIME	10 MSEC	10 MSEC
POWER DISSIPATION		
ACTIVE	250 MW	400 MW
STANDBY	100 MW	150 MW

trolled risetime and a programming voltage that is trimmed after die fabrication to match the characteristics of each memory array. Full functionality has been observed over a wide temperature range (-55-125°C).

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REFERENCES

- [1] W. S. Johnson et al., "A 16Kb electrically erasable nonvolatile memory," in *ISSCC Dig. Tech. Papers*, pp. 152-153, Feb. 1980.
- [2] A. Gupta et al., "A 5V-only 16K EEPROM utilizing oxynitride dielectrics and EPROM redundancy," in *ISSCC Dig. Tech. Papers*, pp. 184-185, Feb. 1982.
- [3] G. Landers, "5-volt-only EE-PROM mimics static-RAM timing," *Electronics*, June 1982, pp. 127-130.
- [4] A. Lancaster et al., "A 5V-only EEPROM with internal program/erase control," in *ISSCC Dig. Tech. Papers*, pp. 164-165, Feb. 1983.
- [5] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. SC-11, June 1976, pp. 374-378.
- [6] R. E. Shiner et al., "Characterization and screening of SiO₂ defects in EEPROM structures," in *1983 Proc. 21st Ann. Reliability Physics Symp.*, 1983.
- [7] J. L. McCreary, "Matching properties, and voltage and temperature dependence of MOS capacitors," *IEEE J. Solid-State Circuits*, vol. SC-16, Dec. 1981, pp. 608-616.
- [8] R. A. Blauschild et al., "An NMOS voltage reference," in *ISSCC Dig. Tech. Papers*, pp. 50-51, Feb. 1978.

- [9] B. F. Hosticka *et al.*, "MOS sampled data recursive filters using switched capacitor integrators," *IEEE J. Solid-State Circuits*, vol. SC-12, Dec. 1977, pp. 600-608.
- [10] J. T. Cavés *et al.*, "Sampled analog filtering using switched capacitors as resistor equivalents," *IEEE J. Solid-State Circuits*, vol. SC-12, Dec. 1977, pp. 592-599.



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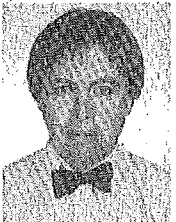
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Jay F. Olund, photograph and biography unavailable at the time of publication.

Vinod K. Dham, for a photograph and biography, see this issue, p. 532.

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