UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PHISON ELECTRONICS CORPORATION,
Petitioner,

v.

VERVAIN, LLC,
Patent Owner.

PGR2024-00048
Patent 11,854,612 B1

Before STACEY G. WHITE, JON M. JURGOVAN, and STEVEN M. AMUNDSON, *Administrative Patent Judges*.

WHITE, *Administrative Patent Judge*.

DECISION
Denying Institution of Post-Grant Review
35 U.S.C. § 324

I. INTRODUCTION

Phison Electronics Corp. ("Petitioner") requests post-grant review of claims 1–7 ("the challenged claims") of U.S. Patent No. 11,854,612 B1 (Ex. 1001, "the '612 patent"). Paper 2 ("Pet."). Vervain, LLC ("Patent Owner") filed a Preliminary Response (Paper 6) and a Disclaimer in a Patent, under 37 C.F.R. § 1.321(a), disclaiming claim 7 of the '612 patent (Ex. 2026). Thus, only claims 1–6 remain at issue.

We have authority to determine whether to institute a post-grant review under 35 U.S.C. § 324 and 37 C.F.R. § 42.4(a). We may not institute a post-grant review unless "the information presented in the petition . . . , if such information is not rebutted, would demonstrate that it is more likely than not that at least 1 of the claims challenged in the petition is unpatentable." 35 U.S.C. § 324(a) (2024).

Upon considering the evidence and arguments presented, we determine, as discussed below, that Petitioner has not demonstrated that it is more likely than not that at least 1 of the claims challenged in the Petition is unpatentable. Therefore, we deny[1] Petitioner's request to institute post-grant review of claims 1–6.

[1] Patent Owner raises discretionary denial under 35 U.S.C. §§ 324, 325(d). Prelim. Resp. 15−22, 62–68. As discussed herein, we deny Petitioner's challenge because it failed to demonstrate that it is "more likely than not" that at least one of the claims challenged in the Petition is unpatentable. Hence, we do not address Patent Owner's request for discretionary denial.

II. BACKGROUND

A. Real Parties-in-Interest

Petitioner identifies Phison Electronics Corporation as the real party-in-interest. Pet. 4. Patent Owner identifies Vervain, LLC, as the real party-in-interest. Paper 3, 1.

B. Related Matters

The parties identify *Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259 (W.D. Tex.) as a related matter. Pet. 5; Paper 3, 1. Patent Owner also identifies *Vervain, LLC v. Kingston Technology Co., Inc. et al.*, No. 1:24-cv-00254 (W.D. Tex.) as a related matter involving the '612 patent, as well as two previous district court cases that involved patents related to the '612 patent: *Vervain, LLC v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC*, No. 6:21-cv-00487 (W.D. Tex.); and *Vervain, LLC v. Western Digital Corp., Western Digital Technologies, Inc. and HGST*, No. 6:21-cv-00488 (W.D. Tex.). Paper 3, 1, 3–4. The parties also identify the following terminated or otherwise concluded Patent Trial and Appeal Board proceedings involving patents related to the '612 patent: PGR2024-00047 (U.S. Patent No. 11,830,546); IPR2021-01547 (U.S. Patent No. 8,891,298); IPR2021-01548 (U.S. Patent No. 9,196,385); IPR2024-01049 (U.S. Patent No. 9,997,240); and IPR2024-01050 (U.S. Patent No. 10,950,300). Pet. 2 n.4; Paper 3, 2–3.

C. Statutory Disclaimer

Patent Owner filed a statutory disclaimer of claim 7 of the '612 patent pursuant to 37 C.F.R. § 1.321. Prelim. Resp. 34; Ex. 2026. A statutory disclaimer is "considered as part of the original patent" as of the date on

which it is "recorded" in the Office. 35 U.S.C. § 253(a). For a disclaimer to be "recorded" in the Office, the document filed by the patent owner must:

> (1) Be signed by the patentee, or an attorney or agent of record;
>
> (2) Identify the patent and complete claim or claims, or term being disclaimed. A disclaimer which is not a disclaimer of a complete claim or claims, or term will be refused recordation;
>
> (3) State the present extent of patentee's ownership interest in the patent; and
>
> (4) Be accompanied by the fee set forth in [37 C.F.R.] § 1.20(d).

37 C.F.R. § 1.321(a); *see also Vectra Fitness, Inc. v. TNWK Corp.*, 162 F.3d 1379, 1382 (Fed. Cir. 1998) (holding that a § 253 disclaimer is immediately "recorded" on the date that the Office receives a disclaimer meeting the requirements of 37 C.F.R. § 1.321(a), and that no further action is required in the Office).

Based on our review of Exhibit 2026 and the Office's public records, we conclude that claim 7 has been disclaimed under 35 U.S.C. § 253(a) in compliance with 37 C.F.R. § 1.321(a), and thus, we will consider only the challenges to claim 1–6.

D. The '612 Patent

The '612 patent titled, "Lifetime Mixed Level Non-Volatile Memory System," describes "a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use of a combination of single-level cell (SLC) and multi-level cell (MLC) NAND flash storage without substantially raising the cost of the NAND flash storage system." Ex. 1001, code (54), 1:44–48.

Non-volatile memory is used for long-term data storage particularly because non-volatile memory retains its data even when the system does not have power. *Id.* at 1: 63–65. NAND flash memory is a common type of non-volatile memory and is known for superior performance, mechanical reliability, ruggedness, and portability. *Id.* at 2:2–6. The '612 patent discusses MLC and SLC NAND flash. SLC stores a single bit of information in a cell and MLC allows for multiple levels per cell and therefore, the storage of multiple bits per cell. *Id.* at 2:11–16. "Generally, MLC NAND flash enjoys greater density than SLC NAND flash, at the cost of a decrease in access speed and lifetime (endurance)." *Id.* at 3:39–41.

According to the '612 patent, a controller maintains two separate banks of NAND flash, including a first bank of economical MLC NAND flash and a second bank of high endurance SLC NAND flash. *Id.* at 5:13–17. After every write operation, the controller conducts a data integrity test. *Id.* at 5:17–18. "If a particular address range fails . . . , the address range is remapped from MLC NAND flash to SLC NAND flash," which "boost[s] the lifetime (endurance) of the storage system." *Id.* at 5:18–22.

Figure 3A of the '612 patent is reproduced below.

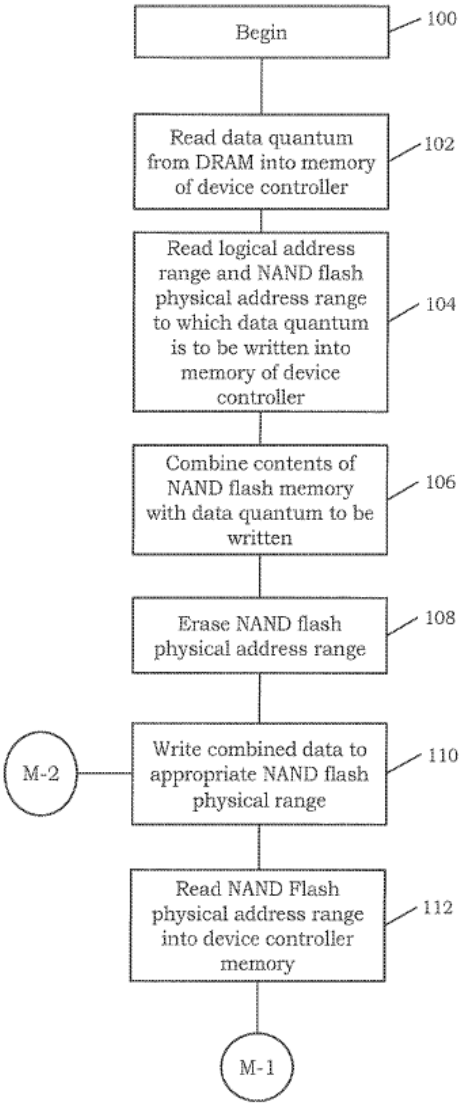

FIG. 3A

Figure 3A is a flow chart illustrating a method for using a NAND flash memory system. *Id.* at 6:19–21. In step 100, a command is received to write a quantum of data stored in DRAM to a particular location in NAND flash memory. *Id.* at 6:21–24. The quantum of data is read from DRAM into memory of a device controller in step 102. *Id.* at 6:24–26. In step 104, the logical address range and the NAND flash physical address range—to which the quantum of data will be written—are read into memory of the device controller. *Id.* at 6:26–29. The quantum of data is combined with the

contents of the NAND flash memory in step 106, and the NAND flash physical address range is erased in step 108. *Id.* at 6:29–32. Then, in step 110, the combined data is written to an appropriate NAND flash physical address range, which is read into the device controller memory in step 112. *Id.* at 6:32–36.

Figure 3B of the '612 patent is reproduced below.

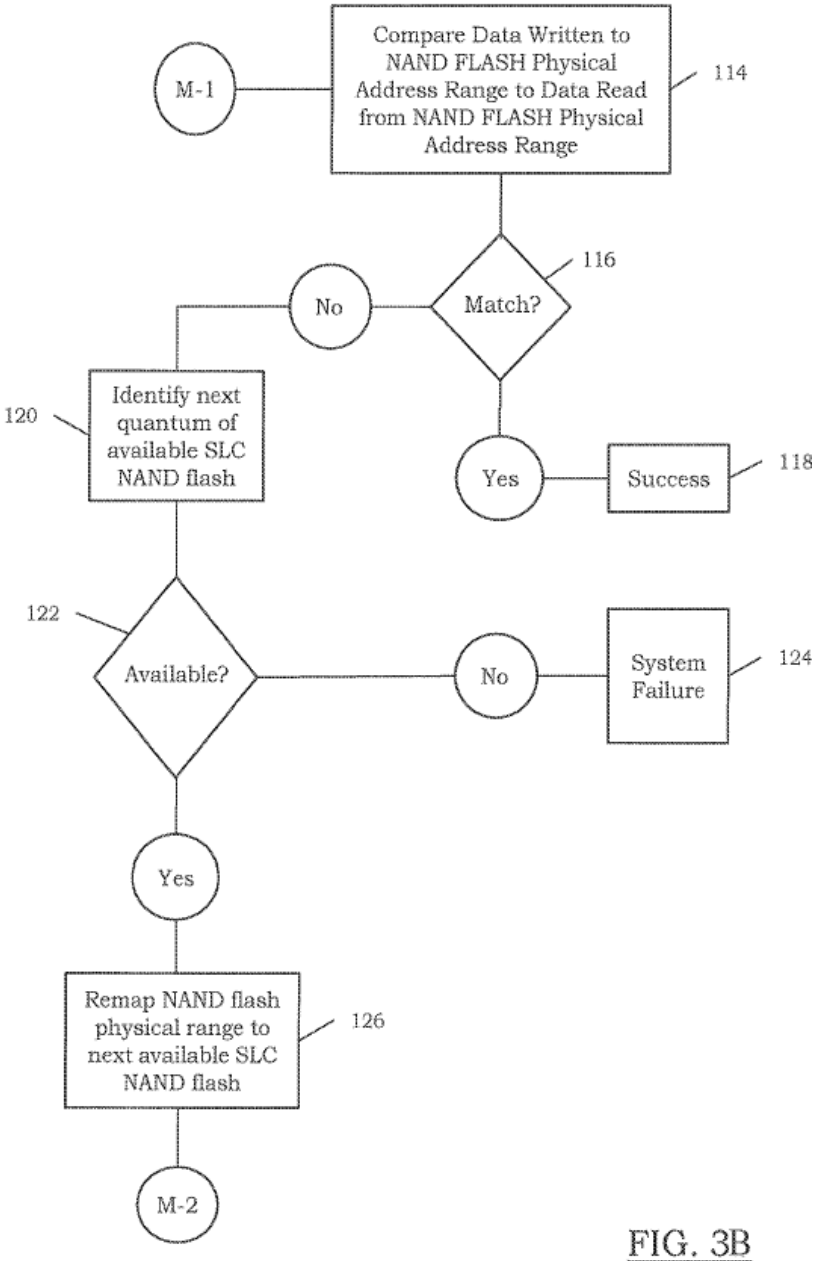

FIG. 3B

Figure 3B continues the flow chart shown in Figure 3A. *Id.* at 6:38. Step 114 compares the written NAND flash physical address range with the retained data representing the combination of the quantum of data to be written and the NAND flash physical address range. *Id.* at 6:38–43. In step 116, if the retained data matches the new data stored in the NAND flash memory, the write operation was successful, and the method exits in step 118. *Id.* at 6:43–45. If the retained data does not match the new data, the method proceeds to step 120, which identifies the next quantum of SLC NAND flash memory addresses available. *Id.* at 6:45–49. Step 122 determines if additional SLC NAND flash memory is available, and, if not, step 124 marks the system as failed and prompts an alert. *Id.* at 6:49–52. If additional SLC NAND flash memory is available, step 126 includes remapping the failed NAND flash physical address range to the next available quantum of SLC NAND flash memory. *Id.* at 6:52–55. Then, the method returns to step 110 to repeat the write operation. *Id.* at 6:56–57.

E. Illustrative Claim

As discussed above, Patent Owner disclaimed claim 7, and only claims 1–6 remain as challenged in this proceeding. *See* Ex. 2026. Of the remaining challenged claims, claim 1 is independent and is reproduced below with bracketed labels, as added by Petitioner. Pet. 18–20.

> 1. [1Pre] A method for storing data comprising:
>
> [1a] maintaining an address table for a memory space containing volatile memory and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space and the volatile memory includes a random access volatile memory element;

[1b] [1b1] mapping logical and physical addresses adaptable to the system by the address table, wherein [1b2] the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps data in at least one of volatile or nonvolatile memories;

[1c] controlling during Write access operations and Read access operations a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element and at least one SLC memory module including at least one SLC nonvolatile memory element and associated memory space using at least one controller;

[1d] storing received data within a controller memory associated with the at least one controller;

[1e] controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory element for storage of the received data;

[1f] transferring [1f1] the stored received data from the controller memory [1f2] to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one given one [sic] of the MLC nonvolatile memory element as stored data;

[1g] retaining the received data in the random access volatile memory as retained data associated with the stored data;

[1h] performing a data integrity test on the stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules [1h1] after at least a Write access operation performed thereon, the performing of the data integrity test further comprising:

> [1h2] reading the stored data to the controller memory;
>
> [1h3] comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

[1i] remapping, [1i1] responsive to a failure of the data integrity test performed on the stored data by the controller, [1i2] the address space to a different physical range of addresses; and

[1j] transferring data corresponding to the retained data to those remapped physical address from those physical addresses determined to have failed the data integrity test.

Ex. 1001, 7:42–8:36.

F. Asserted Grounds of Unpatentability

Petitioner, supported by a declaration of Carl Sechen, Ph.D. (Ex. 1002), asserts the following grounds of unpatentability (Pet. 21–22):

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–6	112	Written Description
1–6	112	Indefiniteness
1–6	103	Gavens[2], "a POSITA's knowledge"

Patent Owner opposes Petitioner's challenge (Prelim. Resp.) and relies on the declaration of Sunil P. Khatri, Ph.D. (Exhibit 2001) to support its opposition.

III. ANALYSIS

A. Eligibility for Post-Grant Review

The post-grant review provisions in § 6(d) of the Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284 (2011), apply only to patents subject to the AIA's first-inventor-to-file provisions. *See* AIA § 6(f)(2)(A) (explaining that the amendments made in § 6(d) "shall apply only to patents described in" § 3(n)(1)). Patents subject to the AIA's

[2] U.S. Patent No. 8,634,240 B2, issued Jan. 21, 2014 (Ex. 1045, "Gavens").

first-inventor-to-file provisions are those that issue from applications "that contain[] or contained at any time . . . a claim to a claimed invention that has an effective filing date . . . on or after" March 16, 2013. AIA § 3(n)(1). Additionally, a "petition for a post-grant review may only be filed not later than the date that is 9 months after the date of the grant of the patent or of the issuance of a reissue patent (as the case may be)." 35 U.S.C. § 321(c). Petitioner has the burden of demonstrating eligibility for post-grant review.

Petitioner "certifies that: (1) the '612 patent is eligible for post-grant review." Pet. 7. The '612 patent issued on December 26, 2023. Ex. 1001, code (45). Petitioner filed the Petition on September 25, 2024, i.e., less than nine months after the date of the grant of the '612 patent. Pet. 79. Patent Owner does not dispute that the '612 patent is eligible for post-grant review. *See* Prelim. Resp.

Petitioner, however, does not carry its burden to show it is more likely than not that any of the challenged claims are unpatentable based on the merits of its challenges and as such, we need not decide whether the '612 patent is eligible for post-grant review. For purposes of analysis, we assume without deciding that the '612 patent is eligible for post-grant review.

B. Level of Ordinary Skill in the Art

As part of our determination as to whether an invention would have been obvious, 35 U.S.C. § 103 requires us to ascertain the level of ordinary skill in the pertinent art at the time of the invention. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). The resolution of this question is important because it allows us to "maintain[] objectivity in the obviousness inquiry." *Ryko Mfg. Co. v. Nu–Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991). The person of ordinary skill in the art is a hypothetical person who is presumed

to have known the relevant art at the time of the invention. *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995).

Factors that may be considered in determining the level of ordinary skill in the art include, but are not limited to, the types of problems encountered in the art, the sophistication of the technology, and educational level of active workers in the field. *Id.* In addition, the level of ordinary skill in the art is reflected by the prior art of record. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Generally, it is easier to establish obviousness under a higher level of ordinary skill in the art. *Innovention Toys, LLC v. MGA Entm't, Inc.*, 637 F.3d 1314, 1323 (Fed. Cir. 2011) ("A less sophisticated level of skill generally favors a determination of nonobviousness . . . while a higher level of skill favors the reverse.").

Petitioner asserts that a person of ordinary skill in the art "would have a bachelor's degree in computer engineering, electrical engineering, computer science, or a closely related field, along with at least two years of experience in the design, development, implementation, or management of memory devices and systems." Pet. 22. Petitioner also asserts that a "person with an advanced degree in a relevant field, such as computer or electrical engineering, would require less experience in the development and use of memory devices and systems, and "one could obtain equivalent knowledge and perspective from other life experiences as well." *Id.* at 22–23 (citing Ex. 1002 ¶¶ 60–61).

Patent Owner's declarant, Dr. Khatri, proposes a definition of the person of ordinary skill in the art. Ex. 2001 ¶ 24. Dr. Khatri, however, notes that his opinions would be the same under either his proposal or Petitioner's proposal. *Id.* ¶¶ 25–26. Patent Owner states that, for purposes

of the Preliminary Response, it "adopts Petitioner's definition of a person of ordinary skill in the art." Prelim. Resp. 13 (citing Pet. 22–23; Ex. 2001 ¶¶ 22–26).

We determine that the current record supports Petitioner's description of an ordinarily skilled artisan. For purposes of this Decision, therefore, we adopt Petitioner's description of an ordinarily skilled artisan. We also note that the applied prior art reflects the appropriate level of skill at the time of the claimed invention. *See Okajima*, 261 F.3d at 1355.

C. Claim Construction

We apply the same claim construction standard that would be used in a civil action under 35 U.S.C. § 282(b), including construing claims in accordance with the ordinary and customary meaning of such claims, as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.200(b) (2024). In applying such standard, claim terms generally are given their plain and ordinary meaning, as would be understood by a person of ordinary skill in the art, at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc).

Petitioner proposes constructions for the claim terms "MLC memory modules" and "SLC memory module." Pet. 23–28. Patent Owner disagrees with Petitioner's constructions, but does not contest them because it argues that construction of these terms is not necessary to resolve the parties' disputes. Prelim. Resp. 14. Based on the record presented, we determine that no claim term requires an explicit construction to decide whether Petitioner satisfies the "more likely than not" standard for instituting a post-

grant review. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

D. Asserted Lack of Written Description

Petitioner asserts that the challenged claims are unpatentable due to a lack of written description. Pet. 28–36. Patent Owner opposes. Prelim. Resp. 22–34. For the reasons discussed below, Petitioner has not persuaded us of a lack of written description for any of the challenged claims.

1. *Claim 1*

a. *[1a] "maintaining an address table for a memory space containing volatile memory and nonvolatile memory space"*

Petitioner asserts that the term "memory space" is not supported as required by 35 U.S.C. § 112(a). Pet. 28–30. According to Petitioner, "the term 'memory space' (7:43–47, 8:3) is mentioned in the specification …only as a measure of memory capacity (5:23–25), and 'space' otherwise referring to commercial market share (2:47)." *Id.* at 30. Thus, Petitioner contends that the phrase "maintaining an address table for a memory space" as recited in claim 1 "is unsupported in the specification, which thus fails to enable a POSITA to practice the claimed invention." *Id.*

Patent Owner responds by arguing that "the specification's use of the term 'memory space' is entirely consistent with how the term is used in the claims to describe the space where data is stored." Prelim. Resp. 24. Patent Owner supports its argument with citations from the specification. *Id.* (citing Ex. 1001, 5:25, Figs. 1, 2A-2B, 4). We are persuaded by Patent Owner's arguments and evidence.

Section 112(a) requires that "[t]he specification shall contain a written description of the invention, and of the manner and process of making and

using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same." The Federal Circuit has held that "[t]he written description requirement is met when the disclosure relied on for support 'reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.'" *RAI Strategic Holdings, Inc. v. Philip Morris Prods. S.A.*, 92 F.4th 1085, 1088 (Fed. Cir. 2024) (quoting *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc) (citation omitted)).

The written description inquiry is a question of fact, is context specific, and must be determined on a case-by-case basis. *Ariad*, 598 F.3d at 1351 (citing *Ralston Purina Co. v. Far-Mar-Co, Inc.*, 772 F.2d 1570, 1575 (Fed. Cir. 1985); *Capon v. Eshhar*, 418 F.3d 1349, 1357–58 (Fed. Cir. 2005)). "[T]he level of detail required to satisfy the written description requirement varies depending on the nature and scope of the claims and on the complexity and predictability of the relevant technology." *Id.* (citing *Capon*, 418 F.3d at 1357–58). Factors used to evaluate the sufficiency of a disclosure include: 1) "the existing knowledge in the particular field"; 2) "the extent and content of the prior art"; 3) "the maturity of the science or technology"; and 4) "the predictability of the aspect at issue." *Id.* (citing *Capon*, 418 F.3d at 1359).

As support for the term "memory space," the '612 patent explains that because "the SLC NAND flash is used to boost the lifetime (endurance) of the storage system, it can be considerably lesser in amount than the MLC NAND flash." Ex. 1001, 5:20–23; *see* Ex. 2001 ¶ 51. As an example, the '612 specification states that "a system may set SLC NAND flash equal to

12.5% or 25% of MLC NAND flash (total non-volatile memory storage space=MLC+SLC)." Ex. 1001, 5:23–25; *see* Ex. 2001 ¶¶ 51, 62. In addition, we find persuasive Dr. Khatri's testimony that one of ordinary skill in the art would have understood that "there are two spaces—MLC and SLC—where data is stored, and the total memory space is the combination of the two." Ex. 2001 ¶ 51.

Further, the '612 patent's Figure 1 depicts "memory space," e.g., dynamic random-access memory (DRAM) 20, one or more disks 24, MLC NAND flash memory module 26, and SLC NAND flash memory module 28. Ex. 1001, 5:37–45, Fig. 1; *see* Ex. 2001 ¶ 64. The '612 patent's Figure 4 also depicts "memory space," e.g., NAND flash memory bank 56 comprising "a plurality of MLC NAND flash memory modules 60a and a plurality of SLC NAND flash memory modules 62a" and NAND flash memory bank 58 comprising "a plurality of MLC NAND flash memory modules 60b and a plurality of SLC NAND flash memory modules 62b." Ex. 1001, 7:8–14, Fig. 4; *see* Ex. 2001 ¶ 64. On the record before us, we find the above noted disclosures to be sufficient to support the disputed claim language.

For these reasons, the '612 patent's disclosure "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *See Ariad*, 598 F.3d at 1351.

b. *"memory element"*

Petitioner asserts that the challenged claims lack written description support "because the term 'memory element' (8:1–2 {step [1c]}, 8:7–8 {step [1e]}, 8:11–13 {step [1f]}, and 8:19–26 {step [1h]}) is not even mentioned in the originally filed common specification." Pet. 33–34.

Patent Owner responds by correctly pointing out that "[t]he specification does not need to use the exact claim language." Prelim. Resp. 32 (citing *Ariad*, 598 F.3d at 1352). Patent Owner persuasively explains that "[t]he specification states that cells of SLC or MLC flash memory may store a single bit or multiple bits per cell, respectively. The specification shows in great detail, albeit with different words, how MLC and SLC memory elements are used to store data. *Id.* (internal citations omitted) (citing Ex. 1001, 2:11-18, 5:46-7:14 Figs. 1, 4).

We are persuaded by Patent Owner's arguments and evidence. The Federal Circuit has held that the written-description requirement "does not demand any particular form of disclosure" or "that the specification recite the claimed invention *in haec verba*." *Ariad*, 598 F.3d at 1352. This is applicable here, where the exact term "memory element" is not used, but there is strong evidence that the inventor had possession of that subject matter. For example, Figures 2A–2B depict "memory elements," such as MLC and SLC blocks. Ex. 1001, 6:4–19, Figs. 2A–2B; *see* Ex. 2001 ¶ 55. The '612 patent's Figure 4 also depicts "memory elements," e.g., "a plurality of MLC NAND flash memory modules 60a," "a plurality of MLC NAND flash memory modules 60b," "a plurality of SLC NAND flash memory modules 62a," and "a plurality of SLC NAND flash memory modules 62b." Ex. 1001, 7:4–11, Fig. 4; *see* Ex. 2001 ¶ 55.

Further, the '612 patent incorporates by reference the '452 patent. Ex. 1001, 1:29–37. The '452 patent describes an "exemplary NAND memory integrated circuit" as an "element" of a "nonvolatile memory system." Ex. 1004, 2:52–54, Fig. 2; *see* Ex. 2001 ¶ 82. Petitioner admits that the '452 patent's "exemplary NAND memory integrated circuit"

corresponds to a "NAND flash memory module." Pet. 34 n.9. On the record before us, we find the above noted disclosures to be sufficient to support the disputed claim language.

For these reasons, the '612 patent's disclosure "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *See Ariad*, 598 F.3d at 1351.

c. *[1b2] "the mapping is performed as necessitated by the system to maximize lifetime"*

Petitioner contends that the phrase "the mapping is performed as necessitated by the system to maximize lifetime" is not supported as required by 35 U.S.C. § 112(a). Pet. 30–32. Petitioner argues that there is "no mention of 'maximiz[ing] lifetime' of anything" in the '612 specification. *Id.* at 30–31. Petitioner's declarant, Dr. Sechen, supports Petitioner by opining that the "[t]here is no recitation, much less supporting disclosure of when and how 'the system' 'necessitates' 'maximiz[ation of] lifetime' and of what." Ex. 1002 ¶ 75.

Patent Owner responds by arguing that the '612 specification "explains—as is claimed—that mapping is performed to increase the "reliability and lifetime" of the memory." Prelim. Resp. 28 (citing Ex. 1001, 1:41–48). Patent Owner here again supports its assertions with citations to the text and figures of the specification. *See id.* (citing Ex. 1001, 1:41–48, 3:26–33, 5:67–6:3, 6:64–7:3, Figs. 2A–2B, 3A–3B); *see also* Ex. 2001 ¶ 52 (supporting testimony from Dr. Khatri).

We are persuaded by Patent Owner's argument and evidence. For example, the '612 patent explains that "mapping is performed to increase the 'reliability and lifetime' of the memory." Ex. 1001, 1:41–42; *see* Ex. 2001 ¶¶ 52, 66. Synonyms and near synonyms for "maximize" include the words

"increase," "boost," and "prolong." Ex. 2017, 1; *see* Ex. 2001 ¶ 67. These synonyms for "maximize" are used in '612 patent's specification when it discusses system lifetime. *See, e.g.*, Ex. 1001, 1:43–44, 3:25–33, 5:20–22, 7:21–23; Ex. 2001 ¶ 67.

Also, as Patent Owner asserts, the '612 patent's Figures 2A–2B and 3A–3B show how "data is remapped to boost or prolong the lifetime of the system." Ex. 2001 ¶¶ 52, 67; *see* Prelim. Resp. 28–29. For instance, Figures 2A–2B and the related descriptions in the specification disclose remapping data for an MLC/block to an SLC/block after a failed data integrity test. Ex. 1001, 6:11–18, Figs. 2A–2B; *see* Ex. 2001 ¶¶ 52, 67.

Further, the '612 patent discloses various wear-leveling techniques for transferring data to less-used blocks or higher-performance blocks including (1) "select[ing] an available target block with the lowest overall erase count" and (2) remapping from MLC NAND flash memory to SLC NAND flash memory. Ex. 1001, 3:26–33, 5:67–6:3, 6:64–7:3, code (57); *see* Ex. 2001 ¶¶ 52, 68. According to the patent, remapping from MLC NAND flash memory to SLC NAND flash may include allocating "hot" blocks (those blocks that receive frequent writes) to SLC NAND flash memory and allocating "cold" blocks (those blocks that only receive infrequent writes) to MLC NAND flash memory. Ex. 1001, 6:58–7:3.

The wear-leveling techniques disclosed in the '612 patent boost or prolong lifetime such that "the lifetime of the memory is maximized," e.g., by repeatedly performing one or more of them. *See* Ex. 2001 ¶¶ 52, 68; Ex. 1001, 3:26–33, 5:67–6:3, 6:64–7:3, code (57).

Moreover, an ordinarily skilled artisan would understand that "the lifetime of the system is maximized by transferring data to blocks with

higher endurance, whether it is a block that is less-used, or a higher-performance block," as the patent discloses. Ex. 2001 ¶ 68.

For these reasons, the '612 patent's disclosure "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *See Ariad*, 598 F.3d at 1351.

d. *[1c] "controlling during Write access operations and Read access operations a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element and at least one SLC memory module including at least one SLC nonvolatile memory element and associated memory space using at least one controller"*

Petitioner asserts that the "controlling" step of limitation 1c is unsupported because the terms "memory elements," "memory space," "Write access operations and Read access operations" are unsupported and "[n]o details are provided as to what 'controlling' means." Pet. 33. Further, "no structure was given to the abstract 'controller.'" *Id.* (citing Ex. 1002 ¶ 66).

Patent Owner responds by asserting that the '612 patent "clearly supports the 'controlling' step of limitation [1c]." Prelim. Resp. 30 (citing Ex. 2001 ¶¶ 52–54). Patent Owner directs us to Figure 1 of the '612 patent, which depicts a "device controller." *Id.* Patent Owner further explains that one of ordinary skill in the art would have understood the write and read operations recited in the claims noting that the '612 specification "explains that data is written to NAND flash from 'memory within the device controller,' and is subsequently read from NAND flash into 'device controller memory.'" Prelim. Resp. 31 (citing Ex. 1001, 6:24–37).

We are persuaded by Patent Owner's arguments and evidence. As discussed above we were not persuaded by Petitioner's arguments regarding the terms "memory elements" and "memory space." We find Patent Owner's evidence and arguments to be persuasive and that based on the record before us the '612 patent further supports the recited write and read access and supports the recited controlling and controller. As has been noted in regards to other terms, the test is not whether the specification recites the same words as the claims, but rather whether the specification shows that the inventor had possession of the subject matter.

Here, Figure 1 depicts a controller and in particular it illustrates "[a] processor 12 is coupled to a device controller 14, such as a chipset." Ex. 1001, 5:27–28. It further provides a detailed description of the controller and its functions:

> The device controller 14 provides interface functions to the processor 12. In some computer systems, the device controller 14 may be an integral part of the (host) processor 12. The device controller 14 provides a number of input/output ports 16 and 18, such as, for example, serial ports (e.g., USB ports and Firewire ports) and network ports (e.g., Ethernet ports and 802.11 "Wi-Fi" ports). The device controller 14 may also control a bank of, for example, DRAM 20, In addition, the device controller 14 controls access to one or more disks 24, such as, for example ; a rotating magnetic disk, or an optical disk, as well as two or more types of NAND flash memory.

Id. at 5:31–41. On this record, we find that this description is sufficient to support the recited controller and controlling.

As to the recited read and write operations, here again we find Patent Owner's cited evidence to be persuasive. Figures 3A–3B describe a method for utilizing NAND flash memory, which includes read and write access operations. *See* Ex. 1001, 6:19–24; Prelim. Resp. 30 (citing Ex. 1001, 4:26–

49, 6:19–57). Based on the record before us, we find these Figures and supporting text are sufficiently detailed as to show that the inventor had possession of the recited read and write operations.

For these reasons, the '612 patent's disclosure "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *See Ariad*, 598 F.3d at 1351.

e. *[1i] "remapping . . . the address space to a different physical range of addresses"*

Petitioner asserts that the term "space" as recited in the term "address space" of limitation 1i is not supported as required by 35 U.S.C. § 112(a). *See* Pet. 34. According to Petitioner, this leaves the "question of how an 'address space' is mapped to a 'physical range,' then remapped to a different one, which in any case is unsupported in those terms." *Id.* at 35. Patent Owner responds that this term is fully supported and directs us to Figures 2A–2B, which it argues describes remapping address space to a different physical range of addresses. Prelim. Resp. 32.

Here again, we are persuaded by Patent Owner's arguments and evidence. As support for the recited remapping an address space to a different physical range of addresses, Figures 2A–2B and the related descriptions in the specification disclose remapping data for an MLC/block to an SLC/block after a failed data integrity test. Ex. 1001, 6:11–18, Figs. 2A–2B; *see* Ex. 2001 ¶¶ 52, 67. Specifically, it states that Figure 2B "shows the quanta of data which failed the data integrity verification check (*see* FIG. 2A) remapped to the next available range of physical addresses within the SIX NAND flash memory module 28, in this example, SLC/block 0." Ex. 1001, 6:11–15. On this record, we are persuaded that this is a sufficient

disclosure to show that the inventor had possession of the recited subject matter.

2. *Claim 3*

a. *"embedding at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements in the at least one controller"*

Claim 3 depends from claim 1 and further recites, in relevant part "embedding at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements in the at least one controller." Ex. 1001, 8:40–43. Petitioner argues that claim 3 lacks proper written description support because "there is no mention of 'elements' in the common specification, much less 'embedding' such 'elements,' or disclosure of any of these 'elements in the device controller." Pet. 35.

Patent Owner directs us to the discussion in the '612 specification of a storage system combining HDD, SLC, and MLC in a single hybrid system. Prelim. Resp. 34 (citing Ex. 1001, 3:60–62). Patent Owner then explains that the '612 patent incorporates by reference the '452 patent. *Id.* (citing Ex. 1001, 1:29–37). Patent Owner points out that the '452 patent "further explains that a non-volatile memory system 'can be combined with . . . ***NAND***, flash chips, ***controllers***, PSRAM's, ***DRAM's***, or other similar functions to offer ***a total 'system-in-package' (SIP) or 'system-on-chip' (SOC)***." *Id.* (quoting Ex. 1004, 4:14–17). Dr. Khatri opines that one of ordinary skill in the art "would understand that these SIP/SOC are 'embedded' systems where the memory (including nonvolatile/volatile memory) is embedded in or with the controller." Ex. 2001 ¶ 58 (citing Ex. 1004, 4:14–17).

On this record, we are persuaded by Patent Owner's argument and evidence. As noted above, we are not persuaded by Petitioner's assertions that the recited "memory element" is unsupported. Further, in the context of the claim, Patent Owner has reasonably explained that one of ordinary skill in the art would have understood the disclosures of the '612 patent to support the recited embedding of memory elements in a controller. On this record, we are persuaded that this is a sufficient disclosure to show that the inventor had possession of the recited subject matter.

E. Asserted Indefiniteness

Petitioner asserts that the challenged claims are indefinite and thus, unpatentable. Pet. 36–42. Patent Owner opposes. Prelim. Resp. 35–49. For the reasons discussed below, Petitioner has not persuaded us of indefiniteness for any of the challenged claims.

1. *"memory element"*

Petitioner contends that a person of ordinary skill in the art would not have understood the term "memory element" and thus, claim 1 and in particular steps 1e, 1f, and 1h of the "maintaining an address table … for memory elements" are indefinite. Pet. 39. Dr. Sechen supports Petitioner by opining that there is no support for the term "memory element" and that "element" is a broad term susceptible to a number of meanings. Ex. 1002 ¶¶ 74, 84.

Patent Owner responds by asserting that "there is nothing confusing or indefinite about 'memory element.' A [person of ordinary skill in the art] would have readily understood that a 'memory element' is simply an element of memory." Prelim. Resp. 44 (citing Ex. 2001 ¶¶ 80–85). Patent Owner further provides evidence of the usage of the term. *See* Prelim. Resp.

44–45 (citing Ex. 1001, 1:29–37, Ex. 2012, 2:52–54, Ex. 2011 ¶ 59, Ex. 2014 ¶¶ 9, 17–20, Ex. 2013, 312).

Section 112(b) requires that "[t]he specification [of a patent] shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention." 35 U.S.C. § 112(b). A patent "is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014); *see* USPTO Memorandum on the Approach to Indefiniteness Under 35 U.S.C. § 112 in AIA Post-Grant Proceedings (Jan. 6, 2021).[3] Thus, our task is to ascertain whether one of ordinary skill in the art would have understood the scope of the claims with reasonable certainty.

On the record before us, we find that one of ordinary skill in the art would have understood the scope of the term "memory element" and we agree with Patent Owner that the term "memory element" has a "well understood" meaning to an ordinarily skilled artisan. Prelim. Resp. 44–45; *see* Ex. 1001, 1:29–37, Ex. 2012, 2:52–54, Ex. 2011 ¶ 59, Ex. 2014 ¶¶ 9, 17–20, Ex. 2013, 312. For example, the Oxford Dictionary of Computing defines "memory element" as a "device that stores one item of information." Ex. 2013, 312.

As for Petitioner's contention concerning ambiguity because "memory element" may refer to "a cell, a block or something else less than a

[3] *Available at* https://www.uspto.gov/sites/default/files/documents/IndefinitenessMemo.pdf

memory or memory module," we note that claim "breadth is not indefiniteness." *See BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1367 (Fed. Cir. 2017).

For all of the foregoing reasons, Petitioner has not met its burden to demonstrate the indefiniteness of the disputed claim language.

2. *[1a] "maintaining an address table for a memory space containing volatile memory and nonvolatile memory space"*

Petitioner argues that the phrase "maintaining an address table for a memory space containing volatile memory and nonvolatile memory space" is indefinite because the term "memory space" is unclear as to whether it refers to logical or physical memory and thus, is unpatentable under 35 U.S.C. § 112(b). Pet. 37. Petitioner contends that "[i]t is further indefinite by including a description of the object (address table) using mismatched concepts of MLC and SLC memory 'spaces' and nonvolatile 'memory' and 'memory element.'" *Id.*

Patent Owner responds by pointing out that "claim 1 of the Challenged Patent requires that memory space be 'associated' with physical memory elements and that non-volatile memory space 'includes both multi-level cell (MLC) space and single level cell (SLC) space.'" Prelim. Resp. 35 (citing Ex. 1001, 7:43–48, 8:1–3). Dr. Khatri also opines that an ordinarily skill artisan "would have understood that 'memory space' simply refers to where data is stored. Data could be stored in a volatile memory space. Data could also be stored in a non-volatile memory space." Ex. 2001 ¶ 60.

We are not persuaded by Petitioner's arguments. Claim 1 recites "nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space and the volatile memory includes a random access volatile memory element." Ex. 1001, 7:45–48. First, as noted above

we are not persuaded by Petitioner's indefiniteness argument concerning the term "memory element." As to the term "memory space," on the record before us, we agree with Dr. Khatri's opinion that a person of ordinary skill in the art "reading the claim language, in light of the specification and prosecution history, would have readily understood what is meant by 'memory space.'" Ex. 2001 ¶ 60. Further, as Patent Owner correctly asserts, "the surrounding claim language specifies that data may be stored in memory elements, and these memory elements may be mapped into the memory space." *See* Ex. 1001, 7:33–36; Prelim. Resp. 36.

Additionally, the '612 patent discloses that the "total non-volatile memory storage space=MLC+SLC." Prelim. Resp. 36 (citing Ex. 1001, 5:25). On the record before us, we are persuaded that an ordinarily skilled artisan would have understood that disclosure to mean that "the 'memory storage space' refers to the total amount of space where data can be stored in a given memory, and the 'memory space' refers to where data is stored." Ex. 2001 ¶ 62.

Also, as Patent Owner points out, a patent application published in 2007 and assigned to Petitioner uses "memory space" to refer to "the 'addressable locations' where data is stored." Prelim. Resp. 36–37 (citing Ex. 2007 ¶ 7). Further, a 2010 textbook titled "Inside NAND Flash Memories" and the Declaration of Dr. David Liu from IPR2021-01550 also indicate that "memory space" refers to where data is stored. *Id.* (citing Ex. 2003, 485, 493; Ex. 2011 ¶ 63). We find this evidence to be sufficient to show that Petitioner has not met its burden to show an improper lack of clarity as to this phrase.

As for Petitioner's contention concerning ambiguity because "memory space" may refer to something "logical" or something "physical," even if the challenged claims encompassed "logical" memory as well as "physical" memory, claim "breadth is not indefiniteness." *See BASF*, 875 F.3d at 1367. As such, the potential breadth of this term is not equivalent to indefiniteness of this term and thus, is not a sufficient basis to establish unpatentability under 35 U.S.C. § 112(b).

For all of the foregoing reasons, Petitioner has not met its burden to demonstrate the indefiniteness of the disputed claim language.

3. *[1b2] "the mapping is performed as necessitated by the system to maximize lifetime"*

Petitioner argues that "there are multiple axes of uncertainty in the claim 1 recitation of 'mapping . . . as necessitated by the system to maximize lifetime.'" Pet. 38. Specifically, Petitioner contends it is unclear what mapping is implicated. *Id.* According to Petitioner, this is true because every mapping if following by writing would decrease the expected lifetime. *Id.* "Claim 1 (and particularly the 'maximize lifetime' clause) fails to specify any user-elected strategy/configuration of NAND flash mapping to distribute wear (stress)." *Id.*

In response, Patent Owner states that the '612 patent "discloses increasing the 'reliability and lifetime' of the memory, and the specification is replete with examples of how to do this." Prelim. Resp. 38 (citing Ex. 1001, 1:41–48). Specifically, a person of ordinary skill in the art "reading the specification would have understood that this term refers to transferring data from MLC to SLC, or from heavily used MLC to less used MLC, in order to prolong or otherwise boost the lifetime of the memory." *Id.* (citing Ex. 2001 ¶ 66).

Here again, we are persuaded by Patent Owner's argument and evidence. Dr. Khatri opines that "the main purpose of the 612 Patent is to increase the reliability and endurance (lifetime) of the memory, and the specification is replete with examples of how to do this." Ex. 2001 ¶ 66. In this vein, Patent Owner directs us to the '612 patent's Figures 2A–2B and 3A–3B, which show how "data is remapped to boost or prolong the lifetime of the system." Prelim. Resp. 38. Further evidence is found in Figures 2A–2B and the related descriptions in the specification, which disclose remapping data for an MLC/block to an SLC/block after a failed data integrity test. Ex. 1001, 5:67–6:3, 6:10–18, Figs. 2A–2B; *see* Ex. 2001 ¶ 66. In addition, Figures 3A–3B depict "a method for utilizing a NAND flash memory system" that transfers valid data to SLC NAND flash memory after a failed data integrity test. Ex. 1001, 6:19–20, 6:52–57, 6:58–7:3, Figs. 3A–3B; *see* Ex. 2001 ¶ 68.

In addition, the '612 patent discloses various wear-leveling techniques for transferring data to less-used blocks or higher-performance blocks including (1) "select[ing] an available target block with the lowest overall erase count" and (2) remapping from MLC NAND flash memory to SLC NAND flash memory. Ex. 1001, 3:26–30, 5:65–6:3; *see* Ex. 2001 ¶¶ 66, 86. According to the '612 patent, remapping from MLC NAND flash memory to SLC NAND flash may include allocating "hot" blocks (those blocks that receive frequent writes) to SLC NAND flash memory and allocating "cold" blocks (those blocks that only receive infrequent writes) to MLC NAND flash memory. Ex. 1001, 6:58–64.

The wear-leveling techniques disclosed in the '612 patent boost or prolong lifetime such that "the lifetime of the memory is maximized," e.g.,

by repeatedly performing one or more of them. *See* Ex. 2001 ¶¶ 66, 86; Ex. 1001, 3:19–26, 4:23–26, 5:20–22, code (57). Moreover, an ordinarily skilled artisan would have understood that "the lifetime of the system is maximized by transferring data to blocks with higher endurance, whether it is a block that is less-used, or a higher-performance block," as the patent discloses. Ex. 2001 ¶ 86.

For all of the foregoing reasons, Petitioner has not met its burden to demonstrate the indefiniteness of the disputed claim language.

4. *[1c] "controlling during Write access operations and Read access operations a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element and at least one SLC memory module including at least one SLC nonvolatile memory element and associated memory space using at least one controller"*

Petitioner asserts that limitation 1c "is in essence a step for a vague function of 'controlling' undefined 'Write access operations and Read access operations' among undefined 'memory element[s]' and 'associated memory space' using and [sic] undefined 'at least one controller.'" Pet. 39. Petitioner directs us to 35 U.S.C. § 112(f) and indicates that "a functionally claimed limitation of a general term ('nonce' word) which is not supported in the specification" is indefinite. *Id.* Petitioner's argument, however, is not well developed. Our understanding of the Petitioner's assertion is that "controlling" is, in their view, a vague nonce word and the specification lacks the required structure to support a means-plus-function term. This argument, however, is unavailing.

Patent Owner correctly points out that Petitioner has not provided argument or evidence sufficient to overcome the presumption that this is not a means-plus-function term. *See* Prelim. Resp. 39–40. The Federal Circuit

has held that there is a presumption, albeit not a strong presumption but a presumption nonetheless, that § 112(f) does not apply to a claim term that does not recite the word "means" unless "the challenger demonstrates that the claim term fails to 'recite sufficiently definite structure' or else recites 'function without reciting sufficient structure for performing that function.'" *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015). Petitioner's brief argument does not meet that burden because it lacks sufficient explanation as to why we should view "controlling" or "controller" as lacking the requisite structure.

Patent Owner, on the other hand, argues that the "specification repeatedly refers to controllers as known devices that face specific challenges or perform specific tasks." Prelim. Resp. 41(citing Ex. 1001, 2:43–50, 3:11–17, 3:21–33). Further, a person of ordinary skill in the art "would have understood the 'controller' to be a component that uses firmware to 'control' or 'manage' the data flow to and from the memory." *Id.* at 42 (citing Ex. 2001 ¶ 74). Patent Owner also provides us with evidence of technical dictionaries and textbooks to support its assertion that a controller had a known structure. *Id.* (citing Ex. 2015, 128, Ex. 2008, 39–40).

We find Patent Owner's argument and evidence to be persuasive and based on the record before us, we find that the terms "controller" and "controlling" are supported in the specification such that terms have a sufficient structure for performing the recited functions. Petitioner has not made a sufficient case to overcome the presumption against the application of 35 U.S.C. § 112(f), nor has Petitioner shown that one of ordinary skill in the art would have lacked clarity as to structure of a controller or the

function of controlling. For all of the foregoing reasons, Petitioner has not met its burden to demonstrate the indefiniteness of the disputed claim language.

5. *[1h] "performing a data integrity test on the stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules [1h1] after at least a Write access operation performed thereon"*

Petitioner argues that claim limitation 1h is unclear as to when a data integrity test must be performed and as such, claim 1 is unpatentable as indefinite. Pet. 40–41. As Petitioner notes, the '612 specification states that "[a]fter each write to an address within a particular address range, the device controller 14 will-***as time permits***-perform a read on the address range to ensure the integrity of the written data." Ex. 1001, 5:64–67 (emphasis added); *see also* Pet. 40 (quoting a portion of that language). Petitioner states that the claim is silent as to when the data integrity test must be performed and thus, the permissive language in the specification would have left the person of ordinary skill in the art unclear as to when a test would be performed. Pet. 40–41.

In response, Patent Owner argues that the language is clear. Prelim. Resp. 46–47. According to Patent Owner, "a [person of ordinary skill in the art] would have readily understood that data integrity tests performed after every Write access operation, or only after some Write access operations, to be within the scope of claim 1." *Id.* at 46 (citing Ex. 2001 ¶ 86). Patent Owner contends that claim 1 merely requires that the controller perform a data integrity test after a write access and that this is explained in the specification. *Id.* at 46–47 (citing Ex. 1001, 5:17–18, 5:64–67).

We have reviewed the arguments and evidence provided and based upon the record before us, we agree with Patent Owner that an ordinarily skilled artisan would understand that claim 1 encompasses "data integrity tests performed after every Write access operation" or only "after some Write access operations." *See* Ex. 1001, 5:17–18, 5:64–67; Ex. 2001 ¶ 86; Prelim. Resp. 46–47. Here again, Petitioner's arguments concerning uncertainty confuse "breadth with indefiniteness" and as we have noted above breadth does not equate to indefiniteness. *See BASF*, 875 F.3d at 1367.

6. *[1h3] "comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements"*

Petitioner argues that the phrase, "comparing the stored data **in** the controller memory **in** the given one of the MLC nonvolatile memory elements" is indefinite due to an unclear usage of the term "in." Pet. 41. According to Petitioner, "[t]he grammatical ambiguity of the referent of the preposition 'in' leaves ambiguous whether the stored data is in the controller memory or the MLC memory." *Id.* (citing Ex. 1002 ¶ 86.) That is the entirety of Petitioner's argument on this point. Dr. Sechen's declaration testimony is cited as support, but that testimony does not add any further depth to the argument. *See* Ex. 1002 ¶ 86.

Patent Owner notes that this "cursory argument … fails to explain how this limitation is indefinite." Prelim. Resp. 47. Patent Owner then asserts that "a [person of ordinary skill in the art] would have understood that this limitation refers to 'stored data' which is stored in the controller memory after being read from the MLC nonvolatile memory." *Id*. at 48 (citing Ex. 2001 ¶ 87).

On the record before us, we do not find Petitioner's argument to be persuasive. Claim 1 recites performing a data integrity test on data stored in an MLC memory element and reading the stored data to controller memory. Ex. 1001, 8:18–24. Thus, based on the record before us, we agree with Patent Owner that an ordinarily skilled artisan would have understood this limitation to be directed to data stored in the controller memory after being read from the MLC nonvolatile memory. Prelim. Resp. 48. As such, Petitioner has not met its burden to demonstrate the indefiniteness of the disputed claim language.

7. *[1i] "remapping . . . the address space to a different physical range of addresses"*

As to limitation 1i, Petitioner argues that one of ordinary skill in the art would not have understood how an address space gets mapped to a physical range and then remapped to a different physical range. Pet. 41–42. Petitioner asserts that "space" and "address space" are ambiguous. *Id.* (citing Ex. 1002 ¶ 27). According to Petitioner, "there is lack of clarity whether 'space' is a quantity of space, is 'logical' space as a list of assigned logical 'sectors' conforming to hard disk drive operation or the physical locations in flash memory." *Id.* at 42.

Patent Owner responds by arguing that "the Challenged Patent provides clear guidance regarding how this remapping may be performed." Prelim. Resp. 49. Patent Owner directs us to evidence in the '612 patent and testimony from Dr. Khatri.

We find Patent Owner's showing to be persuasive. In particular, Patent Owner directs us to Figures 2A and 2B, which "describe remapping address space to a different physical range of addresses—namely, remapping the 'physical address range' of 'MLC/Block 2' to the "physical address

range" of 'SLC/Block 0'" after a failed data integrity test. *Id.* (citing Ex. 1001, Figs. 2A–2B; *see also id.* at 6:4–18, 6:52–57). Specifically, the '612 specification states that Figure 2B "shows the quanta of data which failed the data integrity verification check (see FIG. 2A) remapped to the next available range of physical addresses within the SIX NAND flash memory module 28, in this example, SLC/block 0." Ex. 1001, 6:11–15.

Thus, based on the record before us, we agree with Patent Owner that an ordinarily skilled artisan would have understood this limitation to be directed to remapping a physical address range to another physical address range. *Id.* at 49. As such, Petitioner has not met its burden to demonstrate the indefiniteness of the disputed claim language.

F. Asserted Obviousness over Gavens and Knowledge of a POSITA

Petitioner asserts that claims 1–6 would have been unpatentable as obvious over Gavens and the knowledge of a POSITA. Pet. 42–75. Patent Owner opposes. Prelim. Resp. 49–62, 68–84. On this record, we determine that Petitioner has not established that it is more likely than not that it would prevail in showing the challenged claims are unpatentable as obvious over Gavens and the knowledge of a POSITA.

1. *Overview of the Asserted Prior Art*

a. *Gavens*

Gavens is a U.S. patent titled "Non-Volatile Memory and Method with Accelerated Post-Write Read to Manage Errors." Ex. 1045, codes (12, 54). Gavens states that it incorporates by reference numerous patent applications and patents, including Chen, Gorobets, Lee, and Paley. *See, e.g., id.* at 8:40–43, 14:37–40, 16:38–40, 17:4–6, 17:65–67, 20:53–59.

Gavens "relates to the operation of re-programmable non-volatile memory systems such as semiconductor flash memory, and, more specifically, to handling and efficient managing of errors in memory operations." *Id.* at code (54), 1:16–20. Gavens explains that "the integrity of the data being stored is maintained by use of an error correction technique." *Id.* at 3:28–30. "Most commonly, an error correction code (ECC) is calculated for each sector or other unit of data that is being stored at one time, and that ECC is stored along with the data." *Id.* at 3:30–33. Typically, an ECC relates to "a unit group of user data," such as "a sector or a multi-sector page." *Id.* at 3:33–36. "When this data is read from the memory, the ECC is used to determine the integrity of the user data being read." *Id.* at 3:36–38.

Gavens also explains that as "the flash memory ages, its error rate increases rapidly" near the memory's end of life. *Id.* at 3:56–57. Using an "ECC to correct a worst-case number of error bits" near the memory's end of life "consume[s] a great amount processing time," and the memory's performance will degrade. *Id.* at 3:60–63. Gavens identifies "a need to provide a nonvolatile memory of high storage capacity without the need for a resource-intensive ECC over designed for the worse-case." *Id.* at 4:3–5. To address that need, Gavens discloses adaptively rewriting data from a higher-density memory portion to a lower-error-rate memory portion to control error rate. *See, e.g., id.* at 4:9–5:30, 16:14–19:24, code (57), Figs. 14A–14B, 15, 16A–16C, 17.

For example, "a flash memory having an array of memory cells is configured with a first portion and a second portion." *Id.* at 4:14–16, code (57). The "first portion operat[es] with less error but of lower density

storage." *Id.* at code (57). The "second portion operat[es] with a higher density but less robust storage." *Id.* Initially, the data "is written to the second portion for efficient storage." *Id.* at 4:18–19. Then, the data "is read back in a post-write read operation to check for excessive error bits." *Id.* at 4:19–21. "If the error bits exceeded a predetermined amount, the data is rewritten or kept at the less error-prone first portion." *Id.* at 4:21–22. This arrangement "allows a smaller and more efficient error correction code ('ECC') to be designed for correcting a smaller number of errors bits, thereby improving the performance and reducing the cost of the memory." *Id.* at 4:28–31.

Figure 1 of Gavens is reproduced below.

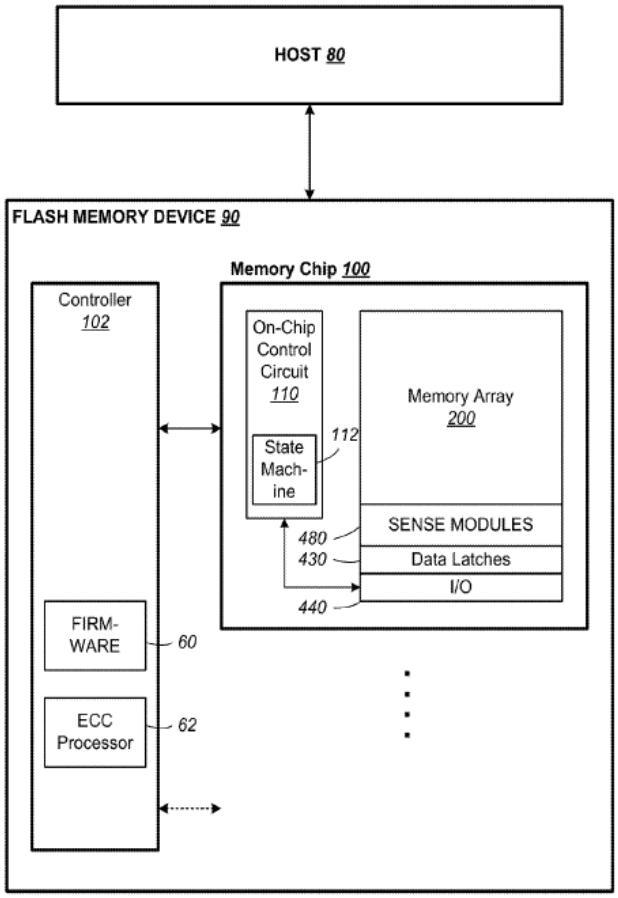

FIG. 1

Figure 1 of Gavens shows host 80 in communication with memory device 90. *Id.* at 8:13–17. Memory device 90 includes at least one memory chip 100. *Id.* at 8:17–18. Memory chip 100 includes memory array 200 of memory cells that are capable of being configured as multi-level cells (MLC) storing multiple bits of data. *Id.* at 8:18–21. Controller 102 controls and manages memory operations for memory chip 100. *Id.* at 8:32–33. Error correction code (ECC) processor 62 processes ECC during operations of memory device 90. *Id.* at 8:45–47.

In a preferred embodiment, the "first portion has each memory cell storing one bit of data," and the "second portion has each memory cell

storing more than one bit of data." *Id.* at 4:32–34. For instance, the "less error-prone [first] portion has each memory cell storing 1 bit of data," and the "high density storage [second] portion of the memory has each memory cell storing 3 bits of data." *Id.* at 5:15–17; *see id.* at 16:22–24.

Gavens's Figure 14B (reproduced below) depicts an array of memory cells configured with a first portion and a second portion:

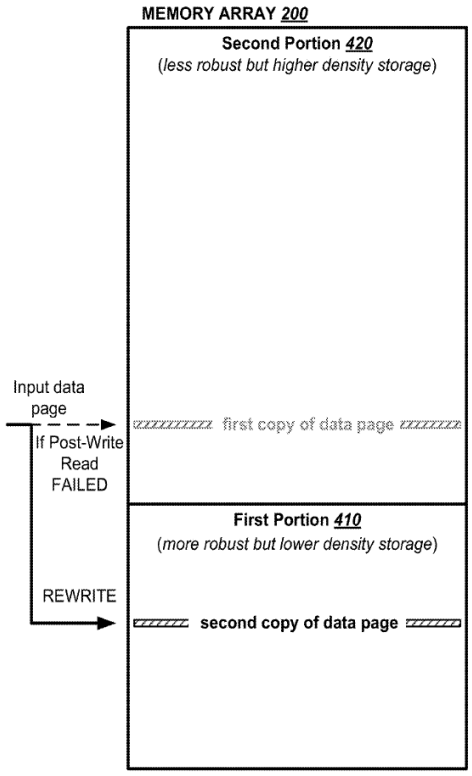

FIG. 14B

Figure 14B illustrates memory array 200 "partitioned into a first portion 410 and a second portion 420." *Id.* at 16:14–17, 17:7–8, Fig. 14B. "The first portion 410 has the memory cells configured as lower density storage with each cell storing less number of bits than that of the second portion." *Id.* at 16:19–22. "The second portion 420 has the memory cells configured as high density storage with each cell storing multiple bits of data." *Id.* at 16:17–19.

Memory array 200 is a flash memory, i.e., a non-volatile memory. *Id.* at 1:18–19, 1:27–28, 4:13–16, 9:36–40, 11:14–18, 17:24–29, 17:41–42.

Preferably, a page of incoming data "to be written to the memory array 200" is "stored in the high density second portion for the sake of efficiency and high capacity." Ex. 1045, 16:41–43. Thus, "a first copy of the data page is written to the second portion." *Id.* at 16:44–45. Then, "the first copy of the data page is read back" in a post-write read operation "to determine if there are any errors." *Id.* at 16:46–47.

If "the number of error bits does not exceed the predetermined amount, the first copy is regarded stored in the second portion [and] is deemed valid." Ex. 1045, 16:51–54. If the post-write read operation, however, detects that "the number of error bits in the data page has exceeded the predetermined amount, a second copy of the data page is rewritten to the first portion." *Id.* at 17:9–11. Figure 14B shows "a rewrite of a second copy of the data page into the first portion of the memory array." *Id.* at 17:7–8, Fig. 14B.

After "the second copy has been written to the first portion, it will replace the first copy in the second portion as the valid copy." *Id.* at 17:15–17. Then, the "first copy will become obsolete," and "a directory in a block management system" will be "updated to direct subsequent access to the second copy." *Id.* at 17:17–20.

2. *Independent Claim 1*

Petitioner asserts that claim 1 would have been obvious over Gavens in view of the knowledge of one of ordinary skill in the art. *See* Pet. 44–69. For the reasons stated below, we are not persuaded by Petitioner's challenge.

Limitation 1a of claim 1 recites "maintaining ***an address table*** for a memory space containing ***volatile memory*** and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space ***and the volatile memory includes a random access volatile memory element***." Ex. 1001, 7:43–48 (emphasis added). Thus, the claim requires an address table for a memory space that has both volatile and non-volatile memory. We are not persuaded by Petitioner's argument and evidence regarding the recited address table or volatile memory.

As to the address table, Petitioner makes no express allegations regarding the address table in its argument regarding limitation 1a. *See* Pet. 45–47; *see also* Prelim. Resp. 68 ("Notably, the Petition's discussion of limitation [1a] fails to address the 'address table' altogether."). In its discussion of limitation 1b, Petitioner states that "Gavens discloses the address table maps logical and physical addresses adaptable to the system." *Id.* at 48. Petitioner appears to point to Gavens's directory as the recited address table. *Id.* There, however, is no cite to any portion of Gavens in either the Petition or Dr. Sechen's declaration that would direct us to what disclosure from Gavens should be applied to the recited address table. *See* Pet. 45–48, Ex. 1002 ¶¶ 97–101. It is not our place to scour Gavens to find an appropriate disclosure and as such, we find that Petitioner has not adequately shown that Gavens would have taught or suggested the recited address table.

As to the recited nonvolatile memory, Petitioner argues that "Gavens discloses memory containing volatile RAM and nonvolatile memory array." Pet. 45 (citing Ex. 1045, 1:18, 26, Fig. 1 (memory array 200 in memory chip

100)). Petitioner also directs us to Gorobets, which is incorporated by reference in Gavens. *Id.* at 45–46. According to Petitioner, Gorobets "explicitly discloses volatile RAM." *Id.* (citing Ex. 1049 ¶ 130, Fig. 20). Petitioner further asserts that "[t]he volatile RAM disclosed by Gorobets necessarily includes random access volatile memory elements." *Id.* at 46.

We are not persuaded by Petitioner's showing. First, Gaven's invention is directed specifically to non-volatile memory. The focus of Gavens is "the operation of re-programmable non-volatile memory systems such as semiconductor flash memory, and, more specifically, to handling and efficient managing of errors in memory operations." *Id.* at code (54), 1:16–20. As Dr. Khatri notes, "the only time that Gavens mentions RAM is in the 'Background of the Invention,' when Gavens is distinguishing its purported invention from RAM." Ex. 2001 ¶ 106. Petitioner directs us to Gavens's memory array 200, but as Dr. Khatri notes "there is no mention of RAM in the memory chip 100, controller chip 102, or anywhere else in the flash memory device 90." *Id.* Patent Owner correctly points out that "Figure 1 depicts a 'Flash Memory Device' including a 'Memory Array 200.' Memory array 200 is 'flash memory.'" Prelim. Resp. 70 (citing Ex. 1045, 4:13–16). As such, we are not persuaded that one of ordinary skill in the art would have found Gavens to teach or suggest the recited volatile memory that includes RAM.

Petitioner also direct us to Gorobets, which is incorporated by reference in Gavens. Pet. 45–46, 43 n.10[4] (citing Ex. 1045, 20:53–59). Gorobets is a US Patent Publication titled "Maintaining Updates of Multi-

[4] Petitioner references Exhibit 1044 in the footnote. That, however, appears to be a typographical error and should be a reference to Exhibit 1049.

level Non-Volatile Memory in Binary Non-Volatile Memory." Ex. 1049, code (54). Gorobets is directed to "the operation of re-programable non-volatile memory systems such as semiconductor flash memory, and more specifically to the management of the interface between a host device and the memory." *Id.* ¶ 2.

Petitioner specifically directs us to paragraph 130 of Gorobets, which discusses Figure 20 of Gorobets and states "Data is transferred from a host 510 onto memory 503, where it is initially stored on the volatile buffer memory RAM 511, which is typically part of the controller. From RAM 513 the data is them written into the non-volatile memory 513." Ex. 1049 ¶ 130. Petitioner, however, does not explain how Gorobets's teaching of RAM 511 is to be applied to the teachings of Gavens. *See* Prelim. Resp. 69 ("Petitioner fails to show how Gorobets's RAM-based buffer applies to or can be combined with Gavens."). In particular, it is unclear how Petitioner alleges that the teaching of RAM 511 should be applied in regards to Gavens in a manner that would teach or suggest an address table that contains both volatile and non-volatile memory. As Patent Owner correctly notes, "Petitioner also does not state whether Gorobets's 'RAM' is being used to modify Gavens's system, and why a POSA would have made any modification." *See* Prelim. Resp. 73. Petitioner's declarant, Dr. Sechen, does not provide testimony that further illuminates Petitioner's argument. *See* Ex. 1003 ¶ 98.

Petitioner also references Gorobets's disclosure of RAM 130 and RAM 102. Pet. 47 (citing Ex. 1049 ¶¶ 18, 56, 109). The Petition, however, contains no discussion of these portions of Gorobets beyond a bare citation and a statement that they "are understood by a [person of ordinary skill in

the art] to be consistent with the system disclosed in Gavens." *Id.*; *see also* Prelim. Resp. 72 (arguing that Petitioner does not explain the application of these teachings). Petitioner's declarant, Dr. Sechen, does not provide testimony that further illuminates Petitioner's argument. *See* Ex. 1003 ¶ 99. "[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). As such, it is insufficient to show merely that volatile memory was known in the art, but rather Petitioner was tasked with establishing that the recited address table containing volatile and non-volatile memory would have been obvious over the cited reference. We find that Petitioner has not provided sufficient explanation or argument to support its assertion that Gavens in light of Gorobets would have taught limitation 1a.

Petitioner's allegations also fall short as to limitation 1d which states "storing received data within a controller memory associated with the at least one controller." Ex. 1001, 8:5–6. First, Petitioner contends that Gavens "discloses a first section 411 for caching in first portion 410" and states that "first section 411 is used as a cache to temporarily store data that will be written permanently to the second portion (which corresponds to MLC)." Pet. 54 (citing Ex. 1045, Fig. 16A). Petitioner then directs us to Gorobets to teach "the step of storing received data within a controller memory (*e.g.*, RAM 511)." *Id.* (citing Ex. 1049, Fig. 20, ¶ 130). Petitioner cites the portions of Gorobets that discuss RAM 511, RAM 130, and RAM 102. *Id.* These are the same RAM memories cited above as to limitation 1a's volatile memory. Here again, Petitioner does not explain the relationship between Gorobets's RAM and the disclosures of Gavens. *See*

Prelim. Resp. 77–78. As Patent Owner argues, "[n]otwithstanding, Gavens and Gorobets are different references, and describe different embodiments. Petitioner, however, provides no explanation how the distinct disclosure of Gorobets ("RAM 511") applies to or can be combined with the previously cited disclosure of Gavens ('first section 411' of Figure 16A)." *Id.* at 78.

Incorporation by reference does not relieve Petitioner of its burden to explain how these teachings are to be applied and why one of ordinary skill in the art would have learned of the recited limitation from the cited material. Petitioner and its declarant do not provide an explanation as to how one of ordinary skill in the art would have viewed these teachings and why that would have taught or suggested the disputed limitation. *See generally* Ex. 1002 ¶¶ 112–113. As such, we find that Petitioner has not met its burden to show that Gavens in light of Gorobets would have rendered obvious limitation 1d.

Finally, as to limitation 1h2, Petitioner provides us with an unexplained inconsistency in its allegations. Limitation 1h2 recites "reading the stored data to the controller memory." Ex. 1001, 8:23. Thus, limitation 1d recites "a controller memory," and limitation 1h2 recites "the controller memory," which based on antecedent basis, would indicate that both limitations are referring to the same controller memory. *See Wi-Lan, Inc. v. Apple, Inc.,* 811 F.3d 455, 462 (Fed. Cir. 2016) (citing *Baldwin Graphic Sys., Inc. v. Siebert, Inc*., 512 F.3d 1338, 1342 (Fed. Cir. 2008) ("Subsequent use of the definite articles 'the' or 'said' in a claim refers back to the same term recited earlier in the claim.")). Petitioner does not present us with argument or evidence to challenge the use of that general principle in this specific case. *Microprocessor Enhancement Corp. v. Texas Instruments*

Inc., 520 F.3d 1367, 1375 (Fed. Cir. 2008) (Petitioner could have overcome that principle because it is not a bright line rule and "mere use of a term with an antecedent does not require that both terms have the same meaning.").

As such it is unclear why Petitioner would direct us to Gorobets's RAM 511 in its challenge to limitation 1d, but point us to Gavens's data latches in its challenge to limitation 1h2. *Compare* Pet. 54 ("Gorobets '912 [Ex. 1049], incorporated by Gavens, discloses the step of storing received data within a controller memory (e.g., RAM 511)") *with* Pet. 62 ("Gavens also discloses reading the stored data to the controller memory. (Fig. 15 ref. 520, col. 17:32–33: Reading the first copy from the second portion; 4:55–60: The first copy in the second portion and the cached copy in the first portion are loaded into a set of data laches [sic] on an integrated circuit chip and compared to check for error bits."). Patent Owner argues that "Petitioner cannot switch between which 'controller memory' it is purporting to rely on for different limitations of the same claim." Prelim. Resp. 83.

Petitioner fails to provide an explanation for this inconsistency. In its challenge to limitation 1d, Petitioner directs us to Gavens's first section 411 in the first portion 410 as caching data and then directs us to Gorobets's RAM 511 as storing the received data in controller memory. *See* Pet. 54. As discussed above, Petitioner's allegations regarding limitation 1d are not sufficiently articulated, but that issue is only compounded in the challenge to limitation 1h2 which is directed to the same controller memory recited in limitation 1d. The allegations directed to 1h2, however, indicate that Petitioner is relying on loading data into data latches on an integrated circuit. Petitioner lacks a clear explanation as to how these teachings are related or

how they collectively teach or suggest the recited controller memory. As such, we are not persuaded by Petitioner's showing for limitation 1h2.

Based on the record before us, we are not persuaded that Petitioner has met its burden to show that claim 1 would have been obvious over Gavens.

3. *Dependent Claims 2–6*

Petitioner contends that dependent claims 2–6 would have been obvious over Gavens and the knowledge of one of ordinary skill in the art. *See* Pet. 69–75. Claims 2–6 depend directly from claim 1. Ex. 1001, 8:35–50. As noted above, however, Petitioner does not establish sufficiently for purposes of institution that claim 1 would have been obvious over the cited art. Petitioner's contentions regarding claims 2–6 do not remedy the deficiencies in Petitioner's arguments as to claim 1. Thus, claims 2–6 have not been shown to be unpatentable under § 103 because the claims would have been obvious over Gavens in view of an ordinarily skilled artisan's knowledge.

IV. CONCLUSION

For the foregoing reasons, we determine that the information presented in the petition fails to demonstrate that it is more likely than not that at least one of the challenged claims is unpatentable. Accordingly, we do not institute a post-grant review of claims 1–6 of the '612 patent.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that no post-grant review is instituted.

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