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A simple two-step phosphorus doping process for shallow junctions by applying a controlled adsorption and a diffusion in an oxidising ambient

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Abstract

A simple phosphorus doping technique for shallow junctions is presented. The low pressure doping process was carried out in a single RTP reactor chamber by using a two-step process: a controlled adsorption of phosphorus on the silicon surface and a rapid thermal diffusion in an oxidising ambient without the deposition of an oxide capping layer. A low concentration of 50vpm phosphine diluted in hydrogen allowed a sufficient phosphorus supply while the deposition of phosphorus on the reactor walls was insignificant. The

phosphine decomposed on the clean silicon surface at a temperature of 550°C, at which the silicon surface is saturated by the adsorbed phosphorus. The shallow junctions were defined by successive rapid thermal annealing at temperatures above the adsorption temperature. An oxygen pressure of 4.2×10^3 Pa during the annealing prevented the phosphorus from desorption. Therefore, a deposition of an additional oxide-capping layer was not necessary, allowing more simple processing. This doping method provides shallow junctions of depths below 100 nm with sheet resistances below 1000 Ω/sq.

Introduction

The progressive development of CMOS-Technology requires a continual shrinking of the device structures with an ever-increasing complexity. Therefore, there is an ongoing process in stretching the limits of manufacturability to find solutions for the increasing demands in precision, reliability and efficiency. One of the important demands for the increase of the performance of sub-100 nm MOSFETs for the USLI technology is the need of shallow source/drain extension junctions to suppress the short channel effects (SCE) while maintaining a low parasitic series resistance. The introduction of dopants by low energy ion implantation is widely used to tackle these challenges. However, not all the problems connected to the implantation have finally been solved. Crystal damage and channelling and the transient enhanced diffusion (TED) during the high temperature annealing for the activation of the dopants do still not make the requirements for the shallow junctions easy to meet. Additionally, the doping of trenches for next generation memory devices can hardly be carried out by ion implantation because of shadowing effects of these structures. Furthermore, we saw a need for an alternative doping process existing in smaller research laboratories where the implanter facilities are uneconomical. Some alternatives to the ion implantation doping have been studied and are still in the focus of research, such as plasma immersion ion implantation (PII), gas-immersion laser doping (GILD) and vapor phase doping (VPD) (see [1] and citations herein).

We investigated an alternative low pressure rapid thermal doping (RTD) process for the phosphorus doping comparable to the vapor phase doping. Some studies about VPD have been published, e.g. for boron [2], [3], arsenic [4], and phosphorus doping as well [5], [6], [7]. For those experiments, the silicon surface kept at elevated temperatures was exposed to the doping gas allowing the dopant to diffuse directly into the bulk. The conventional vapor phase doping of phosphorus required a considerably higher partial pressure of the phosphine doping gas compared to the VPD of boron with diborane [8] because of an increased thermal desorption of phosphorus at the elevated doping temperatures. The deposition of an additional capping layer is a method to prevent such a desorption. New doping processes sometimes referred to as atomic-layer doping (ALD) were presented for boron doping [9] and arsenic doping [10], applying an oxide capping layer in order to avoid dopant loss from the surface. In this report a similar low pressure doping process is presented, which is composed of the adsorption of phosphorus on the silicon surface and a rapid thermal diffusion in an oxidising ambient without the deposition of an oxide capping layer.

Section snippets

Experimental

The substrates used for all the doping experiments were p-type boron-doped 150mm diameter silicon wafers (100) with a resistivity of about 10Ωcm. Initially, the wafers were cleaned by a conventional chemical etch procedure, a Caro etch at 120°C for 5min and a HF dip. They were rinsed in de-ionized water and spin dried in a N_2-atmosphere at elevated temperature. Immediately after the cleaning, the wafers were loaded into a load lock chamber that was evacuated subsequently. All the handling and…

Conventional vapor phase doping with phosphorus

The first doping experiments were carried out in a nitrogen-containing atmosphere by using the phosphine-rich gas diluted in nitrogen. A mean sheet resistance of 527Ω/sq was achieved for a ramp cycle of 60s ramp-up time to 900°C, a steady state of 30s and a ramp-down for 60s. The doping pressure was 1×10^3 Pa which corresponds to a partial pressure of the phosphine gas of about 100Pa. SIMS measurements of wafer samples revealed maximum concentrations of phosphorus of 1.2×10^{20} cm^{-3}. Sato et al. …

Conclusions

A low pressure phosphorus doping process for shallow junctions in silicon using low-concentration phosphine in hydrogen as doping source was presented. Low phosphine partial pressures of less than 5×10^{-1} Pa were not sufficient for a conventional vapor phase doping because of the high desorption rate of phosphorus at the doping temperature. The required high partial pressures of phosphine of about 100 Pa for those processes resulted in a rapid contamination of the chamber walls with phosphorus.…

Acknowledgements

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Tertiarybutylarsine damage-free thin-film doping and conformal surface coverage of substrate-released horizontal Si nanowires

2020, Applied Surface Science

> *Citation Excerpt :*
> …Another problem with the greater exposure to the perimeter of the 3D devices is when the doping process etches the available surface severely damaging or destroying these devices. Gas-phase doping of silicon has been reported by several groups using various sources [30–40], and our recent work on gas-phase doping of silicon was performed using arsine (AsH_3) gas to dope Si nanowires [41], where suitability for doping was shown. However severe attack of Si nanowires was seen for flowrates of 50 sccm and 250 sccm, while flowrates of 10 sccm and 20 sccm showed moderate etching.…

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> …We found that by such method doped silicon samples showed a characteristic increase of the sheet resistance during the initial surface contact with air, which allows to obtain information of a very close

sub-surface region of the silicon. The doping process of the silicon wafers had been described in detail in previous papers [4,5]. A phosphorus source was deposited on the silicon surface by adsorption of phosphine....

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