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# Integrated Electrochemical Deposition of Copper Metallization for Ultralarge-Scale Integrated Circuits

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An electrochemical deposition process for copper (Cu) metallization has been developed and investigated by the integration of nanoscaled palladium (Pd) catalyzation, electroless plating of Cu seed layers, and electroplating of Cu films in this study. Following surface cleaning and etching, sensitization and activation of $Si/SiO_2/TaN$ substrates were performed to obtain uniformly distributed Pd catalysts of only about 10 nm. Smooth and continuous 30 nm thick Cu seed layers with low electrical resistivity were electrolessly deposited using the nanosized Pd catalysts as nucleation sites. Copper metallization with high purity, small surface roughness, low electrical resistivity of 1.77 $\mu\Omega$ cm, low residual stresses, and good adhesion to substrates was achieved using the subsequent electroplating on the electroless seed layers and postannealing. Good gap-filling capability on finely patterned structures was performed and exhibited the great application potential of low-temperature integrated electrochemical deposition process for next-generation Cu metallization of ultralarge-scale integrated circuits.
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As the packing density of semiconductor devices drastically increases, multilevel interconnection has been applied to compromise the insufficient surface area on integrated circuit (IC) chips. At the same time, the reduction in metal linewidths and pitches results in the rise of interconnect resistance and parasitic capacitance, leading to serious resistance-capacitance (RC) delay.[1,2] The RC delay has many drawbacks, especially the problem of low signal transmission speed, becoming the most difficult issue to overcome. Copper with lower electrical resistivity, high thermal conductivity, good mechanical properties, and high migration resistance has been used as interconnect metallization in dual-damascene structures of ultralarge-scale integrated (ULSI) circuits to replace aluminum and to directly reduce the metal line resistance.[3-5]

Copper metallization technology mainly includes traditional ULSI techniques such as physical vapor deposition (PVD) and chemical vapor deposition (CVD), or newly developed electrochemical deposition including electroplating and electroless plating.[6-23] The PVD method provides precise composition control but presents poor step coverage in deep submicrometer dimension features, resulting in problems like overhangs or voids.[6-8] Though CVD has better step coverage, its development is also limited because high processing temperatures and expensive equipment are required in addition to the combustible and toxic precursors.[9,10] Electroplating has the advantages of low processing temperature, low cost, high throughput, and good film quality, and thus becomes more attractive.[3,11-15] However, due to the need of sputtered Cu seed layers for electroplating, this deposition technique is inadequate for next-generation metallization below 90 nm. Recently, the deposition of uniform Cu seed layers only 20 nm thick into trenches or vias with good sidewall step coverage and a high aspect ratio of 10 has been developed using atomic layer deposition (ALD).[16,17] However, extremely expensive precursors and equipment are required for ALD, and it is still under investigation.

Electroless Cu deposition is a low-cost process of autocatalytic nucleation and growth at low temperatures without the necessity of electric power. It provides good gap-filling capability on finely patterned features and has been intensively studied as seed layers for Cu electroplating.[18-23] One of the most important factors to dominate the success of seed layer deposition is the uniform and nanoscaled catalyzation to activate the inert substrates prior to electroless plating. However, the discontinuity and high electrical resistivity of electroless Cu seed layers up to 6-8 $\mu\Omega$ cm caused by the incorporation of large-sized and high-resistance Pd catalysts renders its application limited, although much research of catalyzation mechanisms has been performed.[19,20,24-28] Hsu *et al.* have also developed several methods for catalyzation and electroless plating to obtain continuous Cu films with low resistivity, but all the thicknesses of Cu films are still too large for them to be used as seed layers for sub-90 nm metallization.[21-23]

Therefore, this paper reports the modified preparation of uniform, nanoscaled Pd catalysts by sensitization-activation of $Si/SiO_2/TaN$ substrates and the following electroless plating of thin, smooth, conformal Cu seed layers using the nanosized catalysts as nucleation sites. The subsequent electroplating was applied using electroless Cu seed layers to accomplish Cu metallization with good quality. A low-temperature and integrated electrochemical deposition process for sub-90 nm Cu metallization is thus proposed and summarized in this study. The microstructures and formation mechanism of Pd catalysts, electroless Cu seed layers, and electroplated Cu films were characterized and analyzed. Their purity, surface roughness, electrical resistivity, residual stresses, adhesion to substrates, and gap-filling capability were also investigated.

## Experimental

Blanket and patterned 150 mm (100) silicon wafers with thermal oxide ($SiO_2$) layers 550 nm thick were used as substrates in this study. For patterned substrates, different features of trenches and damascene structures with various sizes of 0.18-0.35 $\mu$m were formed on the $SiO_2$ layers using standard photolithography and plasma etching processes. Tantalum nitride (TaN) layers 50 nm thick were deposited on these substrates as a diffusion barrier by dc magnetron sputtering. The TaN layers were identified as stoichiometric TaN 1:1 with (111) preferential orientation by Rutherford backscattering spectroscopy (RBS) and X-ray diffractometry (XRD). These $Si/SiO_2/TaN$ substrates were degreased and cleaned in acetone for 10 min under ultrasonic vibration and rinsed in deionized (DI) water after each step to remove residual chemicals.

The cleaned $Si/SiO_2/TaN$ substrates were chemically wet-etched using buffered oxide etchant/nitric acid ($BOE/HNO_3$) and hydrogen fluoride (HF, 10%) solutions at 35°C for 1 min to remove native oxides on TaN surfaces for easy catalyzation and good adhesion of catalysts. The etched substrates were then catalyzed in a sensitization solution composed of tin dichloride ($SnCl_2$, 10 g/L) and hydrogen chloride (HCl, 40 mL/L) at 25°C for 40 s, and then in an activation solution of palladium dichloride ($PdCl_2$, 0.25 g/L) and HCl (2.5 mL/L) at 60-80°C for another 40 s to deposit Pd catalysts.

The catalyzed $Si/SiO_2/TaN$ substrates were electrolessly Cu-deposited in the plating solution listed in Table I at a temperature of 50°C. Some minor surfactants like polyethylene glycol (PEG) were added to reduce the surface tension of plating solution and to improve the gap-filling ability.

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**Table I. Solution composition for electroless Cu plating.**

| Component | Concentration |
|---|---|
| Copper sulfate, $CuSO_4 \cdot 5H_2O$ | 6 g/L |
| Ethylenediaminetetraacetic acid, EDTA | 32 g/L |
| $\alpha,\alpha'$-Dipyridyl, $(C_5H_4N)_2$ | 100 mg/L |
| Potassium ferricyanide, $K_4[Fe(CN)_6]$ | 57.3 mg/L |
| Hydrogen chloride, HCl | 1 mL/L |
| Formaldehyde, HCHO (37%) | 7.5 mL/L |
| Sodium hydroxide, NaOH | pH 12.6 |
| Polyethylene glycol, PEG (200) | 0.5 g/L |
| Polyethylene glycol, PEG (2000) | 0.5 g/L |

Electrolessly deposited Cu films were used as Cu seed layers and subsequently dc electroplated in the solution listed in Table II at 25°C under different current densities. A copper plate of 5 $\times$ 5 $cm^2$ with a purity of 99.95% was set as anode to provide Cu ions. The electroplated Cu films were then annealed at different temperatures in an argon (Ar) atmosphere of 200 mTorr for 30 min.

A scanning electron microscope (SEM; Hitachi S4000) was used to observe the surface morphologies, cross-sectional microstructures, thickness, and gap filling of Pd catalysts and Cu films. The surface morphologies and roughness of as-received, catalyzed, and Cu-deposited substrates were examined by atomic force microscopy (AFM; Digital Instruments NS3a controller with D3100 stage) under a tapping mode. A transmission electron microscope (TEM; JEOL-2000FXII) with energy-dispersive spectrometry (EDS) and selective-area diffraction (SAD) analysis was used to examine the plan-view, cross-sectional microstructures, and composition of the deposited catalysts and Cu films. The depth profiling of the elemental distribution was analyzed by Auger electron spectroscopy (AES; AES670 XI), and RBS was also used to analyze the composition.

The XRD measurement (MAC MXP18 system) with Cu K$\alpha$ radiation (1.5405 Å) and grazing-angle incidence (0.5°) was carried out to characterize the crystalline structure under a scanning speed of 4 °/min. The electrical resistivity of deposited Cu films was measured by a four-point probe method. The adhesion of Cu films to substrates was carried out using an ASTM tape test with 3M Tesa Tape and a peeling load of 500 g. Silicon cantilever beams of 4 $\times$ 0.4 $cm^2$, 140 $\mu$m thick were sputtered with TaN layers of 40 nm thick, Pd-catalyzed, electrolessly plated with 30 nm thick Cu seed layers, and electroplated with 270 nm thick Cu films for stress hysteresis measurement. Curvatures before and after Cu film deposition were measured using a laser ellipsometer to calculate the stress variation during thermal cycles from room temperature to 400°C.

## Results and Discussion

*Catalyzation of $Si/SiO_2/TaN$ substrates.*—The purposes of chemical etching of $Si/SiO_2/TaN$ substrates prior to catalyzation are to remove the native oxides on TaN surfaces and to improve the sensitization and activation. Hence, both uniform removal of native oxides and mildly isotropic etching must be considered for the selection of proper chemical etching. Table III lists the average surface roughness of $Si/SiO_2/TaN$ substrates after different chemical etching conditions obtained by AFM surface scanning. Obviously, different surface morphologies with larger roughness were found after chemical etching. However, severely anisotropic etching by buffered oxide etch (BOE)/$HNO_3$/deionized (DI) water solutions resulted in excessively large roughness up to 2.17 nm from as-received 0.2 nm. Large roughness of the TaN barrier layers result in rough deposition of subsequent Pd catalysts and electroless Cu seed layers, and thus cause inhomogeneous distribution of electric field during Cu electroplating. With decreasing concentration of BOE/$HNO_3$, the roughness still remained at 1.15 nm. Using 10% HF as an etching solution, the roughness was only 0.23 nm, similar to that of the as-received sample and indicating the proper etching condition.

**Table II. Solution composition for Cu electroplating.**

| Component | Concentration |
|---|---|
| Copper sulfate, $CuSO_4 \cdot 5H_2O$ | 30 g/L |
| Sulfuric acid, $H_2SO_4$ | 90 g/L |
| Hydrogen chloride, HCl | 0.1 mL/L |
| 2-Aminobenzothiazol, 2-ABT | 50 mL/L |
| Polyethylene glycol, PEG (200) | 0.5 g/L |
| Polyethylene glycol, PEG (2000) | 0.5 g/L |

**Table III. Average surface roughness of $Si/SiO_2/TaN$ substrates after different chemical etching conditions.**

| Etching solution | Roughness (nm) |
|---|---|
| No etching | 0.20 |
| BOE:$HNO_3$:DI water = 1:1:2 | 2.17 |
| BOE:$HNO_3$:DI water = 1:1:3 | 1.27 |
| BOE:$HNO_3$:DI water = 1:1:6 | 1.15 |
| 10% HF | 0.23 |

The preparation of small and dense Pd catalysts dominates the successful deposition of subsequently thin and continuous electroless Cu seed layers because Cu nucleates on these catalysts and then grows. Agglomeration of Pd catalysts causes insufficient and nonuniformly distributed nuclei for electroless Cu deposition and thus results in the discontinuity and rough surfaces of Cu seed layers. Besides, weak adhesion due to voids and defects between seed layers and substrates leads to film peeling.[29,30] Two typical catalyzation methods have been developed in our group: sensitization-activation and displacement-activation.[21-23] Smaller and denser Pd catalysts can be achieved by sensitization-activation and lead to continuous Cu films, fitting the request for Cu seed layers and being selected in this research.

Figure 1 shows the AFM 2D images of 75°C Pd-catalyzed TaN surfaces that had been previously etched with BOE/$HNO_3$/DI water

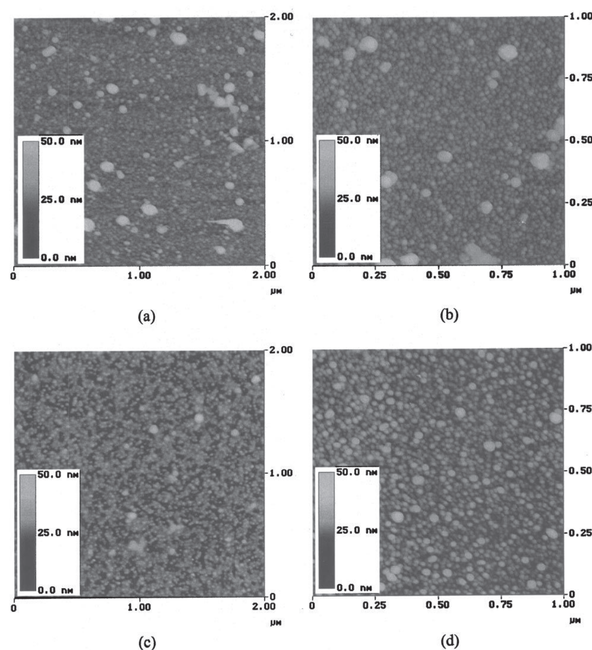



**Figure 1.** AFM 2D images of 75°C Pd-catalyzed TaN surfaces previously etched with (a) BOE:$HNO_3$:DI water = 1:1:2, (b) BOE:$HNO_3$:DI water = 1:1:3, (c) BOE:$HNO_3$:DI water = 1:1:6, and (d) 10% HF solutions.

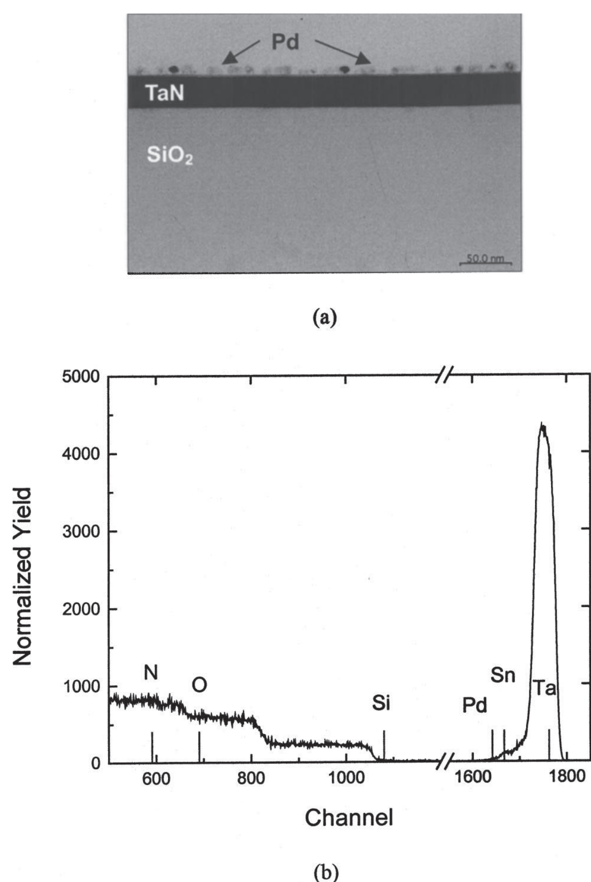



**Figure 2.** (a) TEM cross-sectional microstructure and (b) RBS spectrum of 10% HF-etched and 75°C Pd-catalyzed $Si/SiO_2/TaN$ substrates.

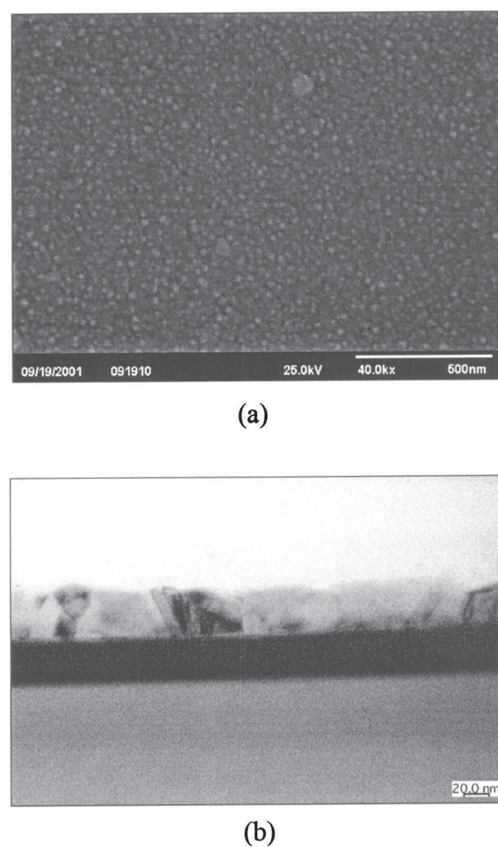



**Figure 3.** (a) SEM surface morphology and (b) TEM cross-sectional microstructure of electrolessly plated Cu seed layers on $Si/SiO_2/TaN$ substrates previously 10% HF etched and Pd catalyzed at 75°C.

and 10% HF solutions for 30 s. After catalyzation, surface roughness increased because of the seeding of Pd catalysts observed. Although small Pd catalysts were obtained by using $BOE/HNO_3/DI$ water etching, many large Pd particles precipitated, increasing surface roughness and reducing distribution uniformity. Using 10% HF etching and sensitization-activation, many uniform and dense Pd catalysts were obtained with 1.71 nm roughness, revealing the good quality of this catalyzation process. Figure 2a shows the cross-sectional TEM microstructure of 10% HF-etched and sensitization-activated $Si/SiO_2/TaN$ substrates. Small deposited Pd catalysts of only about 5-10 nm were clearly identified with uniform distribution. The large amount of nanosized Pd catalysts seemed not to agglomerate but smoothly distributed to a single layer. With the adsorption of oxidized $Sn^{4+}$ ions prior occupying the surface sites to lower interface energy during sensitization-activation, these Pd nuclei therefore stabilized at the scales of several nanometers under the equilibrium of surface, interface, and bulk energy.[23,31] Thus, in the deposited catalysts, Sn was incorporated into Pd catalysts, and the ratio of Pd to Sn was characterized as 4.6 by RBS analysis shown in Fig. 2b.

*Electroless plating of Cu seed layers*.—Figure 3a shows the surface morphology of 1 min electrolessly plated Cu seed layers on $Si/SiO_2/TaN$ substrates that had been previously 10% HF etched and Pd catalyzed at 75°C. Under the contribution of well-distributed and nanoscaled Pd catalysts by sensitization-activation, continuous and smooth 20 nm thick Cu films were already obtained by electroless plating for just 1 min. Through nucleation, quasi-two-dimensional growth, and coalescence processes, the Cu deposits connected to each other and then thoroughly covered the substrates. The deposition process rapidly entered the final step, film growth. Figure 3b shows the cross-sectional microstructure of 1.5 min electrolessly plated Cu seed layers with a thickness of 30 nm. The Cu seed layers were constructed of small Cu grains of about 10-20 nm. Voids were neither found inside the seed layers nor between the layers and substrates. A few twins were observed in accordance with the much smaller twin-boundary energy than the grain-boundary energy.[20]

With increasing catalyzation temperature from 65 to 80°C, the nucleus density of Pd catalysts for electroless Cu deposition increased from the order of $10^3$ to $10^4/\mu m^2$, and thus dense and smaller Cu grains formed. Because defects were more likely to exist in the films catalyzed at low temperatures, the Cu seed layers, therefore, exhibited lower electrical resistivity as the catalyzation temperature increased, as shown in Fig. 4. However, due to the much higher resistivity of Pd than that of Cu, the resistivity of Cu seed layers catalyzed at 80°C increased. Also, the resistivity of all seed layers was higher than 4.0 $\mu\Omega$ cm. Electrolessly plated 30 nm thick Cu seed layers on 10% HF-etched and 75°C Pd-catalyzed $Si/SiO_2/TaN$ substrates exhibited small roughness of only 3.68 nm and the lowest electrical resistivity. They were selected as the seed layers for further Cu electroplating or even directly as sub-90 nm interconnect metallization.

The electrolessly plated 30 nm thick Cu seed layers were further annealed to verify their stability under thermal processes. Recrystallization, coalescence, and grain growth occurred in the annealed seed layers, associating with smoothened surfaces and unclear grain boundaries. With increasing annealing temperatures, grain growth

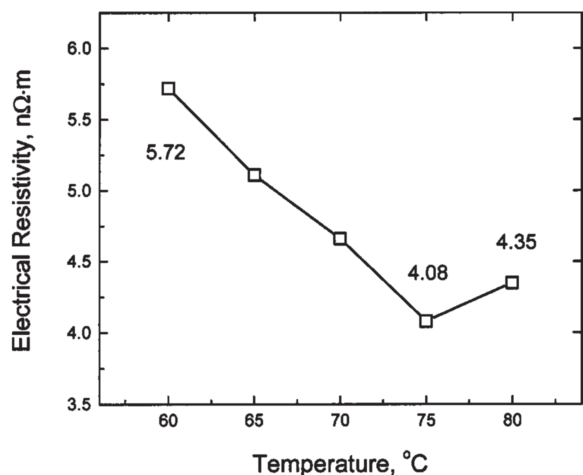



**Figure 4.** Electrical resistivity of electrolessly plated Cu seed layers on $Si/SiO_2/TaN$ substrates previously 10% HF etched and Pd catalyzed at different temperatures.

and surface smoothening were more obvious. The grain size of as-deposited seed layers increased from 10 to 20 nm to 40 and 60 nm after 400 and 700°C annealing, respectively, from SEM observation. The corresponding AFM surface roughness of 400 and 700°C annealed seed layers decreased to 1.92 and 1.13 nm, respectively, from as-deposited 3.68 nm. Figure 5 shows the RBS and AES analyses of Cu seed layers after thermal annealing. The RBS signals of elements except Cu appeared at channel numbers lower than their regular channel edges because of the shielding effect of their depths below surfaces. From depth calculation, the components Sn and Pd were only found at the interfaces between as-deposited Cu seed and TaN barrier layers, while slight signals of them were analyzed to exist at the surfaces of Cu seed layers after annealing at 400°C. The Pd peak of the as-deposited film spread to higher channel number after thermal annealing, and the distribution change revealed the solid solution of Sn and Pd into Cu by typical interdiffusion. At this temperature, no penetration of Cu into Si was found. As the temperature increased to 600°C, slight amounts of Ta and N were even found at the surfaces. Until annealing at 700°C, much higher than the temperatures for practical barriers staying stable, severe diffusion of TaN into Cu and the interdiffusion of Cu and $SiO_2$ through TaN occurred as shown in Fig. 5d. Because the deposited Cu films were annealed in an argon atmosphere, no obvious oxidation was found

**Figure 5.** RBS spectra of electrolessly plated Cu seed layers, (a) as deposited and annealed at (b) 400 and (c) 600°C; (d) AES analysis of Cu seed layers annealed at 700°C.

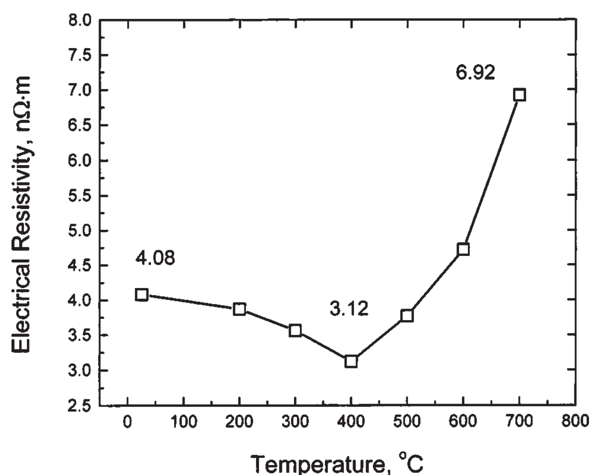



**Figure 6.** Electrical resistivity of electrolessly plated Cu seed layers annealed at different temperatures.

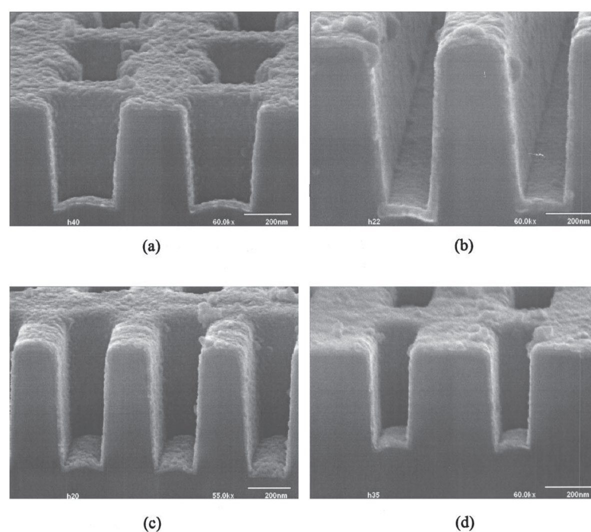



**Figure 7.** SEM surface morphologies of electrolessly plated Cu seed layers on patterned $Si/SiO_2$ /TaN substrates with different-sized features: (a) 0.35, (b) 0.25, (c) 0.20, and (d) 0.18 μm.

after annealing even under 700°C from AES analysis.

However, from the XRD patterns, no evidence of impurity interdiffusion or formation of new crystalline structure was found even in 700°C annealed specimens. The difference from what was found in RBS and AES analyses was attributed to the slight amount of impurity crystallites under the detection limit of XRD measurement. Besides, though the correspondence of Cu(111) facet to TaN(111) was expected because of their similar lattice constants, the XRD patterns exhibited no preferential orientation of electroless Cu seed layers. The measured peak intensity ratio I(111)/I(200) was 2.7, close to that under powder diffraction, 2.0. This might be attributed to the interference of Pd catalysts between Cu seed layers and TaN barriers. Less (111) preferential orientation would cause minor Cu stress migration.[32] Figure 6 shows that the electrical resistivity of electrolessly plated Cu seed layers decreased from 4.08 μΩ cm to the minimum value of 3.12 μΩ cm with annealing at 400°C. Grain recrystallization, coalescence, and growth reduced the amounts of defects and grain boundaries, accompanied by the elimination of residual hydrogen at these sites, thus reducing the resistivity. Though the interdiffusion of Sn and Pd with Cu occurred at 400°C from RBS analyses, the resulting slight increment in resistivity was compensated by defect elimination. With higher annealing temperatures, the resistivity drastically increased due to the interdiffusion of more impurities like TaN and even $SiO_2$.

Under the ASTM tape test, 60% of as-deposited Cu seed layers was found to peel basically due to the accumulation of hydrogen, and even bubbling or blistering, at interfaces between them and the substrates during electroless plating. However, no peeling of the seed layers occurred once they were annealed at 400°C, because defects like the residual hydrogen at interfaces were eliminated to enhance the bonding of seed layers to substrates, achieving higher adhesion strength. Figure 7 shows the surface morphologies of 1.5 min electrolessly plated Cu seed layers on patterned $Si/SiO_2$ /TaN substrates with different-sized features. One of the most important advantages for using electroless Cu deposition as seed layers is its excellent step coverage in these deep submicrometer features because of the uniform nucleation and growth of Cu on nanosized Pd catalysts. Electroless plating provided excellent sidewall step coverage similar to bottom step coverage with the same Cu seed layer thickness.

*Electroplating of copper films.*—To evaluate the feasibility of integrated electrochemical deposition, 1.5 min electrolessly plated, 400°C annealed Cu seed layers with a thickness of 30 nm were used for subsequent Cu electroplating. Attributed to the good uniformity of seed layers, smooth surfaces of electrodeposited Cu films were obtained under current densities of 1-4 $mA/cm^2$, as shown in Fig. 8a and b. The thickness of 5 min deposited films under a current density of 3.33 $mA/cm^2$ was about 180 nm, equivalent to a deposition rate of 36 nm/min. Though larger current densities than 4 $mA/cm^2$ contributed higher deposition rates, as shown in Fig. 8c and d, loosely packed rough films precipitated at local sites where the solution concentration was not uniform due to the rapid consumption and insufficient supply of $Cu^{+2}$ ions. The same results were also observed from AFM images. As shown in Fig. 9, the surface roughness of Cu films decreased and reached the minimum value of 5.47 nm as the current density increased to 3.33 $mA/cm^2$, and then large precipitated particles increased the surface roughness as the current density exceeded 3.33 $mA/cm^2$.

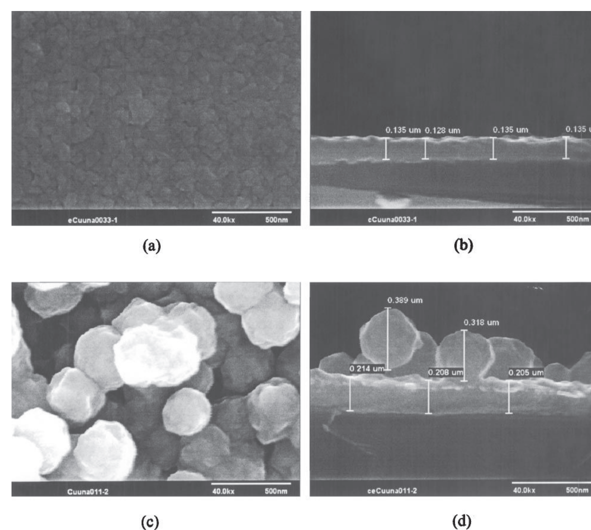



**Figure 8.** SEM (a) surface morphology and (b) cross-sectional microstructure of electroplated Cu films under a current density of 3.33 $mA/cm^2$; (c) surface morphology and (d) cross-sectional microstructure of electroplated Cu films under 11 $mA/cm^2$.

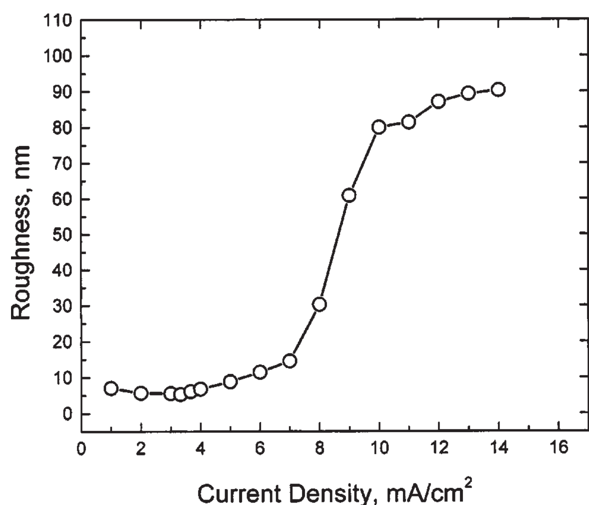
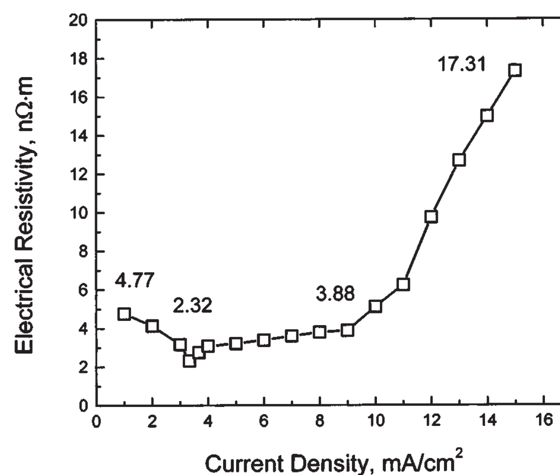



**Figure 9.** Average surface roughness of electroplated Cu films under different current densities.



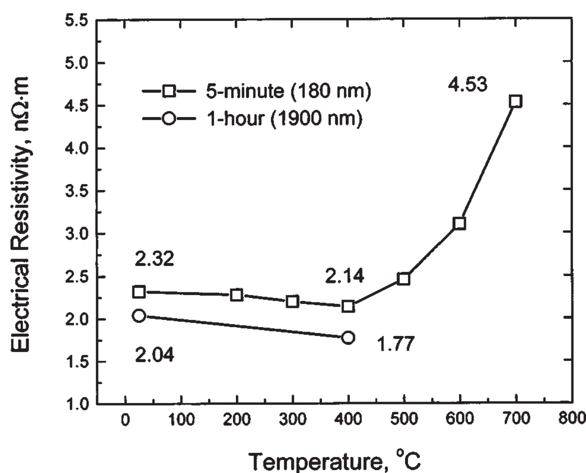
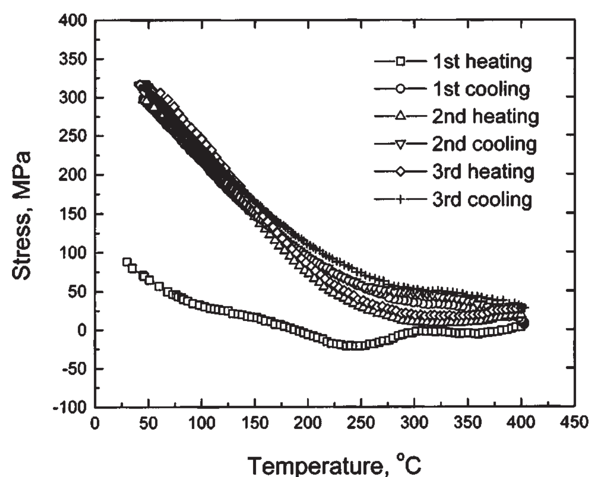




**Figure 10.** Electrical resistivity of electroplated Cu films, (a) deposited under different current densities and (b) annealed at different temperatures.

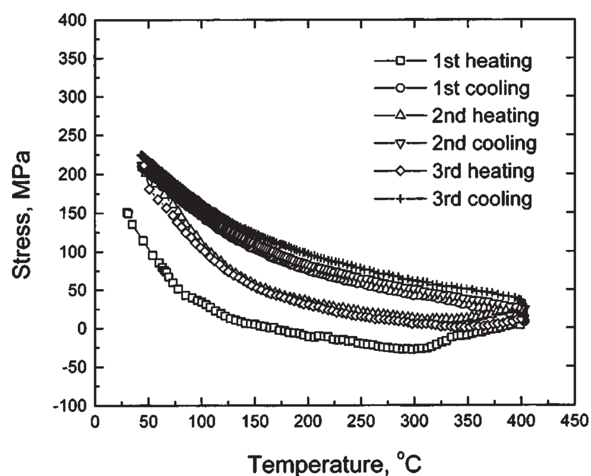
As a result of surface roughness, the electrical resistivity of 180 nm electroplated Cu films, shown in Fig. 10a, reached a minimum of 2.32 μΩ cm under a current density of 3.33 $mA/cm^2$. Thicker films of 1900 nm obtained by a longer plating time of 1 h even exhibited lower resistivity of 2.04 μΩ cm. Figure 10b shows the electrical resistivity of electroplated Cu films after thermal annealing at different temperatures. The resistivity of 180 nm and 1900 nm Cu films after annealing at 400°C was further lowered to 2.14 and 1.77 μΩ cm, respectively. The values were much closer to that of pure Cu, 1.68 μΩ cm, because of the elimination of defects and grain boundaries associated with the release of adsorbed hydrogen. Similar to Cu seed layers, the interdiffusion of impurities drastically increased the resistivity under higher annealing temperatures. However, from the XRD patterns, no evidence of impurity interdiffusion or formation of new crystalline structure was found due to the small amount of impurity crystallites.

Thermal stresses form during thermal processes and remain at room temperature due to the difference in coefficients of thermal expansion (CTEs) between different materials.[33] Different processing methods lead to different thermomechanical behaviors of materials. Figure 11 shows the stress hystereses of electroplated Cu films using electrolessly plated and sputtered Cu seed layers during three thermal cycles. The as-electroplated Cu films using electroless Cu seed layers exhibited smaller residual tensile stresses of about 80 MPa because of the low-temperature integrated electrochemical process. Using sputtered seed layers, the residual tensile stresses were much larger, about 150 MPa, due to the strong radical bombardment and the large difference between sputtering and room temperature. During thermal cycles, hysteresis loops were observed for both Cu films. With increasing temperature, residual tensile stresses were eliminated and then compressive stresses piled up due to the larger CTE of Cu than substrates. As the temperature reached about 250-300°C, Cu started to yield and thus the compressive stresses were released. At 300-350°C, stress-induced Cu recrystallization and grain growth occurred and then reduced the sites for yielding dislocations to sink, so compressive stresses stabilized. Above 350°C, compressive stresses released to zero due to easy Cu yielding/softening under high temperatures. During cooling, tensile stresses slowly accumulated under the competition of CTE difference and Cu yielding. Because the dissolution of Sn and Pd catalysts into Cu films at high temperatures resulted in a strong solution-strengthening effect, the yield strength of Cu films using electroless seed layers was highly enhanced. Therefore, as the temperature was lowered to 250°C, Cu yielding gradually ended and then tensile stresses rapidly increased. Stress hystereses with narrow loops during second and third thermal cycles located at 150-400°C. In comparison, the yield-ending temperature for those using sputtered seed layers was lower than 200°C, and the wide hysteresis loops surrounded at room temperature to 400°C. The high mechanical strength of the Cu films using electroless Cu seed layers would achieve higher thermomechanical stability of patterned structures during thermal processes. Although the residual stresses of the Cu films using electroless Cu seed layers after thermal processes were slightly higher than those using sputtered seed layers and might cause the Cu metallization to a more tensile state, during cooling to temperatures around 200°C at which stress migration would most probably occur,[32] both stresses of the films using different seed layers were at the same level of about 100 MPa.

20% of electroplated Cu films peeled under an ASTM tape test, however, only around specimen edges due to some cutting defects and etching of acid plating solution. Similarly to electrolessly plated Cu seed layers, 100% electroplated Cu films passed the peeling test after annealing at 400°C. Using electroless seed layers, excellent superfilling of electroplated Cu films was also achieved on patterned $Si/SiO_2/TaN$ substrates with different-sized features including 0.18

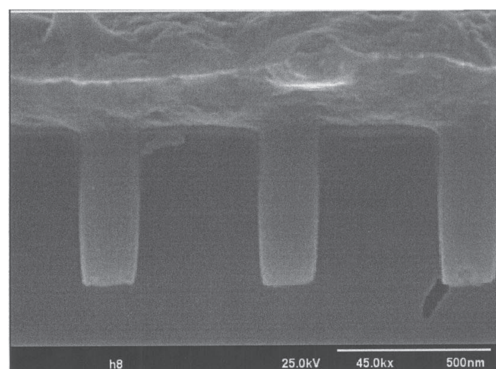



(a)

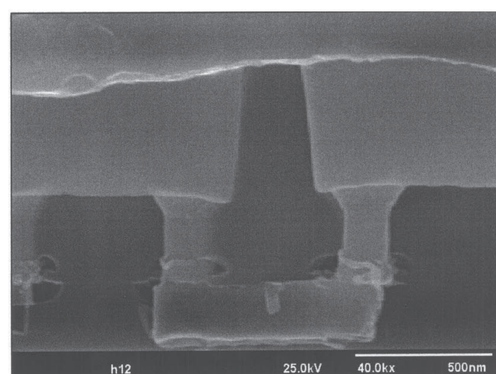



(b)

**Figure 11.** Stress hystereses during three thermal cycles of electroplated Cu films using (a) electrolessly plated and (b) sputtered Cu seed layers.




(a)




(b)

**Figure 12.** SEM cross-sectional microstructures of electroplated Cu films on patterned $Si/SiO_2$/TaN substrates with different-sized features: (a) 0.18 μm trenches and (b) dual-damascene structures.

μm trenches and dual-damascene structures as shown in Fig. 12. Because of the advantages including small surface roughness, low electrical resistivity, low residual stresses, good adhesion to substrates, and excellent gap-filling capability, the application potential of low-temperature integrated electrochemical deposition process constructed of nanoscaled Pd catalyzation, electroless plating of continuous Cu seed layers, and electroplating of smooth Cu films for ULSI sub-90 nm interconnect metallization is thus highly predicted.

## Conclusions

A low-temperature electrochemical deposition process for sub-90 nm Cu metallization was developed by integrating nanoscaled Pd catalyzation, electroless plating of Cu seed layers, and electroplating of Cu films in this study. First, uniformly distributed Pd catalysts of only about 10 nm were obtained by 10% HF etching and sensitization-activation of $Si/SiO_2$/TaN substrates. Second, electroless Cu plating on these nanosized Pd catalysts was applied to obtain smooth and continuous 30 nm thick Cu seed layers with low electrical resistivity and good step coverage. Last, Cu metallization with high purity, small roughness, low electrical resistivity, low residual stresses, good adhesion to substrates, and excellent superfilling was achieved using electroplating on the electroless Cu seed layers. Thermal annealing at 400°C further reduced the electrical resistivity of Cu films to 1.77 μΩ cm with minor impurity interdiffusion. Associating with good gap-filling capability into small-sized features including dual-damascene structures, the great properties of the integrated electrochemically deposited Cu films render this process highly promising to next-generation Cu metallization for sub-90 nm ULSI circuits.

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