

Invited Review

# Directional and preferential sputtering-based physical vapor deposition

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**Abstract**

Physical sputtering techniques are characterized by a mostly isotropic deposition profile, which is useful for depositing films over steps, edges and lines. However, it fails for deposition into modest ( $>1:1$ ) aspect ratio features due to overhang formation and subsequent void formation. A number of techniques have addressed this issue. Sputtering at high sample temperatures has been used to allow some degree of surface tension to help fill structures. Bias sputtering has been found to be useful for reducing void formation in low aspect ratio features. Collimated sputtering has been developed to filter the depositing atoms, resulting in mostly-normal incidence deposition. Finally, post-ionization of the sputtered atoms has been developed to deposit films primarily from metal ions, which are accelerated to the sample surface by means of a d.c. sample bias. Each of these techniques can lead to deposition within high aspect ratio features and will allow the application of sputter deposition for future semiconductor manufacturing processes.

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**1. Introduction**

Physical vapor deposition (PVD) techniques have been among the most commonly used deposition technologies for thin films for applications ranging from microelectronics to automobile parts to food packaging. Evaporation-based deposition, which will not be discussed in this manuscript, has been widely used and described [1–3], but is generally not considered a viable manufacturing technology in many fields, particularly semiconductor manufacturing, because of the difficulty of alloy control, batch-processing issues, and the difficulty of scaling to large wafers. Sputter-based PVD, however, is widely used and has had several recent developments which will enhance its future capabilities.

Sputtering is a fairly simple process which is based on the impact of an energetic particle onto a surface. If sufficient energy and momentum are transferred into the near-surface atoms by the impact, one or more of those atoms may have enough energy to overcome the local binding energy and be emitted from the surface. The emitted atom or atoms are known as sputtered atoms, and if collected on some nearby surface form the basis for sputter deposition. The physics and dynamics of the sputtering process

have been discussed at great length elsewhere, and excellent reviews are available [4, 5].

Sputtered atoms are emitted from the surface in a mostly random manner. The angular emission distribution is generally described as a cosine function, normalized to emission at the surface normal. Depending on the choice of incident particle, energy, sample species and orientation, departures from this cosine distribution are routinely observed [4, 6, 7]. This may have modest effects on the directionality or compositional control [8] of the deposited films. However, to a first approximation, the emission follows roughly a cosine distribution.

For semiconductor manufacturing applications, sputter deposition typically involves the use of magnetron sputtering sources. This is due to the high deposition rate and relatively low level of energetic bombardment of the sample. Systems used for semiconductors typically use cathodes of a diameter 50% greater than the wafer or part diameter, cathode-to-sample distances of a few centimeters, and operating pressures of a few millitorr. In some cases, the magnetic field of the magnetron is physically translated or rotated over time. This improves the uniformity of the deposit as well as increases target utilization. With magnetron sputtering, the depositing

atoms arrive at the sample surface in a mostly isotropic nature. This is due to cosine emission profile, the wide area of the sputtering target, the short cathode–sample distance and some gas scattering. This mostly isotropic deposition is useful in depositing continuous films over various surface topographies (steps, lines, etc), which is advantageous for electrical conductivity and continuity. This advantage of “step coverage” has caused sputtering to be widely used for the deposition of interconnects on semiconductors, which are patterned from the blanket film using reactive ion etching (RIE).

More recently, driven by the increasing density of features on a semiconductor, different patterning techniques have evolved which rely on the etching of trenches and vias into an existing dielectric layer. The open trenches and vias are then filled with metal, which can leave some metal deposited on the upper surface of the dielectric. This unwanted metal is removed using chemical–mechanical polishing, and the result is a metal line or via interconnection which is embedded in the dielectric with a flush, exposed surface [9].

The aspect ratios of these embedded lines and vias ranges from 0.5 to 5 or more (aspect ratio equals depth/width). This has limited the applicability of many deposition technologies, both from a directional or conformal point of view, and also from a materials point of view. Chemical vapor deposition has the advantage of mostly conformal deposition and can be readily used for high aspect ratio features. However, the materials choice is somewhat limited. Tungsten is routinely used for studs or vertical interconnects. Titanium nitride as a diffusion barrier is becoming available, and there is active work on Cu and Al for interconnects [10]. Some manufacturing-scale hardware for Al and Cu is starting to become available, but many of the manufacturing challenges are formidable, such as rate, doping, uniformity, reliability, safety, temperature and cost.

Still another alternate technology for metal deposition is electroless or electroplating [11]. While this is limited to Au, Cu and Cu alloys [12], it has potential because of eventual low costs and high rates. It does require the wafer to be immersed in a plating bath, which introduces new requirements for defect-free, continuous films on both sides of the wafer. It also introduces new challenges for semiconductor-equipment manufacturers, most of whom have little experience with electroplating technology in manufacturing applications.

Sputtering-based PVD, however, has been generally incompatible with the high aspect ratio topographies envisioned for near-term semiconductor interconnect technology. The same feature, the near isotropic deposition, which made sputter deposition advantage-

ous for step-coverage applications results in the deposition of overhangs near the top edges of high aspect ratio features, eventually resulting in void formation. The remainder of this paper deals with techniques and operating modes which extend sputtering into the high aspect ratio deposition applications or selectively deposit sputtered material on specific surfaces or within structures.

## 2. Hot sputter deposition

One means of reducing void formation is to strongly enhance the surface mobility of the depositing atoms by raising the sample temperature. This technique utilizes conventional or directional (see below) magnetron sputtering and sample temperatures elevated to 0.8–0.95 of the melting point. Because of the temperatures involved, this technique has mostly been used with the deposition of Al and Al alloys [13–16]. At temperatures of 500 °C to 600 °C, sputtered Al films exhibit macroscopic movement on the sample surface, which can result in the accumulation of the deposited metal within trenches or vias. Often this effect does not occur uniformly during the deposition time at elevated temperature, i.e. it is not predominantly a surface diffusion-driven effect. Studies have shown that a void is still present until a minimum flat-plane thickness of the deposited metal is reached, and then the metal is pulled into the via by surface tension [16]. It is also possible to demonstrate this same effect by post-heating samples deposited at room temperature.

It is necessary with the hot sputter deposition of Al or AlCu films to deposit a diffusion barrier to reduce contamination of the Al from nearby Si. Typically Ti or Ti/TiN has been used at thicknesses of 500–700 Å. It has also been found to be necessary to first deposit at least thin layers of Ti or Al within the trench or via to help draw nearby Al into the via opening.

This technique has been used to successfully fill trenches and vias of sub-0.5 μm width and aspect ratios of up to 4:1 [15]. A variation of this technique uses AlGe alloys, which have a low eutectic temperature (424 °C) and reasonable conductivity [15].

There are several concerns with using high temperatures (>500 °C) during sputter deposition. The first is the formation of precipitates within both the deposited metal as well as existing structures on the wafer [17]. A second concern is the effect on dopant profiles. A potentially serious problem is the effect of thermal stress mismatch (between the metal and dielectric layers), due to the multiple thermal cycles that would be necessary for any multi-level interconnect technology. A fourth problem could be an effect of scavenging, in that larger features may preferentially accumulate metal at the expense of finer features. And finally,

from a practical point of view, elevated temperatures in this range can result in technical problems with the sputtering system, caused by local outgassing or thermal expansion. However, even with these potential problems, the technique remains one of the few ways to deposit metal lines and studs using manufacturing-scale PVD systems and it is a potential deposition process for 64–256 Mbit DRAM production.

### 3. Sputtering with ion bombardment

Concurrent ion bombardment during sputter deposition is routinely achieved by means of applying a negative potential to the substrate, known generically as bias sputtering. Ions from the plasma bombard the growing film and may cause physical sputtering as well as drive various chemical reactions. Bias sputtering has commonly been used to help planarize films that are being deposited over steps or lines [18] because the sputter yield of the non-planar areas of the film is greater than the yield in the planar areas.

Bombardment of the sample with ions has been found to be desirable to modify either the physical or chemical structure of the film. A common example is the deposition of TiN. To form TiN, Ti is reactively sputtered in a background gas containing  $N_2$ . However, it is also necessary to either heat the surface to 400–700 °C or else bombard the surface with ions to cause the nitride reaction to occur. For many substrates, raising the sample temperature is not realistic, and ion bombardment is preferred. Due to the relatively good plasma confinement with conventional magnetron sputtering (as opposed to r.f.-diode sputtering), the bias currents are inadequate. This has led to the development of the unbalanced magnetron [19] in which the plasma confinement is designed to be weaker, and ions from the plasma are more likely to drift to the sample location to form the bias current.

Bias sputtering can be used to enhance the deposition of films into low aspect ratio structures (<1:1) which have fairly wide lateral dimensions (>0.8  $\mu\text{m}$ ) [20]. The concurrent ion bombardment can sputter-back the overhanging film which is deposited at the upper edge of a trench or via, again taking into account the increased sputter yield of non-planar surfaces. However, this effect has been found to fail at aspect ratios of 1:1 and higher, resulting in void formation. For features narrower than about 0.8  $\mu\text{m}$  there can also be considerable redeposition of the sputtered material across the feature onto the opposing side. This results in increased overhang deposition and rapid void formation. Bias sputtering may also contribute to measurable sample heating, and as such, promote surface diffusion and surface tension effects. Some of the earlier work on elevated-temperature

sputter deposition used both high levels of bias as well as elevated temperatures to reduce void formation.

A variation of bias sputtering for selective sputter deposition into structures on a wafer surface has recently been developed by Berg et al. [21]. They utilize the observation that the sputter yield for a very thin layer of any particular material is sensitive to the species of the underlying material [22]. Their technique uses bias sputtering at carefully controlled ion energies. This bombardment sputters (re-sputters) the depositing film, but the yield is dependent on the local substrate material. For one case they described, Al was sputter deposited into a window of oxide on Si (Fig. 1). Prior to deposition, the top of the oxide was coated with a 3000 Å layer of W. Under 300 eV bias sputter conditions, there was no net deposition on the W mask, yet there was significant net deposition into the window structure, which had a Si base. The W mask was slowly eroded by the incident ions, and then would be completely removed by a subsequent reactive step.

This technique may become useful in the selective filling of trench and via structures, particularly since the materials used (Si, oxide, Al and W) are commonly used in semiconductor applications. There are related effects, such as bevel formation, ion reflection off the sides of structures and the resultant trench formation, and also redeposition which must be addressed with this technology.

In general, though, bias sputtering is limited by (a) the wide emission distribution of the sputtered atoms from the cathode, and (b) the negative effects of high-current or high-energy ion bombardment during deposition, which can result in sample damage, beveling, redeposition, charging effects, and simple heating of the substrate.

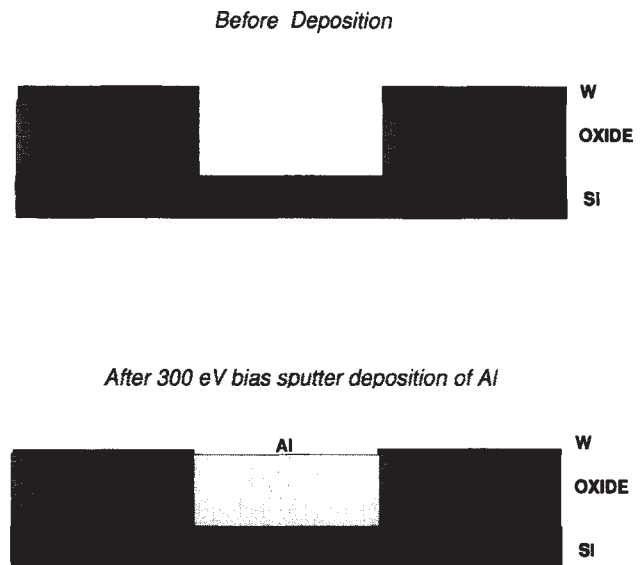


Fig. 1. Cross-section of substrate-selective sputter deposition [21].

#### 4. Directional sputter deposition

The principle feature driving the nearly-isotropic deposition nature of sputtering is the cosine emission profile. Most magnetron cathodes are operated in pressure–distance regimes where the sputtered atoms travel in a straight trajectory from the cathode to the sample without gas-phase collisions. One solution to the broad emission profile of sputtering has been to filter the emitted atoms by means of an adsorbing, directional filter [23, 24]. This filter, generally known as a collimator, is typically an array of closely-packed oriented tubes which are configured with their axis normal to the cathode/sample planes (Fig. 2). Emitted, sputtered atoms from the cathode which have a trajectory along the axis of the tube will pass through the tube and land on the sample. Atoms with more oblique trajectories will be collected on the inner walls of the collimator.

This is a subtractive process, and results in significant reduction of the deposition rate. Pictorially this can be seen in Fig. 3, which shows (in 2-D) a cosine-like emission profile from a surface. The effect of the collimator is to eliminate all but a narrow cone of the depositing atoms. The aspect ratio of the collimator will determine the effective shape of this cone: high aspect ratio collimators will narrow the distribution to a smaller and smaller half-angle.

Collimated sputter deposition has been shown to be applicable to the filling and lining of high aspect ratio structures [24–40]. The mostly normal deposition flux will fill a trench or via from the bottom up and the overhangs common with conventional sputtering are significantly reduced. Collimated sputter deposition has been extended to a variety of different sputtering systems as well as different cathode materials. Perhaps the most widely used application is for the deposition of Ti or TiN diffusion barrier films to line trenches and vias [25–27, 33–40]. Trench and via filling applications in manufacturing with AlCu or Cu have tended to be limited to modest aspect ratios (1.5:1) because of the low, net deposition rate at higher aspect ratio.

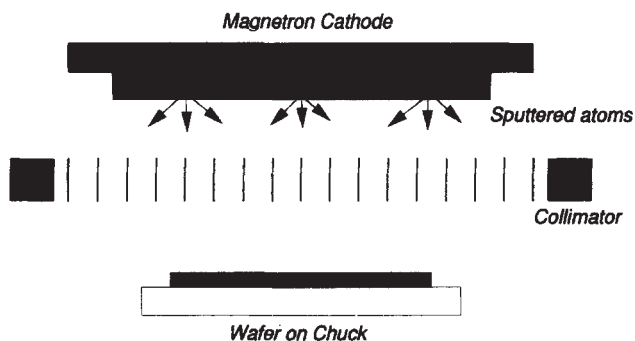
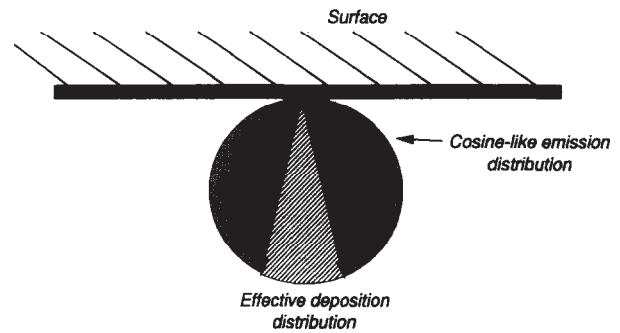


Fig. 2. Collimated magnetron sputter-deposition system.



For a 2cm high collimator located 2cm from cathode:	
Aspect Ratio	Emission Width (degrees)
1:1	28 (i.e. +/- 14)
2:1	14
3:1	11
4:1	7

Fig. 3. Cosine emission distribution for sputtered atoms, as modified by filtering with a collimator.

A number of studies have examined both the directionality of the deposition [28, 29, 31], the uniformity of the deposition across a collimator hole [29, 31] and across the wafer [41], clogging of the collimator holes [30], and the microstructure of the deposited films [34, 42, 43]. The deposited film structures can be fairly sensitive to sample temperature due to the extreme directionality of the depositing atoms [24]. Depositions at cold temperatures (i.e. near room temperature) result in very columnar depositions on the sidewalls of vias and trenches. These low-density deposits are undesirable, and are generally eliminated by moving towards deposition temperatures closer to 1/3 or more of the film melting point to encourage recrystallization.

A number of practical problems have become apparent regarding the implementation of collimated sputtering in manufacturing. The most obvious is the eventual closure of the collimator holes due to the deposited layers. Even holes with diameters exceeding 1.5 cm show significant degradation (i.e. partial closure) on the scale of depositing a few hundreds of wafers. The closure effect results in an increase, with sputtering time, of the effective aspect ratio of the collimator, and a subsequent reduction in the deposition rate. Generally, it has been found that the practical collimator lifetime is of the order of the cathode lifetime for cathodes about 1 cm thick. In addition, over time as the effective collimator aspect ratio changes, the deposition uniformity across the sample can also change [41].

The collimator is usually cooled because it is closely exposed to the dense plasma. The choice of materials used includes 1–2 cm thick sheets of Cu, Al or Al alloy with a close-packed array of round or hexagonal holes

machined in the sheet, cast Al honeycombed structures, as well as arrays of square or hexagonal channels or tubes which are made by spotwelding thin sheet metal pieces. For some applications, the collimator material is chosen to have a similar thermal expansion coefficient to the depositing film to reduce thermal-cycle-induced film peeling and flaking.

The collimator functions as an array of pin-hole cameras, each imaging a specific area of the cathode onto the sample. This changes the deposition uniformity requirements for the cathode, often requiring redesign of the magnet assembly. Most cathodes are designed to etch at a slightly faster rate near the cathode perimeter to make up for losses out to the sides of the system. With a collimator in place, imaging the cathode emission directly onto the sample, this higher etching rate is no longer desired, and a much higher degree of uniformity across the cathode is needed.

Collimated sputter deposition has proved to be a useful technology for semiconductor applications. It is, however, relatively slow and requires the aspect ratio of the collimator be equal to or greater than the highest aspect ratio feature on the sample. This, in turn, exaggerates many of the problems listed here.

One related means of reducing the deleterious effects of the collimator is to sputter deposit with a very long cathode–sample distance without a physical collimator. This was first used with hollow-cathode supported discharges and lift-off technology [44]. At long throw distances and low pressures, atoms with trajectories away from normal incidence tend to impact the walls of the chamber, and only atoms with near-normal incidence deposit on the sample. This is functionally equivalent to using the chamber walls as the collimator, and many of the intrinsic problems with low rates and thick deposits on fixtures remain. In addition, this technology is geometrically limited to relatively low aspect ratio depositions. The sputtered atoms in this case must not suffer gas-phase collisions, which, coupled with a minimum pressure of operation needed for conventional magnetron cathodes (0.5 mTorr), limits the effective throw distance to about 20–25 cm. For a 200 mm wafer, the practical upper limit for the aspect ratio of the deposit is then about 1.3:1.

## 5. Collimation with concurrent ion bombardment

The introduction of a collimator between the cathode and the sample has the effect of essentially eliminating the presence of any significant number of ions or electrons at the sample position. Collimators are usually grounded, and their orientation with respect to the magnetic field of the magnetron results

in very efficient electron collection. This has the advantage of reducing the thermal load on the sample, which has been shown to allow the use of photoresist masks on uncooled wafers without degradation to the mask ( $<80^{\circ}\text{C}$ ) [23, 24].

To provide any level of concurrent ion bombardment during collimated sputter deposition the addition of separate ion sources has been required, which are mounted such that ions impact the film surface at non-thermal incidence [45] (Fig. 4). In this example, a Kaufman-type ion source is configured such that the ion beam impacts the surface at about  $15^{\circ}$  from the horizontal. This has distinct geometrical advantages over a normal incidence ion bombardment (i.e. conventional bias sputtering) for the filling of trenches and vias. The grazing-angle ion bombardment results in preferential sputtering of film material deposited on top of the trench structure, with very little sputtering of the material deposited into the trench structure.

The results of grazing-angle ion bombardment during collimated sputter deposition are shown in Fig. 5. In this case, Al was deposited using collimated sputtering with concurrent 600 eV Ar-ion bombardment. The result at longer times can be either planarized films on top of the filled structure, or else the top film materials can be removed almost entirely.

This technique does not fix the intrinsic problem with sputtering, that the atoms are emitted from the cathode with a cosine distribution. However, it reduces the amount of filtering required with the collimator. In general, the aspect ratio of the collimator can be reduced to less than that of the sample features, because the grazing angle sputtering reduces the build-up which would shadow the fill. By reducing the aspect ratio of the collimator, several of the technical problems caused by the collimator (deposition build-up, flaking, uniformity changes, etc) can be reduced. However, this technique does not lead to any significant increase in deposition rate into the trench or via. That is because the atoms which eventually

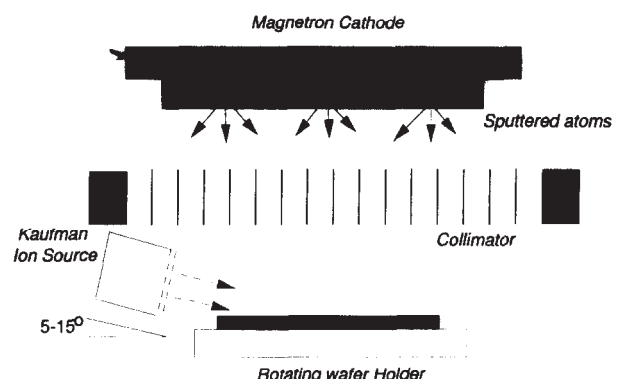


Fig. 4. Grazing-angle ion bombardment during collimated magnetron sputter deposition.

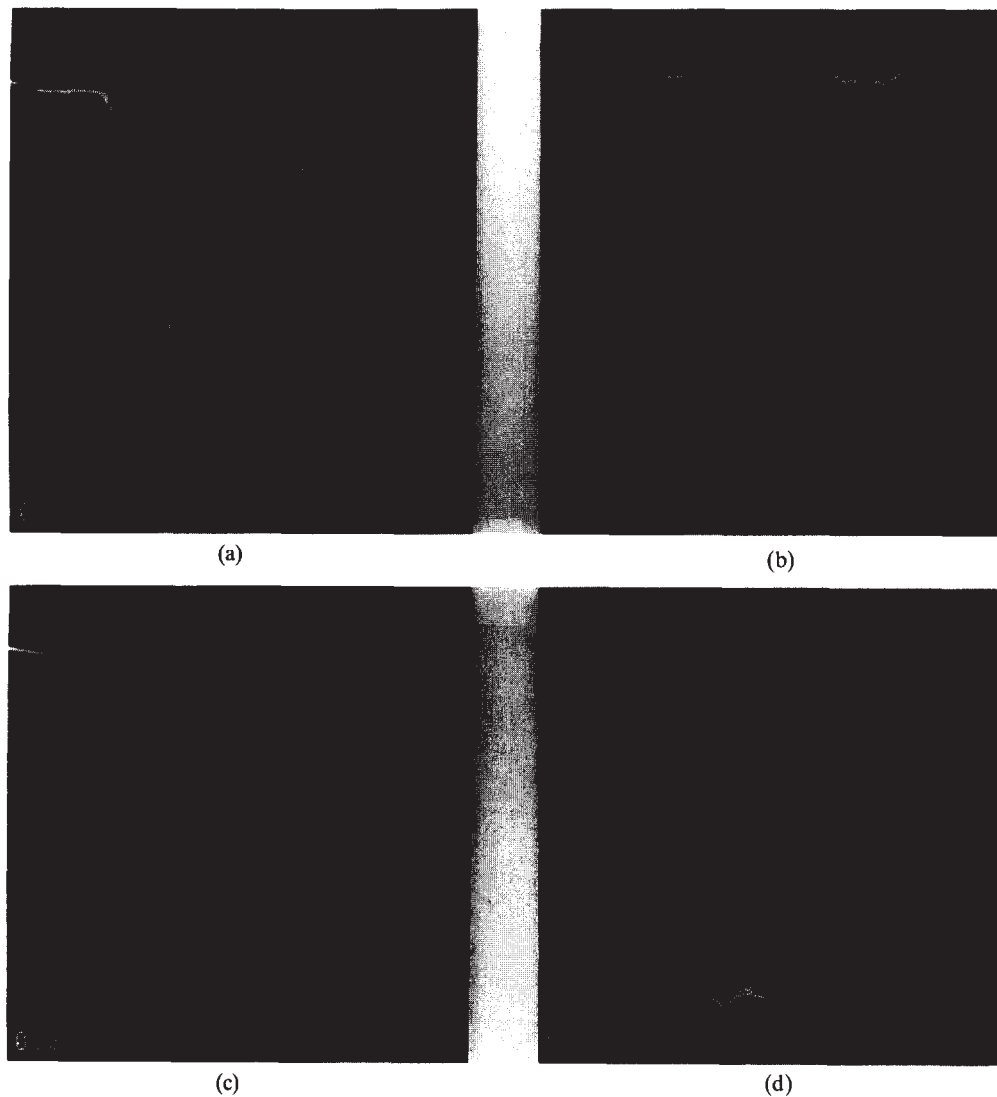


Fig. 5. Results of collimated sputter deposition in the presence of grazing-angle ion bombardment. (a)–(d) show increasing levels of ion bombardment at 600 eV at grazing incidence [45].

deposit deep within those structures require a near-normal trajectory from the cathode to the sample, which is fundamentally limited by the cosine distribution of the sputtering process. This process does allow, however, the deposition of filled features plus a planar, blanket-film top layer. This planar film can be subsequently patterned by means of RIE. This combined process eliminates the need for a number of process steps: polishing the via, deposition of interfacial layers and potentially some lithographic steps. It also eliminates the interface between the via (stud) and the metal lines, removing concerns about inter-diffusion and spiking, resistive contacts, etc.

## 6. Ionized deposition

The intrinsic problem with considering sputtering-based technology for directional applications is, again,

the cosine-like profile of the emitted atoms. A solution is to deposit films mostly from ions, rather than neutrals. Metal ions in a plasma arc accelerated across the sample sheath at normal incidence, and impact the surface at very close to  $90^\circ$ . In addition, the incoming kinetic energy of the ions is simply dependent on the difference between the plasma potential and the substrate potential. The directional component of the depositing ions is useful in projecting the metal species down into high aspect ratio features. The energetic component is desirable because it can be used to re-sputter the depositing film, resulting in the etch-back of sputter-deposited overhangs at steps as well as redistribution of the sputtered atoms on the wafer surface. If 100% of the metal atoms which were sputtered from a cathode could be ionized, in the order of 50% could be used for deposition. The other 50% would be re-used in sputtering the cathode. This compares with only 2–10% efficiency of collimated

sputtering. The difficulty is in obtaining large numbers of condensable, metal ions.

Early work on ionized or partially ionized deposition utilized ionization of an evaporated flux of metals atoms, in a technique known as ion plating [46]. Some fraction of these evaporated atoms were ionized by passing the vapor stream through an electron beam or by inducing a weak plasma near the sample. The relative level of ionization in this case was generally very small, of the order of a few percent, and this was not found to be suitable for high aspect ratio deposition applications.

This technology was extended to higher ionization fractions by Holber et al. [47], using an ECR plasma to ionize metal from a vapor stream to deposit metal into semiconductor features. This followed earlier work by Kidd in sputter-based ECR ionization [48]. In Holber's work, they also chose to deposit off to the side rather than within sight of the evaporation source (Fig. 6). This reduced the number of non-ionized metal species to virtually zero at the wafer position. With this technique, they were able to deposit Cu films from  $\text{Cu}^+$  ions into 4:1 aspect ratio features on a wafer surface. Holber also observed a strong self-sputtering effect. The net, flat-plane deposition rate which had a maximum of about  $4000 \text{ \AA min}^{-1}$  at very low substrate voltages fell linearly to zero at about 225 V (i.e. approximately 230 eV). At this point, the effective self-sputter yield exceeded 1.0, and each of the depositing atoms on planar surfaces was removed.

During conventional sputtering (diode or magnetron), the emitted flux is virtually 100% neutral. This ignores the contribution of negative ions, which can be significant in any compound deposition process involv-

ing oxygen either in the target or the working gas. For metal sputtering in an inert gas, only a few percent at best of the emitted neutral atoms are ionized during transit through the plasma. For magnetron sputtering, even though the plasma densities can be extremely high ( $10^{12} \text{ cm}^{-3}$  and greater), the relative ionization of the sputtered species as they pass through the plasma in most systems is a few percent or less primarily because of the very small plasma volume, the high velocity of the sputtered atoms, and the low gas pressure. There have been recent reports of self-sustained magnetron operation, in which sufficient ionization of the sputtered atoms takes place in the plasma to allow the reduction or removal of the working background gas [49]. This phenomena is limited at present to cathode materials with relatively high sputter yields, such as Cu or Ag, and very high cathode power densities.

The ionization of a significant fraction of the sputtered atoms (e.g., 30–100%) in conventional sputtering devices has required the addition of a second plasma in the region between the cathode and the sample. Two techniques have demonstrated this effect, the first using an inductively-coupled r.f. plasma [50–52], and the second using an ECR plasma [53, 54].

The first case is shown in Fig. 7. In this experiment, a conventional magnetron cathode system is configured with a r.f. multi-turn electrode with a diameter of the order of the cathode diameter located midway between the cathode and the sample. The r.f. coil was powered at 13.56 MHz in such a manner as to produce a predominantly inductively-coupled plasma in the background gas in the sample region. Plasma densities in this case can approach  $10^{12} \text{ cm}^{-3}$  with electron temperatures of a few electronvolts. Sputtered atoms which enter this discharge region have a high prob-

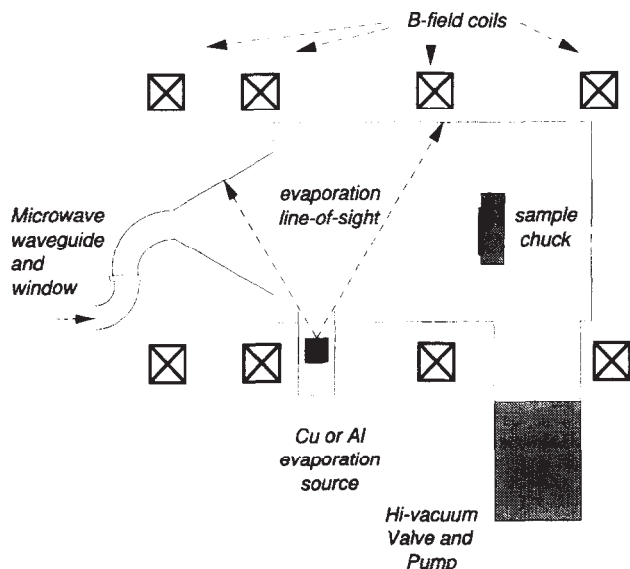


Fig. 6. ECR-based ionized deposition of evaporated metal flux [47].

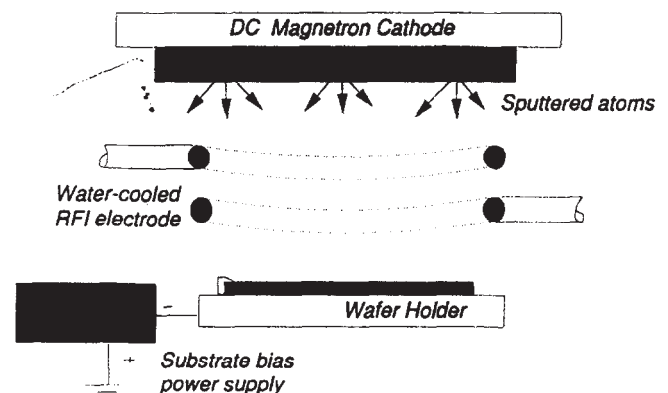


Fig. 7. Ionized magnetron sputter deposition system [52].

ability of becoming ionized due to the high electron density and the relatively low ionization potential for most metals (5–8 eV). The mean free path for ionization is simply:

$$l = v_m / (n) \langle \sigma v \rangle$$

where  $n$  is the electron density,  $\sigma$  the cross-section for ionization,  $v$  the electron velocity and  $v_m$  the metal-atom velocity. The average value of the product of the cross-section and electron velocity is needed because of the variety of electron energies and the energy dependence of the cross-section. For a plasma density of  $10^{12} \text{ cm}^{-3}$ , the mean free path for a sputtered metal atom (Al or Cu, for example) is about 40 cm, assuming no gas-phase collisions. The presence of these collisions tends to increase the effective path length of the sputtered atom as well as to slow down the sputtered atom, which also increases its effective cross-section [55]. The relative ionization measured with this experiment ranges from 10–20% at 5 mTorr up to 85% at 30–40 mTorr [51, 52]. This is consistent with the mean free-path predictions.

The ionized metal particles are then accelerated by means of a negative d.c. bias on the sample surface, and impact with an energy equal to the difference between the plasma potential (5–20 V positive) and the substrate potential.

The ECR approach relies on acceleration of ions from an inert-gas ECR plasma onto a negatively-biased metal surface or cathode. Metal atoms sputtered from this cathode enter the ECR plasma and may be ionized and then accelerated across a sample sheath for deposition. This differs from the r.f. approach just described in that there is only a single plasma: this plasma is used for sputtering the cathode as well as deposition of the ionized, sputtered atoms.

In the ECR experiment [54] a fixed-magnet inert-gas ECR plasma is set up in a chamber by positioning a large permanent magnet just outside the top of the chamber, and ducting in microwave power (2.45 GHz) at 1–5 kW (Fig. 8). This generates an ECR plasma in the chamber with densities approaching  $10^{12} \text{ cm}^{-3}$ . An annular, water-cooled Cu cathode is configured adjacent to this ECR plasma. Ions from the plasma are accelerated by a several hundred volt negative potential on the cathode, causing sputtering and emission of the metal atoms into the ECR discharge. Some fraction of the metal atoms can be ionized, and then upon reaching the sample position can be accelerated by a negative substrate bias. The only fundamental difference in these two approaches, aside from the choice of r.f. or ECR frequencies, is that in the ECR case the cathode is operating in an ion-saturation-current mode, rather than a magnetron mode. This is intrinsically self-limiting, as high metal levels will cool

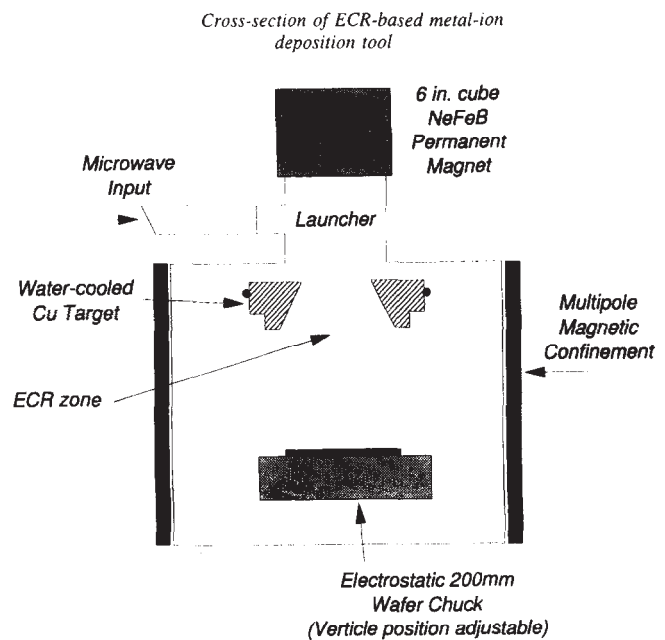


Fig. 8. ECR-based ionized deposition based on sputtering of a cathode adjacent to the ECR region [54].

the plasma resulting in lower density and/or lower electron temperature and hence less bombardment of the cathode. Therefore, the relative ionization of the depositing films should be constant as the microwave power and hence the deposition rate are increased.

The films deposited in these two experiments originate both from ions, which are accelerated by the substrate potential, as well as low-energy sputtered (neutral) atoms which have passed through the plasma. The deposition into trench structures is strongly dependent on the ratio of ions to neutrals: the ions are directional and the neutrals are mostly isotropic. An example is shown in Fig. 9, where the ratio of ions to neutrals was increased from about 30% to about 70% (Figs. 9(a)–9(c)). Relative ionization levels of about 70% appear sufficient to directly fill 1.5:1, 4000 Å wide trenches with AlCu at room temperature.

The microstructural character of these films is different, as might be expected, from conventionally sputter-deposited films [42]. AlCu films deposited with a high ion-to-neutral ratio resulted in highly-preferred (111) orientation, relatively abrupt film/substrate interfaces, and no indication of surface faceting. While the film layers did contain inhomogenous strain due to residual ion-irradiation-induced defects, both the Ar incorporation levels and the residual stress were very low [42]. TiN films were also reactively deposited using the ionized magnetron sputter deposition technique. The film quality was sensitive to the ion energy over the range of 20–100 eV. At low ion energies, the films were dark and highly resistive. As the ion energy was increased (at room temperature), the films became more consistent with the bright yellow–gold

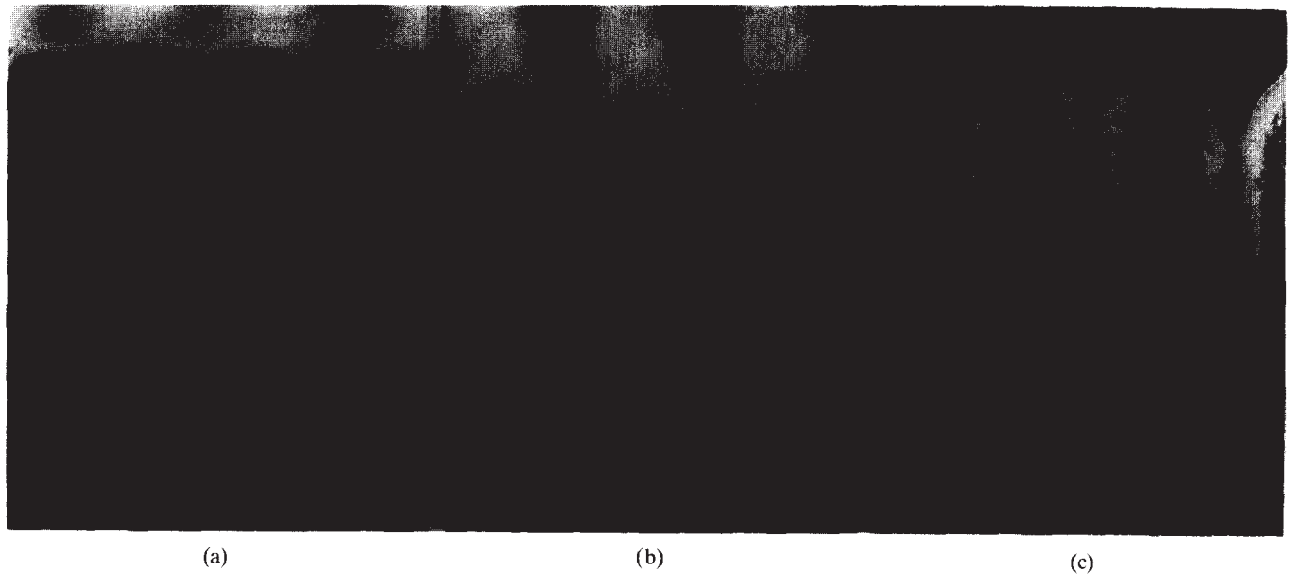


Fig. 9. Cross-section of directed deposition as a function of relative ionization: (a) approx. 30% ionized; (b) approx. 50% ionized; and (c) approx. 68% ionized.

color of TiN, and the resistivity dropped to levels in the 35–40 mΩ cm range (Fig. 10). The films were stable and showed no degradation in either appearance or resistivity over periods in room air exceeding 12 months.

Increased ion energies can result in significant resputtering of the depositing film. In some cases, this

can result in the etching back of overhangs at the edges of trenches and vias, resulting in better filling capability. Resputtering also results in the redistribution of atoms inside a trench or via, which helps to eliminate self-shadowing which can occur at corners. However, as mentioned earlier, faceting and subsequent redeposition in narrow structures can lead to

#### RESISTIVITY (Micro-Ohm-cm)

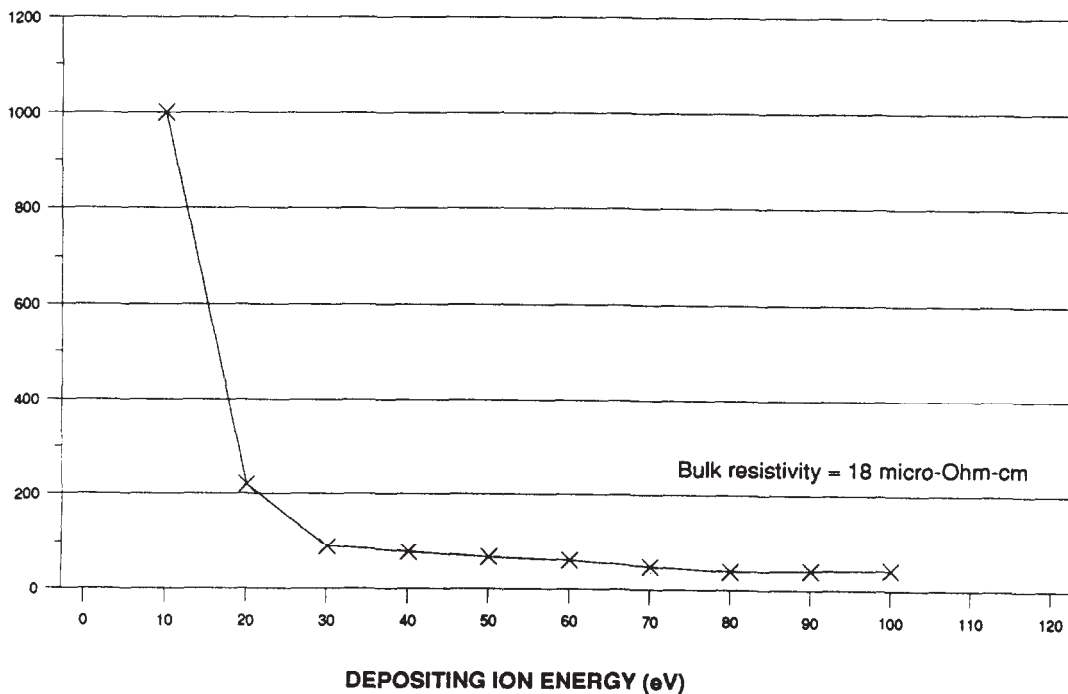


Fig. 10. Electrical resistivity of 500 Å TiN films on Si deposited using ionized magnetron sputter deposition as a function of ion energy (sample potential plus plasma potential). Samples were water-cooled 5 in diameter Si wafers.

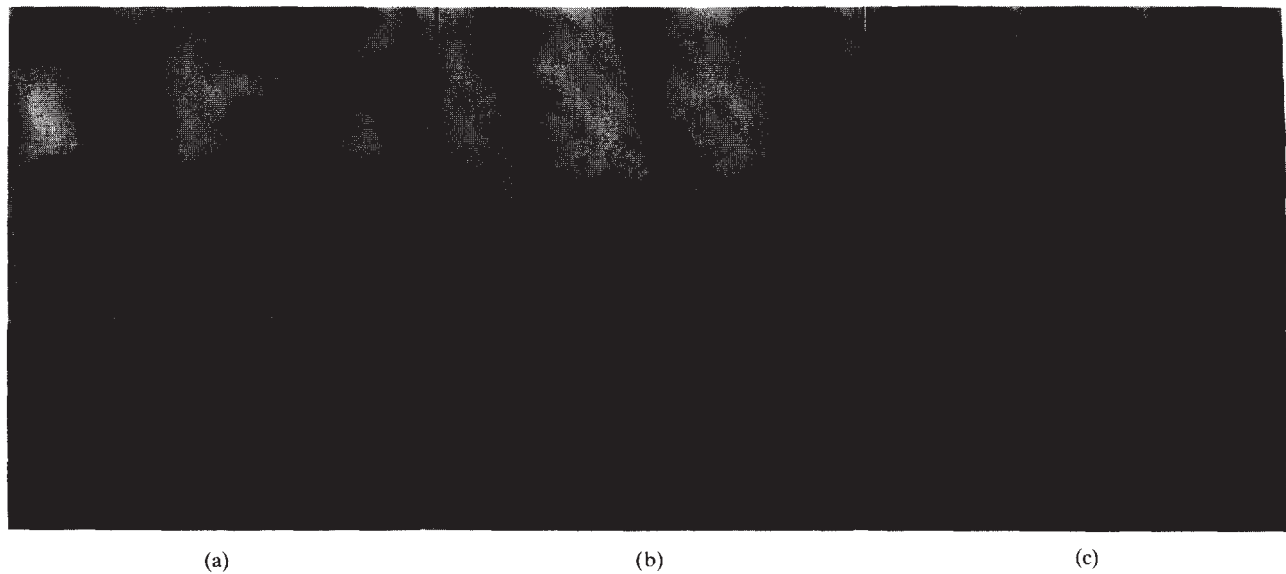


Fig. 11. Cross-sections of AlCu films deposited into trenches using ionized magnetron sputter deposition as a function of ion energy: (a) 20 eV; (b) 70 eV; (c) 120 eV. The relative ionization in these cases was approximately 50% (i.e. 50% of depositing Ti particles were ionized).

lateral deposition on the opposing side of the feature, eventually closing off the feature and forming a void. This can be seen in Fig. 11, where under constant relative ionization (50%), increasing the ion energy and the subsequent sputtering level results in rapid closure of the feature. Recent modeling results confirm this result (Fig. 12) [56]. This effect, though, is only apparent at widths below about  $0.8\ \mu\text{m}$ . For larger lateral dimensions ( $\geq 1\ \mu\text{m}$ ), redeposition does not appear to be significant, regardless of the aspect ratio.

Ionized sputter deposition has also been used to fill multilevel features on a wafer. Typically, these features take the form of a low aspect ratio trench or pad with a hole or via located on the bottom of the feature. These two-layer, or “dual damascene” features eliminate the interface between the via and the pad, which significantly reduces both the number of process steps as well as the reliability and longevity of the structure. An example of using ionized PVD for this type of feature is shown in Fig. 13. In this two-step figure, a  $0.4\ \mu\text{m}$  diameter via is located under a line of width  $1.6\ \mu\text{m}$ . Since the via is not centered

under the line, the aspect ratio of the feature is then direction dependent.

Ionized deposition techniques (both r.f. and ECR based) have the potential for applications both in lining and filling trenches and vias on semiconductors, although it seems likely that for trench-fill applications low ion energies are necessary to suppress sputtering and redeposition. One clear advantage of these techniques is that they are sputtering based, which allows easy control of alloy composition. In addition, these techniques make use of the extensive base of sputtering hardware and experience, which should make their transition into manufacturing applications more rapid. The techniques may eventually replace collimated sputter deposition, which has become widely studied primarily for diffusion barrier and adhesion layer applications. The removal of collimators from the deposition chamber should result in reduced contamination as well as higher effective cathode utilization. The technique has also recently been applied to non-semiconductor applications, such as coating inertial confinement fusion targets or the deposition of hard, carbon-nitride coatings [57].

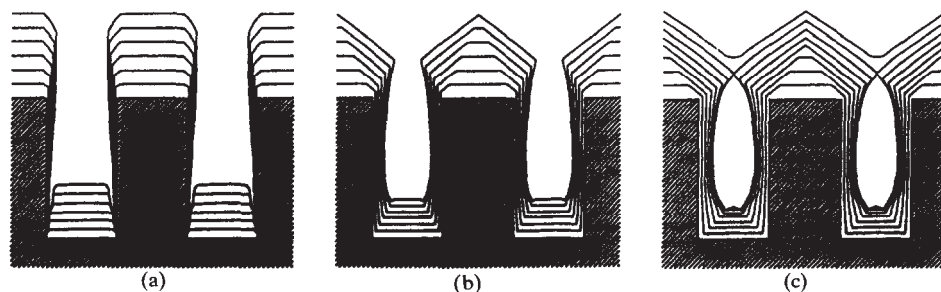


Fig. 12. Computer modeling of Al depositions comparable under conditions similar to Fig. 11(a)–(c) [56]. Total sputtering yields: (a) 0.0; (b) 0.6; (c) 0.8.

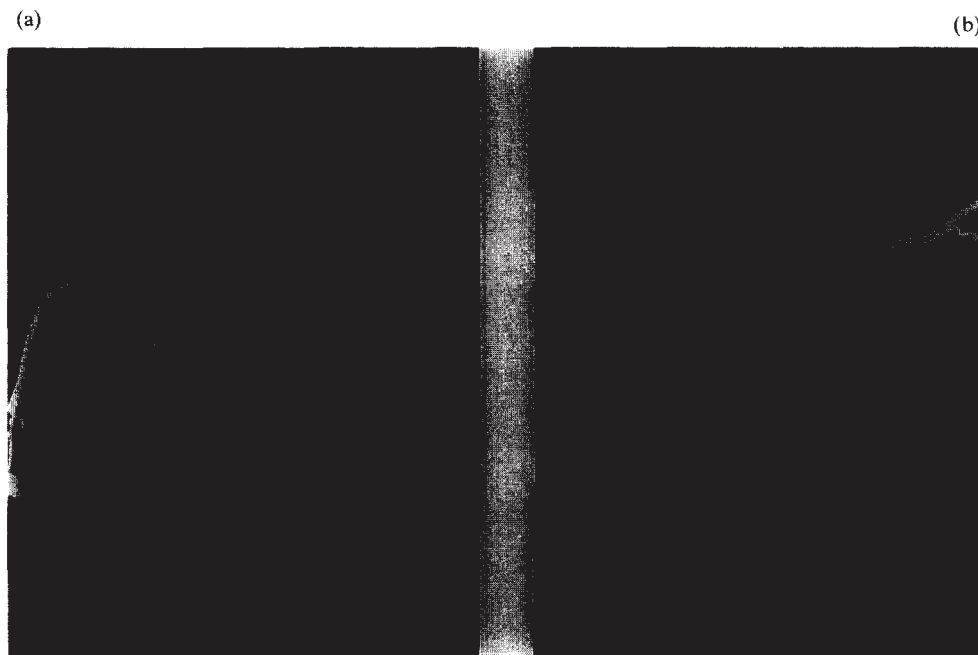


Fig. 13. Cross-section of a two-layer, "dual damascene" trench and via structure. Deposition using ionized magnetron sputtering at  $-60$  V sample bias. (a) 30% filled feature. (b) 80% filled feature.

## 7. Conclusion

Directional and preferential sputtering technologies will extend the use of physical sputtering for several additional generations of microelectronics applications. The preferential deposition technique has the advantage of being mask-less, in that it uses fundamental aspects of the sputtering process to selectively deposit films into features. The raised-temperature sputtering is an interim technology that uses simple re-flow of deposited films in a manner that can be used for fill applications. The technique is limited by the relatively extreme temperature requirements and many residual problems, the worst of which will be simply thermal stress. Collimated sputter deposition and collimated-with-grazing ion bombardment are also interim technologies. By the nature of collimation, a very large fraction of the sputtered flux is collected prior to reaching the film surface. The resultant depositions may be of high quality, but the cost in terms of wasted material, deposition rate and residual issues caused by the thick deposits on the collimators will limit this technology to relatively thin or specialized applications. The ionized technique shows most promise for future application. By ionizing the sputtered atoms, the directionality and energy is easily controlled, which allows much better control of the deposition process for microelectronics applications. There are concerns, however, related to sample heating or large sample currents that must be resolved before this technique can be used routinely.

## References

- [1] R.F. Bunshah, in R.F. Bunshah, (ed.) *Handbook of Deposition Technologies for Films and Coatings*, Noyes Publications, Park Ridge, NJ, 1993, p. 131.
- [2] C. Deshpandey and R.F. Bunshah, in J.L. Vossen and W. Kern (eds.), *Thin film Processes, II*, Academic, New York, 1991, p. 79.
- [3] R. Glang, in L.I. Maissel and R. Glang (eds.), *Handbook of Thin Film Technology*, McGraw Hill, New York, 1970, pp. 1–3.
- [4] P.C. Zalm, *Surf. Interface Anal.*, 11 (1988) 1.
- [5] D. Ruzic, in S.M. Rossnagel, J.J. Cuomo and W. Westwood (eds.), *Handbook of Plasma Processing Technology*, Noyes Publications, Park Ridge, NJ, 1990, Chapt. 3.
- [6] G. Brauer, D. Hasselkamp, W. Kruger and A. Scharmann, *Nucl. Instr. Meth.*, B, 12 (1985) 458.
- [7] C.H. Becker and K.T. Gillen, *Appl. Phys. Lett.*, 45 (1984) 1063.
- [8] P.J. Rudeck, J.M.E. Harper and P.M. Fryer, *Appl. Phys. Lett.*, 53 (1988) 845; *J. Vac. Sci. Technol. A*, 7 (1989) 2289.
- [9] C.W. Kaanta, W.J. Cote, J.E. Cronin, J.S. Landis, W. Hill and J.G. Ryan, *Proc. VMIC Conf.*, 1991, p. 144.
- [10] A.E. Kaloyeros and M.A. Fury, *MRS Bulletin*, (1993) 22.
- [11] J.S.H. Cho, H.-K. Kang, S.S. Wong and Y. Shacham-Diamand, *MRS Bulletin*, (1993) 31.
- [12] J.M.E. Harper, J. Gupta, D.A. Smith, J.W. Chang, K.L. Holloway, C. Cabral, Jr., D.P. Tracey and D.B. Knorr, *Appl. Phys. Lett.*, in press.
- [13] K. Ngan, R. Mosely, Z. Xu and I. Raaijmakers, *Proc. VMIC Conf.*, June 7–8, 1994, p. 452.
- [14] Z. Xu, H. Kieu, T. Yao and I.J. Raaijmakers, *Proc. VMIC Conf.*, June 7–8, 1994, p. 158.
- [15] S. Ogawa, H. Nishimura, T. Kouzaki and R. Sinclair, *Advanced Metallization for ULSI Applications 1992*, Materials Research Society, Pittsburgh, PA, 1993, p. 345.

- [16] K.-C. Chen, S.-T. Hsia, J.-N. Kuo, H. Yen and C.-Y. Lee, *Proc. VMIC Conf.*, June 7–8, 1994, pp. 195, 374.
- [17] E.G. Colgan and K.P. Rodbell, *J. Appl. Phys.*, **75** (1994) 3423.
- [18] J.S. Logan, in S.M. Rossnagel, J.J. Cuomo and W.D. Westwood (eds.), *Handbook of Plasma Processing Technology*, Noyes, Park Ridge, NJ, 1990, Chapt. 5.
- [19] B. Windows and N. Savvides, *J. Vac. Sci. Technol. A*, **4** (1986) 196.
- [20] Y. Homma, S. Tunekawa, A. Satou and T. Terada, *J. Electrochem. Soc.*, **140** (1993) 855.
- [21] S. Berg, I.V. Katardjiev, C. Nender and P. Carlsson, *Thin Solid Films*, **241** (1994) 1.
- [22] J.M.E. Harper, S. Berg, C. Nender, I.V. Katardjiev and S. Motakef, *J. Vac. Sci. Technol. A*, **10** (1992) 1765.
- [23] D. Mikalsen and S.M. Rossnagel, *US Patent 4,824,544* April 25, 1989.
- [24] S.M. Rossnagel, D. Mikalsen, H. Kinoshita and J.J. Cuomo, *J. Vac. Sci. Technol. A*, **9** (1991) 261.
- [25] R.V. Joshi and S. Brodsky, *Proc. 1992 VMIC Conf.*, June 9–10, 1992, p. 253; R.V. Joshi and S. Brodsky, *Appl. Phys. Lett.*, **61** (1992) 2613.
- [26] R. Joshi, J.J. Cuomo, G.W. Dibello and S.M. Rossnagel, *IBM Tech. Discl. Bull.*, **35** (1992) 456.
- [27] S. Roehl, L. Camilletti, W. Cote, D. Cote, E. Eckstein, K.H. Froehner, P.I. Lee, D. Restaino, G. Roeska, V. Vynorius, S. Wolff and B. Vollmer, *Proc. 1992 VMIC Conf.*, June 9–10, 1992, p. 22.
- [28] D.S. Taylor, M.K. Jain, T.S. Cale, M.G. Fissel and I.J. Raaijmakers, *Advanced Metallization for ULSI Applications 1992*, Materials Research Society, Pittsburgh, PA, 1993, p. 353.
- [29] D. Liu, S.K. Dew, M.J. Brett, T. Janacek, T. Smy and W. Tsai, *Thin Solid Films*, **236** (1993) 267.
- [30] D.S. Bang, J.P. McVittie, M.M. Islamraja and K.C. Saraswat, *Proc. 1994 VMIC Conf.*, June 7–8, 1994, p. 554.
- [31] Z. Lin and T.S. Cale, *Proc. 1994 VMIC Conf.*, June 7–8, 1994, p. 552.
- [32] D. Lium, S.K. Dew, M.J. Brett, T. Janacek, T. Smy and W. Tsai, *J. Appl. Phys.*, **74** (1993) 1339.
- [33] T. Hara, T. Nomura and S.C. Chen, *Jpn. J. Appl. Phys.*, **31** (1992) L1746.
- [34] T.J. Licata, T.D. Sullivan, R.S. Bass, J.G. Ryan and D.B. Knorr, *MRS Proc.*, **309** (1993) 87.
- [35] W. Tsai, M. Delfino, J.A. Fair and D. Hodul, *Proc. VMIC Conf.*, June 9–10, 1992, p. 283.
- [36] S. Meikle, S. Kim and T. Doan, *Proc. VMIC Conf.*, June 9–10, 1992, p. 289.
- [37] J. van Gogh, K. Feldmeier, T. Takayama, J. Katsuki and K. Kobayashi, *Proc. VMIC Conf.*, June 9–10, 1992, p. 310.
- [38] H. Kotani, Y. Takata, Y. Hayashide, A. Ohsaki, M. Iwasaki, T. Tsutsumi, M. Matsuura, A. Ishii, Y. Maekawa, I. Tottori, K. Mori, Y. Ii, Y. Tamaguchi and T. Katayama, *Proc. VMIC Conf.*, June 9–10, 1992, p. 15.
- [39] W. Tsai and M. Biberger, *Proc. VMIC Conf.*, June 7–8, 1994, p. 460.
- [40] M. Moïn pour, G. Tseui, R. Sadjadi, D. Hwang, J. Cham, F. Moghadam, S. Tripathi, J. Magana and M.L. Dass, *Proc. VMIC Conf.*, June 7–8, 1994, p. 446.
- [41] R. Powell, private communication, June 1994.
- [42] Y.-W. Kim, J. Moser, I. Petrov, J.E. Greene and S.M. Rossnagel, *J. Vac. Sci. Technol.*, **A12**(6) (1995) 3169.
- [43] J. Givens, T. McDevitt, O. Cain, E. Adams, M. Gibson, J. Riendeau, S. Hazel and D. Sieloff, *Thin Solid Films*, submitted.
- [44] J.J. Cuomo and S.M. Rossnagel, *J. Vac. Sci. Technol.*, **A**, **4** (1986) 393.
- [45] S.M. Rossnagel and R. Sward, *J. Vac. Sci. Technol. A*, submitted.
- [46] D. Mattox, in R.F. Bunshah (ed.) *Handbook of Deposition Technologies for Films and Coatings*, Noyes Publications, Park Ridge, NJ, 1993, p. 320.
- [47] W.M. Holber, J.S. Logan, H.J. Grabarz, J.T.C. Yeh, J.B.O. Caughman, A. Sugarman and F. Turene, *J. Vac. Sci. Technol. A*, **11** (1993) 2903.
- [48] P. Kidd, *J. Vac. Sci. Technol. A*, **9** (1991) 466.
- [49] W. Posadowski and Z.J. Radzinski, *J. Vac. Sci. Technol. A*, **11** (1993) 2980.
- [50] M.S. Barnes, J.C. Forster and J.H. Keller, *US Patent 5,178,739*, Jan. 12, 1993.
- [51] S.M. Rossnagel and J. Hopwood, *Appl. Phys. Lett.*, **63** (1993) 3285.
- [52] S.M. Rossnagel and J. Hopwood, *J. Vac. Sci. Technol.*, **B**, **12** (1994) 449.
- [53] S. Shingubara, N. Morimoto, S. Takehiro, H. Shindo and Y. Horiike, *Advanced Metallization for ULSI Applications 1992*, Materials Research Society, Pittsburgh, PA, 1993, p. 257.
- [54] L.A. Berry, S.M. Gorbakkin and R.L. Rhodes, *Thin Solid Films*, submitted.
- [55] R.S. Robinson, *J. Vac. Sci. Technol.*, **16** (1979) 185.
- [56] S. Hamaguchi and S.M. Rossnagel, *J. Vac. Sci. Technol.*, **B** **13**(2) (1995) 183.
- [57] D. Li, Y.W. Chung, S. Lopez, M.S. Wong and W.D. Sproul, *J. Vac. Sci. Technol.*, **A**(13) (1995).