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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

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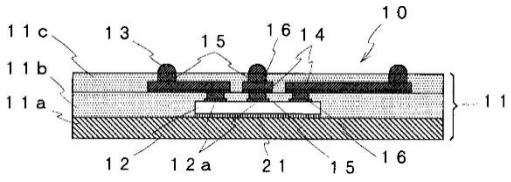
(54) [Title of the Invention] Manufacturing Method for Electronic Circuit Device

(57) [Abstract]

[Problem] To provide a method for manufacturing an electronic circuit device that improves the reliability of the electrical connections between the pads of semiconductor integrated circuits and circuit boards.

[Solution] A bare chip 12 of a semiconductor integrated circuit is mounted on a base substrate 11a on a side with a terminal pads 12a facing upward, an insulating layer 11b is formed on the top surface of the base substrate 11a to cover the terminal pads 12a of the bare chip 12, the insulating layer 11b on the terminal pads 12a is removed to form via holes 15, the via holes 15 are filled with a conductor 16 to establish a conductive connection with the terminal pads 12a, and wiring conductors 14 are formed on the top surface of the insulating layer 11b. An insulating layer 11c is also formed on the wiring conductors 14. In this way, a electronic circuit device 10 is manufactured using the buildup system.



[Claims]

[Claim 1]

A method for manufacturing an electronic circuit device with a multilayer circuit board and a chip-type electronic component having terminal pads on a main surface, the electronic circuit device being manufactured by performing the steps of:
mounting the chip-type electronic component on a base substrate with the main surface on which the terminal pads are formed facing upward;
forming an insulating layer on the top surface of the base substrate to cover the terminal pads of the chip-type electronic component mounted on the base substrate from the sides to the top surface;
removing a portion of the insulating layer above the terminals pad to form via holes;
filling the via holes with a conductor to establish a conductive connection with the terminal pads; and
forming wiring conductors on the top surface of the insulating layer.

[Claim 2]

The method for manufacturing an electronic circuit device according to claim 1, comprising the steps of:
forming a second insulating layer on top of the insulating layer on which the wiring conductors are formed;
removing the second insulating layer above predetermined positions of the wiring conductors to form via holes; and
filling the via holes with a conductor to establish an electrical connection with the wiring conductors.

[Claim 3]

The method for manufacturing an electronic circuit device according to claim 1, wherein a photosensitive resin with electrical insulation properties is used as a material for forming the insulating layer, and the photosensitive resin is coated on the portion to be insulated, and after exposing and curing the photosensitive resin via a photomask covering positions where the via holes are to be formed, non-exposed portions are removed to form via holes.

[Claim 4]

The method for manufacturing an electronic circuit device according to claim 1, wherein a chip electronic component whose terminal pads are made of copper is used, and
in the step of filling the via holes with conductive material to establish a conductive connection to the terminal pads,
an oxide layer on the surface of the terminal pads exposed in the via holes is removed, and
after a palladium treatment is applied to the surface of the terminal pads, a copper plating layer is chemically grown on the surface of the terminal pads to fill the via holes with a conductor.

[Claim 5]

The method for manufacturing an electronic circuit device according to claim 1, wherein in the step of forming the wiring conductors on the surface of the insulating layer, the wiring conductors are formed after roughening the surface of the insulating layer.

[Claim 6]

The method for manufacturing an electronic circuit device according to claim 1, wherein copper is used as the conductor filling the via holes, and in the step of forming the wiring conductors on the surface of the insulating layer,
a copper plating layer is chemically formed on a surface of the insulating layer and the conductors,
the surface of the copper plating layer is coated with a photosensitive resin,
after exposing and curing the photosensitive resin via a photomask covering positions where the via holes are to be formed, non-exposed portions are removed to form via holes,

after removing the photosensitive resin from the non-exposed portion and exposing the copper plating layer, the copper plating layer is dipped in a copper pyrophosphate plating solution and rendered electrically conductive, and
after electrically growing the copper plating layer on the exposed portion of the copper plating layer, the photosensitive resin is removed and the exposed portion of the copper plating layer formed chemically is removed to form the wiring conductors.

[Claim 7]

The method for manufacturing an electronic circuit device according to claim 1, wherein in the step of forming the insulating layer, after spin coating a resin with electrical insulation properties, the resin is cured to form the insulating layer.

[Claim 8]

The method for manufacturing an electronic circuit device according to claim 2, comprising the steps of:
forming lands on a surface of the second insulating layer that are connected conductively to the conductors in the via holes; and
mounting an electronic component on the surface of the second insulating layer and conductively connecting terminal electrodes of the electronic component to the lands.

[Claim 9]

The method for manufacturing an electronic circuit device according to claim 1, wherein the chip-type electronic component is a bare chip of a semiconductor integrated circuit device.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to an electronic circuit device with a multilayer structure and a manufacturing method therefor.

[0002]

[Prior Art]

In recent years, as electronic devices have become smaller, high density mounting of electronic circuit devices with bare semiconductor integrated circuit (IC) chips have come into use. In addition, circuit boards used in electronic circuit devices are being reduced in size by increasing the number of layers, and buildup substrates are increasingly being used to increase the number of layers on a circuit board.

[0003]

When mounting a bare semiconductor IC chip on a circuit board, a flip chip connection is used to mount the chip by connecting the signal pads of the bare chip directly to connection lands on the circuit board.

[0004]

In general, a bare semiconductor IC chip has an array of pads that constitute electrodes along the periphery of one of its surfaces. When a bare chip is mounted directly on a circuit board, solder bumps are formed on the surface of pads, and a flip chip connection is used to electrically connect these solder bumps to the connecting lands on the circuit board via an anisotropic conductive film or an anisotropic conductive resin.

[0005]

[Problem to Be Solved by the Invention]

However, because the pitch between the pads of bare semiconductor IC chips has become even narrower with advances in miniaturization technology, the size of conductive particles in anisotropic conductive films and anisotropic conductive resins is approaching the size of the pads and the pitch between the pads of bare semiconductor IC chips, and this is increasingly causing problems with short circuiting between pads. This is one factor keeping production costs from being lowered.

[0006]

In light of this problem, it is an object of the present invention to provide a method for manufacturing electronic circuit devices that improves the reliability of the electrical connections between the pads of semiconductor integrated circuits and circuit boards.

[0007]

[Means for Solving the Problem]

In order to achieve this object, the invention in claim 1 is a method for manufacturing an electronic circuit device with a multilayer circuit board and a chip-type electronic component having terminal pads on a main surface, the electronic circuit device being manufactured by performing the steps of: mounting the chip-type electronic component on a base substrate with the main surface on which the terminal pads are formed facing upward; forming an insulating layer on the top surface of the base substrate to cover the terminal pads of the chip-type electronic component mounted on the base substrate from the sides to the top surface; removing a portion of the insulating layer above the terminals pad to form via holes; filling the via holes with a conductor to establish a conductive connection with the terminal pads; and forming wiring conductors on the top surface of the insulating layer.

[0008]

In this method for manufacturing an electronic circuit device, an electronic circuit device is manufactured by using a buildup system in which after mounting the chip-type electronic component on a base substrate with the main surface on which the terminal pads are formed facing upward, an insulating layer is formed on the top surface of the base substrate to cover the terminal pads of the chip-type electronic component, and the insulating layer above a terminal pad is removed to form a via hole, and after the via hole has been filled with a conductor to establish a conductive connection with the terminal pad, a wiring conductor is formed on the top surface of the insulating layer. This produces an electronic circuit device in which the chip-shaped electronic components are embedded inside a multilayer circuit board.

[0009]

The invention in claim 2 is the method for manufacturing an electronic circuit device according to claim 1, comprising the steps of: forming a second insulating layer on top of the insulating layer on which the wiring conductors are formed; removing the second insulating layer above predetermined positions of the wiring conductors to form via holes; and filling the via holes with a conductor to establish an electrical connection with the wiring conductors.

[0010]

The invention in claim 3 is the method for manufacturing an electronic circuit device according to claim 1, wherein a photosensitive resin with electrical insulation properties is used as a material for forming the insulating layer, and the photosensitive resin is coated on the portion to be insulated, and after exposing and curing the photosensitive resin via a photomask covering positions where the via holes are to be formed, non-exposed portions are removed to form via holes.

[0011]

In this method of manufacturing an electronic circuit device, the insulating layer is formed using a photosensitive resin. In this way, an insulating layer of the desired thickness can be easily formed, and via holes of the desired diameter can be accurately formed at the desired locations.

[0012]

The invention in claim 4 is the method for manufacturing an electronic circuit device according to claim 1, wherein a chip electronic component whose terminal pads are made of copper is used, and in the step of filling the via holes with conductive material to establish a conductive connection to the terminal pads, an oxide layer on the surface of the terminal pads exposed in the via holes is removed, and after a palladium treatment is applied to the surface of the terminal pads, a copper plating layer is chemically grown on the surface of the terminal pads to fill the via holes with a conductor.

[0013]

In this method for manufacturing an electronic circuit device, the oxide layer of the terminal pad is removed and palladium is applied to the surface of the terminal pad by palladium treatment, which facilitates the growth of a chemical copper plating layer.

[0014]

The invention in claim 5 is the method for manufacturing an electronic circuit device according to claim 1, wherein in the step of forming the wiring conductors on the surface of the insulating layer, the wiring conductors are formed after roughening the surface of the insulating layer.

[0015]

In this method for manufacturing an electronic circuit device, the wiring conductors are formed after roughening the surface of the insulating layer, which increases the contact area between the surface of the insulating layer and the wiring conductors and the bonding strength between them.

[0016]

The invention in claim 6 is the method for manufacturing an electronic circuit device according to claim 1, wherein copper is used as the conductor filling the via holes, and in the step of forming the wiring conductors on the surface of the insulating layer, a copper plating layer is chemically formed on a surface of the insulating layer and the conductors, the surface of the copper plating layer is coated with a photosensitive resin, after exposing and curing the photosensitive resin via a photomask covering positions where the via holes are to be formed, non-exposed portions are removed to form via holes, after removing the photosensitive resin from the non-exposed portion and exposing the copper plating layer, the copper plating layer is dipped in a copper pyrophosphate plating solution and rendered electrically conductive, and after electrically growing the copper plating layer on the exposed portion of the copper plating layer, the photosensitive resin is removed and the exposed portion of the copper plating layer formed chemically is removed to form the wiring conductors. This makes it easy to form wiring conductors.

[0017]

The invention in claim 7 is the method for manufacturing an electronic circuit device according to claim 1, wherein in the step of forming the insulating layer, after spin coating a resin with electrical insulation properties, the resin is cured to form the insulating layer.

[0018]

The invention in claim 8 is the method for manufacturing an electronic circuit device according to claim 2, comprising the steps of: forming lands on a surface of the second insulating layer that are connected conductively to the conductors in the via holes; and mounting an electronic component on

the surface of the second insulating layer and conductively connecting terminal electrodes of the electronic component to the lands.

[0019]

The manufacturing method for an electronic circuit device produces an electronic circuit device in which electronic components are mounted on a multilayer circuit board in which chip-type electronic components are embedded.

[0020]

The invention in claim 9 is the method for manufacturing an electronic circuit device according to claim 1, wherein the chip-type electronic component is a bare chip of a semiconductor integrated circuit device.

[0021]

This method for manufacturing an electronic circuit device can easily produce multilayer circuit boards in which bare chips of semiconductor integrated circuit elements have been embedded.

[0022]

[Embodiments of the Invention]

Embodiments of the present invention will now be described with reference to the drawings.

[0023]

FIG. 1 is a side cross-sectional view of an electronic circuit device in the first embodiment of the present invention. In the figure, 10 is an electronic circuit device in which a bare chip 12 of a semiconductor integrated circuit is embedded inside a multilayer circuit board 11 and has solder bumps 13 serving as external electrodes on the top surface of the multilayer circuit board 11 connected to terminal pads of the bare chip 12. In other words, the electronic circuit device 10 is a bare chip 12 package formed in a multilayer circuit board.

[0024]

The multilayer circuit board 11 consists of a plurality of insulating layers 11a-11c, wiring conductors 14 provided between the insulating layers, and conductors 16 filling the via holes 15. The bottom insulating layer 11a in the figure serves as the base substrate, and the material can be a resin, metal, ceramic, etc. The other insulating layers 11b, 11c are made of resin.

[0025]

The bare chip 12 has a rectangular plate shape and a plurality of terminal pads 12a made of copper (Cu) arranged in a grid pattern on one of the main surfaces (the top surface in FIG. 1). Each of these terminal pads 12a is conductively connected to a solder bump 13 formed on the surface of the top insulating layer 11c via conductors 16 and wiring conductors 14 in via holes 15.

[0026]

An electronic circuit device 10 with the configuration described above is formed using the following manufacturing method. The manufacturing method for the electronic circuit device 10 will be described with reference to FIG. 2 to FIG. 15.

[0027]

First, an alumina substrate 21 with a thickness of 0.3 mm is prepared as the insulating layer 11a serving as the base substrate. A bare chip 12 is bonded to the top surface of the insulating layer 11a

with epoxy resin 22, with the back side of the bare chip 12 facing upward, that is, the side with the terminal pads 12a facing upward (FIG. 2).

[0028]

Here, the epoxy resin 22 is applied so that it is 5 μm thick after curing. The linear expansion coefficient of the epoxy resin 22 is adjusted to within ± 20% of the linear expansion coefficient of the alumina substrate 21 and silicon (Si).

[0029]

Next, an epoxy-based photosensitive resin (viscosity: 20 ps) 23 that is resistant to the plating solution used below is spin-coated to cover the bare chip 12 placed on the alumina substrate 21 (FIG. 3). The spin coater is adjusted so that the top of the bare chip 12 is coated to a thickness of 20 μm. Polyimide or some other resin may be used in the insulating layer as long as it is resistant to the plating solution.

[0030]

Next, after the photosensitive resin 23 has dried, the photosensitive resin 23 is exposed, developed, and cured using a photomask (not shown) whose pattern is arranged to cover only the Cu terminal pads 12a of the bare chip 12. In this way, an insulating layer 11b is formed with openings only above the Cu terminal pads 12a (FIG. 4). These openings 23a become the via holes 15.

[0031]

Next, the oxide layer formed on the surface of the Cu terminal pads 12a is removed with an acidic solution, followed by palladium treatment. Palladium selectively adheres to the surface of the Cu terminal pads 12a. This is followed by Cu chemical plating. This causes a Cu plating layer 24 to grow on the Cu terminal pads 12a. The Cu chemical plating process is carried out in this way until the via holes 15 are completely filled with a the Cu plating layer 24 (FIG. 5). Cu plating layers 24 fill the via holes 15 and become conductors 16.

[0032]

After the via holes 15 have been filled with Cu plating 24, the surface of the insulating layer 11b is roughened moderately using a solution composed primarily of potassium permanganate. This increases the contact area between the surface of the insulating layer 11b and the wiring conductors 14 formed on it, which increases the bonding strength between them and improves reliability.

[0033]

Next, a chemical Cu plating is applied to the top surface of insulating layer 11b and the Cu filling the via holes 15 to form a Cu plating layer 25 with a thickness of 0.3 μm (FIG. 6).

[0034]

Next, the surface of this chemical Cu plating layer 25 is coated with a photosensitive resin 26 to a thickness of 10 μm (FIG. 7).

[0035]

Next, after the photosensitive resin 26 has dried, the photosensitive resin 26 is exposed, developed, and cured using a photomask (not shown) in which the wiring pattern of the first layer has been arranged. In this way, an insulating layer with openings 26a corresponding to the wiring pattern is formed (FIG. 8).

[0036]

Afterward, the Cu chemical plating layer 25 is electrified in a pyrophosphate Cu plating bath (current density: 60 A/m^2) to grow an electrical Cu plating layer 27 with a height of 10 μm in the wiring pattern openings 26a (FIG. 9).

[0037]

Next, the insulating layer formed by the photosensitive resin 26 is removed with a special delaminating solution (FIG. 10), and then the exposed portions of the Cu chemical plating layer 25 alone are completely removed using an 8% wt-HCl solution (FIG. 11). This forms the first layer of wiring conductors 14.

[0038]

Afterward, the surface of the Cu plating layer 27 is blackened with a solution composed primarily of sodium chlorite, and the same photosensitive resin (viscosity: 20 ps) 23 described above is spin-coated to cover the Cu plating layer 27 (FIG. 12). The spin coater is adjusted so that the coating is applied at a thickness of 20 μm on the Cu plating layer 27.

[0039]

Next, after the photosensitive resin 23 has dried, the photosensitive resin 23 is exposed, developed, and cured using a photomask (not shown) whose pattern is arranged to cover only the positions where via holes 15 have been formed. The photomask used has a pattern where there are the via holes 15 connecting the first and second layer wiring.

[0040]

In this way, an insulating layer 11c is formed with openings 23a that will become via holes 15 (FIG. 13).

[0041]

Next, an oxide layer formed on the surface of the Cu wiring conductors 14 exposed at the bottom of the openings 23a is removed with an acidic solution, followed by palladium treatment as described above. Palladium selectively adheres to the surface of the Cu wiring conductors 14. Afterward, Cu chemical plating is applied. This causes a Cu plating layer 28 to grow on the Cu wiring conductors 14. Cu chemical plating is performed in this way until the via holes 15 have been completely filled with a Cu plating layer 28 (FIG. 14). The Cu plating layer 28 filling the via holes 15 become conductors 16.

[0042]

After the via holes 15 have been filled by Cu plating, solder bumps 13 are formed on the Cu plating layers 28 in the via holes 15 exposed on the surface of the top insulating layer 11c (FIG. 15). This completes the electronic circuit device 10.

[0043]

Solder bumps 13 are formed by plating or solder balls. Bonding pads may also be formed instead of solder bumps 13.

[0044]

By repeating the steps described above as appropriate, a multilayer circuit board with the desired number of layers can be formed. Other bare chips can be embedded in any layer, and chip electronic components other than bare chips can also be easily embedded.

[0045]

Since this manufacturing method is a buildup system in which via holes 15 are formed in the insulating layer 11b above the terminal pads 12a of the bare chips 12 and in which Cu plating formed in the via holes 15 become conductors 16, the electrical connection between terminal pads 12a and conductors 16 can be improved.

[0046]

Also, because the via holes 15 are formed using photosensitivity, via holes 15 with a fine diameter are easy to form, and sufficient insulation can be maintained between adjacent via holes when the pitch between the terminal pads 12a of the bare chip 12 is narrower.

[0047]

Conductors 16 are formed in the via holes 15 using a plating process, making them easy to form.

[0048]

A second embodiment of the present invention will now be described.

[0049]

FIG. 16 is a side cross-sectional view of the electronic circuit device 30 in the second embodiment of the present invention. In this figure, elements that are identical to those in the first embodiment are denoted by the same reference numbers, and further explanation of these elements has been omitted. The difference between the second embodiment and the first embodiment is that instead of an alumina substrate 21 serving as the base substrate, a base substrate 31 is used in which some portions are made of a metal 32 with high thermal conductivity and other portions are made of resin. The bare chip 12 is mounted on the surface of the metal 32. This allows the heat generated by the bare chip 12 to dissipate efficiently to the outside.

[0050]

A third embodiment of the present invention will now be described.

[0051]

FIG. 17 is a side cross-sectional view of the electronic circuit device 40 in the third embodiment of the present invention. In this figure, elements that are identical to those in the first embodiment are denoted by the same reference numbers, and further explanation of these elements has been omitted. The difference between the third embodiment and the first embodiment is that a multilayer circuit board 41 with four insulating layers 41a-41d is provided by increasing the number of layers, lands 42 for mounting components and the wiring conductors 43 are formed on the top surface of the multilayer circuit board 41 to mount electronic components 44, and solder bumps 45 for connections are formed on the bottom surface of the base substrate 41a at the bottom. Here, the manufacturing method is the same as in the first embodiment.

[0052]

The embodiments described above are examples of the present invention, which is not limited to these embodiments.

[0053]

[Effects of the Invention]

As explained above, the method for manufacturing an electronic circuit device according to claims 1 to 9 of the present invention uses a buildup system in which chip-type electronic components are embedded inside multilayer circuit boards, via holes are formed on the terminal pads of the chip-type electronic component and filled with conductors to connect the terminal pads and conductors, and wiring

conductors are formed to connect to the conductors. In this way, the electrical connection between the terminal pads, the conductors, and the wiring conductors can be improved, and short-circuits between terminal pads become less likely even when pitch between terminal pads is narrower.

[0054]

In claim 3, in addition to the effects described above, the via holes are formed using photosensitivity. In this way, via holes with a fine diameter are easy to form, and sufficient insulation can be maintained between adjacent via holes when the pitch between the terminal pads of the bare chip is narrower.

[0055]

In claim 4, in addition to the effects described above, conductors in via holes with conductive connections to terminal pads can be easily formed.

[0056]

In claim 5, in addition to the effects described above, the wiring conductors are formed after roughening the surface of the insulating layer. This increases the contact area between the surface of the insulating layer and the wiring conductors and the bonding strength between them.

[0057]

In claim 6, in addition to the effects described above, wiring conductors can be easily formed on an insulating layer.

[0058]

In claim 7, in addition to the effects described above, it is easier to form an insulating layer with a flat surface and no unevenness.

[0059]

In claim 8, in addition to the effects described above, smaller electronic circuit devices with chip-type electronic components can be realized.

[0060]

In claim 9, in addition to the effects described above, smaller electronic circuit devices with chip-type electronic components can be realized, and the multilayer circuit board itself, in which bare chips of semiconductor integrated circuits have been embedded, serves as a bare chip package.

[Brief Description of the Drawings]

[FIG. 1]

FIG. 1 is a side cross-sectional view of the electronic circuit device in the first embodiment of the present invention.

[FIG. 2]

FIG. 2 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 3]

FIG. 3 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 4]

FIG. 4 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 5]

FIG. 5 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 6]

FIG. 6 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 7]

FIG. 7 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 8]

FIG. 8 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 9]

FIG. 9 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 10]

FIG. 10 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 11]

FIG. 11 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 12]

FIG. 12 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 13]

FIG. 13 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 14]

FIG. 14 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 15]

FIG. 15 is a process diagram used to explain the manufacturing method in the first embodiment of the present invention.

[FIG. 16]

FIG. 16 is a side cross-sectional view of the electronic circuit device in the second embodiment of the present invention.

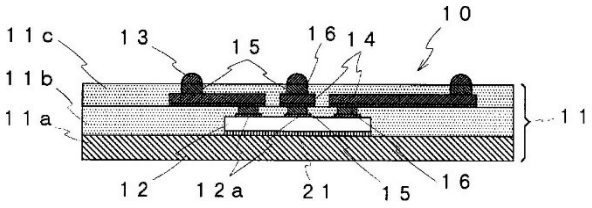
[FIG. 17]

FIG. 17 is a side cross-sectional view of the electronic circuit device in the third embodiment of the present invention.

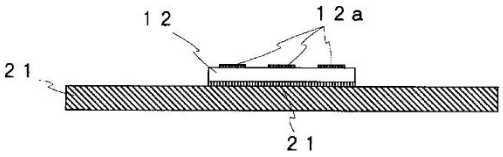
[Key to the Drawings]

10, 30, 40: Electronic circuit device
11: Multilayer circuit board
11a, 11b, 11c: Insulating layer
12: Semiconductor integrated circuit bare chip
12a: Terminal pad
13: Solder bump
14: Wiring conductor
15: Via hole
16: Conductor
21: Alumina substrate
22: Epoxy resin
23: Photosensitive resin
23a: Opening
24: Cu plating layer
25: Cu plating layer
26: Photosensitive resin
27: Cu plating layer
28: Cu plating layer
31: Base substrate
32: Thermally conductive metal
41: Multilayer circuit board
41a-41d: Insulating layer
42: Land
43: Wiring conductor
44: Electronic component
45: Solder bump

[FIG. 1]



[FIG. 2]



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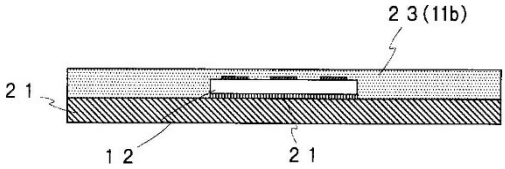

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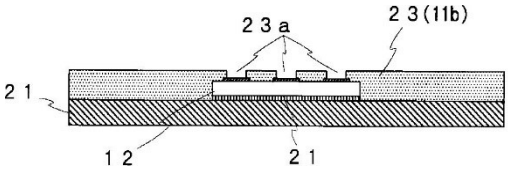
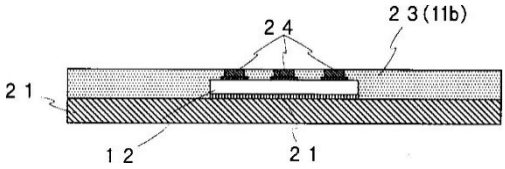
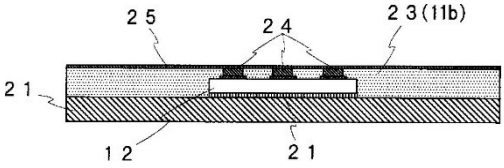


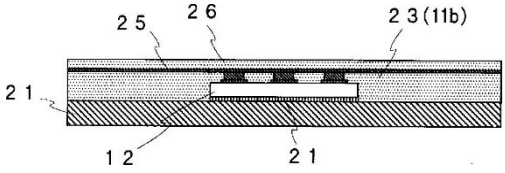
[FIG. 5]



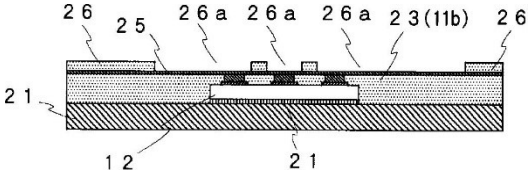
[FIG. 6]



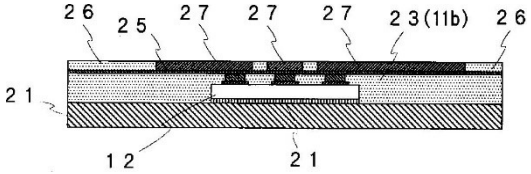
[FIG. 7]



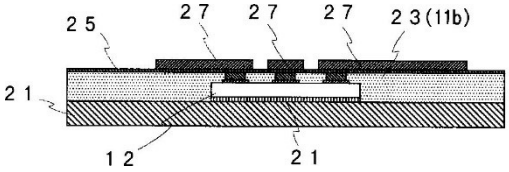
[FIG. 8]



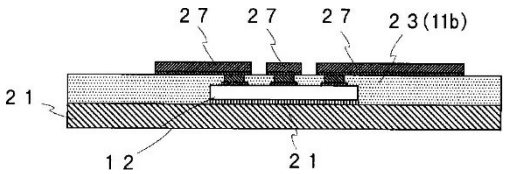
[FIG. 9]



[FIG. 10]



[FIG. 11]



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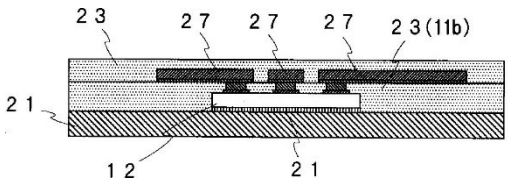
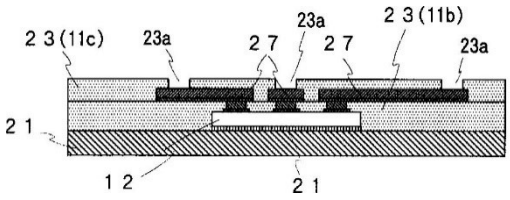
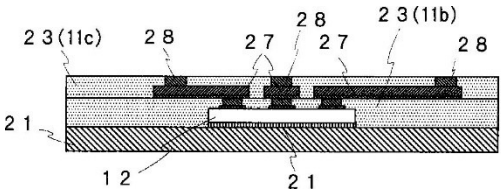


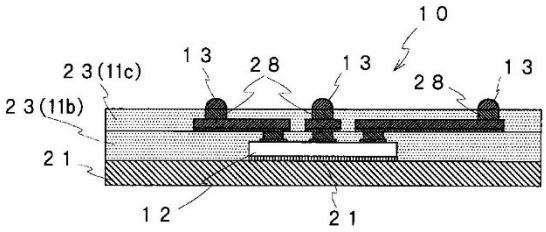
[FIG. 13]



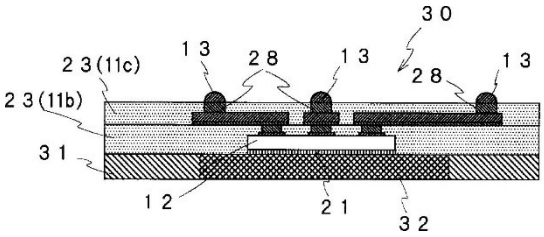
[FIG. 14]



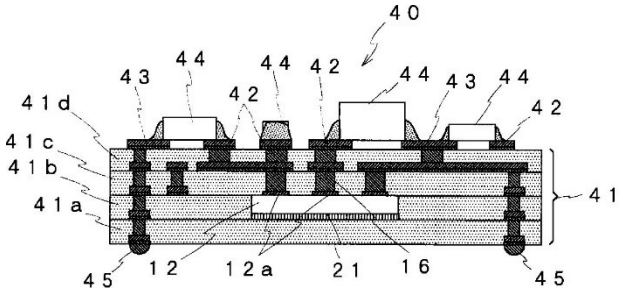
[FIG. 15]



[FIG. 16]



[FIG. 17]



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