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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

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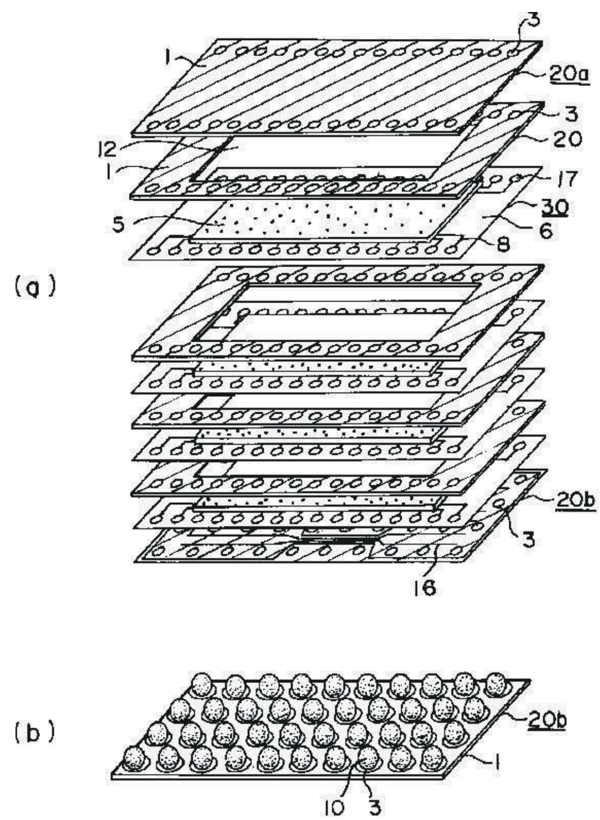
(54) [Title of the Invention] SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE MANUFACTURING METHOD

(57) [ABSTRACT]

PROBLEM
To provide: a semiconductor device using a laminated package that is thin, has excellent sealability and elasticity, and that can be easily formed with a simplified manufacturing process; and a manufacturing method thereof.

MEANS FOR SOLUTIONS
The semiconductor device includes: a plurality of wiring substrates 30 having a plurality of vias with a connection electrode formed below a land 17 and having wiring 8 electrically connected to the connection electrode; a semiconductor element 5 mounted on the wiring substrate and electrically connected to the wiring; and a plurality of conductive via insulating substrates 20 having a chip cavity section 12 that is larger than the semiconductor element volume in which the semiconductor element is stored when the semiconductor element is mounted and having a connection electrode embedded in the plurality of vias and formed below a land 3. The thickness of the semiconductor element is approximately 30 to 200 μm. A semiconductor device having a thin laminated package can be obtained. Even if the semiconductor element is slightly stretched due to bending the semiconductor device, a space between the semiconductor element and the chip cavity section absorbs the stretching of the semiconductor element.



What is claimed is:

[Claim 1]
A semiconductor device, comprising:
a plurality of wiring substrates each having a plurality of vias each with a connection electrode formed and wiring electrically connected to the connection electrode;
a semiconductor element mounted on the wiring substrate and electrically connected to the wiring; and
a plurality of conductive via insulating substrates having a chip cavity section that is larger than the semiconductor element volume in which the semiconductor element is stored when the semiconductor element is mounted and having a formed connection electrode embedded in the plurality of vias; wherein
one of the conductive via insulating substrates and one of the wiring substrates are laminated such that the connection wiring of the conductive via insulating substrate and connection electrode of the wiring substrate are electrically connected to the wiring substrate to form a laminate, and a plurality of these laminates are laminated and integrated in a condition where the semiconductor element mounted to the wiring substrate is completely stored in the chip cavity section.

[Claim 2]
A semiconductor device, comprising:
a plurality of wiring substrates each having a plurality of vias each with a connection electrode formed and wiring electrically connected to the connection electrode;
a semiconductor element mounted on the wiring substrate and electrically connected to the wiring;
a plurality of conductive via insulating substrates having a chip cavity section that is larger than the semiconductor element volume in which the semiconductor element is stored when the semiconductor element is mounted and having a connection electrode formed embedded in the plurality of vias; and
a conductive via insulating substrate of an upper layer laminated above a conductive via insulating substrate of an uppermost layer when the wiring substrate and the conductive via insulating substrate are laminated, and having connection electrodes formed embedded in the plurality of vias; wherein
one of the conductive via insulating substrates and one of the wiring substrates are laminated such that the connection wiring of the conductive via insulating substrate and connection electrode of the wiring substrate are electrically connected to the wiring substrate to form a laminate, and a plurality of the laminates are laminated and integrated in a condition where the semiconductor element mounted to the wiring substrate is completely stored in the chip cavity section.

[Claim 3]
The semiconductor device according to claim 1 or 2, wherein the semiconductor element has a thickness of approximately 30 to 200 μm.

[Claim 4]
The semiconductor device according to any one of claims 1 to 3, further comprising: a conductive via insulating substrate of a lower layer in which a plurality of the laminated laminates are laminated, and having a connection electrode formed embedded in the plurality of vias; wherein a wiring substrate on a lowermost layer of the laminate is in contact with a first surface of the conductive via insulating substrate of the lower layer, the connection electrode of the wiring substrate on the lowermost layer and the connection electrode of the conductive via insulating substrate of the lower layer are electrically connected, and a plurality of external terminals electrically connected with the connection electrode formed in the via through wiring are formed on a second surface of the lower layer.

[Claim 5]
The semiconductor device according to any one of claims 1 to 4, wherein a stress-absorbing space is formed between the chip cavity section of the conductive via insulating substrate and the semiconductor element stored in the chip cavity section.

[Claim 6]
The semiconductor device according to claim 4, wherein a flexible adhesive is filled into the space.

[Claim 7]
A method of manufacturing a semiconductor device, comprising:
a step of forming a plurality of wiring substrates each having a plurality of vias each with a connection electrode formed and wiring electrically connected to the connection electrode;
a step of mounting a semiconductor element electrically connected to the wiring on the wiring substrate;
a step of forming a plurality of conductive via insulating substrates formed in an adhesive layer on a back surface having a chip cavity section that is larger than the semiconductor element volume in which the semiconductor element is stored when mounting the semiconductor element and having a connection electrode formed embedded in the plurality of vias; and
a step of laminating one of the conductive via insulating substrates and one of the wiring substrates such that the connection wiring of the conductive via insulating substrate and connection electrode of the wiring substrate are electrically connected to the wiring substrate, adhering these using the adhesive to form a laminate, laminating a plurality of the laminates in a condition where the semiconductor element mounted to the wiring substrate is completely stored in the chip cavity section, and then integrating these.

[Claim 8]
A method of manufacturing a semiconductor device, comprising:
a step of forming a plurality of wiring substrates having wiring formed on a main surface;
a step of mounting a semiconductor element electrically connected to the wiring on the wiring substrate having wiring;
a step of forming a plurality of conductive via insulating substrates formed in an adhesive layer on a back surface having a chip cavity section that is larger than the semiconductor element volume in which the semiconductor element is stored when mounting the semiconductor element;
a step of alternately laminating the plurality of conductive via insulating substrates and the plurality of wiring substrates, adhering these using the adhesive to form a laminate, laminating a plurality of the laminates in a condition where the semiconductor element mounted to the wiring substrate is completely stored in the chip cavity section, and then integrating these; and
a step of forming a via penetrating these in a condition where the plurality of laminates are laminated, and forming a connection electrode in the via.

[Claim 9]
The method of manufacturing a semiconductor device according claim 7 or 8, further comprising a step of cutting an integrated laminate in the direction of lamination after the step of integrating a plurality of laminates obtained by mounting a plurality of the semiconductor elements on the wiring substrates, forming a plurality of the conductive sections in the conductive via insulating substrates, and laminating these wiring substrates and conductive via insulating substrates.

[Claim 10]
The method of manufacturing a semiconductor device according to any one of claims 7 to 9, wherein the semiconductor element has a thickness of approximately 30 to 200 μm.

DETAILED DESCRIPTION OF THE INVENTION

[0001]
TECHNOLOGICAL FIELD OF THE PRESENT INVENTION
The present invention relates to: a semiconductor device using a laminated package in which a plurality of semiconductor elements are laminated; and a manufacturing method thereof.

[0002]
CONVENTIONAL TECHNOLOGY
Semiconductor devices are often used by laminating semiconductor elements to achieve high-density mounting. Conventionally used laminated packages are described in Japanese Unexamined Patent Application H9-219490, Japanese Unexamined Patent Application H10-135267, and Japanese Unexamined Patent Application H10-163414, for example. In these conventional packages, after packages such as TSOP (Thin Small Outline Package), TCP (Tape Carrier Package), BAG (Ball Grid Array), or the like are completely assembled, each package is laminated by individually laminating external terminals provided in advance on each package, and further electrical connections are made. In other words, in addition to the assembly step for each package, a lamination processing step is added for each package in conventional laminated packages. Therefore, a sequential method is used in which the number of steps increases by the number of laminations, and the increase in processing cost due to this method and increase in cost due to the use of individually laminated members such as spacers and the like pose major problems.

[0003]
PROBLEMS TO BE SOLVED BY THE INVENTION
Furthermore, in addition to the problems described above, laminating separate packages causes adhesion and lamination interfaces for each package, and the mechanical strength of the laminated package are limited only by the electrical connections. Moreover, for example, in the conventional examples described in Japanese Unexamined Patent Application H10-163414, Japanese Unexamined Patent Application H10-135267, and the like, semiconductor elements have a floating structure, which makes it difficult to ensure mechanical strength and sufficient reliability. Furthermore, there are problems with difficulty in using a conventional method described above to form a thin laminated package that is suitable for thin semiconductor chips with a thickness of approximately 30 to 200 μm for the development of semiconductor devices which are expected to become thinner and denser in the future and have increased application, such as IC cards, mobile phones, and the like, and with applicability due to lack of elasticity for use in resilient media such as IC cards. In view of the foregoing, an object of the present invention is to provide: a semiconductor device using a laminated package that is thin, has excellent sealability and elasticity, and can be easily formed without a complicated manufacturing process; and a manufacturing method thereof.

[0004]
MEANS FOR SOLVING THE PROBLEM
A first aspect of a semiconductor device of the present invention is that it contains: a plurality of wiring substrates each having a plurality of vias each with a connection electrode formed and wiring electrically connected to the connection electrode; a semiconductor element mounted on the wiring substrate and electrically connected to the wiring; and a plurality of conductive via insulating substrates having a chip cavity section that is larger than the semiconductor element volume in which the semiconductor element is stored when the semiconductor element is mounted and having a connection electrode formed embedded in the plurality of vias; where one of the conductive via insulating substrates and one of the wiring substrates are laminated such that the connection wiring of the conductive via insulating substrate and connection electrode of the wiring substrate are electrically connected to the wiring substrate to form a laminate, and a plurality of the laminates are laminated and integrated in a condition where the semiconductor element mounted to the wiring substrate is completely stored in the chip cavity section.

[0005]
A second aspect of a semiconductor device of the present invention is that it contains: a plurality of wiring substrates each having a plurality of vias each with a connection electrode formed and wiring electrically connected to the connection electrode; a semiconductor element mounted on the wiring substrate and electrically connected to the wiring; a plurality of conductive via insulating substrates having a chip cavity section that is larger than the semiconductor element volume in which the semiconductor element is stored when the semiconductor element is mounted and having a connection electrode formed embedded in the plurality of vias; and a conductive via insulating substrate of an upper layer laminated above a conductive via insulating substrate of an uppermost layer when the wiring substrate and the conductive via insulating substrate are laminated, and having connection electrodes formed embedded in the plurality of vias; where one of the conductive via insulating substrates and one of the wiring substrates are laminated such that the connection wiring of the conductive via insulating substrate and connection electrode of the wiring substrate are electrically connected to the wiring substrate to form a laminate, and a plurality of the laminates are laminated and integrated in a condition where the semiconductor element mounted to the wiring substrate is completely stored in the chip cavity section. The thickness of the semiconductor element may be approximately 30 to 200 μm.

[0006]
A conductive via insulating substrate of a lower layer may be provided, in which a plurality of the laminated laminates are laminated and having a connection electrode formed embedded in the plurality of vias. The wiring substrate on a lowermost layer of the laminate may be in contact with a first surface of the conductive via insulating substrate of the lower layer, the connection electrode of the wiring substrate on the lowermost layer and the connection electrode of the conductive via insulating substrate of the lower layer may be electrically connected, and a plurality of external terminals electrically connected with the connection electrode formed in the via through wiring may be formed on a second surface of the lower layer. A stress-absorbing space may be formed between the chip cavity section of the conductive via insulating substrate and the semiconductor element stored in the chip cavity section. A flexible adhesive may be filled into the space.

[0007]
With the configuration above, a semiconductor device having a thin laminated package can be obtained. Furthermore, the laminated package is sandwiched between the conductive via insulating substrates on upper and lower sides, and therefore has high sealability with respect to the semiconductor element.

Furthermore, the semiconductor element is stored in the chip cavity section formed in the conductive via insulating substrate. However, the thickness and area of the chip cavity section is smaller than the semiconductor element, and therefore, even if the semiconductor element is stored therein, a space is formed between the semiconductor element and the inner wall of the chip cavity section. For example, a space is present between the semiconductor element and the chip cavity section even if the semiconductor element is slightly stretched due to bending the semiconductor device, and thus the space can absorb stretching of the semiconductor element. Therefore, stress generated when an external force is applied to the semiconductor device can be absorbed. Furthermore, the space is filled with an adhesive material that adheres the conductive via insulating substrate to the wiring substrate. In particular, if a flexible adhesive material such as silicon resin or the like is used, stress can be absorbed and sealability can be improved to enhance the moisture resistance of the semiconductor device.

[0008]
A first aspect of a method of manufacturing a semiconductor device of the present invention is that it includes a step of forming a plurality of wiring substrates each having a plurality of vias each with a connection electrode formed and wiring electrically connected to the connection electrode, a step of mounting a semiconductor element electrically connected to the wiring on the wiring substrate, and a step of forming a plurality of conductive via insulating substrates formed in an adhesive layer on a back surface having a chip cavity section that is larger than the semiconductor element volume in which the semiconductor element is stored when mounting the semiconductor element and having a connection electrode formed embedded in the plurality of vias; and includes a step of laminating one of the conductive via insulating substrates and one of the wiring substrates such that the connection wiring of the conductive via insulating substrate and connection electrode of the wiring substrate are electrically connected to the wiring substrate, adhering these using the adhesive to form a laminate, laminating a plurality of the laminates in a condition where the semiconductor element mounted to the wiring substrate is completely stored in the chip cavity section, and then integrating these.

[0009]
Furthermore, a second aspect of a method of manufacturing a semiconductor device of the present invention includes: a step of forming a plurality of wiring substrates having wiring formed on a main surface; a step of mounting a semiconductor element electrically connected to the wiring on the wiring substrate; a step of forming a plurality of conductive via insulating substrates formed in an adhesive layer on a back surface having a chip cavity section that is larger than the semiconductor element volume in which the semiconductor element is stored when the mounting semiconductor element; a step of alternately laminating the plurality of conductive via insulating substrates and the plurality of wiring substrates, adhering these using the adhesive to form a laminate, laminating a plurality of the laminates in a condition where the semiconductor element mounted to the wiring substrate is completely stored in the chip cavity section, and then integrating these; and a step of forming a via penetrating these in a condition where the plurality of laminates are laminated, and forming a connection electrode in the via. Also provided may be a step of cutting an integrated laminate in the direction of lamination after the step of integrating a plurality of laminates obtained by mounting a plurality of the semiconductor elements on the wiring substrates, forming a plurality of the conductive sections in the conductive via insulating substrates, and laminating these wiring substrates and conductive via insulating substrates. By collectively laminating and cutting a semiconductor element layer, a supporting wiring substrate, and a conductive via insulating substrate, manufacturing is possible in fewer steps than with conventional techniques for laminating packages.

[0010]
EMBODIMENTS OF THE INVENTION
Embodiments of the present invention will be described below while referring to the drawings. First, Embodiment 1, which is a semiconductor device using a laminated package, will be described while referring to FIG. 1. FIG. 1(a) is a perspective view of a semiconductor device using a laminated package, and FIG. 1(b) is a perspective view illustrating external terminals of a conductive via laminated board of a lower layer of the laminated package. This embodiment is an example of four laminated semiconductor elements, but the number of semiconductor elements to be laminated is not limited to four, as in the present invention. Any required number of two or more can be laminated. The package includes a conductive via laminated board 20 that stores a semiconductor element 5, a wiring substrate 30 on which the semiconductor element 5 is mounted, a conductive via laminated board 20a of an upper layer sealing the package, and a conductive via laminated board 20b of a lower layer having an external terminal 10. In other words, the package is formed by laminating a plurality of laminates of the conductive via laminated board 20 and wiring substrates 30 between the conductive via laminated boards 20a, 20b of the upper layer and lower layer, the plurality of laminates then being heated and pressurized to form an integral structure (see FIG. 5).

[0011]
The wiring substrate 30 on which the semiconductor element is mounted is an insulating board 6 such as a polyimide substrate with an approximately 40 μm thick copper foil, printed laminated board, or the like. The insulating board 6 has a connection electrode 7 (see FIG. 4(b)) embedded in a via. The copper foil on the insulating board 6 is patterned into a shape having a land 17 on the connection electrode 7 as well as wiring 8 formed in another region and electrically connected to the semiconductor element 5. The thickness of the semiconductor element 5 (thickness of a silicon chip) is approximately 30 to 200 μm, and preferably approximately 50 to 150 μm. The conductive via laminated board 20 is an insulating board 1 such as a polyimide substrate with an approximately 75 μm thick copper foil, a printed laminated board, or the like. The insulating board 1 has a connection electrode 2 (see FIG. 4(a)) embedded in a via. The copper foil on the insulating board 1 is patterned into a shape having a land 3 on the connection electrode 2 as well as wiring 16 formed in another region. An opening section (chip cavity section) 12 is formed in a center portion of the insulating substrate 1 to store the semiconductor element.

[0012]
In the present invention, the thickness of the conductive via laminated board 20 may have the same thickness as or be thinner than that of the wiring substrate 30 so long as the semiconductor element 5 is stored in the opening section 12. At this time, the conductive via laminated board is coated with an adhesive material 4 such that the adhesive material 4 fills the chip cavity section 12 when an integration process is performed. The conductive via laminated board 20a of the upper layer has wiring and a land, with a connection electrode embedded in the via.

The land 3 is formed on the connection electrode. Furthermore, the conductive via laminated board 20b of the lower layer has wiring and a land, and the external terminal 10 is formed on a back surface.

[0013]
The semiconductor device of this embodiment can obtain a semiconductor device having a thin laminated package by the configuration as described above. Furthermore, the upper and lower sides of the laminate are sandwiched by the conductive via laminated boards, and therefore, sealability with respect to the semiconductor element is high. Furthermore, the semiconductor element is stored in the chip cavity section formed in the conductive via laminated board. However, the thickness and area of the chip cavity section is smaller than the semiconductor element, and therefore, even if the semiconductor element is stored therein, a space is formed between the semiconductor element and the inner wall of the chip cavity section. For example, a space is present between the semiconductor element and the chip cavity section even if the semiconductor element is slightly stretched due to bending the semiconductor device, and thus the space can absorb stretching of the semiconductor element. Therefore, stress generated when an external force is applied to the semiconductor device can be absorbed. Furthermore, the space is filled with a flexible adhesive material such as an elastomer or the like that adheres the laminated conductive via laminated board to the wiring substrate. In particular, if a flexible adhesive material such as silicon resin or the like is used, stress can be absorbed and sealability can be improved to enhance the moisture resistance of the semiconductor device.

[0014]
Next, Embodiment 2 will be described while referring to FIGS. 2 to 5. FIGS. 2 to 5 are partial cross-sectional views of the semiconductor device illustrated in FIG. 1, cross-sectional views of a manufacturing process of the semiconductor device, and cross-sectional views of the manufacturing process describing a method of manufacturing a semiconductor device with a plurality of semiconductor elements laminated. The semiconductor device includes a plurality of the wiring substrates 30 on which the semiconductor elements 5 are mounted and a plurality of the conductive via laminated boards 20 having an opening section 12 with a space for storing the semiconductor elements 5 mounted on the wiring substrates 30, and the conductive via laminated boards 20 and wiring substrates 30 are alternately laminated to achieve a laminated structure of the semiconductor elements.

[0015]
The insulating board 1 such as a polyimide substrate with a copper foil, a printed laminated board, or the like is used in the conductive via laminated board 20. First, a YAG laser, a carbon dioxide gas laser, etc. are used to form a plurality of vias 13 on an insulating board 1 such as a printed laminated board in the portion of the insulating board 1 such as a copper foil printed laminated board where vias and wiring are to be formed. Thereafter, a mask 14 is applied to a copper foil 15 in the via and wiring portion, which is etched to form the wiring pattern 16 and the land 3. Furthermore, the connection electrode 2 is embedded in the via 13 by screen printing a conductive resin paste with a silver or copper filler. The method of forming the connection electrode 2 can also include copper or gold plating on an inner wall of the via and then embedding a conductive material in the via. A thermosetting adhesive material 4 such as an epoxy resin or the like is coated on the back surface of the insulating board 1 such as a printed laminated board or the like. A region where the semiconductor elements are stored on the insulating board 1 such as a printed laminated board or the like is punched out and used as the chip cavity section 12 (FIG. 2).

[0016]
The wiring substrate 30 on which the semiconductor element 5 is mounted is the insulating board 6 such as a polyimide substrate with a copper foil, a printed laminated board, or the like. A YAG laser, a carbon dioxide gas laser, or the like is used to form a plurality of vias on the insulating board 6 in a portion on the insulating board 6 containing a copper foil printed laminated board or the like where a via and wiring are formed. Thereafter, a mask is applied to a copper foil in the via and wiring portion, which is etched to form the wiring pattern 8 and the land 17. Furthermore, the connection electrode 7 is embedded in the via by screen printing a conductive resin paste with a silver or copper filler. The method of forming the connection electrode 7 can also include copper or gold plating on an inner wall of the via and then embedding a conductive material in the via. A semiconductor element (chip) 5 is die-bonded and mounted on the wiring substrate 30 using a flip chip method or the like. In order to mount the semiconductor element 5 on the wiring substrate 30, connection terminals 11 such as a solder ball or the like are connected to the wiring pattern 8. The connection terminals 11 are covered and protected by an underfill resin 9 (FIG. 3). Furthermore, the conductive via laminated board 20 is aligned with the wiring substrate 30 and laminated such that the semiconductor element 5 is positioned in the chip cavity section 12 (FIG. 4). Then, after aligning, the laminate is pressed at the curing temperature of the adhesive material 4 by a vacuum press or other heating compression machine. Finally, a laminated package is formed by cutting along the outline of each package with a blade, router, or the like (FIG. 5).

[0017]
In this embodiment, a plurality of chip cavity sections are formed in the conductive via laminated board 20, a plurality of semiconductor elements are mounted on the wiring substrate 30, and these are alternately laminated to form a plurality of semiconductor element laminates. Finally, each semiconductor element laminate is individually bladed to improve the efficiency of the laminated package formation. In this embodiment, as illustrated in FIG. 5, four semiconductor elements 5, for example, are laminated to form a laminate. The semiconductor element 5 is sealed by being sandwiched between the conductive via laminated boards 20a, 20b, which do not have chip cavity sections above and below the laminate. An external terminal with an appropriate shape is formed on the conductive via laminated board 20b of the lower layer. By collectively laminating and cutting a semiconductor element layer, a supporting wiring substrate, and a conductive via insulating substrate, manufacturing is possible in fewer steps than with conventional techniques for laminating packages.

[0018]
Next, Embodiment 3 will be described while referring to FIGS. 6 and 7. FIGS. 6 and 7 are cross-sectional views of a manufacturing process describing a method of manufacturing a semiconductor device with a plurality of semiconductor elements laminated. The semiconductor device includes a plurality of wiring substrates 50 on which semiconductor elements 25 are mounted and a plurality of conductive via laminated boards 40 having an opening section 32 with a space for storing the semiconductor elements 25 mounted on the wiring substrates 50, and the conductive via laminated boards 40 and wiring substrates 50 are alternately laminated to achieve a laminated structure of the semiconductor elements. The insulating board 21 such as a polyimide substrate with a thin copper layer, a printed laminated board, or the like is used in the conductive via laminated board 40. First, the copper foil printed laminated board 1 of a portion where the vias and wiring are formed on the printed laminate 1 is masked on a copper foil in the via and wiring portion, which is then etched to form a land 23.

A thermosetting adhesive material 24 such as an epoxy resin or the like is coated on the back surface of the printed laminated board 1. A region where the semiconductor elements are stored on the printed laminated board 21 is punched out and used as the chip cavity section 32. In this embodiment, two chip cavity sections are provided. In the present invention, it is advantageous to provide two or more chip cavity sections in the conductive via laminated board to make the manufacturing process more efficient.

[0019]
The wiring substrate 30 on which the semiconductor element 25 is mounted is an insulating board 26 such as a polyimide substrate with a thin copper layer, a printed laminated board, or the like. A mask is applied to a copper foil in the via and wiring portion of the printed laminated board 26, which is etched to form the wiring pattern 28 and the land 37. A semiconductor element (chip) 25 is die-bonded and mounted on the wiring substrate 50 using a flip chip method or the like. In this embodiment, two semiconductor elements 25 are mounted on the wiring substrate 50. Furthermore, the conductive via laminated board 40 is aligned with the wiring substrate 50 and laminated such that the semiconductor element 25 is positioned in the chip cavity section 32. Then, after aligning, the laminate is pressed at the curing temperature of the adhesive material 24 by a vacuum press or other heating compression machine. After curing the adhesive material 24, a through hole 33 is formed penetrating through the lands 23, 37 forming vias using a drill with a diameter of 0.25 mm to 0.4 mm. Thereafter, electroplating of copper, gold, or the like is applied inside the through hole 33 and on the lands to form a connection electrode
31. Finally, a laminated package is formed by cutting along the outline of each package with a blade, router, or the like.

[0020]
In this embodiment, a plurality of chip cavity sections are formed in the conductive via laminated board 40, a plurality of semiconductor elements are mounted on the wiring substrate 50, and these are alternately laminated to form a plurality of semiconductor element laminates. Finally, each semiconductor element laminate is individually bladed to improve the efficiency of the laminated package formation. In this embodiment, four semiconductor elements 25, for example, are laminated to form a laminate. The semiconductor element 25 is sealed by being sandwiched between the conductive via laminated boards 40a, 40b, which do not have chip cavity sections above and below the laminate. An external terminal with an appropriate shape is formed on a back surface of the conductive via laminated board 40b of the lower layer. By collectively laminating and cutting a semiconductor element layer, a supporting wiring substrate, and a conductive via insulating substrate, manufacturing is possible in fewer steps than with conventional techniques for laminating packages.

[0021]
Next, Embodiment 4 will be described while referring to FIG. 8. FIG. 8 is a cross-sectional view of the semiconductor device. In this embodiment, the same semiconductor device as in Embodiment 3 illustrated in FIG. 7 is processed. The semiconductor device includes a plurality of the wiring substrates 50 on which the semiconductor elements 25 are mounted and a plurality of the conductive via laminated boards 40 having a space for storing the semiconductor elements 25 mounted on the wiring substrates 50 and having the chip cavity section 32, and the conductive via laminated boards 40 and wiring substrates 50 are alternately laminated to achieve a laminated structure of the semiconductor elements. In this embodiment, four semiconductor elements 25, for example, are laminated to form a laminate. The semiconductor element 25 is sealed by being sandwiched between the conductive via laminated boards 40a, 40b, which do not have chip cavity sections above and below the laminate.

[0022]
The connection electrode 31 connected to each semiconductor element 25 via wiring is formed inside the via of the laminate. The connection line 31 includes a connection electrode 31a that connects to the ground (GND) line, and connection electrodes 31b, 31c that connect to a signal line. Furthermore, metal films 33 such as aluminum, copper, or the like are formed on the conductive via laminated boards 40a, 40b in the upper and lower layers. The metal film is formed, for example, by sputtering or from a metal foil. The metal film 33 is electrically connected to the connection electrode 31a, which is connected to the ground line, and is in a non-contact state with the connection electrodes 31b, 31c, which are connected to the signal line. The metal film 33 has a shielding effect when connected to the ground line. This effect can be adjusted by adjusting the material and thickness of the metal film, the material and width of the connection electrode, and the like as needed.

[0023]
Next, Embodiment 5 will be described while referring to FIG. 9. FIG. 9 is a cross-sectional view of a semiconductor device and a semiconductor element incorporated in the semiconductor device. In this embodiment, the same semiconductor device as in Embodiment 3 illustrated in FIG. 7 is processed. The semiconductor device includes a plurality of the wiring substrates 50 on which the semiconductor elements 25 are mounted and a plurality of the conductive via laminated boards 40 having a space for storing the semiconductor elements 25 mounted on the wiring substrates 50 and having the chip cavity section 32, and the conductive via laminated boards 40 and wiring substrates 50 are alternately laminated to achieve a laminated structure of the semiconductor elements. In this embodiment, four semiconductor elements 25, for example, are laminated to form a laminate. The semiconductor element 25 is sealed by being sandwiched between the conductive via laminated boards 40a, 40b, which do not have chip cavity sections above and below the laminate. The semiconductor element 25 used in this semiconductor device is formed by sequentially laminating silicon chips a, b, C, D via bumps 34, which are connection electrodes attached thereto. In this embodiment, it is possible to obtain a laminated package which is thinner than the semiconductor devices of Embodiments 1 to 4, and which can be formed in multiple layers.

[0024]
EFFECT OF THE INVENTION
With the configuration above, the present invention can obtain a semiconductor device having a thin laminated package. Furthermore, the laminated package is sandwiched between the conductive via insulating substrates on upper and lower sides, and therefore, sealability with respect to the semiconductor element can be increased.

Furthermore, the semiconductor element is stored in the chip cavity section formed in the conductive via insulating substrate. However, the thickness and area of the chip cavity section is smaller than the semiconductor element, and therefore, even if the semiconductor element is stored therein, a space is formed between the semiconductor element end the inner wall of the chip cavity section. Therefore, stress generated when an external force is applied to the semiconductor device can be absorbed. Furthermore, the space is filled with an adhesive materiel that adheres the conductive via insulating substrate to the wiring substrate. In particular, if a flexible adhesive material such as silicon resin or the like is used, stress can be absorbed and sealability can be improved to enhance the moisture resistance of the semiconductor device. Furthermore, by collectively laminating and cutting a semiconductor element layer, a supporting wiring substrate, and a conductive via insulating substrate, manufacturing is possible in fewer steps than with conventional techniques for laminating packages.

BRIRF DESCRIPTION OF THE DRAWINGS

FIG. l is a perspective view of a semiconductor device and conductive via insulating substrate of Embodiment 1;
FIG. 2 is a cross-sectional view of a conductive insulating substrate of Embodiment 2;
FIG. 3 is a cross-sectional view of a wiring substrate of Embodiment 2;
FIG. 4 is a cross-sectional view of a manufacturing process of a semiconductor device of Embodiment 2;
FIG. 5 is a cross-sectional view of a manufacturing process of the semiconductor device of Embodiment 2;
FIG. 6 is a cross-sectional stew of a manufacturing process of a semiconductor device of Embodiment 3;
FIG. 7 is a cross-sectional view of a manufacturing process of the semiconductor device of Embodiment 3;
FIG. 8 is a cross-sectional view of a semiconductor device of Embodiment 4: and
FIG. 9 is a cross-sectional stew of a semiconductor device and semiconductor element of Embodiment 5.

DESCRIPTION OF REFERENTIEL NUMERICALS

1, 6, 21. 26: Insulating plate. 2, 7, 31, 31a, 31b. 31c: Connection electrode. 3, 17. 23. 37: Land. 4, 24: Adhesive material: 5. 25: Semiconductor element: 8, 16, 28: Wiring: 9: Under 11 resin, l0: External terminal: 11: Connection terminal (solder ball); 12, 32: Chip cavity section: 13: Yia: 14: Mask: 15: Copper foil: 20. 20a. 20b, 40. 40a, 40b: Conductive via insulating substrate. 25s. 2sb, 25c, 25d: Silicon chip: 30. 50: Wiring substrate. 33: Through hole.

FIG. 1

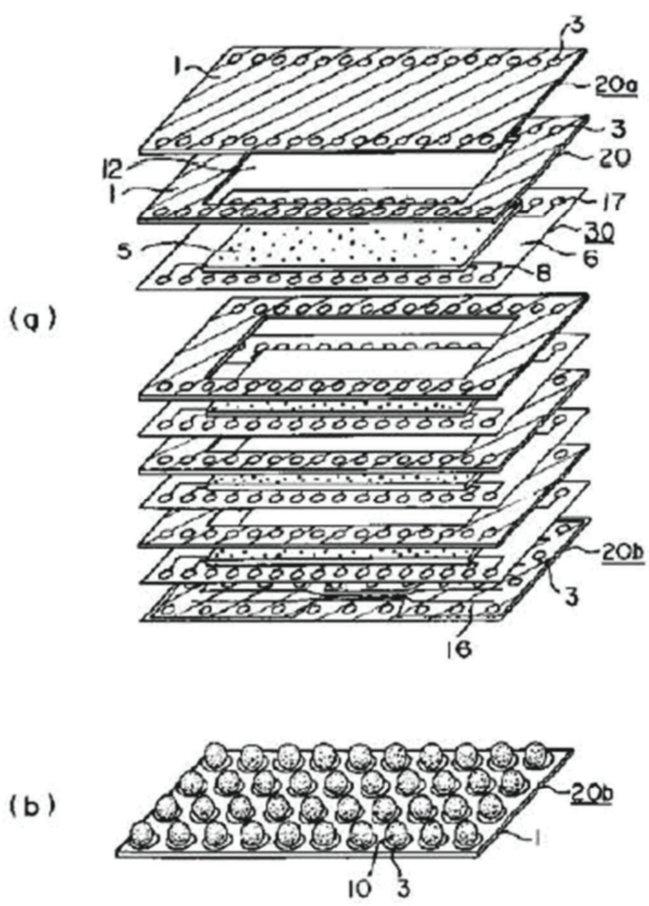


FIG. 2

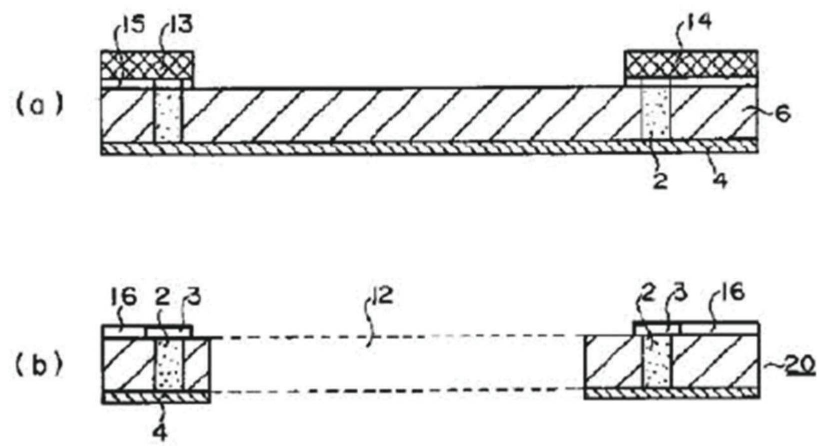


FIG. 3

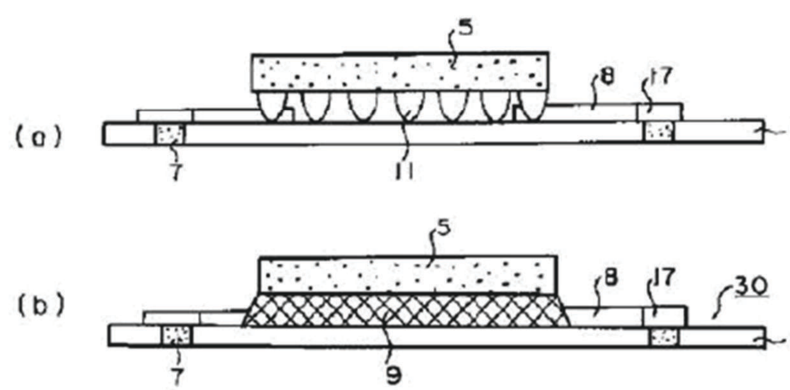


FIG. 4

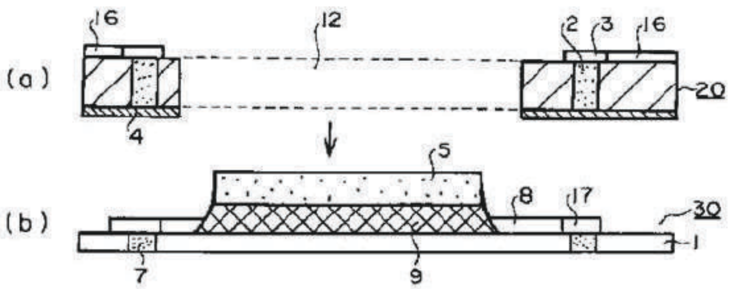


FIG. 5

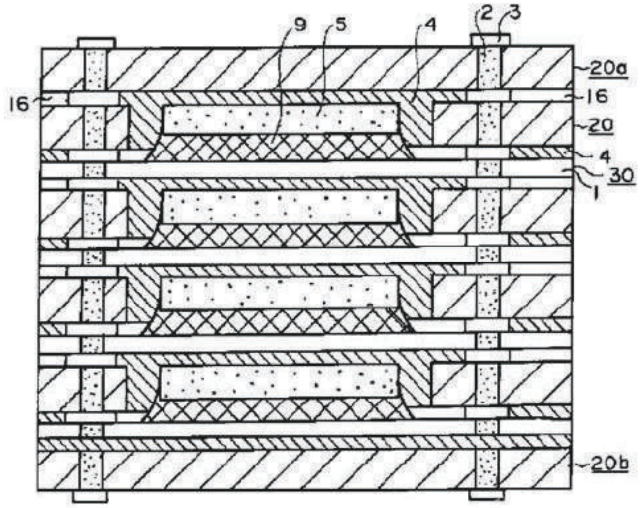


FIG. 6

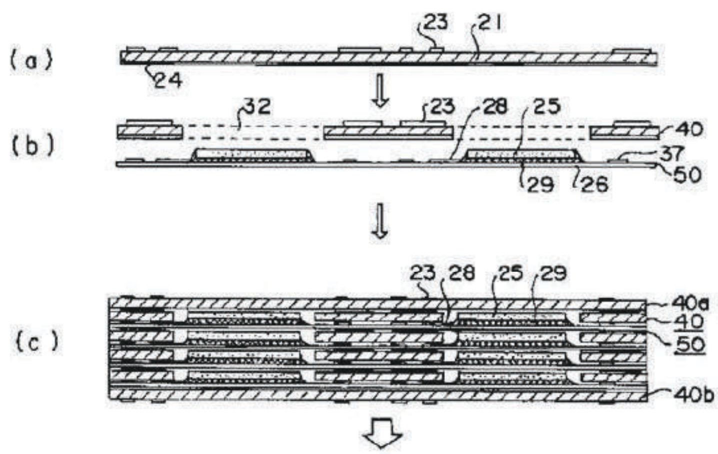


FIG. 7

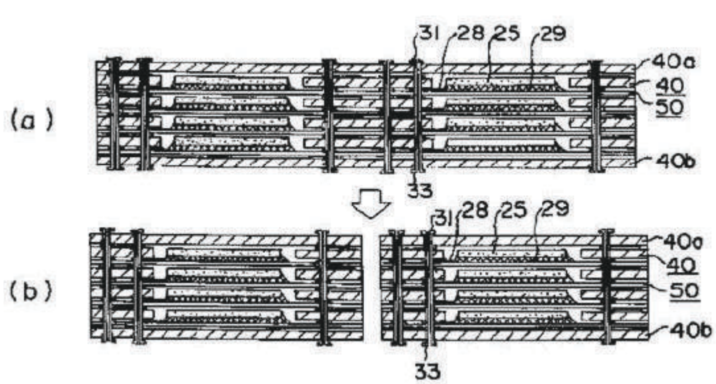


FIG. 8

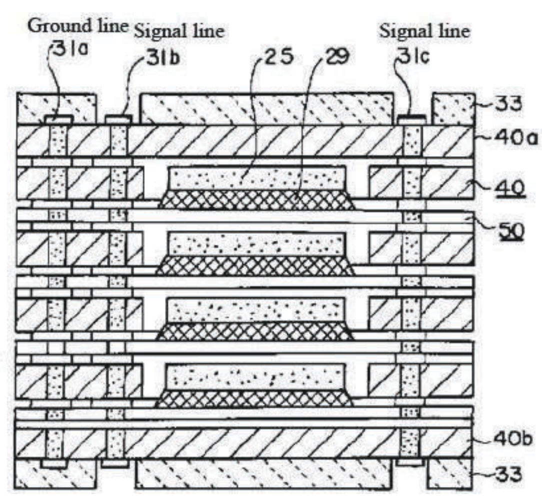


FIG. 9