Encapsulants Used in Flip-Chip Packages

Darbha Suryanarayana, Tien Y. Wu, and Jack A. Varcoe

***Abstract*—Low thermal expansion encapsulants have been used in a wide range of IBM flip-chip products to enhance the fatigue life of solder interconnections and to prevent environmental attack. In order to determine whether an encapsulant can satisfy all requirements of a given product or process, the physical behaviors of the encapsulant must be carefully characterized. Typical material properties of interest are: viscosity and flow coverage, thermal expansion, modulus, glass transition temperature, filler size, alpha activity, adhesion, ionics content, fracture toughness, and electrical properties. The sensitivity of these properties to process variables such as encapsulant dispensing, gelling, curing, and post curing exposures to environment and reliability experiments need to be explored. An overall evaluation of all these properties is essential for determining the ultimate performance of the encapsulant on specific products. This paper presents a systematic approach to quantify these encapsulant properties. Various test methods and their relevant technical aspects are discussed. Results achieved on a few selected materials are also presented as examples.**

I. Introduction

SEMICONDUCTOR devices packaged into various forms, such as molded flat packs for surface mounting, die attach wire-bonding and chip-on-boards, bare chip mounting in tape automated bonding, and flip-chip packaging are widely known in the electronic industry [1], [2]. Different passivations schemes are also known to protect the devices from an attack by various environmental factors such as moisture, solvents, gases, and radiation. The device level passivation is done using a thin layer of polyimide coat as well as quartz deposited on the face of the chip. On the other hand, thick-film coatings are applied on the assembled parts using thermosetting molding compounds as encapsulants. Typical polymer systems used are silicones, urethanes, epoxies, polyimides, polyimide siloxanes, conformal coatings (e.g. paraxylylene) and a few others [3]–[7]. Among these, the epoxies cured with anhydride are rigid materials offering high glass transition temperature (T_g), good chemical resistance, low moisture absorption, favorable viscosity for flow and adhesion strength to the packaging materials. In addition, the coefficient of thermal expansion (CTE) of the epoxies are lowered with the addition of ceramic fillers which leads to stress reduction between the substrate and the encapsulant. On the contrary, the addition of fillers to silicones or urethanes is not effective. At room temperature, silicones are above their T_g which results in a high CTE. The effect of epoxy encapsulant on the solder fatigue life enhancement in flip-chip packages has been the subject matter of several recent papers [8]–[10]. In this paper, we report new findings on the encapsulants used in flip-chip packages.

The flip-chip (or face down) process practiced in IBM since 1960's, consists of solder bump bonding between the chip and the substrate using a "controlled collapse chip connection" technique, and the solder joint is called C4. This process has been most suitable for gang bonding of large number of area array solder joints in pin grid arrays as well as multi chip modules in IBM [1], [11].

Although the C4 joints have been very reliable, the C4 technology has been limited by controlling the size of the foot print. The use of large chips in flip-chip mounting has been limited due to the possibility of thermal stress-induced failures at the C4 joints, particularly at the outer most joints. Thermal expansion differentials of silicon and the substrate during the accelerated thermal cycling testing (ATC) can cause localized stresses at the C4 joints, which can lead to device failures [11], [12]. Hence, most of the flip-chip packaging applications are limited to low CTE ceramic substrates.

However, the recent development trends towards the need for large chips on ceramics as well as flip-chip attachment on flexible organic chip carriers have placed new challenges on C4 technology for materials as well as processing. The use of encapsulation has been identified as a solution to the new demands.

II. C4—Encapsulation

The concern on C4 fatigue reliability of flip-chip mounted packages has been recently solved by inserting a novel glass filled epoxy under the flip-chips packages, as shown in Fig. 1. The CTE of the epoxy is particularly matched with the z-expansion of solder, which is about 28 ppm/°C for the 95Pb/5Sn solder.

A. Material Requirements

Typical properties of the flip-chip encapsulants are given in Table I. The material selection for C4-encapsulation were based on extensive study undertaken using more than 20 different formulations covering a variety of polymers. They were applied as "glob-tops" on chips as well as under the chips. From the ATC testing stand point of view, the epoxy encapsulant present underneath the chip (see Fig. 1) has been highly favored.

As we surveyed early filled epoxies from available commercial sources, we noticed specific concerns on encapsulant flow under the chips due to high viscosity. Large fillers have tendency to block the flow of encapsulant in narrow gap. Some encapsulants containing solvents caused massive bubbles and voids under the chips. Material sourcing outside

Manuscript received March 1, 1993; revised July 31, 1993. This paper was presented at the 1993 Electronic Components and Technology Conference, Orlando, FL, June 1–4, 1993.

The authors are with Endicott Electronic Packaging, IBM Microelectronics Division, Endicott, NY 13760.

IEEE Log Number 9213224.

0148–6411/93$03.00

TABLE I
DESIRED PROPERTIES OF C4-ENCAPSULANTS

Solids	100%
Viscosity	< 20 cps
CTE Kcps	< 40
Tg	$> 125°$ C
Modulus	> 9.0 GPa
Fracture toughness	> 1.3 MPa-m$^{1/2}$
Cure temp	$< 130°$ C
Filler size	$< 50\mu$m
Filler content	> 50 wt%
Ionics (Cl)$^-$	< 20 ppm
Extractable chlorinated solvents	< 20 ppm
Alpha activity (for memory chips)	$< .005$ Count/h/cm^2
Shelf life (@ $-$ 40° C)	> 6 months
Pot life	> 16 h
High electrical resistivity	$> 10^{12}$ ohms-cm
Low dielectric constant	< 4
Good chemical resistance	Solvents and Humidity
Flow under larger chips	Required
C4 life improvement	$5 - 10\times$
T&H reliability	2000 h

Note: All values are @ 25°C unless specified.

US created further concerns since some of them are not registered under Toxic Substance Control Act required in the US. These factors have contributed to the development of a novel flip-chip encapsulant, which was tested extensively, qualified and implemented in manufacturing.

B Encapsulation Process

A typical encapsulation process consists of dispensing a bead of the encapsulant along one or two edges of the chip, using a positive displacement pump. For encapsulant with low viscosity, material flow under the chip is completed simply by capillary action. The flow can also be accelerated by heating the chip carrier. After completion of the flow, the encapsulant should exit cleanly from the other edges to form thick fillets. The encapsulated parts then go through curing in an oven. After full cure, the epoxy develops physical properties and offer reinforcement.

The two essential properties for C4 life improvement are high modulus and matching CTE with solder. These findings were also confirmed by the finite element modelling, which is a numerical technique used for predicting the stresses [13]. In addition to the mechanical reinforcement, the chemical protection as well as the adhesion offered by the encapsulant can also play roles on the ultimate C4 fatigue performance.

Our current studies showed that the encapsulated C4s on metallized ceramics (MC) modules revealed no detectable failures even after testing up to 10,000 cycles at a temperature delta of 100°C [13]. This corresponds to $5 - 10\times$ improvement in fatigue life when compared to the control parts with no encapsulation. The C4 life improvement was also demonstrated on large sized chips (14.7 mm). In addition, the flip-chip attachment on high CTE organic chip carriers was also successfully demonstrated with dramatic improvement in C4 reliability.

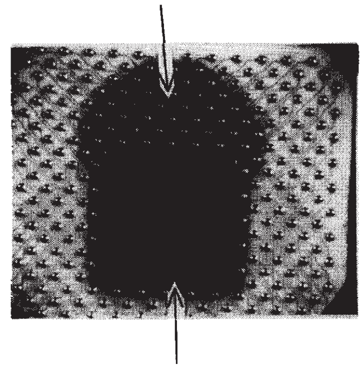


Fig. 1. C4-encapsulated flip-chip assembly on metallized pin grid array ceramic chip carrier. The chip size is 12.6×12.6 mm^2.

III. RESULTS AND DISCUSSION

A Liquid Encapsulant Properties

Since the encapsulants have limited pot life at room temperature, they are normally stored in deep freezer (@ $-$ 40°C). The liquid epoxies as received require significant testing in order to compare their properties against a list of material specifications, that includes IR spectra match, viscosity control, filler content, filler size, ionics and residual chlorinated solvents, as given in Table I.

Since the encapsulant's viscosity is an indicator of flow, it is monitored using conventional techniques. Typical viscosity values for the room temperature are in the range of 10–30 Kcps under low shear rates. These values are an order of magnitude lower than the conventional epoxies used in "glob top" applications. Even though, the encapsulant viscosity is higher at room temperature, it is considerably lowered at elevated temperatures, which makes it easier to flow under the chip.

While the viscosity of the material determines the flow of encapsulant to a large extent, the desired flow cannot be obtained by specifying the viscosity alone. The flow rate as a function of time depends on various properties of the material such as viscosity, temperature, surface tension, gel time, gap under the chip, and also the wettability of the surfaces in test. It has been observed that two materials having the equivalent viscosities might reveal significantly different flow characteristics. The encapsulant flow was monitored on simulated quartz chips assembled on parts [9].

In addition, measurement of flow rates were also done using glass slide experiment. Typical results showing flow distance versus time for different encapsulants are shown in Fig. 2. In what follows, the encapsulants evaluated by the current study are designated by Roman numerals.

It is believed that the ionized impurities, such as Na^+, Cl^-, etc., have an adverse effect on the insulation resistance of encapsulants. The concentration of these ions and their

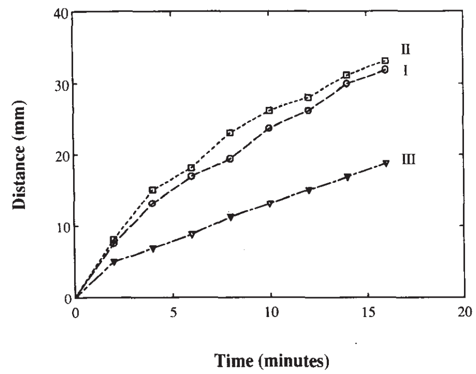


Fig. 2. Encapsulant flow measured under glass capillary column for flip-chip encapsulants (I–III) at 65°C.

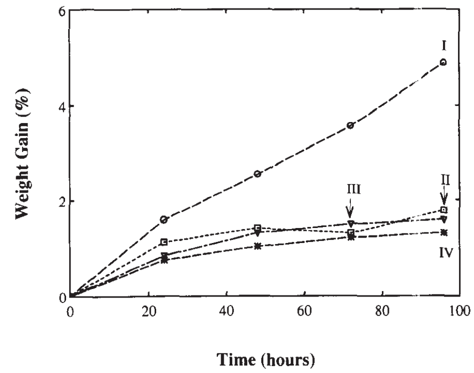


Fig. 4. Percentage of weight gain versus time of exposure, during the pressure cooker test, determined on flip-chip encapsulants (I–IV).

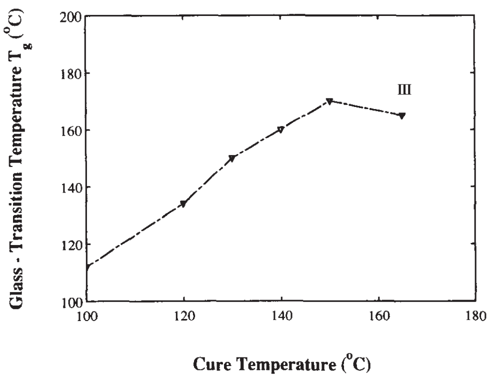


Fig. 3. Effect of Cure temperature on the T_g values determined on encapsulant (III).

mobility will be high under excessive moisture absorption levels present in certain epoxies, which can lead to insulation resistance breakdown during the temperature and humidity testing. Hence, it is necessary to study the

- Quantity of ionized impurities in the epoxies.
- Residual chlorinated solvents.
- Moisture sensitivity.

Ionized impurities normally exist in epoxy resin and in fillers with epoxy resin containing a higher level of chlorine. This is due to the by-products (chlorine containing compounds) generated during the production of epoxy resins. In addition, some suppliers use the chlorinated solvents for cleaning their processing equipment, and the solvent residue can be picked up by the encapsulant. Traceable levels of these solvents can be picked up by using careful analysis. These ionics have been specially monitored in our encapsulants against our specification level of 20 ppm maximum for the ionics as well as the chlorinated solvents.

B Effect of Cure Temperature

1) Thermal Properties: Since the physical properties of epoxies are highly dependent on the cure temperature and time, they were also measured using conventional thermal analysis methods. Samples were prepared by curing them individually at various temperatures ranging from 100–170°C. Similarly, the cure times were also varied between 2 and 6 h. The CTE was determined by thermal mechanical analyzer (TMA) and the T_g was determined by differential scanning calorimetry (DSC).

The T_g values seem to improve after prolonged curing (2–6 h) at a given temperature. The maximum observed T_g values are reported in Fig. 3. The samples cured at low temperatures gave low T_g values in the range of 120–140°C. Samples cured at high temperatures gave higher values. The T_g has also been measured by TMA yielding lower values, however, the trend is same. The CTE values were found to be more or less unaffected by the degree of cure.

The lower T_g values indicate that the material is only partially cured, that is, with less degree of cross-linking. The degree of cure will have direct impact on the ultimate material performance particularly on moisture sensitivity as well as the crack resistance. These subjects will be dealt in the subsequent sections.

2) Moisture Sensitivity: Since encapsulated parts are required to go through T&H reliability testing, the effect of cure on moisture uptake is examined here. These experiments were done by subjecting the cured encapsulant samples in a pressure cooker test (PCT). The PCT approach is a more aggressive test which yields rapid turnaround. The moisture uptake was typically monitored for every 24 h of PCT. The percentage of weight gain (ΔW) versus time of exposure was determined on selected encapsulants as shown in Fig. 4. Fig. 5 shows the dependency of water update on the encapsulant's curing condition. The water uptake is found to be higher for the low temperature cured samples when compared to the fully cured samples. This is expected since the partially cured epoxies have more unreactive sites than fully cured epoxies for reacting with water.

These curves show a nonlinear rise in the ΔW values versus time, which can be fitted into parabolic equation of the form ($\Delta W = kt^{1/2}$), thus obeying the Fick's law of diffusion. The constant k represents the reaction kinetics which itself is a function of temperature (T) as well as diffusion constant (D).

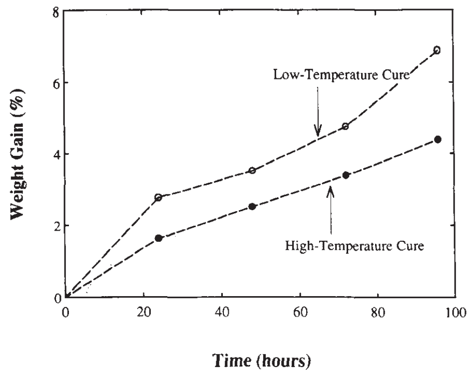


Fig. 5. Effect of cure temperature on moisture absorption studied on the encapsulant I. Samples were cured at lower temperature (100°C/4 h) as well as at high temperature (130°C/4 h), as shown in the plot.

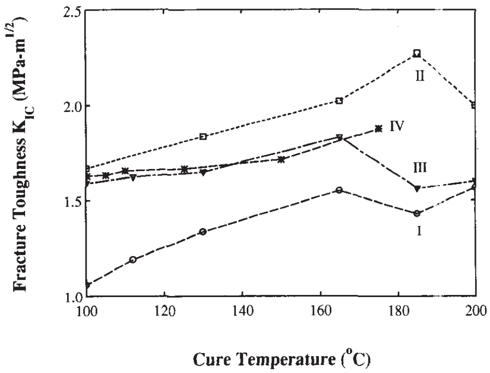


Fig. 6. Effect of cure temperature on fracture toughness for selected encapsulants (I–IV).

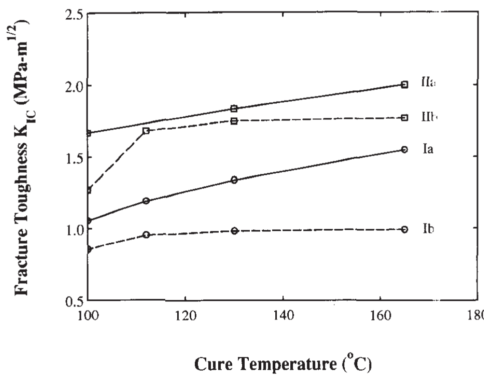


Fig. 7. Effect of temperature and humidity on fracture toughness of encapsulants I and II, where a and b refer to samples without and with T&H exposure, respectively.

3) Fracture Toughness: One of the potential threats of encapsulation is the formation of microscopic crack. It has been observed that, in some instances, microcracks or surface flaws of the encapsulants can propagate under repeated loads or a combination of loads and environmental attack which eventually lead to failure. To ensure the mechanical integrity of designs associated with a given encapsulant, the crack resistance as well as the variation of crack resistance of the encapsulant must be carefully characterized. To quantify the crack resistance, the fracture toughness experiment used extensively for metals and plastics was adopted.

The fracture toughness is an intrinsic material property, which signifies the resistance of a brittle elastic material to crack propagation. The fracture toughness value of an encapsulant depends on many factors, for example, resins, fillers, additives, defects, and process conditions such as cure time, cure temperature, and humidity history. It also depends on the loading mode. For practical importance, only the opening mode, i.e., the commonly denoted mode I fracture toughness is discussed here. There are many accepted methods for measuring the mode I fracture toughness [14]. In the current study, the plane strain compact tension test method was adopted [14], [15].

Fig. 6 shows typical results of how fracture toughness values vary with cure temperature (cure time between 2 to 6 h). It is seen that, the fracture toughness increases with cure temperature until a critical level. Beyond that level, fracture toughness either becomes constant or start to decline. A similar trend was also observed in the T_g measurements as previously shown in Fig. 3. It implies that crack resistance is proportional to the degree of cross-linking until a maximum value is reached. When cured at extremely high temperatures, crack resistance starts to decrease due to the degradation of epoxy systems or formation of cracks. This suggests that an optimal cure temperature range is likely to exist for each encapsulant. Process conditions should be designed to fall between this range to obtain best mechanical strength. Fig. 7 shows a comparison of freshly cured encapsulants versus samples exposed to temperature and humidity. It shows that, after 24 h of exposure to 80°C at 85% relative humidity, encapsulants cured at all temperatures show a consistent decline of crack resistance. This indicates that the effect of operating environment should also be considered when choosing the right encapsulants.

IV. Summary

- Novel flip-chip encapsulant has been developed and qualified for manufacturing.
- The encapsulant's properties such as flow, thermal, fracture toughness, and moisture stability are essential for performance improvement.
- Encapsulation technology continues to grow as new materials and processes are developed.

Acknowledgment

The authors thank J. V. Ellerson, K. K. Nair, and D. Thorne for their technical support.

REFERENCES

[1] R. R. Tummala and E. J. Rymaszewski, Eds., *Microelectronics Packaging Handbook.* New York: Van Nostrand Reinhold, 1989.

[2] D. P. Seraphim, R. C. Lasky, and C. Y. Li, *Principles of Electronic Packaging.* New York: McGraw-Hill, 1989.

[3] J. E. Anderson, V. Markovac, and P. R. Troyk, "Polymer encapsulants for microelectronics: Mechanisms for protection and failure," *IEEE Trans. Components Hybrids, Manufacturing,* vol. 11, pp. 152–158, Jan. 1988.

[4] H. M. Tong, L. Mok, K. R. Grebe, H. L. Yeh, K. K. Srivastava, and J. T. Coffinn, "Parylene encapsulation of ceramic packages for liquid nitrogen applications," in *40th ECTC Proceedings*, Las Vegas, NV, 1990, pp. 345–350.

[5] E. Suhir and J. M. Segelken, "Mechanical behavior of flip-chip encapsulants," *J. Electron. Packaging*, vol. 112, pp. 327–332, 1990.

[6] S. Yamaoka, A. Kusuhara, and Y. Okabe, "Liquid dropping resin for IC encapsulation," *IEEE Trans. Hybrids, and Manufacturing Technol.*, vol. 11, pp. 145–151, Jan. 1988.

[7] R. J. M. Zwiers, H. J. L. Bressers, B. Ouwehand, and D. Baumann, "Development of a new low-stress hyperred LED encapsulant," *IEEE Trans. Hybrids, Manufacturing Technol.*, vol. 12, pp. 387–392, 1989.

[8] F. Nakano, T. Soga, and S. Amagi, "Resin-insertion effect on thermal cycle resistivity of flip-chip mounted LSI devices," in *ISHM'87 Proc.*, pp. 536–541.

[9] D. Suryanarayana, R. Hsiao, T. P. Gall, and J. M. McCreary, "Enhancement of flip-chip fatigue life by encapsulation," *IEEE Trans. Components Hybrids, Manufacturing*, vol. 14, no. 1, pp. 218–223, 1991.

[10] T. Gabrykewicz, D. Sengupta, and T. Thuruthumaly, "Glob top material selection for flip chip devices," in *Proc. 1986 Int. Symp. Microelectronics*, Reston, VA, 1986, pp. 707–713.

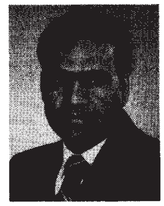
[11] N. G. Koopman, T. C. Reiley, and P. A. Totta, "Chip-to-package interconnections," in *Microelectronics Packaging Handbook*, R. R. Tummala and E. J. Rymaszewski, Eds. New York: Van Nostrand Reinhold, 1989, pp. 361–453.

[12] L. S. Goldmann, "Geometric optimization of controlled collapse interconnections," *IBM J. Res. Develop.*, pp. 251–265, May 1969.

[13] J. Clementi, J. McCreary, T. M. Niu, J. Palomaki, J. Varcoe, and G. Hill, "Flip chip encapsulation on ceramic substrates," in *Proc. 43rd Electron. Components Technol. Conf.*, IEEE, Orlando, FL, June 1993, p. 175.

[14] J. E. Stawley and W. F. Brown, "Fracture toughness testing methods," *ASTM STP*, vol. 281, pp. 133–145, 1965.

[15] D. Broek, *Elementary Engineering Fracture Mechanics.* Martinus Nijhoff, 1982, pp. 170–176.



Darbha Suryanarayana received his Ph.D. degree in physics in 1975, from Indian Institute of Technology, Madras, India; and the B.Sc degree from Andhra University, Waltair (India).

He is an Advisory Engineer at Endicott Electronic Packaging, IBMMicroelectronics Division, Endicott, New York. He joined IBM in 1982 at East Fishkill Facility, NY and later joined IBM Endicott in 1984. Prior to IBM, he worked as Research Associate at: University of Houston, Houston, Texas (1980–82), Oakland University, Rochester, Michigan (1977–80), University of Saskatchewan, Saskatoon (Canada) (1975–77). His current R&D activities include materials, processing and evaluations of underfill encapsulants used for flip chip mounted packages. He also worked on metallization of thermally conductive aluminum nitride ceramics, sol-gel composites and polyimide thinfilms. His academic research activities include polymer chain dynamics, structure of polymer gels, defects in crystalline solids and free radical study using electron spin resonance and electron spin echo modulation spectroscopic techniques. He has published over 50 scientific research papers in several international journals; author of a number of industrial technical reports, US patents and inventions.

Dr. Suryanarayana was listed in who is who in technology today and a fellow in American Institute of Chemists.

Tien Y. Wu received the M.S. and Ph.D. degrees in mechanical engineering and applied mechanics from University of Pennsylvania in 1984 and 1988, respectively.

He remained there as a Post-doctoral Fellow for another year. Dr. Wu is currently working as an advisory engineer in Materials Science group, at Endicott Electronic Packaging, IBM Microelectronics Division, Endicott, New York. His research and development activities are in the areas of composite material characterization, mechanical design, process optimization, analytical and experimental analysis of interfacial crack propagation, and reliability prediction for electronic packages.

Jack A. Varcoe, photograph and biography not available at time of publication.