EXHIBIT B

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AND PRIVATE LABEL PC, LLC

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

POLARIS POWERLED TECHNOLOGIES, LLC, Plaintiff, v. WESTERN DIGITAL CORPORATION, WESTERN DIGITAL TECHNOLOGIES, INC., NEWEGG, INC., ZONES, LLC, AND PRIVATE LABEL PC, LLC, Defendants,	CASE NO. 2:24-cv-02864-ODW-MAR **PATENT L.R. 3-3 AND 3-4 INVALIDITY DISCLOSURES OF WESTERN DIGITAL DEFENDANTS** Hon. Otis D. Wright

I. INTRODUCTION

Pursuant to the Parties Joint Rule 26(f) Report and the Patent Rules of the Northern District of California which are adopted by this Court, Defendants Western Digital Corporation and Western Digital Technologies, Inc. (collectively, "Western Digital" or "Defendant") hereby serves these Invalidity Contentions and accompanying document production on Plaintiff Polaris PowerLED Technologies, LLC ("Polaris" or "Plaintiff").

Polaris has asserted through its Infringement Contentions that Western Digital infringes:

Asserted Patent	Asserted Claims
U.S. Patent No. 8,601,346 (the "'346 Patent")	1-3, 5, 6, 10, 11, 14-16
U.S. Patent No. 8,554,968 (the "'968 Patent")	1-3, 6-11, 14-18
U.S. Patent No. 9,183,085 (the "'085 Patent")	1, 2, 4, 14, 15, 16

Western Digital hereby provides its disclosures and related documents pertaining only to the asserted claims identified by Polaris in its Infringement Contentions.

Western Digital reserves the right to amend or further supplement these disclosures and associated document production, should Polaris provide any information that it failed to provide in its Infringement Contentions, should Polaris amend its disclosures in any way, or should additional prior art or facts come to light, including facts learned through discovery, which is still ongoing in this action.

Western Digital's Invalidity Contentions are based on its present understanding of the asserted claims and the apparent interpretation of claims used by Polaris in its Infringement Contentions. Western Digital's Invalidity Contentions, including the concurrently served invalidity claim charts, may reflect alternative positions based on Polaris' Infringement Contentions. These Invalidity Contentions are not an admission by Western Digital that the accused products, including any current or past versions of these products, or any of Western Digital's technologies, are covered by or infringe the asserted claims. Furthermore, by including prior art that anticipates or renders obvious claims based on Polaris's application of the claim language, Western Digital is not adopting or agreeing with Polaris' apparent interpretation or application of the claims. Western Digital's Invalidity Contentions are made in a variety of alternatives and do not represent Western Digital's agreement with Polaris' apparent application or views as to the meaning, definiteness, written description support for, or enablement of any asserted claim. Western Digital's Invalidity Contentions are also subject to any future Claim Construction proceedings and corresponding rulings by the Court as to the meaning and construction of claim terms.

To the extent that any of the prior art discloses the same or similar functionality or feature of any of the accused products, Western Digital reserves the right to argue in the alternative that said feature or functionality does not practice any limitation of any of the asserted claims. Western Digital also reserves the right to argue, in the alternative, that if said feature or functionality is found to practice any limitation of any of the asserted claims of the Patents-in-Suit, then the prior art discloses the limitation and that the claim is not patentable.

Moreover, Western Digital reserves the right to revise its ultimate contentions concerning the invalidity of the asserted claims which may change depending upon any finding as to the priority date of the asserted claims and/or positions that Polaris may take concerning infringement and/or invalidity. Western Digital reserves the right to rely on discovery, papers, and evidence filed, served, or submitted by Polaris in connection with this litigation, other co-pending litigation, and prior litigation involving the Patents-in-Suit. Western Digital further reserves the right to rely on discovery, papers, and evidence filed, served, or submitted by Polaris in connection with any proceedings in the U.S. Patent Office or any foreign patent office involving the Patents-in-Suit. Western Digital further reserves the right to rely upon expert testimony in support of its Invalidity Contentions.

The references cited in the attached exhibits may disclose the elements of the claims either explicitly and/or inherently and/or may be relied upon to show the state of the art and/or the knowledge of one of skill in the art in the relevant timeframes. In addition, identification of elements and supporting evidence in the attached claim charts is meant to be exemplary, and not limiting or exhaustive. Western Digital has provided citations to exemplary portions of the prior art in this document and in the attached exhibits for the purpose of fairly disclosing Western Digital's Invalidity Contentions. Western Digital specifically reserves the right to supplement its contentions with additional citations and evidence and specifically reserve the right to rely on all portions of the cited references in arguing that the asserted claims of the Patents-in-Suit are invalid.

In the attached exhibits, absence of identification of elements in a particular reference is not meant to be and should not be taken as an admission that these elements are not present under any application of the claims asserted by Polaris. The obviousness combinations discussed herein and in the exhibits are in the alternative to Western Digital's anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not anticipatory. To date, Polaris has not identified any secondary considerations that it contends would have a bearing on the obviousness of the asserted claims. Western Digital reserves the right to dispute any arguments regarding secondary considerations raised by Polaris, including through a response by expert testimony.

Prior art not included in this disclosure, whether known or not known to Western Digital, may become relevant. In particular, Western Digital is currently unaware of the extent, if any, to which Polaris may contend that certain limitations of the Patents-in-Suit are not disclosed in the prior art identified by Western Digital. To the extent that such an issue arises, Western Digital reserves the right to identify other prior art and additional combinations of prior art (including combinations of the currently cited references with the knowledge of one of ordinary skill of the art at the time of the alleged inventions), that would explain or render obvious the allegedly missing limitation(s).

Furthermore, because discovery is ongoing, Western Digital reserves the right to revise, amend, and/or supplement the information provided herein, including identifying, charting, and relying on additional prior art, should discovery yield additional information or prior art. Western Digital has not had the opportunity to take the depositions of any of the inventors of the Patents-in-Suit and/or other persons having potentially relevant information. Discovery in this case is ongoing, and Western Digital's investigation regarding invalidity of the Patents-in-Suit over prior art and regarding other grounds of invalidity, including those based on public use or on-sale bar under 35 U.S.C. § 102(b) and failure to comply with 35 U.S.C. § 112 is ongoing. Western Digital reserves the right to amend or supplement its Invalidity Contentions when and if additional information becomes available.

These Invalidity Contentions are limited to Western Digital's current positions regarding the grounds of invalidity specifically called for in the rules adopted by the Court under this Court's Patent Standing Order. Western Digital is not required to include herein any explanation or contention regarding any other defense that Western Digital may wish to assert in these actions. Western Digital reserves the right to assert and pursue all other defenses that may be available, including all of the affirmative defenses pled in Western Digital's answer and any other grounds, including but not limited to non-infringement.

In addition to the prior art identified below and the accompanying invalidity claim charts, Western Digital hereby incorporates by reference any of the prior art and invalidity claim charts that have been or will be disclosed in any action related to the Patents-in-Suits. As non-limiting examples, Western Digital's incorporation by reference also includes all proceedings at the U.S. Patent and Trademark Office related to the Patents-in-Suit, and any other related patents or patent applications, including any reexaminations of the Patents-in-Suit, reissue proceeding, and any postgrant challenges to the Patent-in-Suit including any *Inter Partes* Review proceedings. Western Digital's incorporation by reference further includes, and is not limited to, invalidity claim charts obtained from third parties in response to subpoena requests otherwise.

II. LEGAL STANDARDS

A. 35 U.S.C. § 102

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent, or

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States, or

(c) he has abandoned the invention, or

(d) the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor's certificate filed more than twelve months before the filing of the application in the United States, or

(e) the invention was described in — (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language; or

(f) he did not himself invent the subject matter sought to be patented, or

(g) (1) during the course of an interference conducted under section 135 or section 291, another inventor involved therein establishes, to the extent permitted in section 104, that before such person's invention thereof the invention was made by such other inventor and not abandoned, suppressed, or concealed, or (2) before such person's invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it. In determining priority of invention under this subsection, there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

35 U.S.C. § 102.

B. 35 U.S.C. § 103

In *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007), the United States Supreme Court clarified the standard for what types of inventions are patentable and emphasized that inventions arising from ordinary innovation, ordinary skill, or common sense are not patentable. In that regard, a patent claim may be obvious if the combination of elements was obvious to try or there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. *Id*. at 402, 420. In addition, when a reference is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. *Id*. at 401, 420. "If a person of ordinary skill in the art can implement a predictable variation . . . § 103 likely bars its patentability." *Id*. at 401.

In determining whether a claim is obvious, "[o]ften, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *Id.* at 418. In determining whether a claim is obvious, "a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id*. When prior art elements are combined according to known methods to yield predictable results, the claimed invention is obvious. *Id*. at 417. In addition, "[o]ne of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims." *Id*. at 419-20. "Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *Id*. at 420. Furthermore, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense." *Id*. at 421.

According to the Supreme Court, a person of ordinary skill may have been motivated to combine the teachings known in the prior art based on one or more of the following rationales, for example: (1) to combine prior art elements according to known methods to yield predictable results; (2) to substitute one known element for another to obtain predictable results; (3) to use a known technique to improve similar devices (methods, or products) in the same way; (4) to apply a known technique to a known device (method, or product) ready for improvement to yield predictable results; (5) to choose from a finite number of identified, predictable solutions, with a reasonable expectation of success ("obvious to try"); (6) to adapt known work in one field of endeavor for use in either the same field or a different one based on design incentives or other market forces when the variations would have been predictable;

(7) to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention based on a teaching, suggestion, or motivation in the prior art. *See Id.* at 401.

The Supreme Court has also held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton," that a motivation to combine may be simply "common sense," and that "familiar items may have obvious uses beyond its primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. *Id.* at 420-21. The Supreme Court further held that it is sufficient that a combination of elements was "obvious to try," holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 421.

C. 35 U.S.C. § 112

Under Section 112, first paragraph, the inventor must adequately set forth and describe three items: (1) the invention (the description requirement); (2) the manner and process of making and using the invention (the enablement requirement); and (3) the best mode contemplated by the inventor of carrying out his invention (the best mode requirement). *See University of Rochester v. G.D. Searle & Co., Inc.*, 358 F.3d 916, 921 (Fed. Cir. 2004), reh'g en banc denied, 375 F.3d 1303 (Fed. Cir. 2004).

"The purpose of the written description requirement is to require an inventor to disclose his invention to the public in such a manner as to allow 'a person of skill in the art to recognize that the patentee invented what is claimed.'" *Tobinick v. Olmarker*, 753 F.3d 1220, 1225 (Fed. Cir. 2014) (citing *Synthes USA, LLC v. Spinal Kinetics, Inc.*, 734 F.3d 1332, 1341 (Fed. Cir. 2013)). In accordance with the enablement requirement, the inventor must set forth in the patent specification sufficient information to enable a person skilled in the relevant art to make and use the invention. *Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 55 USPQ2d 1279 (Fed. Cir. 2000).

D. 35 U.S.C. § 101

35 U.S.C., section 101 specifies "four independent categories of inventions or discoveries that are eligible for [patent] protection: processes, machines, manufactures, and compositions of matter." *Bilski v. Kappos*, 561 U.S. 593, 601 (2010). But the Supreme Court has carved out three implicit exceptions: "laws of nature, physical phenomena, and abstract ideas." *Id.* at 601 (citations omitted). These principles are not patent-eligible because "they are the basic tools of scientific and technological work," which are "free to all men and reserved exclusively to none." *Mayo Collaborative Servs. v. Prometheus Labs*., Inc., 566 U.S. 66, 71 (2012) (citations omitted).

Courts evaluate patent eligibility using a two-step test articulated by the Supreme Court in *Alice Corp. v. CLS Bank Int'l,* which requires determining: (1) whether the claims are directed to an abstract idea or other patent-ineligible concept; and (2) if so, whether the claim elements include an inventive concept sufficient to transform the claimed abstract idea into a patent-eligible application. 573 U.S. 208, 217-218 (2014).

1. Alice Step One

The Federal Circuit has described step one of the Alice Test as "looking at the 'focus' of the claims." *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350, 1353 (Fed. Cir. 2016). A patent's specification is "helpful in illuminating what a claim is directed to," and should be considered both for "what it states and what it does not." *Chamberlain Grp., Inc. v. Techtronic Indus. Co.*, 935 F.3d 1341, 1346 (Fed. Cir. 2019) (internal quotations omitted); *ChargePoint, Inc. v. SemaConnect, Inc.*, 920 F.3d 759, 768 (Fed. Cir. 2019). One "telltale sign of abstraction" occurs when the claimed functions are "mental processes that 'can be performed in the human mind' or 'using a pencil and paper.'" *PersonalWeb Techs. LLC v. Google LLC*, 8 F.4th 1310, 1316 (Fed. Cir. 2021) (citations omitted), *cert. denied*, 142 S. Ct. 1445 (2022).

2. Alice Step Two

At step two of the Alice inquiry, the Court should "consider the elements of each claim both individually and as an ordered combination to determine whether the additional elements transform the nature of the claim into a patent-eligible application." *Alice*, 573 U.S. at 217 (2014) (internal quotations omitted). The Court must assess whether the inventive concept makes the claim "amount[] to significantly more than a patent upon the [abstract idea] itself." *Id.* at 218-19. For purposes of step two, "[s]imply appending conventional steps, specified at a high level of generality, [i]s not enough to supply an inventive concept." *Chamberlain*, 935 F.3d at 1348 (Fed. Cir. 2019) (quoting *Alice*, 573 U.S. at 222). Further, "merely adding computer functionality to increase the speed or efficiency of the process does not confer patent eligibility on an otherwise abstract idea." *PersonalWeb*, 8 F.4th at 1319.

Courts may resolve disputes of subject-matter eligibility under section 101 at the Rule-12 stage "where the undisputed facts, considered under the standards required by that Rule, require a holding of ineligibility under the substantive standards of law." *AI Visualize, Inc. v. Nuance Commc'ns, Inc.*, 97 F.4th 1371, 1377-78 (Fed. Cir. 2024).

III. THE STATE OF THE ART

A person or ordinary skill in the art ("POSITA") as of the relevant time period would have had a working knowledge of the memory system art that is pertinent to the Asserted Patents, including memory systems and memory controllers.

Flash memory was invented in the mid-1980s and saw an explosive growth throughout the 1990s. Dipert, Brian R., & Levy, Markus, *Designing with Flash Memory* 1st ed., at 1-4 McGraw-Hill Professional (2003) ("Designing with Flash Memory"). It is well-known in the art that the "Achilles Heel" of flash memory is the degradation of the flash memory as data is constantly written and erased over the memory's lifespan. *Id.* at 35. To combat this "Achilles Heel," many well-known redundant cell and internal error correction coding (ECC) schemes are implemented. *Id.* ECC algorithms such as Bose-Chaudhuri-Hocquenghem (BCH), Low Density Parity Check (LDPC), and Reed-Solomon (RS) were well known ways of correcting errors in flash memory. Lasser at [0009]. Another way of combatting errors in flash memory is to employ a Redundant Array of Inexpensive Disks (RAID), wherein encoded data is "striped" across multiple disks, so that even if the case of a disk's total failure the data will be available. Bruce Jacob et al., *Memory Systems: Cache, DRAM, Disk*, at 34 (Morgan Kaufmann 2007) ("*Memory Systems*"). Methods for storing data, error correcting, and interfacing with host systems were particularly well-understood in the early 2000s, as evidenced by the copious disclosure in the prior art references provided herein. A POSITA familiar with flash memory storage would have been particularly aware of the concepts of "data striping," "error correction," and "interrupts," and would have been aware of the many solutions and variations on those solutions that already existed in the prior art.

IV. PRIORITY OF THE ASSERTED PATENTS

1. The '346 Patent

Western Digital is still investigating Polaris' claim to priority dating back to at least as early as August 16, 2010. Although the '346 Patent claims priority to U.S. Provisional Patent No. 61/374,242, the Asserted Claims of the '346 Patent are not entitled to the priority date of the provisional application because the provisional application does not provide written description support for the claims. The invalidating prior art identified herein predates the date of the '242 provisional application. However, Western Digital reserves the right to challenge Polaris' claim to priority for the asserted claims, including if or when the priority date becomes relevant for a specific invalidity ground.

2. The ’085 Patent

Western Digital is still investigating Polaris’ claim to priority dating back to at least as early as May 22, 2012. Western Digital reserves the right to challenge Polaris’ claim to priority for the asserted claims.

3. The ’968 Patent

Although the ’968 Patent claims priority to U.S. Provisional Patent No. 61/374,242, the Asserted Claims of the ’968 Patent are not entitled to the priority date of the provisional application because the provisional application does not provide written description support for the claims. Solely by way of non-limiting example, the provisional patent application fails to disclose the following elements of the independent claims:

- “an interrupt manager configured to . . . generate an interrupt vector state based on the completion queue state” (claim 1)
- “an interrupt manager configured to . . . determine the completion queue of the host processing unit contains an unprocessed completion status based on the interrupt vector state” (claim 1)
- “an interrupt vector state memory configured to store a plurality of interrupt vector states corresponding to a plurality of interrupt vectors in the host processing unit” (claim 8)
- “an interrupt manager controller . . . configured to . . . map at least one completion queue state of the plurality of completion queue states to an interrupt vector state of the plurality of interrupt vector states” (claim 8)
- “an interrupt manager controller . . . configured to . . . generate the interrupt vector state based on each completion queue state mapped to the interrupt vector state” (claim 8)
- “an interrupt manager controller . . . configured to . . . determine a completion queue corresponding to a completion queue state mapped to

the interrupt vector state contains an unprocessed completion status based on the interrupt vector state" (claim 8)

- "generating an interrupt vector state by the nonvolatile memory controller based on the completion queue state, the interrupt vector state associated with an interrupt vector in the host processing unit" (claim 16)
- "determining by the nonvolatile memory controller based on the interrupt vector state that the completion queue contains an unprocessed completion status" (claim 16)

The provisional application also fails to disclose multiple features recited in the asserted dependent claims and additional elements in the independent claims. During the prosecution of the '968 Patent, the Examiner recognized the provisional application's failure to support the claims in a non-final office action mailed February 6, 2012 and invited the applicant "to point out where the provisional application provides a basis for the claimed subject matter in order to receive the benefit of the filing date of the provisional." The applicant did not address the provisional in its response to the office action, effectively conceding that the provisional application does not support the claims.

V. THE '346 PATENT

E. INVALIDITY CONTENTIONS BASED ON U.S.C. §§ 102-103

Western Digital contends that the asserted claims are invalid as anticipated by prior art under 35 U.S.C. § 102 and/or that the asserted claims are obvious in view of prior art and/or the knowledge of a person having ordinary skill in the art under 35 U.S.C. § 103. Western Digital reserves the right to rely on any identified piece of prior art to anticipate the asserted claims and/or to render obvious the asserted claims in view of the knowledge of one having ordinary skill in the art or in combination with other references identified herein.

The table below lists prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the '346 Patent. The charts submitted as Exhibits A1-A11 to these Invalidity Contentions and this Section specifically point out, as non-limiting examples, where the prior art identified by Western Digital anticipates, either expressly or inherently, and/or renders obvious each element of the asserted claims under at least 35 U.S.C. §§ 102(a), (b), (e), or (g). Western Digital's citations to exemplary and illustrative portions of the prior art references should not be construed as admissions that other portions of the identified prior art references are not also relevant to the validity of the claims. Other passages of the identified prior art references are not also relevant to the validity of the claims. Other passages of the identified prior art may additionally disclose, either expressly or inherently, information relevant to the validity of one or more elements of the asserted claims. Western Digital reserves the right to rely on any unquoted portions of the prior art as further evidence of the invalidity of the asserted claims. Moreover, Western Digital reserves the right to rely on any evidence, including expert testimony, to provide context to or aid in understanding the prior art and the cited portions of the identified prior art. Where Western Digital cites a particular drawing or figure, the citation is expressly intended to encompass the drawing or figure, as well as any text associated with the drawing or figure. Similarly, where Western Digital cites to a particular description of or text associated with a drawing or figure, the citation is expressly intended to encompass that drawing or figure as well. The evidence cited for each independent claim included in the exhibit is necessarily incorporated for each subsequent dependent claim in the exhibit.

Certain pieces of identified prior art inherently or implicitly disclose features of the asserted claims. Western Digital reserves the right to rely on inherency and/or secondary documents to demonstrate the invalidity of the asserted claims based on the inherent or implicit disclosure in these cited prior art documents. Further, Western Digital may rely on any evidence, including expert testimony, to establish the implicit or inherent disclosure of certain features of the prior art to invalidate the asserted claims. Western Digital also reserves the right to rely on any evidence, including expert testimony, to prove that the disclosures or prior art cited herein are enabled or to explain the meaning of a term used in the disclosures or any prior art cited herein.

Western Digital identifies below a number of Prior Art Systems and Services, the function of which is not publicly available. Western Digital intends to conduct third-party discovery and reserves the right to amend these Contentions upon the discovery of additional information concerning the identified Prior Art Systems and Services.

1. Identification of Prior Art Patents, Patent Publications, and Printed Publications to the Asserted Claims of the '346 Patent

Exhibit	Reference	Filing/Priority Date	Date of Issue or Publication	Short Cite
A1	U.S. Patent Application Publication No. 2011/0078496 to Jeddeloh	September 29, 2009	March 31, 2011	Jeddeloh
A2	U.S. Patent No. 5,950,225 to Kleiman	February 28, 1997	September 7, 1999	Kleiman
A3	U.S. Patent No. 8,341,332 to Ma et al	August 5, 2008	December 25, 2012	Ma
A4	U.S. Patent No. 6,161,165 to Solomon et al	March 11, 1997	December 12, 2000	Solomon
A5	U.S. Patent No. 8,074,149 to Stolowitz	December 29, 2009	December 6, 2011	Stolowitz
A6	U.S. Patent 7,930,475 to Kleinman	February 22, 2007	April 19, 2011	Kleiman II

A7	U.S. Patent No. 6,092,215 to Hodges et al.	September 29, 1997	July 18, 2000	Hodges
A8	U.S. Patent No. 7,917,695 to Ulrich et al.	February 8, 2008	March 29, 2011	Ulrich
A9	U.S. Patent No. 8,074,011 to Flynn et al.	December 6, 2006	December 6, 2011	Flynn
A10	U.S. Patent No. 7,617,360 to Arai et al.	May 23, 2005	November 10, 2009	Arai

2. Identification of Prior Art Systems/Services to The Asserted Claims of the '346 Patent

Exhibit	System/Service	Relevant Dates	Person/Entities Involved in Prior Use, Sale, or Offers for Sale	Short Cite
--	SharkMp6 and SpinnerMp6 Products included in Appendix D[1]	2006 through August 16, 2010	Western Digital, SanDisk	
--	Micron Technology, Inc. products embodying US Patent Application Publication No. 2011/0078496 to Jeddeloh	2009	Micron Technology, Inc.	
--	Hitachi, Ltd. products embodying	2005	Hitachi, Ltd.	

[1] Identification of SharkMp6 and SpinnerMp6 as prior art systems and any associated theory of invalidity is based on the apparent interpretation of claims used by Polaris in its Infringement Contentions.

	US Patent No. 7,617,360 to Arai			
--	Fusion-io, Inc. products embodying US Patent No. 8,074,011 to Flynn et al.	2006	Fusion-io, Inc.	
--	Super Talent Electronics, Inc. products embodying US Patent No. 8,341,332 to Ma	2008	Super Talent Electronics, Inc.	
--	Network Appliance, Inc. (also known as NetApp, Inc.) products embodying US Patent No. 5,950,225 to Kleiman and/or US Patent No. 7,930,475 to Kleiman	1997	Network Appliance, Inc. NetApp, Inc.	
--	EMC Corporation products embodying US Patent No. 6,161,165 to Solomon	1997	EMC Corporation Dell EMC	
--	NVIDIA Corporation products embodying US Patent No. 8,074,149 to Stolowitz	2009	NVIDIA Corporation	
--	IBM, Corp. products embodying US Patent No. 6,092,215 to Hodges	1997	IBM, Corp.	
--	Overland Storage Inc.	2011	Overland Storage Inc.	

			Overland Tandberg Sphere 3D Corp.	

Nothing in the Charts for the above-identified references should be construed as an express or implied admission that Defendants agree with Plaintiff's infringement or claim construction theories. Defendants contend that they do not infringe any claim of the '346 Patent. But to the extent that Plaintiff argues that Defendants infringe the '346 Patent based on the theories within its infringement contentions, Defendants contend that the functionality cited in Plaintiff's infringement contentions predate the '346 Patent.

3. Obviousness Combinations

To the extent that any one of the anticipating references is found not to disclose a limitation recited in the Asserted Claims, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the Asserted Patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and any claim(s) from which this claim depends and/or (ii) to combine said reference with any other of the references in Exhibits A1-A11 and/or with a POSITA's general knowledge. Generally, motivation to combine any of these references exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. Below, Western Digital provides specific examples of combinations of prior art that render the asserted claims of the Patent-in-Suit obvious. All claims that are anticipated by a particular reference are also rendered obvious by that same reference alone, or in combination of two or more references. These specific references and/or combinations are merely examples of the grounds set forth in the Exhibits.

A POSITA would have been motivated to combine any of the references described in attached Exhibits A1-A11, including for the reasons described below. A PHOSITA at the time of filing of the Asserted Patent would have understood the references listed above, alone or in combination, to contain explicit and/or implicit teachings, suggestions, and/or rationales to combine them for at least the following exemplary reasons.

Western Digital contends that it would have been obvious to modify the above-listed prior art to include any allegedly missing element, in view of the knowledge of one of ordinary skill in the part, the admitted prior art of the Asserted Patent, and/or in combination with any of the other prior art references identified for the Asserted Patent. Western Digital reserves the right to rely upon any combination of prior art references whether listed herein or otherwise. The combinations and modifications of the prior art, which render obvious the asserted claims of the Patent-in-Suit, arise from ordinary innovation, ordinary skill, common sense, and/or would have been obvious to try or otherwise predictable. In addition, design improvements and other market forces would have prompted those combinations and modifications.

A POSITA having knowledge of the above listed patents, articles, and systems, among other things, would be motivated, taught, and suggested to combine the prior art discussed in Exhibits A1-A11 with one another in a number of ways, including as detailed below.

Each of the references cited in Exhibits A1-A11 is analogous art to the ’346 Patent: (1) each reference is from the same field of endeavor as the alleged invention (even if the reference addresses a different problem); and/or (2) each reference is reasonably pertinent to the problem faced by the named inventors of the ’346 Patent (even if the reference is not in the same field of endeavor as the claim invention). It therefore would have been obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. All of the prior art references in Exhibits A1-A11 are related to systems and methods for generating parity data in the field of nonvolatile memory controllers, were authored, designed, and developed during the same time period, and a person of ordinary skill in the art would have been motivated to apply the teachings of any one reference to any other reference because they would improve upon such a reference's teachings.

Group A	Group B
• Jeddeloh • Arai • Flynn • Kleimann II • Ma	• Kleimann I • Kleimann II • Solomon • Stolowitz • Hodges • Ulrich

The invention of the '346 Patent combines two well-known concepts: (1) using multiple processing units to perform a data stripe operation on a plurality of data blocks and (2) a parity calculator employing "on-the-fly" parity calculations by updating a data block in a page frame "without storing each data block in a data buffer."[2] These concepts were well-known prior to the priority date of the '346 Patent. For example, the above "Group A" references contain extensive disclosure related to data striping, including using multiple processing units and requesting data in response to a command. The above "Group B" references contain extensive disclosure contain extensive disclosure on parity calculation, including parity calculator structure and on-the-fly parity calculations. The above table should not be construed as an admission that any specific limitation is not disclosed by any reference. Western Digital's detailed contentions with respect to each individual reference and how said claims map to the specific limitations of the claims are contained in Exhibits A1-A11.

As explained in detail in the attached charts, data striping and on-the-fly parity calculations were well known concepts prior to the filing date of the '346 Patent. A POSITA would have been motivated to combine these two concepts, and thus a

[2] While it is understood that the claims of the '346 Patent contain many limitations, the elements of the invention generally fall within these three categories. The precise mapping of references to individual limitations is disclosed in Exhibits A1-A11.

POSITA would have been motivated to combine any Group A reference with any of the Group B references. For instance, a POSITA would have been motivated to implement the on-the-fly parity techniques in the Group B references because on-the-fly techniques "perform[] XOR operations on data transferred to and from the disk drives without requiring separate transfers." Kleimann I at 1:67-2:2; Solomon at 1:57-2:11; Hodges at 2:30-32; Stolowitz at 10:19-45; Ulrich at 83:1-84:40. Further, on-the-fly techniques "dynamically compute[] a set of parity information for the RAID stripe, without requiring additional resources from any part of the system," thereby increasing throughput and efficiency. Kleimann I at 3:17-20; Solomon at 1:57-2:11; Ulrich at 83:1-84:40; Stolowitz at 10:19-45; Ulrich at 83:1-84:40.

Combining the references of Group A and Group B would yield predictable results because the parity calculations in both Group A and Group B are all calculated for the same purpose—a RAID parity stripe operation. *See e.g.*, Jeddeloh at [0006]; Flynn at 23:58-24:3; Solomon at Abstract; Kleimann I at Abstract; Kleiman II at 1:40-2:6; Hodges at 2:1-20; Ma at 8:22-30; Stolowitz at Abstract; Arai at 1:11-67.

As a non-binding example, a POSITA would have found it obvious for Jeddeloh' s parity calculator to use an on-the-fly technique as taught by Kleiman. Jeddeloh describes a parity calculator generally: "RAID XOR circuitry 226 can calculate parity data based on data received from the host interface circuitry 214." Jeddeloh, [0027]. A POSITA would have looked to known techniques to implement the RAID XOR circuitry. *KSR*, 550 U.S. at 416-18.

Kleiman provides an example of one known way to implement RAID circuitry. Kleiman implements a parity calculation technique that calculates parity date on-the-fly: "method of operating a system for performing fly-by XOR." Kleiman 3:37-38. In particular, "the fly-by XOR element 180 ... copies the data being transferred and adds it (by performing an XOR operation) to the accumulated parity information in the associated XOR accumulator buffer." Kleiman 3:60-65. Then, "[w]hen all data for the recognized memory buffer has been transferred, the associated XOR accumulator buffer holds the computed parity for the RAID stripe." Kleiman, 3:65-67.

A POSITA would have been motivated to utilize Kleiman's on-the-fly technique because the on-the-fly technique "performs XOR operations on data transferred to and from the disk drives without requiring separate transfers." Kleiman, 1:67-2:2. Additionally, the on-the-fly technique "dynamically computes a set of parity information for the RAID stripe, without requiring additional resources from any part of the system 100." Kleiman 3:17-20.

The results of the proposed combination would have been predictable because Kleiman's on-the-fly parity calculation is done for the same reason parity data is calculated in Jeddeloh—creating parity data for a RAID stripe operation. *See KSR*, 550 U.S. at 416-18. Jeddeloh explains that "write data can be striped across multiple solid state memory devices in a RAID operation." Jeddeloh, [0028]. Then, "The memory system, e.g., RAID XOR circuitry 226 ... can calculate parity data for the write data." Jeddeloh, [0044].

Kleiman likewise performs parity calculation for a RAID scheme. Kleiman explains that "When a RAID stripe is read or written, either entirely or partially, the fly-by XOR element 180 thus dynamically computes a set of parity information for the RAID stripe." Kleiman, 3:14-17. Accordingly, a POSITA would have reasonably predicted Kleiman's on-the-fly technique to be successful within Jeddeloh' s RAID scheme.

For the same reasons above, a POSITA would have been motivated to combine Jeddeloh with other references that teach these well-known fly-by parity techniques (Group B references). See e.g., Solomon, abstract ("A high performance data path for performing XOR on the fly."); Stolowitz, 10:34-37 ("Segments of these data words, e.g. see data paths 342, 344, are written to each of the drives. At this point, a logical XOR operation can be performed between the corresponding bits of the segments 'on the fly.'"). Moreover, to the extent that Kleiman fails to teach any reference, a

POSITA would have been motivated to substitute features from such references for the features in Kleiman. *KSR*, 550 U.S. at 416-18. And a POSITA would be motivated to combine these well-known fly-by parity techniques to yield predictable results of increased efficiency in parity calculations. *Id.*

A POSITA would have further found it obvious to substitute any of the Group A references with any other Group A reference because all of the Group A references disclose memory control systems compatible with the relevant standards—PCIe, DMA, etc. Jeddeloh at [0016], [0025]-[0026], [0033], [0039]; Ma at 23:21-35; Flynn at 13:1-16, 22:49-58.

As a non-limiting example, since Jeddeloh's switch may be a DMA module (Jeddeloh at [0033]), a POSITA would have found it obvious to look to known techniques for DMA operations between a switch and a plurality of memory controllers. Since the aim of the standards is to create a coherent technology with compatible elements, a POSITA would reasonably expect a combination of variations in PCIe and DMA compatible circuitry to be successful. For the same reason, a POSITA would have understood that two or more Group A references could successfully be combined. Accordingly, to the extent that any limitation is not disclosed by a Group A reference, a POSITA would expect to succeed and would be motivated to combine two Group A references.

To the extent that Group B references also disclose conformance with any of the relevant standards—e.g., PCIe, DMA, etc.—such is another reason a POSITA would be motivated to combine a Group A and Group B reference. *See e.g.*, Solomon at 2:60-3:3, 4:22-41; Ulrich at Fig. 44.

Finally, all the references above—both Group A and Group B—pertain to the same field of endeavor: error correction/detection, specifically RAID data striping, and thus a POSITA would find it obvious to combine the above references. *See e.g.*, Jeddeloh at [0006]; Flynn at 23:58-24:3; Solomon at Abstract; Kleimann I at Abstract; Kleiman II at 1:40-2:6; Hodges at 2:1-20; Ma at 8:22-30; Stolowitz at

Abstract; Arai at 1:11-67. This is especially true of references with the same author or same assignee.

An exemplary list of possible combinations is given in Appendix A.

F. INVALIDITY CONTENTIONS BASED ON U.S.C. § 112

At least in view of Polaris' apparent construction of the Asserted Claims in its infringement Contentions, the Asserted Claims are invalid because the specification as filed does not enable the claimed method. Thus, the patent disclosure would not enable a person of ordinary skill in the art to practice the method as asserted by Polaris. Further, at least in view of Polaris' apparent construction of the claims in its Infringement Contentions, the Asserted Claims are invalid because the specification as filed does not contain a written description of the claimed invention. In particular, the patent disclosure would not lead a person of ordinary skill in the art to understand that the named inventor had possession of the purported invention as asserted by Polaris. The Asserted Claims are invalid as indefinite under 35 U.S.C. § 112 for failing to particularly point out and distinctly claim the subject matter which the applicants regard as their invention.

Based on Polaris' Infringement Contentions and its apparent interpretation of the terms of the Asserted Claims, the following terms or limitations are indefinite, lack sufficient written description support, and/or are not enabled under § 112:

Claim Element	Claim[3]
"updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer"	Claims 1, 14

[3] All claims dependent from claims that are indefinite, lack sufficient written description support, and/or are not enabled under § 112 for the listed reasons are also indefinite, lack sufficient written description support, and/or are not enabled under § 112 for the same reasons.

"the command processing unit receiving the parity write command configured to write the parity block to a nonvolatile memory based on the parity write command"	Claim 1
"in an arbitrary order"	Claim 12
"distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete"	Claim 5
"the plurality of commands comprising a plurality of data update commands and a parity write command"	Claim 11
"the command distribution unit further configured to determine generation of the parity block is complete and to distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete"	Claim 11
"writing the parity block to a nonvolatile memory device by a command processing unit of the plurality of command processing units based on the parity write command after determining	Claim 14

generation of the parity block is complete"	

G. INVALIDITY CONTENTIONS BASED ON U.S.C. § 101

1. Claim 1 of the '346 Patent is directed to an abstract idea.

The claims of the '346 Patent are directed to an abstract idea—namely, calculating parity data and distributing the data among multiple drives within a nonvolatile memory device using distributed processing techniques. For example, Claim 1 recites generic controllers and processing units for performing data processing functions. Specifically, it recites:

- a "plurality of command processing units" that (1) ***receive*** commands for performing a data-striping operation and (2) ***request*** data blocks, ***receive*** data blocks, and ***write*** data blocks to a nonvolatile memory device, and
- a "parity calculator" including a context memory that (1) ***receives*** data blocks as a sequence and (2) ***generates*** parity blocks without storing the data blocks in a buffer.

Thus, the claims of the '346 Patent are also directed to an abstract mental process of receiving data, manipulating it, and distributing it. *See Elec. Power Grp.*, 830 F.3d at 1353-54.

The patent does not purport to disclose or describe any novel technique for writing data from the command processing units to the non-volatile memory device or any novel parity calculation. Instead, the patent's alleged advance over the prior art is applying the concept of distributed processing to accomplish these data-manipulation tasks by reciting that ***a plurality of*** command processing units—as opposed to a single command processing unit—perform the functions of receiving data and writing it to the nonvolatile memory device and that a separate parity calculator receives the data blocks through the same pathway and calculates parity data on the fly. '346 Patent at 3:16-20, 3:60-4:11. But the "idea of distributed processing—merely splitting up a job into smaller pieces to be completed by multiple participating computers in the hierarchy," is also an abstract idea founded in the "basic concept of divide and conquer." *Coho Licensing LLC v. Glam Media, Inc.*, No. C 14-01576 JSW, 2017 WL 6210882, at *5 (N.D. Cal. Jan. 23, 2017), *aff'd sub nom.*, *Coho Licensing LLC v. Oath Inc.*, 710 F. App'x 892 (Fed. Cir. 2018) (citing *Appistry, Inc. v. Amazon.com, Inc.*, 2015 WL 4210890, at *2 (W.D. Wash. July 9, 2015)); *Kinglite Holdings Inc. v. Micro-Star Int'l Co.*, No. 14-03009, 2016 WL 4205356, at *3-*5 (C.D. Cal. May 26, 2016) (holding claims directed toward computer implementation of the "performance of tasks in an efficient order, such as in parallel, rather than in sequence" patent ineligible). The fact that the claims recite that generic controllers and processors within a nonvolatile memory device carry out this process does not remove them from the realm of abstraction. *See, e.g., Appistry*, 2015 WL 4210890, at *2; *Alice*, 573 U.S. at 223 ("[T]he mere recitation of a generic computer cannot transform a patent-ineligible abstract idea into a patent-eligible invention.").

2. Claim 1 of the'346 Patent lacks any inventive concept apart from the abstract idea it claims.

Implementation of the abstract processes the '346 Patent claims require nothing more than well-understood, routine, and conventional components. *See Riggs Tech. Holdings, LLC v. Cengage Learning, Inc.*, No. 2022-1468, 2023 WL 193162, at *3 (Fed. Cir. Jan. 17, 2023) (internal citation omitted). Claim 1 recites that "command processing units" and a "parity calculator" within the nonvolatile memory controller carry out the data-striping operation and parity calculations. But the specification does not purport to introduce any novel processor for performing these functions. It also does not purport to introduce new methods for calculating parity data or a new way of dividing and distributing data.

Instead, the specification claims that the alleged invention improves prior-art methods of performing well-known data-striping techniques by using distributed processing—specifically, "using a plurality of command processing units . . . [to]

perform[] a data stripe operation more quickly than other methods using only a single dedicated processor to generate parity data." '346 Patent at 3:16-20. But using distributed processing to perform known data-striping techniques is the abstract idea itself and cannot supply the inventive concept. *See Two-Way Media Ltd. v. Comcast Cable Commc'ns, LLC*, 874 F.3d 1329, 1339 (Fed. Cir. 2017) ("merely reciting an abstract idea performed on a set of generic computer components, as claim 1 does here, would not contain an inventive concept."). Even if distributed processing were not part of the claimed abstract idea, neither the specification nor the Complaint gives any indication that the concept of distributed processing was new as of the '346 Patent's alleged invention. *See* '346 Patent; *see also Eolas Techs. Inc. v. Amazon.com, Inc.,* No. 2022-1932, 2024 WL 371959, at *6 (Fed. Cir. Feb. 1, 2024) (noting that the parties did not dispute that "distributed processing was well-understood, routine, conventional activity" as of the claimed invention's 1994 priority date). Simply reciting that a plurality of generic "command processing units" and a generic "parity calculator" carry out that well-known process does not supply an inventive concept. *See, e.g., Coho Licensing*, 2017 WL 6210882, at *6.

The specification of the '346 Patent also alleges that the claimed methods and apparatuses save time because the "parity calculator generates the parity block on the fly as the command processing units are receiving the data blocks for the data stripe operation" by generating parity blocks as it receives the data blocks. '346 Patent at 1:67-2:17. Claim 1 recites that the parity calculator generates parity data by storing data blocks in a page frame, *i.e.*, a segment of memory, as it receives them. *See* '346 Patent at claim 1; Dkt. 1, ¶ 97. Thus, the claim requires using a segment of memory for its conventional purpose of storing information. That is not an inventive concept. *See AI Visualize*, 97 F.4th at 1380 (holding that patentee's "claim that the 'virtual views' are created 'on the fly,' without more, cannot support patent eligibility at Alice step two" where the complaint lacked factual allegations to support that the claims required using unconventional technology to achieve this function).

Taken as an ordered combination, Claim 1 of the '346 Patent recites generic components for calculating parity data and distributing the data among multiple drives within a nonvolatile memory device using distributed processing techniques and lack any inventive concept apart from this abstract idea. Accordingly, it lacks subject-matter eligibility under Section 101. *See id.*

Further, any additional features of the '346 Patent are nothing more than conventional elements which can be found in the prior art including:

- Using multiple command processing units to generate parity data. *See e.g.*, Jeddeloh at [0034]-[0036], [0038], [0040]-[0052], Fig. 3.
- A parity bit calculator that generates the parity block in the page frame as the parity calculator is receiving the data blocks for the data stripe operation, so that the parity calculator need not store all the data blocks of the data stripe at the same time when generating a parity block. *See e.g.*, Kleiman at 3:1-33, 3:35-4:67, 5:39-44, 6:36-7:54; Solomon at 1:39-2:21, 4:22-43, 6:9-30, 8:38-54, 10:21-37, 11:24-67.

3. Claim 1 is representative.

The remaining independent and dependent claims of the '346 Patent are "linked to the same abstract idea" as Claim 1, and Claim 1 is therefore representative. *See Content Extraction & Transmission LLC v. Wells Fargo Bank, Nat. Ass'n*, 776 F.3d 1343, 1349 (Fed. Cir. 2014). The remaining claims recite the same abstract concept of calculating parity data and distributing the data among multiple drives within a nonvolatile memory device using distributed processing techniques. Independent Claim 14 merely states a method of performing the abstract idea articulated in Claim 1. Independent Claim 11 and dependent claims 5 and 7-8 recite an additional generic computing unit—a "command distribution unit"—for distributing commands to the command processing units.

Dependent Claims 10 and 13 recite performing the data stripe operations "in parallel," which simply adds a timing component to abstract idea of using distributed processing for data striping recited in claim 1. Other dependent claims recite (1) additional details about the calculation of parity data, such as using a specific known method for calculating parity data or the use of a stripe count to monitor from completion of the parity block, (2) additional generic "memories" and "data networks" for performing their conventional functions of processing and storing data, or (3) the use of "flow identifiers" to aid in distributing commands. None of these claims alter the fundamental abstract idea claimed or introduce any inventive concept, and claim 1 is thus representative.

Because all of the claims of the '346 Patent are directed to an abstract idea and lack any inventive concept apart from that idea, they lack subject-matter eligibility.

VI. THE '085 PATENT

A. INVALIDITY CONTENTIONS BASED ON U.S.C. §§ 102 AND 103

Western Digital contends that the asserted claims are invalid as anticipated by prior art under 35 U.S.C. § 102 and/or that the asserted claims are obvious in view of prior art and/or the knowledge of a person having ordinary skill in the art under 35 U.S.C. § 103. Western Digital reserves the right to rely on any identified piece of prior art to anticipate the asserted claims and/or to render obvious the asserted claims in view of the knowledge of one having ordinary skill in the art or in combination with other references identified herein.

The table below list prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the '085 Patent. The charts submitted as Exhibits B1-B16 to these Invalidity Contentions and this Section specifically point out, as non-limiting examples, where the prior art identified by Western Digital anticipates, either expressly or inherently, and/or renders obvious each element of the asserted claims under at least 35 U.S.C. §§ 102(a), (b), (e), or (g). Western Digital's citations to exemplary and illustrative portions of the prior art references should not be construed as admissions that other portions of the identified prior art references are not also relevant to the validity of the claims. Other passages of the identified prior art references are not also relevant to the validity of the claims. Other passages of the identified prior art may additionally disclose, either expressly or inherently, information relevant to the validity of one or more elements of the asserted claims. Western Digital reserves the right to rely on any unquoted portions of the prior art as further evidence of the invalidity of the asserted claims. Moreover, Western Digital reserves the right to rely on any evidence, including expert testimony, to provide context to or aid in understanding the prior art and the cited portions of the identified prior art. Where Western Digital cites a particular drawing or figure, the citation is expressly intended to encompass the drawing or figure, as well as any text associated with the drawing or figure. Similarly, where Western Digital cites to a particular description of or text associated with a drawing or figure, the citation is expressly intended to encompass that drawing or figure as well. The evidence cited for each independent claim included in the exhibit is necessarily incorporated for each subsequent dependent claim in the exhibit.

Certain pieces of identified prior art inherently or implicitly disclose features of the asserted claims. Western Digital reserves the right to rely on inherency and/or secondary documents to demonstrate the invalidity of the asserted claims based on the inherent or implicit disclosure in these cited prior art documents. Further, Western Digital may rely on any evidence, including expert testimony, to establish the implicit or inherent disclosure of certain features of the prior art to invalidate the asserted claims. Western Digital also reserves the right to rely on any evidence, including expert testimony, to prove that the disclosures or prior art cited herein are enabled or to explain the meaning of a term used in the disclosures or any prior art cited herein.

Western Digital identifies below a number of Prior Art Systems and Services, the function of which is not publicly available. Western Digital intends to conduct third-party discovery and reserves the right to amend these Contentions upon the discovery of additional information concerning the identified Prior Art Systems and Services.

1. Identification of Prior Art Patents, Patent Publications, and Printed Publications to the Asserted Claims of the '085 Patent

Exhibit	Reference	Filing/Priority Date	Date of Issue or Publication	Short Cite
B1	U.S. Patent No. 8,176,360 to Frost et al.	August 11, 2009	May 8, 2012	Frost
B2	U.S. Patent Application Pub. 2014/0136927 to Li et al.	October 27, 2010	May 15, 2014	Li
B3	U.S. Patent Application Pub. 2011/0072331 to Sakaue et al.	June 1, 2010	Mar. 24, 2011	Sakaue
B4	U.S. Patent Application Pub. 2008/0333490 to Leung et al.	March 8, 2007	September 11, 2008	Leung
B5	U.S. Patent Application Pub. 2011/0090734 to Burger et al.	March 11, 2009	April 21, 2011	Burger
B6	U.S. Patent No. 8,042,029 to Alrod et al.	May 21, 2006	October 18, 2011	Alrod
B7	U.S. Patent No. 7,844,877 to Litsyn et al.	November 15, 2004	November 30, 2010	Litsyn
B8	U.S. Patent No. 8,539,300 to Otsuka et al.	July 13, 2010	September 17, 2013	Otsuka
B9	U.S. Patent Application Pub. 2010/0131806 to Weingarten et al.	September 17, 2008	May 27, 2010	Weingarten

B10	Shark SECC – Supported parameters and modes – Preliminary proposal		March 1, 2008	Shark SECC Spec
B11	Track II SECC – Structure Algorithms		August 11, 2006	Spinner (Track II) SECC
	Spinner Strong ECC (Track II)		February 2007	
B12	U.S. Patent No. 9,037,951 to Cideciyan et al.	December 17, 2009	May 19, 2015	Cideciyan
B13	U.S. Patent No. 8,892,980 to Fillingim	June 15, 2010	November 18, 2014	Fillingim
B14	U.S. Patent No. 8,418,042 to Kanno	March 24, 2010	April 9, 2013	Kanno
B15	U.S. Patent Application Pub. 2010/0241928 to Kim et al.	March 18, 2009	September 23, 2010	Kim
B16	U.S. Patent Application Pub. 2007/0283214 to Lasser	May 10, 2006	December 6, 2007	Lasser

2. Identification of Prior Art Systems/Services to The Asserted Claims of the ’085 Patent

Exhibit	System/Service	Relevant Dates	Person/Entities Involved in Prior Use, Sale, or Offers for Sale	Short Cite
--	Texas Memory Systems, Inc. and/or IBM, Corp. products that embody US	2009	Texas Memory Systems, Inc. IBM Corp.	

	Patent No. 8,176,360 to Frost et al.			
--	LSI Corporation products that embody U.S. Patent Application Pub. 2014/0136927 to Li et al.	2010	LSI Corporation, Avago Technologies, Broadcom, Inc.	
--	Toshiba products that embody U.S. Patent Application Pub. 2011/0072331 to Sakaue et al. and/or US Patent No. 8,418,042 to Kanno	2010	Toshiba	
--	Intel Corporation products that embody U.S. Patent Application Pub. 2008/0333490 to Leung et al.	2007	Intel Corporation	
--	Broadcom Ltd. products that embody U.S. Patent Application Pub. 2011/0090734 to Burger et al.	2009	Broadcom Ltd.	
--	Western Digital or SanDisk products that embody US Patent No. 8,042,029 to Alrod	2006	Western Digital SanDisk	
--	Western Digital, SanDisk, or M-Systems Ltd. products that	2006	Western Digital SanDisk M-Systems	

	embody US Patent Application Publication 2007/0283214 to Lasser			
--	Fuision-io, Inc. products that embody US Patent No. 8,892,980 to Fillingim	2010	Fusion-io, Inc.	
--	IBM Corp. products that embody US Patent No. 9,037,951	2010	IBM Corp.	
--	Panasonic Corp. products that embody US Patent No. 8,539,300	2013	Panasonic Corp.	
--	DensBits Technologies Ltd. products that embody US Patent Application Publication 2007/0283214 to Weingarten	2010	DensBits Technologies Ltd., Broadcom Inc.	
B10; B11	SharkMp6 and SpinnerMp6 Products included in Appendix D[4]	2006 through May 22, 2012	Western Digital SanDisk	

Nothing in the Charts for the above-identified references should be construed as an express or implied admission that Defendants agree with Plaintiff's infringement or claim construction theories. Defendants contend that they do not

[4] Identification of SharkMp6 and SpinnerMp6 as prior art systems and any associated theory of invalidity is based on the apparent interpretation of claims used by Polaris in its Infringement Contentions.

infringe any claim of the ’085 Patent. But to the extent that Plaintiff argues that Defendants infringe the ’085 Patent based on the theories within its infringement contentions, Defendants contend that the functionality cited in Plaintiff’s infringement contentions predate the ’085 Patent. As a non-limiting example, Plaintiff’s infringement contentions allege that the concepts of “puncturing” and “shortening” map to a change in data payload size. *See e.g.*, Infringement Contentions, Exhibit B at 20. Defendants accused products do not infringe the ’085 Patent by implementing the concepts of “puncturing” and/or “shortening.” However, to the extent that it is found that Defendant does infringe by implementing these features, these concepts predate the ’085 Patent, and as disclosed in the charts for the above-identified references, the prior art anticipates and/or renders obvious the ’085 Patent based on this theory.

3. Obviousness Combinations

To the extent that any one of the anticipating references is found not to disclose a limitation recited in the Asserted Claims, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the Asserted Patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and any claim(s) from which this claim depends and/or (ii) to combine said reference with any other of the references in Exhibits B1-B16 and/or with a POSITA’s general knowledge. Generally, motivation to combine any of these references exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. Below, Western Digital provides specific examples of combinations of prior art that render the asserted claims of the Patent-in-Suit obvious. All claims that are anticipated by a particular reference are also rendered obvious by that same reference alone, or in combination of two or more references. These specific references and/or combinations are merely examples of the grounds set forth in the Exhibits.

A POSITA would have been motivated to combine any of the references described in attached Exhibits B1-B16, including for the reasons described below. A POSITA at the time of filing of the Asserted Patent would have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them for at least the following exemplary reasons.

Western Digital contends that it would have been obvious to modify the above-listed prior art to include any allegedly missing element, in view of the knowledge of one of ordinary skill in the part, the admitted prior art of the Asserted Patent, and/or in combination with any of the other prior art references identified for the Asserted Patent. Western Digital reserves the right to rely upon aby combination of prior art references whether listed herein or otherwise. The combinations and modifications of the prior art, which render obvious the asserted claims of the Patent-in-Suit, arise from ordinary innovation, ordinary skill, common sense, and/or would have been obvious to try or otherwise predictable. In addition, design improvements and other market forces would have prompted those combinations and modifications.

A POSITA having knowledge of the above listed patents, articles, and systems, among other things, would be motivated, taught, and suggested to combine the prior art discussed in Exhibits B1-B16 with one another in a number of ways, including as detailed below.

Each of the references cited in Exhibits B1-B16 is analogous art to the ’085 Patent: (1) each reference is from the same field of endeavor as the alleged invention (even if the reference addresses a different problem); and/or (2) each reference is reasonable pertinent to the problem faced by the named inventors of the ’085 Patent (even if the reference is not in the same field of endeavor as the claim invention). It therefore would have been obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. All of the prior art references in Exhibits B1-B16 are related to systems and methods for generating parity data in the field of nonvolatile memory controllers, were authored, designed, and developed during the same time period, and a person of ordinary skill in the art would have been motivated to apply the teachings of any one reference to any other reference because they would improve upon such a reference's teachings.

Group A	Group B	Group C
• Frost • Fillingim • Cideciyan • Kanno • Otsuka • Li • Burger	• Leung • Weingarten • Fillingim • Kim • Li • Alrod • Lasser • Cideciyan • Kanno • Otsuka • Burger • Litsyn • Shark SECC • Track II SECC (Spinner)	• Kanno • Otsuka • Sakaue • Fillingim • Cideciyan • Lasser • Kim • Burger • Li • Litsyn • Shark SECC • Track II SECC (Spinner)

A POSITA would understand that flash memory degrades over its lifetime as it is used. *Memory Systems* at 865, 880. Error correction coding (ECC) schemes are employed to detect and correct errors. Many well-known ECC algorithms exist—e.g., Reed-Solomon (RS), Bose-Chadhuri-Hocquengem (BCH), and Low Density Parity Checks (LDPC). A POSITA would have understood that different ECC algorithms are better suited for different types of errors and vary in reliability, complexity, and efficiency. In addition to variation in algorithm—e.g., RS, BCH, and LDPC—ECC schemes can vary in the parameters that define the ECC scheme—e.g., data payload size, correction capability—what the '085 Patent calls a "gear."

Generally using a more complex ECC algorithm and/or using a ECC "gear" with a larger correction capability increases reliability and longevity of the flash memory since the likelihood of errors increases with usage—the more complex scheme will continue to be able to correct the errors later in the flash memory's lifetime when more errors are likely to occur. Kanno 1:18-52; Lasser at [0012]-[0021]. However, the cost is data processing speed and increased data overhead—more bits are required for ECC meaning there are fewer bits for storing regular information. Lasser at [0019]. This can lead to diminishing returns, especially early in the life of the flash memory if a more complex algorithm or higher "gear" than necessary is used when there is a low probability of errors.

A POSITA would have been motivated to apply the well-known technique of using an ECC scheme including primary and secondary parity symbols with the flash memory system of each '085 reference. A POSITA would have understood that an ECC scheme with primary and secondary parity symbols provide the benefits of improved ECC performance by utilizing the benefits of different ECC algorithms. *See e.g.*, Sakaue at [0005]-[0008] (explaining employing a concatenated code utilizing both an LDPC code and a BCH code for combining their respective benefits); Fillingim at 7:66-8:6; Weingarten at [0040], [0041], [0196]; Lasser at [0012]-[0021], [0053], [0068]-[0069]; Li at [0091]; Burger at [0039]. For example, a second, more complex ECC algorithm may be employed to correct the errors missed by a lower complexity algorithm, thereby allowing the flash memory to make use of the faster, lower complexity algorithm without sacrificing reliability. Lasser at [0012]-[0021], [0053], [0068]-[0069]. Additionally, a POSITA would have understood that utilizing different ECC algorithms increases reliability as some algorithms (e.g., RS, BCH, LDPC) are better suited for handling different types of errors (e.g., random errors, burst errors, etc.).

A POSITA would have understood that another way of increasing reliability while also optimizing data overhead is to dynamically change the "gear" of the ECC scheme—e.g., code rate, payload size, etc.—in response to the error rate of a given page of flash memory. Kim at [0031]; Fillingim at 50:65-51. As the code rate decreases (an increase in strength of the gear), more data can be corrected, but metadata overhead increases (i.e., the more parity bits there are, the fewer bits are left for information data). Kim at [0031]; Fillingim at 50:65-51. A system that is configured to dynamically select a lower code rate for pages that have a higher error rate and a higher code rate for pages that have a lower error rate optimizes the data overhead for areas with a lower error rate without sacrificing reliability for the areas with a higher error rate. Kim at [0029]-[0030], [0047]-[0048]; Fillingim at 20:30-56, 27:6-32, 50:65-51; Burger at [0039]; Leung at [0020]-[0034]; Weingarten at [0164]-[0171], Fig. 12.

A POSITA would have been further motivated to combine the concept of dynamic ECC "gear" selection with the concept of using a plurality of ECC algorithms with primary and secondary parity as both aim to improve the reliability and speed of the ECC system. Further, a POSITA would have been motivated to employ dynamic ECC coding to alleviate some of the issues with data overhead that is created by using a plurality of ECC algorithms with primary and secondary parity. Moreover, multiple prior art references employ a combination of these known techniques to some degree. *See e.g.*, Fillingim at 20:30-56, 27:6-32, 7:66-8:6, 37:58-38:15, 19:39-47, 48:5-49:4; Burger at [0038]-[0039], [0042]-[0044], [0051], [0053]-[0054]; Weingarten at [0040], [0041], [0078], [0196]; Kim [0029]-[0031], [0034], [0047]-[0048]. As a non-limiting example, Burger notes that "each page in a wordline can optionally be encoded with different code rates or different types of codes (***or both***)." Burger at [0039]. A POSITA, in view of Burger, which discloses both the concept of various code types along with dynamic ECC selection would be motivated to employ well-known techniques simultaneously.

For example, Fillingim also teaches that an ECC module might employ a "concatenated code"—e.g., "using two separate codes" such as BCH or RS. Fillingim at 7:66-8:6. It was already known that dynamic ECC selection could work using a variety of algorithms, such as BCH or Reed-Solomon (Leung at [0020]). It was further known that this dynamic ECC selection could be based on the determination of a bit error rate. Weingarten at [0105]. In other words, it was already known that (1) a single gear ECC scheme could be employed for memory with primary and secondary parity, (2) multi-gear schemes could be employed to correct errors, (3) an ECC scheme could be dynamically selected based on the bit error rate, and (4) dynamic ECC could be performed on code with varying types of parity. It thus would have been an obvious variation of any of these inventions to simply employ these ideas in tandem. For example, Weingarten, Fillingim, and Burger all disclose the concept of dynamic ECC scheme selection—including varying code rates, payload size, correction capability, etc.—and also disclose employing a concatenated code. In other words, the interconnectivity of these concepts was well-known, and to the extent that any of these references fails to teach one aspect of dynamic ECC selection and the use of primary and secondary parity, the combination of any two references directed to these concepts would have been combining prior art elements according to known methods to yield predictable results. *KSR*, 550 U.S. at 416-18.

However, a POSITA would also have understood that as an ECC scheme gets more complex, it also becomes more resource intensive and, in some cases, slower. Lasser [0019]. Accordingly, a POSITA would have appreciated a solution which would increase the data read and write speed of the combination. A POSITA would have known that one way of increasing data read and write speed would be to use striping, which allow access to a region (e.g., a stripe) including multiple pages for simultaneous read and write operations. *See e.g.*, Frost, 19:27-65; Fillingim 10:8-48; Cideciyan 10:35-11:57. Such a solution would prevent bottlenecking of operations forced to pass through a single channel. Since allowing two or more flash memory pages to be read simultaneously would increase the overall processing speed, a POSITA would have been motivated to combine simultaneous reads and writes with dynamic ECC selection and using primary and secondary parity. In the combination, an ECC gear is selected for the region based on the bit error rate associated with the region, which allows the system to dynamically select and apply the suitable error correction scheme for the specific region. Applying the selected ECC gear to the specific region can help streamline the read and write process, as the system doesn't need to handle varying levels of ECC across different pages when performing simultaneous reading/writing from the region, and which help to improve throughput and reduce processing time during parallel reads or writes from the region.

Indeed, it was already known that data striping and reading multiple pages simultaneously or in parallel could be employed with dynamic ECC selection. As a non-limiting example, Cideciyan, which discloses a method of dynamic ECC selection (*see e.g.*, Cideciyan at Figs. 11-12), also describes data striping that can be performed "sequentially or in parallel." Cideciyan at 11:43-44. Data striping was a generally known concept and it would have been an obvious variation to merely include this as a tertiary aspect of an invention employing dynamic ECC selection.

The invention of the '085 Patent generally relates to the combination of these three known concepts: (1) the use of primary and secondary parity, (2) dynamic ECC selection, and (3) applying the ECC scheme to a region of a fixed number of pages where the pages of the region can be read simultaneously.[5] However, as explained, each of these three concepts were known in the prior art, alone and in combination, and a POSITA would have been motivated to combine these concepts to practice the claimed invention of the '085 Patent.

The prior art references above disclose these concepts. The full extent of the disclosure of these references is captured in Exhibits B1-B16. The references in Group A contain extensive disclosure related to applying the ECC scheme to a region including pages that can be read simultaneously; the references in Group B contain extensive disclosure related to dynamic ECC selection; and the references in Group C contain extensive disclosure related to primary and secondary parity. For the

[5] While it is understood that the claims of the '085 Patent contain many limitations, the elements of the invention generally fall within these three categories.

foregoing reasons, a POSITA would have been motivated to combine these concepts and thus would have been motivated to combine any Group A reference with any Group B reference and any Group C reference. Moreover, to the extent that a reference contains extensive disclosure related to more than one group, such is evidence that a POSITA would have been motivated to combine these concepts and references. This is especially true of references with the same author or same assignee. An exemplary list of possible combinations is given in Appendix B**.**

B. INVALIDITY CONTENTIONS BASED ON U.S.C. § 112

At least in view of Polaris' apparent construction of the Asserted Claims in its infringement Contentions, the Asserted Claims are invalid because the specification as filed does not enable the claimed method. Thus, the patent disclosure would not enable a person of ordinary skill in the art to practice the method as asserted by Polaris. Further, at least in view of Polaris' apparent construction of the claims in its Infringement Contentions, the Asserted Claims are invalid because the specification as filed does not contain a written description of the claimed invention. In particular, the patent disclosure would not lead a person of ordinary skill in the art to understand that the named inventor had possession of the purported invention as asserted by Polaris. The Asserted Claims are invalid as indefinite under 35 U.S.C. § 112 for failing to particularly point out and distinctly claim the subject matter which the applicants regard as his invention.

Based on Polaris' Infringement Contentions and its apparent interpretation of the terms of the Asserted Claims, the following terms or limitations are indefinite, lack sufficient written description support, and/or are not enabled under § 112:

Claim Element	Claim[6]

[6] All claims dependent from claims that are indefinite, lack sufficient written description support, and/or are not enabled under § 112 for the listed reasons are also indefinite, lack sufficient written description support, and/or are not enabled under § 112 for the same reasons.

"determine[ing] a bit error rate associated with a region comprising a fixed number of two or more flash memory pages or integer functions thereof"	1, 15
"two or more flash memory pages of a region can be read simultaneously"	1, 15
"primary and secondary ECC parity symbols corresponding to the data payload of the region"	1, 15
"lower-latency ECC decode option"	14
"one or more higher-latency ECC decode options"	14
"the ECC encoder"	16
"the processor"	16

C. INVALIDITY CONTENTIONS BASED ON U.S.C. § 101

1. Claim 1 of the '085 Patent is directed to an abstract idea.

Claim 1 of the '085 Patent is directed to the abstract idea of selecting an error coding scheme for a region of a device based on an observed bit error rate. The claim, like others the Federal Circuit has found to claim patent-ineligible abstract ideas, is a "data manipulation claim[] that [is] recited at a high level of result-oriented generality" and thus "amount[s] to the mere implementation of abstract ideas." *Realtime Data LLC v. Array Networks Inc.*, No. 2021-2251, 2023 WL 4924814, at *10 (Fed. Cir. Aug. 2, 2023) (unpublished) (quoting *Koninklijke KPN N.V. v. Gemalto M2M GmbH*, 942 F.3d 1143, 1152 (Fed. Cir. 2019)) (internal alterations omitted).

The claim's steps consist entirely of data processing and manipulation: 1) ***determining*** an error rate associated with a region; 2) ***comparing*** that error rate with one or more predetermined thresholds; and 3) ***selecting*** among ECC schemes of varying levels of strength based partly on that comparison. *See* '085 Patent at Claim 1. Though the claim recites that a generic integrated circuit performs these steps, a human could also perform them mentally, a "telltale sign of their abstraction." *PersonalWeb*, 8 F.4th at 1316; *see also Elec. Power Grp.*, 830 F.3d at 1353–54 (noting that the Federal Circuit has consistently found claims generally reciting "collecting information, analyzing it, and displaying certain results of the collection and analysis" to be abstract); *see also Coffelt v. NVIDIA Corp.,* No. CV16–00457 SJO (KKx), 2016 WL 7507763, at *7 (C.D. Cal. June 21, 2016), aff'd, 680 F. App'x 1010 (Fed. Cir. 2017) (finding claims directed to "selecting a color for a portion of a digital image by calculating and comparing various vectors within a specific region of space" patent-ineligible because they were directed to an abstract, mathematical algorithm capable of being performed on pen and paper).

Although the claim relates to error correction coding schemes, the '085 Patent does not purport to disclose or claim any novel ECC technique. Instead, the claim merely takes ECC techniques "as a given and address[es] the threshold matter of choosing to use one or more such available techniques." *Realtime Data*, 2023 WL 4924814, at *8; *see also* '085 Patent at 1:52-58 (identifying several "ubiquitous" forms of ECC). The claim provides little guidance on how to make this selection—it states only that it must be based "at least partly" on comparing a bit error rate to one or more thresholds. The claim does not provide any details on the ECC schemes themselves other than that they have varying strength levels. As such, the claim is analogous to the claims directed to "choosing to use" one or more known data-compression techniques based on an unparticularized, abstract analysis found to "amount to a mere implementation of abstract ideas" in *Realtime Data*. 2023 WL

4924814, at *7-*8; *see also AI Visualize*, 97 F.4th at 1378 (Fed. Cir. 2024) (finding claims directed to using computers to collect, manipulate, and display data abstract).

Further, though the specification purports to solve a technological problem of increasing efficiency and performance in nonvolatile memory controllers by adapting the amount of memory space allocated to redundant or additional ECC data to an observed rate of error, *see, e.g.*, ’085 Patent at 2:23-27, 50:59-66, the idea of tailoring an amount of protection to a perceived amount of risk long predates nonvolatile memory devices and computers generally. For instance, that concept is fundamental to the insurance industry. Simply applying this abstract concept to the context of nonvolatile memory controllers does not make it any less abstract. *See, e.g.*, *Bilski*, 561 U.S. at 612 (holding claims applying the abstract concept of hedging unpatentable even when restricted to a particular technical environment); *PersonalWeb*, 8 F.4th at 1318 (claims directed to solving problems of access to, retrieval of, and redundancy control of information by using content labeling were not necessarily rooted in computer technology because both the problem and the solution long predated computers).

Accordingly, the claims of the ’085 Patent are directed to an abstract mental process involving data gathering and analysis.

2. Claim 1 of the ’085 Patent lacks any inventive concept apart from the abstract idea it claims.

Claim 1 of the ’085 Patent lacks any inventive concept apart from this abstract idea. The claim merely recites a generic “integrated circuit” for carrying out the claimed steps. As already noted, the specification does not purport to disclose any novel ECC scheme and instead explains that the claimed methods and systems can make use of various “ubiquitous” ECC schemes. ’085 Patent at 1:52-58; 2:39-41; 25:63-65. Instead, the only purported advancement embodied in the claims is the idea of using a measured bit error rate of a region to select among multiple known ECC schemes for use in that region. *See* ’085 Patent at 1:63-2:1, 2:23-27, 50:59-66. But that is the abstract idea itself and therefore cannot provide an inventive concept ***apart*** from that idea, as Alice Step Two requires. *ChargePoint*, 920 F.3d at 774 (quoting *BSG Tech LLC v. Buyseasons, Inc*., 899 F.3d 1281, 1290 (Fed. Cir. 2018)) ("[A] claimed invention's use of the ineligible concept to which it is directed cannot supply the inventive concept that renders the invention 'significantly more' than that ineligible concept."). Even if it were not abstract, the idea of tailoring protection to risk or adjusting "gears" based on the difficulty presented by a region (such as on a bike) is hardly unconventional.

Claim 1 of the '085 Patent is directed to the mental process of selecting an error coding scheme by determining a bit error rate and comparing it to one or more thresholds. The claim adds nothing to this mental process beyond instructions to implement it using conventional means and thus lacks patent-eligible subject matter.

Further, any additional features of the '085 Patent are nothing more than conventional elements which can be found in the prior art including:

- The use of primary and secondary ECC parity symbols that are at least partially orthogonal. *See e.g.*, Cideciyan at 10:35-11:57, Fig. 4, Fig. 5; Kanno at 18:49-62, Fig. 11, 13-17.
- Determining a bit error rate associated with a region associated with a plurality of flash memory pages or integer fractions thereof and comparing the determined bit error rate to one or more predetermined thresholds corresponding to a set of predefined gears comprising at least a first gear and a second gear. *See e.g.*, Leung at [0020]-[0025], [0033]-[0040], [0048], Fig. 4; Kim at [00006]-[0008]; Lasser at [0009]-[0014], [0058]-[0064], [0066]-[0070].
- Allocating one or more remaining regions to one of at least a first gear or a second gear based at least partly on the BER for the region. *See e.g.*, Kanno at 18:49-62, Fig. 11, 13-17; Burger at [0066]-[0068], Fig. 12; Cideciyan at 16:34-17:5; Kim at [0044]-[0045], Fig. 4A-4C.

- Wherein the first gear and the second gear vary by data payload size and correction capability. *See e.g.*, Leung at [0016]-[0021]; Sakaue at [0034]-[0051], [0053]-[0058], Fig. 4.
- Wherein different gears correspond to different error correction coding (ECC) schemes for regions of the flash drive. *See e.g.*, Leung at [0020]-[0040]; Burger at [0038]-[0039], [0046]-[0049]; Cideciyan at 3:54-4:26, 16:34-17:5.
- Dynamically re-gearing regions. *See e.g.*, Leung at [0020]-[0040]; Kim at [00006]-[0008], [0029]-[0034], [0036]-[0037]; Lasser at [0009]-[0014], [0058]-[0064], [0066]-[0070].

3. Claim 1 is representative.

The Court need not address each individual claim when there are representative claims and "all the claims are 'substantially similar and linked to the same abstract idea.'" *Content Extraction*, 776 F.3d at 1348.

Claim 1 of the '085 Patent is representative of all of the patent's claims. Each claim is directed to the same mental process of 1) determining an error rate associated with a region; 2) comparing that error rate with one or more predetermined thresholds corresponding to a set of predefined ECC schemes; and 3) selecting an ECC scheme based partly on that comparison. Independent Claims 15 and 24 merely recite apparatuses for performing the method of Claim 1, with Claim 15 reciting generic "circuits" for performing the claimed steps and Claim 24 reciting "means for" performing them. Dependent Claims 2 and 3 simply require performing the claimed method more than once. Other dependent claims require performing the method of Claim 1 in concert with other conventional methods of flash initialization, read or write operations. Performing the methods in parallel with other operations is itself an abstract idea and does not supply an inventive concept. *See Kinglite Holdings*, 2016 WL 4205356, at *3-*5.

Dependent Claims 31-33 recite well-understood concepts regarding the use of multi-layer parity coding schemes. And the remaining dependent claims merely provide additional detail regarding the estimation of the bit error rate or the parameters of acceptability in comparing the bit error rate to predetermined thresholds. None of these details alter the fundamental abstract idea claimed or introduce any inventive concept, and Claim 1 is thus representative.

Because all of the claims of the ’085 Patent are directed to an abstract idea and lack any inventive concept apart from that idea, they lack subject-matter eligibility.

VII. THE ’968 PATENT

A. INVALIDITY CONTENTIONS BASED ON U.S.C. §§ 102 AND 103

Western Digital contends that the asserted claims are invalid as anticipated by prior art under 35 U.S.C. § 102 and/or that the asserted claims are obvious in view of prior art and/or the knowledge of a person having ordinary skill in the art under 35 U.S.C. § 103. Western Digital reserves the right to rely on any identified piece of prior art to anticipate the asserted claims and/or to render obvious the asserted claims in view of the knowledge of one having ordinary skill in the art or in combination with other references identified herein.

The table below list prior art that anticipates and/or renders obvious one or more of the Asserted Claims of the ’968 Patent. The charts submitted as Exhibits C1-C16 to these Invalidity Contentions and this Section specifically point out, as non-limiting examples, where the prior art identified by Western Digital anticipates, either expressly or inherently, and/or renders obvious each element of the asserted claims under at least 35 U.S.C. §§ 102(a), (b), (e), or (g). Western Digital’s citations to exemplary and illustrative portions of the prior art references should not be construed as admissions that other portions of the identified prior art references are not also relevant to the validity of the claims. Other passages of the identified prior art references are not also relevant to the validity of the claims. Other passages of the identified prior art may additionally disclose, either expressly or inherently, information relevant to the validity of one or more elements of the asserted claims. Western Digital reserves the right to rely on any unquoted portions of the prior art as further evidence of the invalidity of the asserted claims. Moreover, Western Digital reserves the right to rely on any evidence, including expert testimony, to provide context to or aid in understanding the prior art and the cited portions of the identified prior art. Where Western Digital cites a particular drawing or figure, the citation is expressly intended to encompass the drawing or figure, as well as any text associated with the drawing or figure. Similarly, where Western Digital cites to a particular description of or text associated with a drawing or figure, the citation is expressly intended to encompass that drawing or figure as well. The evidence cited for each independent claim included in the exhibit is necessarily incorporated for each subsequent dependent claim in the exhibit.

Certain pieces of identified prior art inherently or implicitly disclose features of the asserted claims. Western Digital reserves the right to rely on inherency and/or secondary documents to demonstrate the invalidity of the asserted claims based on the inherent or implicit disclosure in these cited prior art documents. Further, Western Digital may rely on any evidence, including expert testimony, to establish the implicit or inherent disclosure of certain features of the prior art to invalidate the asserted claims. Western Digital also reserves the right to rely on any evidence, including expert testimony, to prove that the disclosures or prior art cited herein are enabled or to explain the meaning of a term used in the disclosures or any prior art cited herein.

Western Digital identifies below a number of Prior Art Systems and Services, the function of which is not publicly available. Western Digital intends to conduct third-party discovery and reserves the right to amend these Contentions upon the discovery of additional information concerning the identified Prior Art Systems and Services.

1. Identification of Prior Art Patents, Patent Publications, and Printed Publications to the Asserted Claims of the '968 Patent

Exhibit	Reference	Filing/Priority Date	Date of Issue or Publication	Short Cite
C1	U.S. Patent Application Pub. 2010/0262979 to Borchers et al.	August 7, 2009	October 14, 2010	Borchers
C2	PCI Local Bus Specification Revision 3.0	--	February 3, 2004	PCI Spec
	PCI Express® 2.0 Base Specification Revision 0.9	--	September 11, 2006	
C3	U.S. Patent Application Pub. 2011/0197003 to Serebrin et al.	February 5, 2010	August 11, 2011	Serebrin
C4	U.S. Patent No. 8,321,615 to Foong et al.	December 18, 2009	November 27, 2012	Foong
C5	U.S. Patent No. 7,743,195 to Bney-Moshe	December 27, 2006	June 22, 2010	Bney-Moshe
C6	U.S. Patent No. 7,337,248 to Rao et al.	March 19, 2004	February 26, 2008	Rao
C7	U.S. Patent No. 7,263,568 to Shah et al.	March 31, 2004	August 28, 2007	Shah I
C8	U.S. Patent No. 7,853,957 to Shah et al.	October 19, 2006	December 14, 2010	Shah II
C9	U.S. Patent No. 8,291,135 to Subramanian et al.	January 15, 2010	October 16, 2012	Subramanian

C10	U.S. Patent No. 7,197,588 to Tsao et al.	October 13, 2005	March 27, 2007	Tsao
C11	U.S. Patent No. 7,290,077 to Gregg et al.	April 7, 2005	October 30, 2007	Gregg
C12	U.S. Patent Application No. 2007/0271401 to Louzoun et al.	May 16, 2006	November 22, 2007	Louzoun
C13	"Efficient Remote Block-level I/O over an RDMA-capable NIC" by Marazakis et al.		2006	Marazakis
C14	U.S. Patent No. 6,128,669 to Moriarty et al.	September 30, 1997	October 3, 2000	Moriarty
C15	U.S. Patent No. 7,478,186 to Onufryk et al.	June 3, 2004	January 13, 2009	Onufryk
C16	NVMe 1.0		March 1, 2011	NVMe

2. Identification of Prior Art Systems/Services to The Asserted Claims of the '968 Patent

Exhibit	System/Service	Relevant Dates	Person/Entities Involved in Prior Use, Sale, or Offers for Sale	Short Cite
--	SharkMp6 and SpinnerMp6 Products included in Appendix D[7]	2006 through August 16, 2010	Western Digital, SanDisk	

[7] Identification of SharkMp6 and SpinnerMp6 as prior art systems and any associated theory of invalidity is based on the apparent interpretation of claims used by Polaris in its Infringement Contentions.

--	Intel Corporation products that embody US Patent No. 7,263,568 to Shah and US Patent No. 7,853,957 to Shah	2005	Intel Corporation	
--	Intel Corporation products that embody US Patent No. 7,743,195 to Bney-Moshe	2006	Intel Corporation	
--	Intel Corporation products that embody US Patent No. 8,321,615 to Foong	2009	Intel Corporation	
--	Intel Corporation products that embody US Patent Application Publication No. 2007/0271401 to Louzoun	2006	Intel Corporation	
--	Intel Corporation products that embody US Patent No. 7,197.588 to Tsao	2004	Intel Corporation	
--	Sun Microsystems, Inc. products that embody US Patent No. 7,337,248	2004	Sun Microsystems, Inc. Oracle	
--	IBM Corporation products that embody US Patent No. 7,290,077	2005	IBM Corporation	

--	Compaq Computer Corporation products that embody US Patent No. 6,128,669	1997	Compaq Computer Corporation HP Inc.	
--	VMWare, Inc. products that embody US Patent No. 8,291,135	2010	VMWare, Inc.	
--	Advanced Micro Devices, Inc. products that practice US Patent Application No. US 2011/0197003	2010	Advanced Micro Devices, Inc.	
--	Products that practice PCI Local Bus Specification Revision 3.0 or PCI Express® 2.0 Base Specification Revision 0.9			

Nothing in the Charts for the above-identified references should be construed as an express or implied admission that Defendants agree with Plaintiff's infringement or claim construction theories. Defendants contend that they do not infringe any claim of the '968 Patent. But to the extent that Plaintiff argues that Defendants infringe the '968 Patent based on the theories within its infringement contentions, Defendants contend that the functionality cited in Plaintiff's infringement contentions predate the '968 Patent. As a non-limiting example, Plaintiff's infringement contentions allege that Defendants infringe by implementing concepts contained in the NVMe standard. *See e.g.*, Infringement Contentions, Exhibit A. Defendants accused products do not infringe the '968 Patent by implementing the concepts. However, to the extent that it is found that Defendant does infringe by implementing these features, these concepts predate the '968 Patent, and as disclosed in the charts for the above-identified references, the prior art anticipates and/or renders obvious the ’968 Patent based on this theory.

3. Obviousness Combinations

To the extent that any one of the anticipating references is found not to disclose a limitation recited in the Asserted Claims, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the Asserted Patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and any claim(s) from which this claim depends and/or (ii) to combine said reference with any other of the references in Exhibits C1-C16 and/or with a POSITA’s general knowledge. Generally, motivation to combine any of these references exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. Below, Western Digital provides specific examples of combinations of prior art that render the asserted claims of the Patent-in-Suit obvious. All claims that are anticipated by a particular reference are also rendered obvious by that same reference alone, or in combination of two or more references. These specific references and/or combinations are merely examples of the grounds set forth in the Exhibits.

A POSITA would have been motivated to combine any of the references described in attached Exhibits C1-C16, including for the reasons described below. A PHOSITA at the time of filing of the Asserted Patent would have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them for at least the following exemplary reasons.

Western Digital contends that it would have been obvious to modify the above-listed prior art to include any allegedly missing element, in view of the knowledge of one of ordinary skill in the part, the admitted prior art of the Asserted Patent, and/or in combination with any of the other prior art references identified for the Asserted Patent. Western Digital reserves the right to rely upon aby combination of prior art references whether listed herein or otherwise. The combinations and modifications of the prior art, which render obvious the asserted claims of the Patent-in-Suit, arise from ordinary innovation, ordinary skill, common sense, and/or would have been obvious to try or otherwise predictable. In addition, design improvements and other market forces would have prompted those combinations and modifications.

A POSITA having knowledge of the above listed patents, articles, and systems, among other things, would be motivated, taught, and suggested to combine the prior art discussed in Exhibits C1-C16 with one another in a number of ways, including as detailed below.

Each of the references cited in Exhibits C1-C16 is analogous art to the '968 Patent: (1) each reference is from the same field of endeavor as the alleged invention (even if the reference addresses a different problem); and/or (2) each reference is reasonable pertinent to the problem faced by the named inventors of the '968 Patent (even if the reference is not in the same field of endeavor as the claim invention). It therefore would have been obvious for someone of ordinary skill in the art to identify and combine elements from these references and devices. All of the prior art references in Exhibits C1-C16 are related to systems and methods for generating parity data in the field of nonvolatile memory controllers, were authored, designed, and developed during the same time period, and a person of ordinary skill in the art would have been motivated to apply the teachings of any one reference to any other reference because they would improve upon such a reference's teachings.

Group A	**Group B**
• Borchers • Shah I • Shah II • Rao • NVMe 1.0	• Bney-Moshe • Foong • Gregg • Louzoun • Marazakis • Moriarty • Onufryk • PCI Spec

	• Serebrin • Subramanian • Tsao

The references above in Group A anticipate and/or render obvious every limitation of the Asserted Claims of the '968 Patent. However, to the extent that any of the references in Group A do not disclose a limitation, a POSITA would have found it obvious to combine that Group A reference with one or more other Group A reference and/or with one or more Group B references.

First, all of the above references are generally in the same "field of endeavor." *KSR*, 550 U.S. at 417. Specifically, all of the above references relate to nonvolatile memory controllers, specifically directed towards interrupt processing and the use of completion queues to alert a host processing unit as to the status of a command. Since all are aimed at improving the efficiency of these technologies, a POSITA would be motivated to combine the above references to yield variations of the known concepts therein. *Id.*

Second, the above references all disclose well-known concepts for nonvolatile memory controllers, namely "interrupts," "interrupt vectors," "completion queues," "doorbell registers," and "interrupt coalescing"/"interrupt vector states." POSITA would have understood that it was common to use completion status queues to alert a host processing unit to the completion status of a command instead of having the host processing unit constantly poll the completion queue. A POSITA would understand that "[t]oo many CPU interrupts are not desirable since the interrupts preemptor stall the data processing operations by the CPU and after the interrupts are processed by the CPU the data processing operations are then resumed. Consequently, by minimizing CPU interrupts by the adaptive synchronization techniques described herein, data transfer rates may be optimized." *See e.g.*, Rao at 9:20-26. Accordingly, a

POSITA would be motivated to combine these known elements to yield predictable results. *KSR*, 550 U.S. at 416.

Third, a POSITA would have been motivated to combine references that seek to solve the same problems and aim to comply with the relevant standards—e.g., PCIe/PCI, MSI/MSI-X, NVMe, DMA etc. All of the above references are such references that aim to optimize interrupts for nonvolatile memory controllers and aim to comport to the relevant standards. *See e.g.*, Borchers at [0029], [0110]; Shah I at 2:48-3:4; Rao at 4:38-5:17; Tsao at 3:12-31, 4:58-5:10; Onufryk at 1:13-3:57; Foong at 2:37-4:2; Serebrin at [0038]; Moriarty at 1:8-3:12. The standards exist to facilitate compatibility of multiple technologies such that variations and improvements may be used together, substituted, or improved.

Moreover, specific citations to the relevant standards within the references above may be seen as a teaching, suggestion, or motivation to combine the references. As a non-limiting example, a POSITA would have found it obvious to implement Borchers' techniques according to standardized practices such as those defined in the PCIe/PCI standards. Borchers describes a known interface device for communication between a host and memory controller. Borchers explains that "the high speed interface may include a PCIe interface." Borchers, [0110]. "The PCIe interface 108 may include a connector to the host 106 such as, for example, a PCIe connector cable assembly. Other high speed interfaces, connectors and connector assemblies also may be used." Borchers, [0110]. Accordingly, a POSITA would have looked to known techniques for implementing a PCI Express interface. It would have been obvious to look to the known standards documentation such as the PCI Express Base Standard and the PCI standard. Indeed, the PCI Express standard states that "describes the PCI Express architecture, interconnect attributes, fabric management, and the programming interface required to design and build systems and peripherals that are compliant with the PCI Express specification." PCIe, 21.

For example, one aspect of the memory interface is how it implements interrupt signals. Borchers explains that "The interrupt processor 124 is configured to signal the host 106 with an interrupt when new responses are available in the response buffer 123." Borchers, [0035]. A POSITA would have found it obvious to thus implement the interrupt signals according to the PCI Express standard. As stated in the PCI Express standard, "All PCI Express device Functions that are capable of generating interrupts must implement MSI or MSI-X or both." PCIe, 453. "MSI and the MSI Capability structures are defined in the PCI Local Bus Specification, Revision 3.0." PCIe, 453. PCIe describes a "Message Signaled Interrupt (MSI/MSI-X)" which are "Two similar but separate mechanisms that enable a device to request service by writing a system-specified DWORD of data to a system-specified address using a Memory Write Request. Compared to MSI, MSI-X supports a larger maximum number of vectors and independent message address and data for each vector." PCIe, 26. See also PCIe, 458.

The PCI Local Bus Specification also explains that MSI and MSI-x interrupts use vectors. "System software initializes the message address and message data (from here on referred to as the '**vector**') during device configuration, allocating one or more vectors to each MSI capable function." PCI, 231. Accordingly, it would have been obvious that Borchers' interrupt signals, implemented according to the PCI Express standard, would have used interrupt vectors.

Accordingly, the combination of Borchers and the PCIe/PCI standards would have predictably resulted in interrupt signals implemented using interrupt vectors. A POSITA would have had a reasonable expectation of success because the PCIe/PCI standards are tried-and-true, industry vetted implementations. The PCIe standard is "an enhancement to the PCI architecture" which was "the most widely accepted and implemented expansion standard in the world." PCIe, 21; PCI, 15; *KSR*, 550 U.S. at 418.

To extent that any limitation was taught by any of the references above, a POSITA would have been motivated to look to known techniques for interrupt controllers such as that disclosed in the NVMe 1.0 specification. As previously stated, all of the above references are generally directed towards interrupt processing in Non-Volatile Memory (NVM) or other similar storage applications. Accordingly, a POSITA would be motivated to create variations of the inventions in the references by substituting elements from other well-known methods, such as those disclosed in the NVMe 1.0 specification. Moreover, since NVMe 1.0 and the other references are designed for compatibility with the PCIe specification, such is another reason that a POSITA would reasonably expect to succeed in combining any of the above references with the NVMe 1.0 specification. *KSR*, 550 U.S. at 417-418.

As a non-limiting example, Borchers, Shah I, Shah II, and Rao all generally disclose methods for interrupt coalescing via various methods of counters, timers, empty queue indicators, etc. Borchers at [0035]-[0039]; Rao at 8:51-10:37; Shah I at 8:11-17; Shah II at 16:22-29. When implementing the interrupt coalescing methods of these references, a POSITA would have been motivated to implement standard and known techniques such as those taught in the NVMe 1.0 specification. *KSR*, 550 U.S. at 417-418. Further, the NVMe's goal of compatibility and inter-connectivity of a plurality of applications sharing the same goal would provide a design incentive for a POSITA to seek variations from a standard such as the NVMe and other NVMe compatible applications. *KSR*, 550 U.S. at 417-418. Accordingly, a POSITA would have been motivated to combine the NVMe with references such as Borchers, Shah I, Shah II, and Rao.

Moreover, and for the same reasons explained above, a POSITA would have been motivated to combine Borchers, Shah I, Shah II, and Rao together. For example, a POSITA would have an expectation of success in combining the well-known interrupt coalescing techniques disclosed in these references. *Id.* A POSITA also would have been motivated to substitute variations of known interrupt coalescing methods or to use them in parallel. For example, as explained in detail in the charted exhibits, variations of interrupt coalescing such as using timers or counters to determine when to send and interrupt message. To the extent that a reference discloses an interrupt timer (e.g., *Shah I* at 5:21-28), it would have been obvious to substitute known methods for interrupt counters or empty queue indicators (*Rao* at 8:51-10:37), and vice versa. *KSR*, 550 U.S. at 417-418.

As explained in detail in Exhibits C1-C16, the concepts of "interrupts," "interrupt vectors," "completion queues," "doorbell registers," and "interrupt coalescing" were all well-known concepts in the art that a POSITA would have known were applicable to the area of interrupt processing, including in the field of nonvolatile memory controllers. Accordingly—and especially since all of the above reference are designed to be compatible with the common set of relevant standards—a POSITA would generally expect to succeed in combining any two or more of the above references. Thus, to the extent that any of the above references does not include disclosure related to one of these concepts or of any limitation of the Asserted Claims of the '986 Patent, a POSITA would have been motivated to combine two or more of the above references for that element. This is especially true of references with the same author or same assignee. For example, a POSITA would have been motivated to combine and expect to succeed in combining the inventions of *Shah I* and *Shah II* because they have the same inventor, have overlapping disclosure, are related to the same basic field of endeavor, and are aimed at solving the same basic problem. *Compare* Shah I *with* Shah II. The level of overlap between these patents would provide a strong "design incentive[] for a POSITA to combine these two references. *KSR*, 550 U.S. at 417-418.

Moreover, to the extent that any disclosure is directed to a broader field of endeavor related to memory management than nonvolatile memory, it would have been obvious to implement such techniques with known techniques for managing nonvolatile memory. *Id.* As a non-limiting example, while the disclosure in *Shah I* and *Shah II* is broadly applicable to peripheral devices, it would have been obvious to implement the techniques taught therein with known techniques for managing non-volatile memory. *See e.g.*, Shah I at 8:38-9:21; *KSR*, 550 U.S. at 417-418.

The full extent of each reference's disclosure as it pertains to the Asserted Claims is presented in Exhibits C1-C16. An exemplary list of possible combinations is given in Appendix C.

B. INVALIDITY CONTENTIONS BASED ON U.S.C. § 112

At least in view of Polaris' apparent construction of the Asserted Claims in its infringement Contentions, the Asserted Claims are invalid because the specification as filed does not enable the claimed method. Thus, the patent disclosure would not enable a person of ordinary skill in the art to practice the method as asserted by Polaris. Further, at least in view of Polaris' apparent construction of the claims in its Infringement Contentions, the Asserted Claims are invalid because the specification as filed does not contain a written description of the claimed invention. In particular, the patent disclosure would not lead a person of ordinary skill in the art to understand that the named inventor had possession of the purported invention as asserted by Polaris. The Asserted Claims are invalid as indefinite under 35 U.S.C. § 112 for failing to particularly point out and distinctly claim the subject matter which the applicants regard as their invention.

Based on Polaris' Infringement Contentions and its apparent interpretation of the terms of the Asserted Claims, the following terms or limitations are indefinite, lack sufficient written description support, and/or are not enabled under § 112:

Claim Element	Claim[8]
generate an interrupt vector state based on the completion queue state	1

[8] All claims dependent from claims that are indefinite, lack sufficient written description support, and/or are not enabled under § 112 for the listed reasons are also indefinite, lack sufficient written description support, and/or are not enabled under § 112 for the same reasons.

determine the completion queue of the host processing unit contains an unprocessed completion status based on the interrupt vector state	1
generate an interrupt message packet for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue	1
wherein [the/a] completion queue state [of the plurality of completion queue states] includes a doorbell update status indicating whether the host processing unit has performed a doorbell update event in which the host processing unit updates a head pointer stored in the nonvolatile memory controller for the completion queue	1, 11
generate the interrupt vector state based on each completion queue state mapped to the interrupt vector state	8
determine a completion queue corresponding to a completion queue state mapped to the interrupt vector state contains an unprocessed completion status based on the interrupt vector state	8

and to generate an interrupt message packet based on the interrupt vector state for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue	8
the completion queue state including a doorbell update status indicating whether the host processing unit has performed a doorbell update event in which the host processing unit updates a head pointer stored in the nonvolatile memory controller for the completion queue	16
generating an interrupt vector state by the nonvolatile memory controller based on the completion queue state, the interrupt vector state associated with an interrupt vector in the host processing unit	16
determining by the nonvolatile memory controller based on the interrupt vector state that the completion queue contains an unprocessed completion status	16

C. INVALIDITY CONTENTIONS BASED ON U.S.C. § 101

1. Claim 1 of the '968 Patent is directed to an abstract idea.

The claims of the '968 Patent are directed to using a nonvolatile memory controller to monitor whether any items on a list of information to be processed have not yet been processed and generate an alert as to the existence of any unprocessed information.

The Court need not look further than the preamble of Claim 1, which clearly states the purpose of the invention: "***alerting a host processing unit to an unprocessed completion status contained in a completion queue of the host processing unit***." The steps for achieving this purpose are 1) ***generating*** a "completion queue state" and an "interrupt vector state," each of which includes information about one or more completion queues; 2) ***determining*** whether there are unprocessed completion statuses in the queue; and 3) ***generating*** an alert to the host processing unit concerning the unprocessed completion statuses. *See* '968 Patent at Claim 1. Thus, the claims focus on generating, analyzing, and communicating information, which "places them in the familiar class of claims directed to a patent-ineligible concept." *Trinity Info Media, LLC v. Covalent, Inc*., 72 F.4th 1355, 1362 (Fed. Cir. 2023) (quoting *Elec. Power Grp.*, 830 F.3d at 1353 (Fed. Cir. 2016); *see also AI Visualize,* 97 F.4th at 1378 (holding that creation of data from other data is nothing more than abstract data manipulation). Although the information is of a particular type—lists of completion statuses and information concerning whether the host has processed them—monitoring and distributing information is an abstract idea. *Trinity Info Media*, 72 F.4th at 1362.

Indeed, despite the claim's requirement they be performed by a generic nonvolatile memory controller, these steps amount to nothing more than the abstract concept of status monitoring and reporting, which has been performed by humans throughout history. *See, Chamberlain*, 935 F.3d at 1346 (holding claims directed to "wirelessly communicating status information about a system" abstract); *Broadcom*

Corp. v. Netflix Inc., 598 F. Supp. 3d 800, 807 (N.D. Cal. Apr. 13, 2022) (method for allocating tasks across servers was merely an implementation of a project management process). The Federal Circuit has consistently held that processes which can and have been performed by humans are abstract ideas despite implementation on computer technology. *See Intell. Ventures I LLC v. Erie Indem. Co.*, 850 F.3d 1315, 1330 (Fed. Cir. 2017) ("Remotely accessing and retrieving user-specified information is an age-old practice that existed well before the advent of computers and the Internet."); *Intell. Ventures I LLC v. Symantec Corp.*, 838 F.3d 1307, 1314 (Fed. Cir. 2016) ("[I]t was long-prevalent practice for people receiving paper mail to look at an envelope and discard certain letters, without opening them, from sources from which they did not wish to receive mail based on characteristics of the mail. The list of relevant characteristics could be kept in a person's head. . . . The patent merely applies a well-known idea using generic computers . . . .").

The fact that Claim 1 restricts these steps to a particular technological environment—an "interrupt manager" within a nonvolatile memory controller—does not alter the fact that the claims focus on abstract processes of monitoring whether tasks requiring processing of information have been completed and providing an alert if not. *See, e.g.*, *Trinity Info Media*, 72 F.4th at 1362 ("The '685 patent's requirements that the abstract idea be performed on a 'hand-held device' or that matches are 'reviewable by swiping' does not alter our conclusion that the focus of the asserted claims remains directed to an abstract idea."); *WhitServe LLC v. Dropbox, Inc*., 854 F. App'x 367, 371 (Fed. Cir. 2021) (unpublished) ("Whether the records are stored onsite of offsite does not alter the conclusion that the claims are directed to the abstract idea of maintaining data records.").

Further, the claim provides little specificity on ***how*** to determine that a completion queue includes unprocessed completion statuses and when to generate an interrupt message packet. Instead, it recites only that the determination must be based on an "interrupt vector state," which is based on a "completion queue state" that includes an indication of whether the host processing unit has updated a head pointer (i.e., a location on a completion queue) stored in the nonvolatile memory controller. But the claim provides little guidance on what information these "states" include beyond that the completion queue state must include an indication of whether the host processing unit has updated a head pointer. The lack of specificity in the claim reinforces that its focus is on the general idea of having an interrupt manager within the nonvolatile memory controller monitor whether the completion statuses have been processed and sending an alert rather than on a specific, technological solution. *See, e.g.*, *AI Visualize*, 97 F.4th at 1379 (holding that the claims' failure to provide specificity on ***how*** to create frames or virtual views reinforced that they were directed to an abstract idea).

2. Claim 1 of the '968 Patent lacks any inventive concept apart from the abstract idea it claims.

The specification makes clear that the alleged advance claimed by the '968 Patent is the use of the interrupt manager to perform the status monitoring and alerting, which is the abstract idea itself. According to the specification, using the interrupt manager to monitor the completion queue means that the host processing unit need not include resources for this task. '968 Patent at 16:28-32. Use of the interrupt manager for generating alerts to the host processing unit concerning incomplete tasks also saves the processors of the nonvolatile memory controller from expending resources for such. '968 Patent at 16:32-42. In effect, the host processing unit and nonvolatile memory controller processors each outsource status monitoring and alerting to the interrupt manager in an attempt to conserve resources.

But the specification acknowledges that the concept of communicating tasks between a nonvolatile memory controller and a host processing unit and generating interrupts in a host-processing unit was well known at the time of the alleged invention. *See, e.g.*, '968 Patent at 1:26-35, 16:53-67 (listing known types of interrupts the claimed system could use). Simply moving the task of monitoring completion statuses and determining when to generate interrupts from one generic processor to another is not inventive. Gathering, analyzing, and communicating information are standard functions of processors, regardless of where those processors reside. *See, e.g.*, *WhitServe*, 854 F. App'x at 372 (rejecting an argument that "the unconventional step of storing backup data onsite" supplied an inventive concept). Instead, the '968 Patent's claimed advance consists of outsourcing status monitoring and alerting to a nonvolatile memory controller, which is itself an abstract idea, using generic processing components. *See, e.g.*, *Broadcom Corp.*, 598 F. Supp. 3d at 807.

Claim 1 of the '968 Patent amounts to nothing more than ordinary steps, performed through ordinary components in their ordinary function. *Two-Way Media*, 874 F.3d at 1339. An inventive concept must reflect something more than "the application of an abstract idea using well-understood, routine, and conventional activities previously known to the industry." *Cellspin Soft, Inc. v. Fitbit, Inc.*, 927 F.3d 1306, 1315 (Fed. Cir. 2019) (internal citation omitted).

Further, any additional features of the '968 Patent are nothing more than conventional elements which can be found in the prior art including:

- A dedicated interrupt manager within the non-volatile memory controller. *See e.g.*, Borchers at [0017]- [0021], [0035], Fig. 1C; Serebrin at [0056]-[0057]
- Separate memories for completion queue state and interrupt vector state. *See e.g.*, Borchers at [0017]- [0021], [0035], Fig. 1C; Serebrin at [0056]-[0057]; Shah II at 3:65-67.

3. Claim 1 is representative.

The '968 Patent has two additional independent claims: Claims 8 and 16. These claims recite substantially similar limitations to those included in Claim 1 and are directed toward the same mental process: using a nonvolatile memory controller to monitor whether any items on a list of information to be processed have not yet been processed and generate an alert as to the existence of any unprocessed information. Claim 16 recites a method of performing the same steps the interrupt manager performs in claim 1. Claim 8 and dependent Claim 9 recite generic "completion queue state" and "interrupt vector state" memories for storing multiple completion queue and interrupt vector states that a generic "interrupt manager controller" generates, associates, and uses to determine that a completion queue contains an unprocessed completion status and generate an interrupt message.

A number of dependent claims recite additional data the interrupt manager keeps track of in connection with the claimed process, including event counts that the interrupt manager can use to inhibit generation of an interrupt until a certain number of events (e.g., receipts of completion messages) have occurred; time indicators the interrupt manager can use to prevent generating an interrupt message packet before a threshold amount of time since the last one; empty queue indicators for indicating whether a completion queue is empty; and event flags within completion messages. These dependent claims simply add additional information to the mental process of Claim 1 and do not alter the abstract character of the claims.

Claims 2 and 3 recite using specific, preexisting types of interrupts. Claim 8 recites that the interrupt manager controller is a sequential logic circuit, a type of logic circuit the specification does not describe because it was well known at the time of the alleged invention. *See* '968 Patent at 17:57-59. These well-known features do not add inventive concepts and instead act as generic conduits for carrying out the abstract idea claimed. *See In re TLI Commc'ns LLC Pat. Litig.*, 823 F.3d 607, 612 (Fed. Cir. 2016). The remaining dependent claims merely recite elements which are present in Claim 1. *See* '968 Patent at Claims 11, 17, and 18.

Because all of the claims of the '968 Patent are directed to an abstract idea and lack any inventive concept apart from that idea, they lack subject-matter eligibility.

VIII. PATENT L.R. 3-4 DOCUMENT PRODUCTION ACCOMPANYING INVALDITY CONTENTIONS

A. DOCUMENTS SUFFICIENT TO SHOW OPERATION OF ACCUSED INSTRUMENTALITY

Pursuant to Patent L.R. 3-4(a), Western Digital is producing documentation sufficient to show the operation of any aspects or elements of an Accused Instrumentality identified by Polaris in its Patent L.R. 3-1(c) chart. As previously articulated, Polaris has failed to provide "a chart identifying specifically where and how each limitation of each asserted claim is found with each Accused Instrumentality" in accordance with Local Patent Rule 3-1(c). At this stage, Western Digital objects to providing documents about any product other than Western Digital's Black-branded SSDs which was sufficiently included in Polaris's Infringement Contentions.

The documents have the following Bates numbers: WDTECH00006173 - WDTECH00002985; WDTECH00002987 - WDTECH00006172. Western Digital is also making certain source code relating to the Accused Instrumentality available in the Dallas, Texas office of its counsel.

B. PRIOR ART

Pursuant to Patent L.R. 3-4(b), Western Digital is producing a copy of the prior art identified pursuant to Patent L.R. 3-3(a). The documents have the following Bates numbers: WD_INV00000001-WD_INV00003741.

C. AGREEMENTS OR COMPARABLE LICENSES

Pursuant to Patent L.R. 3-4(b), Western Digital is producing agreements that may be related to the accused instrumentality or may be comparable to a license that would result from a hypothetical reasonable royalty negotiation. The documents have the following Bates numbers: WDTECH00001154 - WDTECH00001191.

Western Digital reserves the right to produce additional agreements that may be comparable to the extent that the are discovered.

D. SALES, REVENUE, COST, AND PROFITS

Pursuant to Patent L.R. 3-4(b), Western Digital is producing documents sufficient to show the sales, revenue, cost, and profits for the Accused Instrumentalities identified.

As previously articulated, Polaris has failed to provide "a chart identifying specifically where and how each limitation of each asserted claim is found with each Accused Instrumentality" in accordance with Local Patent Rule 3-1(c). At this stage, Western Digital objects to providing documents about any product other than Western Digital's Black-branded SSDs which was sufficiently included in Polaris's Infringement Contentions.

The documents have the following Bates numbers: WDTECH00002986.

E. AGREEMENTS USED TO SUPPORT DENYING INFRINGEMENT'S DAMAGES CASE

At this time, Western Digital has not identified any agreements that may be used to support denying infringement damages. Western Digital reserves the right to produce additional documents to support denying infringement damages to the extent additional documents are discovered.

Date: December 16, 2024 HAYNES AND BOONE, LLP

/s/Stephanie N. Sivinski
Kenneth G. Parker
David B. Clark
Stephanie N. Sivinski
Caroline W. Fox
Marron E. Frith

WESTERN DIGITAL CORPORATION and WESTERN DIGITAL TECHNOLOGIES, INC.,

CERTIFICATE OF SERVICE

I, the undersigned, declare that I am over the age of 18 years and not a party to the within action. I am employed in the County of Orange, State of California, within which county the subject service occurred. My business address is 600 Anton Boulevard, Suite 700, Costa Mesa, California 92626.

On ***December 16, 2024***, I served the following document described as***: PATENT L.R. 3-3 AND 3-4 INVALIDITY DISCLOSURES OF WESTERN DIGITAL DEFENDANTS*** on the interested party in this action, addressed as follows, and in the manner so indicated:

Robert F. Kramer rkramer@krameralberti.com David Alberti dalberti@krameralberti.com Sal Lim slim@krameralberti.com Russell S. Tonkovich rtonkovich@krameralberti.com Jeremiah Armstrong jarmstrong@krameralberti.com Hong S. Lin hlin@krameralberti.com Aidan Brewster abrewster@krameralberti.com 577 Airport Blvd., Suite 250 Burlingame, A 94010 *[Attorneys for Plaintiff Polaris PowerLED Technologies, LLC]*	

☐ **BY ELECTRONIC FILING.** I caused such document(s) to be electronically filed and served through the United States District Court's CM/ECF System for the within action. This service complies with the Federal Rules of Civil Procedure. The file transmission was reported as complete and a copy of the Court's Notice of Electronic Filing will be maintained with the original document(s) in our office.

☒ **BY ELECTRONIC DELIVERY.** I caused a true and correct copy of such document to be served via electronic delivery to the interested parties in this action as indicated above.

I declare that I am employed in the offices of a member of the bar of this Court at whose direction this service was made. Executed on ***December 16, 2024***, at San Clemente, California.

/s/Tara Hamilton
Tara Hamilton

APPENDIX A

Appendix A – Exemplary References and Combinations of References

‘346 Patent Exemplary Combinations
Arai+Flynn+Hodges
Arai+Flynn+Kleimann I
Arai+Flynn+Kleimann II
Arai+Flynn+Solomon
Arai+Flynn+Stolowitz
Arai+Flynn+Ulrich
Arai+Hodges
Arai+Kleimann I
Arai+Kleimann II
Arai+Kleimann II+Hodges
Arai+Kleimann II+Kleimann I
Arai+Kleimann II+Solomon
Arai+Kleimann II+Stolowitz
Arai+Kleimann II+Ulrich
Arai+Ma+Hodges
Arai+Ma+Kleimann I
Arai+Ma+Kleimann II
Arai+Ma+Solomon
Arai+Ma+Stolowitz
Arai+Ma+Ulrich
Arai+Solomon
Arai+Stolowitz
Arai+Ulrich
Flynn+Hodges
Flynn+Kleimann I
Flynn+Kleimann II
Flynn+Kleimann II+Hodges
Flynn+Kleimann II+Kleimann I
Flynn+Kleimann II+Solomon
Flynn+Kleimann II+Stolowitz
Flynn+Kleimann II+Ulrich
Flynn+Ma+Hodges
Flynn+Ma+Kleimann I
Flynn+Ma+Kleimann II
Flynn+Ma+Solomon

Appendix A – Exemplary References and Combinations of References

‘346 Patent Exemplary Combinations
Flynn+Ma+Stolowitz
Flynn+Ma+Ulrich
Flynn+Solomon
Flynn+Stolowitz
Flynn+Ulrich
Hodges+Arai+Ulrich
Hodges+Flynn+Ulrich
Hodges+Jeddeloh+Ulrich
Hodges+Kleimann II+Ulrich
Hodges+Ma+Ulrich
Jeddeloh+Arai+Hodges
Jeddeloh+Arai+Kleimann I
Jeddeloh+Arai+Kleimann II
Jeddeloh+Arai+Solomon
Jeddeloh+Arai+Stolowitz
Jeddeloh+Arai+Ulrich
Jeddeloh+Flynn+Hodges
Jeddeloh+Flynn+Kleimann I
Jeddeloh+Flynn+Kleimann II
Jeddeloh+Flynn+Solomon
Jeddeloh+Flynn+Stolowitz
Jeddeloh+Flynn+Ulrich
Jeddeloh+Hodges
Jeddeloh+Kleimann I
Jeddeloh+Kleimann II
Jeddeloh+Kleimann II+Hodges
Jeddeloh+Kleimann II+Kleimann I
Jeddeloh+Kleimann II+Solomon
Jeddeloh+Kleimann II+Stolowitz
Jeddeloh+Kleimann II+Ulrich
Jeddeloh+Ma+Hodges
Jeddeloh+Ma+Kleimann I
Jeddeloh+Ma+Kleimann II
Jeddeloh+Ma+Solomon
Jeddeloh+Ma+Stolowitz

Appendix A – Exemplary References and Combinations of References

'346 Patent Exemplary Combinations
Jeddeloh+Ma+Ulrich
Jeddeloh+Solomon
Jeddeloh+Stolowitz
Jeddeloh+Ulrich
Kleimann I+Arai+Hodges
Kleimann I+Arai+Solomon
Kleimann I+Arai+Stolowitz
Kleimann I+Arai+Ulrich
Kleimann I+Flynn+Hodges
Kleimann I+Flynn+Solomon
Kleimann I+Flynn+Stolowitz
Kleimann I+Flynn+Ulrich
Kleimann I+Jeddeloh+Hodges
Kleimann I+Jeddeloh+Solomon
Kleimann I+Jeddeloh+Stolowitz
Kleimann I+Jeddeloh+Ulrich
Kleimann I+Kleimann II+Hodges
Kleimann I+Kleimann II+Solomon
Kleimann I+Kleimann II+Stolowitz
Kleimann I+Kleimann II+Ulrich
Kleimann I+Ma+Hodges
Kleimann I+Ma+Solomon
Kleimann I+Ma+Stolowitz
Kleimann I+Ma+Ulrich
Kleimann II+Hodges
Kleimann II+Kleimann I
Kleimann II+Ma+Hodges
Kleimann II+Ma+Kleimann I
Kleimann II+Ma+Solomon
Kleimann II+Ma+Stolowitz
Kleimann II+Ma+Ulrich
Kleimann II+Solomon
Kleimann II+Stolowitz
Kleimann II+Ulrich
Ma+Hodges

Appendix A – Exemplary References and Combinations of References

‘346 Patent Exemplary Combinations
Ma+Kleimann I
Ma+Kleimann II
Ma+Solomon
Ma+Stolowitz
Ma+Ulrich
Solomon+Arai+Hodges
Solomon+Arai+Stolowitz
Solomon+Arai+Ulrich
Solomon+Flynn+Hodges
Solomon+Flynn+Stolowitz
Solomon+Flynn+Ulrich
Solomon+Jeddeloh+Hodges
Solomon+Jeddeloh+Stolowitz
Solomon+Jeddeloh+Ulrich
Solomon+Kleimann II+Hodges
Solomon+Kleimann II+Stolowitz
Solomon+Kleimann II+Ulrich
Solomon+Ma+Hodges
Solomon+Ma+Stolowitz
Solomon+Ma+Ulrich
Stolowitz+Arai+Hodges
Stolowitz+Arai+Ulrich
Stolowitz+Flynn+Hodges
Stolowitz+Flynn+Ulrich
Stolowitz+Jeddeloh+Hodges
Stolowitz+Jeddeloh+Ulrich
Stolowitz+Kleimann II+Hodges
Stolowitz+Kleimann II+Ulrich
Stolowitz+Ma+Hodges
Stolowitz+Ma+Ulrich

APPENDIX B

Appendix B – Exemplary References and Combinations of References

'085 Patent Exemplary Combinations
Burger+Alrod
Burger+Frost+Alrod
Burger+Frost+Leung
Burger+Frost+Leung+Kanno
Burger+Frost+Leung+Sakaue
Burger+Frost+Li
Burger+Frost+Litsyn
Burger+Frost+Shark SECC
Burger+Frost+Track II SECC (Spinner)
Burger+Frost+Weingarten
Burger+Frost+Weingarten+Kanno
Burger+Frost+Weingarten+Sakaue
Burger+Kim
Burger+Lasser
Burger+Leung
Burger+Li+Alrod
Burger+Li+Leung
Burger+Li+Litsyn
Burger+Li+Shark SECC
Burger+Li+Track II SECC (Spinner)
Burger+Li+Weingarten
Burger+Litsyn
Burger+Shark SECC
Burger+Track II SECC (Spinner)
Burger+Weingarten
Cideciyan+Alrod
Cideciyan+Burger
Cideciyan+Burger+Alrod
Cideciyan+Burger+Kim
Cideciyan+Burger+Lasser
Cideciyan+Burger+Leung
Cideciyan+Burger+Leung+Frost
Cideciyan+Burger+Litsyn
Cideciyan+Burger+Shark SECC

Appendix B – Exemplary References and Combinations of References

'085 Patent Exemplary Combinations
Cideciyan+Burger+Track II SECC (Spinner)
Cideciyan+Burger+Weingarten
Cideciyan+Frost+Alrod
Cideciyan+Frost+Burger
Cideciyan+Frost+Kim
Cideciyan+Frost+Lasser
Cideciyan+Frost+Leung
Cideciyan+Frost+Leung+Sakaue
Cideciyan+Frost+Li
Cideciyan+Frost+Litsyn
Cideciyan+Frost+Shark SECC
Cideciyan+Frost+Track II SECC (Spinner)
Cideciyan+Frost+Weingarten
Cideciyan+Frost+Weingarten+Kanno
Cideciyan+Frost+Weingarten+Sakaue
Cideciyan+Kanno
Cideciyan+Kim
Cideciyan+Lasser
Cideciyan+Leung
Cideciyan+Li
Cideciyan+Li+Alrod
Cideciyan+Li+Burger
Cideciyan+Li+Kim
Cideciyan+Li+Lasser
Cideciyan+Li+Leung
Cideciyan+Li+Litsyn
Cideciyan+Li+Shark SECC
Cideciyan+Li+Track II SECC (Spinner)
Cideciyan+Li+Weingarten
Cideciyan+Litsyn
Cideciyan+Otsuka
Cideciyan+Shark SECC
Cideciyan+Track II SECC (Spinner)
Cideciyan+Weingarten
Fillingim+Alrod

Appendix B – Exemplary References and Combinations of References

‘085 Patent Exemplary Combinations
Fillingim+Burger
Fillingim+Burger+Alrod
Fillingim+Burger+Kim
Fillingim+Burger+Lasser
Fillingim+Burger+Leung
Fillingim+Burger+Litsyn
Fillingim+Burger+Shark SECC
Fillingim+Burger+Track II SECC (Spinner)
Fillingim+Burger+Weingarten
Fillingim+Cideciyan
Fillingim+Cideciyan+Alrod
Fillingim+Cideciyan+Burger
Fillingim+Cideciyan+Kim
Fillingim+Cideciyan+Lasser
Fillingim+Cideciyan+Leung
Fillingim+Cideciyan+Li
Fillingim+Cideciyan+Litsyn
Fillingim+Cideciyan+Shark SECC
Fillingim+Cideciyan+Track II SECC (Spinner)
Fillingim+Cideciyan+Weingarten
Fillingim+Frost+Alrod
Fillingim+Frost+Burger
Fillingim+Frost+Cideciyan
Fillingim+Frost+Kim
Fillingim+Frost+Lasser
Fillingim+Frost+Leung
Fillingim+Frost+Leung+Sakaue
Fillingim+Frost+Li
Fillingim+Frost+Litsyn
Fillingim+Frost+Shark SECC
Fillingim+Frost+Track II SECC (Spinner)
Fillingim+Frost+Weingarten
Fillingim+Kanno
Fillingim+Kim
Fillingim+Lasser

Appendix B – Exemplary References and Combinations of References

'085 Patent Exemplary Combinations
Fillingim+Leung
Fillingim+Leung+Sakaue+Kanno
Fillingim+Leung+Weingarten+Sakaue
Fillingim+Li
Fillingim+Li+Alrod
Fillingim+Li+Burger
Fillingim+Li+Kim
Fillingim+Li+Lasser
Fillingim+Li+Leung
Fillingim+Li+Litsyn
Fillingim+Li+Shark SECC
Fillingim+Li+Track II SECC (Spinner)
Fillingim+Li+Weingarten
Fillingim+Litsyn
Fillingim+Otsuka
Fillingim+Shark SECC
Fillingim+Track II SECC (Spinner)
Fillingim+Weingarten
Frost+Alrod
Frost+Burger
Frost+Cideciyan
Frost+Fillingim
Frost+Kanno
Frost+Kim
Frost+Lasser
Frost+Leung
Frost+Leung+Li+Sakaue
Frost+Leung+Sakaue+Kanno
Frost+Leung+Weingarten+Sakaue
Frost+Li
Frost+Litsyn
Frost+Otsuka
Frost+Shark SECC
Frost+Track II SECC (Spinner)
Frost+Weingarten

Appendix B – Exemplary References and Combinations of References

‘085 Patent Exemplary Combinations
Frost+Weingarten+Li+Sakaue
Kanno+Alrod
Kanno+Burger
Kanno+Burger+Alrod
Kanno+Burger+Kim
Kanno+Burger+Lasser
Kanno+Burger+Leung
Kanno+Burger+Litsyn
Kanno+Burger+Shark SECC
Kanno+Burger+Track II SECC (Spinner)
Kanno+Burger+Weingarten
Kanno+Cideciyan+Alrod
Kanno+Cideciyan+Burger
Kanno+Cideciyan+Kim
Kanno+Cideciyan+Lasser
Kanno+Cideciyan+Leung
Kanno+Cideciyan+Li
Kanno+Cideciyan+Litsyn
Kanno+Cideciyan+Otsuka
Kanno+Cideciyan+Shark SECC
Kanno+Cideciyan+Track II SECC (Spinner)
Kanno+Cideciyan+Weingarten
Kanno+Fillingim+Alrod
Kanno+Fillingim+Burger
Kanno+Fillingim+Cideciyan
Kanno+Fillingim+Kim
Kanno+Fillingim+Lasser
Kanno+Fillingim+Leung
Kanno+Fillingim+Li
Kanno+Fillingim+Litsyn
Kanno+Fillingim+Otsuka
Kanno+Fillingim+Shark SECC
Kanno+Fillingim+Track II SECC (Spinner)
Kanno+Fillingim+Weingarten
Kanno+Frost+Alrod

Appendix B – Exemplary References and Combinations of References

'085 Patent Exemplary Combinations
Kanno+Frost+Burger
Kanno+Frost+Cideciyan
Kanno+Frost+Fillingim
Kanno+Frost+Kim
Kanno+Frost+Lasser
Kanno+Frost+Leung
Kanno+Frost+Li
Kanno+Frost+Litsyn
Kanno+Frost+Otsuka
Kanno+Frost+Shark SECC
Kanno+Frost+Track II SECC (Spinner)
Kanno+Frost+Weingarten
Kanno+Kim
Kanno+Lasser
Kanno+Leung
Kanno+Li
Kanno+Li+Alrod
Kanno+Li+Burger
Kanno+Li+Kim
Kanno+Li+Lasser
Kanno+Li+Leung
Kanno+Li+Litsyn
Kanno+Li+Shark SECC
Kanno+Li+Track II SECC (Spinner)
Kanno+Li+Weingarten
Kanno+Litsyn
Kanno+Otsuka
Kanno+Otsuka+Alrod
Kanno+Otsuka+Burger
Kanno+Otsuka+Kim
Kanno+Otsuka+Lasser
Kanno+Otsuka+Leung
Kanno+Otsuka+Li
Kanno+Otsuka+Litsyn
Kanno+Otsuka+Shark SECC

Appendix B – Exemplary References and Combinations of References

‘085 Patent Exemplary Combinations
Kanno+Otsuka+Track II SECC (Spinner)
Kanno+Otsuka+Weingarten
Kanno+Shark SECC
Kanno+Track II SECC (Spinner)
Kanno+Weingarten
Kim+Alrod
Kim+Burger+Alrod
Kim+Burger+Leung
Kim+Burger+Litsyn
Kim+Burger+Shark SECC
Kim+Burger+Track II SECC (Spinner)
Kim+Burger+Weingarten
Kim+Cideciyan+Alrod
Kim+Cideciyan+Leung
Kim+Cideciyan+Litsyn
Kim+Cideciyan+Shark SECC
Kim+Cideciyan+Track II SECC (Spinner)
Kim+Cideciyan+Weingarten
Kim+Fillingim+Alrod
Kim+Fillingim+Leung
Kim+Fillingim+Litsyn
Kim+Fillingim+Shark SECC
Kim+Fillingim+Track II SECC (Spinner)
Kim+Fillingim+Weingarten
Kim+Frost+Alrod
Kim+Frost+Burger
Kim+Frost+Kanno+Leung
Kim+Frost+Kanno+Weingarten
Kim+Frost+Leung
Kim+Frost+Li
Kim+Frost+Litsyn
Kim+Frost+Sakaue+Leung
Kim+Frost+Sakaue+Weingarten
Kim+Frost+Shark SECC
Kim+Frost+Track II SECC (Spinner)

Appendix B – Exemplary References and Combinations of References

‘085 Patent Exemplary Combinations
Kim+Frost+Weingarten
Kim+Kanno+Alrod
Kim+Kanno+Leung
Kim+Kanno+Litsyn
Kim+Kanno+Shark SECC
Kim+Kanno+Track II SECC (Spinner)
Kim+Kanno+Weingarten
Kim+Leung
Kim+Li+Alrod
Kim+Li+Burger
Kim+Li+Leung
Kim+Li+Litsyn
Kim+Li+Shark SECC
Kim+Li+Track II SECC (Spinner)
Kim+Li+Weingarten
Kim+Litsyn
Kim+Otsuka+Alrod
Kim+Otsuka+Leung
Kim+Otsuka+Litsyn
Kim+Otsuka+Shark SECC
Kim+Otsuka+Track II SECC (Spinner)
Kim+Otsuka+Weingarten
Kim+Shark SECC
Kim+Track II SECC (Spinner)
Kim+Weingarten
Lasser+Alrod
Lasser+Burger+Alrod
Lasser+Burger+Kim
Lasser+Burger+Leung
Lasser+Burger+Litsyn
Lasser+Burger+Shark SECC
Lasser+Burger+Track II SECC (Spinner)
Lasser+Burger+Weingarten
Lasser+Cideciyan+Alrod
Lasser+Cideciyan+Kim

Appendix B – Exemplary References and Combinations of References

‘085 Patent Exemplary Combinations
Lasser+Cideciyan+Leung
Lasser+Cideciyan+Litsyn
Lasser+Cideciyan+Shark SECC
Lasser+Cideciyan+Track II SECC (Spinner)
Lasser+Cideciyan+Weingarten
Lasser+Fillingim+Alrod
Lasser+Fillingim+Kim
Lasser+Fillingim+Leung
Lasser+Fillingim+Litsyn
Lasser+Fillingim+Shark SECC
Lasser+Fillingim+Track II SECC (Spinner)
Lasser+Fillingim+Weingarten
Lasser+Frost+Alrod
Lasser+Frost+Burger
Lasser+Frost+Kim
Lasser+Frost+Leung
Lasser+Frost+Li
Lasser+Frost+Litsyn
Lasser+Frost+Shark SECC
Lasser+Frost+Track II SECC (Spinner)
Lasser+Frost+Weingarten
Lasser+Kanno+Alrod
Lasser+Kanno+Kim
Lasser+Kanno+Leung
Lasser+Kanno+Litsyn
Lasser+Kanno+Shark SECC
Lasser+Kanno+Track II SECC (Spinner)
Lasser+Kanno+Weingarten
Lasser+Kim
Lasser+Leung
Lasser+Li+Alrod
Lasser+Li+Burger
Lasser+Li+Kim
Lasser+Li+Leung
Lasser+Li+Litsyn

Appendix B – Exemplary References and Combinations of References

‘085 Patent Exemplary Combinations
Lasser+Li+Shark SECC
Lasser+Li+Track II SECC (Spinner)
Lasser+Li+Weingarten
Lasser+Litsyn
Lasser+Otsuka+Alrod
Lasser+Otsuka+Kim
Lasser+Otsuka+Leung
Lasser+Otsuka+Litsyn
Lasser+Otsuka+Shark SECC
Lasser+Otsuka+Track II SECC (Spinner)
Lasser+Otsuka+Weingarten
Lasser+Shark SECC
Lasser+Track II SECC (Spinner)
Lasser+Weingarten
Li+Alrod
Li+Burger
Li+Frost+Alrod
Li+Frost+Leung
Li+Frost+Litsyn
Li+Frost+Shark SECC
Li+Frost+Track II SECC (Spinner)
Li+Frost+Weingarten
Li+Kim
Li+Lasser
Li+Leung
Li+Litsyn
Li+Shark SECC
Li+Track II SECC (Spinner)
Li+Weingarten
Litsyn+Alrod
Litsyn+Burger+Alrod
Litsyn+Burger+Leung
Litsyn+Burger+Shark SECC
Litsyn+Burger+Track II SECC (Spinner)
Litsyn+Burger+Weingarten

Appendix B – Exemplary References and Combinations of References

'085 Patent Exemplary Combinations
Litsyn+Cideciyan+Alrod
Litsyn+Cideciyan+Leung
Litsyn+Cideciyan+Shark SECC
Litsyn+Cideciyan+Track II SECC (Spinner)
Litsyn+Cideciyan+Weingarten
Litsyn+Fillingim+Alrod
Litsyn+Fillingim+Leung
Litsyn+Fillingim+Shark SECC
Litsyn+Fillingim+Track II SECC (Spinner)
Litsyn+Fillingim+Weingarten
Litsyn+Frost+Alrod
Litsyn+Frost+Leung
Litsyn+Frost+Shark SECC
Litsyn+Frost+Track II SECC (Spinner)
Litsyn+Frost+Weingarten
Litsyn+Kanno+Alrod
Litsyn+Kanno+Leung
Litsyn+Kanno+Shark SECC
Litsyn+Kanno+Track II SECC (Spinner)
Litsyn+Kanno+Weingarten
Litsyn+Leung
Litsyn+Li+Alrod
Litsyn+Li+Leung
Litsyn+Li+Shark SECC
Litsyn+Li+Track II SECC (Spinner)
Litsyn+Li+Weingarten
Litsyn+Otsuka+Alrod
Litsyn+Otsuka+Leung
Litsyn+Otsuka+Shark SECC
Litsyn+Otsuka+Track II SECC (Spinner)
Litsyn+Otsuka+Weingarten
Litsyn+Shark SECC
Litsyn+Track II SECC (Spinner)
Litsyn+Weingarten
Otsuka+Alrod

Appendix B – Exemplary References and Combinations of References

‘085 Patent Exemplary Combinations
Otsuka+Burger
Otsuka+Burger+Alrod
Otsuka+Burger+Kim
Otsuka+Burger+Lasser
Otsuka+Burger+Leung
Otsuka+Burger+Litsyn
Otsuka+Burger+Shark SECC
Otsuka+Burger+Track II SECC (Spinner)
Otsuka+Burger+Weingarten
Otsuka+Cideciyan+Alrod
Otsuka+Cideciyan+Burger
Otsuka+Cideciyan+Kim
Otsuka+Cideciyan+Lasser
Otsuka+Cideciyan+Leung
Otsuka+Cideciyan+Li
Otsuka+Cideciyan+Litsyn
Otsuka+Cideciyan+Shark SECC
Otsuka+Cideciyan+Track II SECC (Spinner)
Otsuka+Cideciyan+Weingarten
Otsuka+Fillingim+Alrod
Otsuka+Fillingim+Burger
Otsuka+Fillingim+Cideciyan
Otsuka+Fillingim+Kim
Otsuka+Fillingim+Lasser
Otsuka+Fillingim+Leung
Otsuka+Fillingim+Li
Otsuka+Fillingim+Litsyn
Otsuka+Fillingim+Shark SECC
Otsuka+Fillingim+Track II SECC (Spinner)
Otsuka+Fillingim+Weingarten
Otsuka+Frost+Alrod
Otsuka+Frost+Burger
Otsuka+Frost+Cideciyan
Otsuka+Frost+Fillingim
Otsuka+Frost+Kim

Appendix B – Exemplary References and Combinations of References

‘085 Patent Exemplary Combinations
Otsuka+Frost+Lasser
Otsuka+Frost+Leung
Otsuka+Frost+Li
Otsuka+Frost+Litsyn
Otsuka+Frost+Shark SECC
Otsuka+Frost+Track II SECC (Spinner)
Otsuka+Frost+Weingarten
Otsuka+Kim
Otsuka+Lasser
Otsuka+Leung
Otsuka+Li
Otsuka+Li+Alrod
Otsuka+Li+Burger
Otsuka+Li+Kim
Otsuka+Li+Lasser
Otsuka+Li+Leung
Otsuka+Li+Litsyn
Otsuka+Li+Shark SECC
Otsuka+Li+Track II SECC (Spinner)
Otsuka+Li+Weingarten
Otsuka+Litsyn
Otsuka+Shark SECC
Otsuka+Track II SECC (Spinner)
Otsuka+Weingarten
Sakaue+Alrod
Sakaue+Burger
Sakaue+Burger+Alrod
Sakaue+Burger+Kim
Sakaue+Burger+Lasser
Sakaue+Burger+Leung
Sakaue+Burger+Litsyn
Sakaue+Burger+Shark SECC
Sakaue+Burger+Track II SECC (Spinner)
Sakaue+Burger+Weingarten
Sakaue+Cideciyan

Appendix B – Exemplary References and Combinations of References

‘085 Patent Exemplary Combinations
Sakaue+Cideciyan+Alrod
Sakaue+Cideciyan+Burger
Sakaue+Cideciyan+Kanno
Sakaue+Cideciyan+Kim
Sakaue+Cideciyan+Lasser
Sakaue+Cideciyan+Leung
Sakaue+Cideciyan+Li
Sakaue+Cideciyan+Litsyn
Sakaue+Cideciyan+Otsuka
Sakaue+Cideciyan+Shark SECC
Sakaue+Cideciyan+Track II SECC (Spinner)
Sakaue+Cideciyan+Weingarten
Sakaue+Fillingim
Sakaue+Fillingim+Alrod
Sakaue+Fillingim+Burger
Sakaue+Fillingim+Cideciyan
Sakaue+Fillingim+Kanno
Sakaue+Fillingim+Kim
Sakaue+Fillingim+Lasser
Sakaue+Fillingim+Leung
Sakaue+Fillingim+Li
Sakaue+Fillingim+Litsyn
Sakaue+Fillingim+Otsuka
Sakaue+Fillingim+Shark SECC
Sakaue+Fillingim+Track II SECC (Spinner)
Sakaue+Fillingim+Weingarten
Sakaue+Frost+Alrod
Sakaue+Frost+Burger
Sakaue+Frost+Cideciyan
Sakaue+Frost+Fillingim
Sakaue+Frost+Kanno
Sakaue+Frost+Kim
Sakaue+Frost+Lasser
Sakaue+Frost+Leung
Sakaue+Frost+Li

Appendix B – Exemplary References and Combinations of References

‘085 Patent Exemplary Combinations
Sakaue+Frost+Litsyn
Sakaue+Frost+Otsuka
Sakaue+Frost+Shark SECC
Sakaue+Frost+Track II SECC (Spinner)
Sakaue+Frost+Weingarten
Sakaue+Kanno
Sakaue+Kanno+Alrod
Sakaue+Kanno+Burger
Sakaue+Kanno+Kim
Sakaue+Kanno+Lasser
Sakaue+Kanno+Leung
Sakaue+Kanno+Li
Sakaue+Kanno+Litsyn
Sakaue+Kanno+Otsuka
Sakaue+Kanno+Shark SECC
Sakaue+Kanno+Track II SECC (Spinner)
Sakaue+Kanno+Weingarten
Sakaue+Kim
Sakaue+Lasser
Sakaue+Leung
Sakaue+Li
Sakaue+Li+Alrod
Sakaue+Li+Burger
Sakaue+Li+Kim
Sakaue+Li+Lasser
Sakaue+Li+Leung
Sakaue+Li+Litsyn
Sakaue+Li+Shark SECC
Sakaue+Li+Track II SECC (Spinner)
Sakaue+Li+Weingarten
Sakaue+Litsyn
Sakaue+Otsuka
Sakaue+Otsuka+Alrod
Sakaue+Otsuka+Burger
Sakaue+Otsuka+Kim

Appendix B – Exemplary References and Combinations of References

‘085 Patent Exemplary Combinations
Sakaue+Otsuka+Lasser
Sakaue+Otsuka+Leung
Sakaue+Otsuka+Li
Sakaue+Otsuka+Litsyn
Sakaue+Otsuka+Shark SECC
Sakaue+Otsuka+Track II SECC (Spinner)
Sakaue+Otsuka+Weingarten
Sakaue+Shark SECC
Sakaue+Track II SECC (Spinner)
Sakaue+Weingarten
Shark SECC+Alrod
Shark SECC+Burger+Alrod
Shark SECC+Burger+Leung
Shark SECC+Burger+Track II SECC (Spinner)
Shark SECC+Burger+Weingarten
Shark SECC+Cideciyan+Alrod
Shark SECC+Cideciyan+Leung
Shark SECC+Cideciyan+Track II SECC (Spinner)
Shark SECC+Cideciyan+Weingarten
Shark SECC+Fillingim+Alrod
Shark SECC+Fillingim+Leung
Shark SECC+Fillingim+Track II SECC (Spinner)
Shark SECC+Fillingim+Weingarten
Shark SECC+Frost+Alrod
Shark SECC+Frost+Leung
Shark SECC+Frost+Leung+Sakaue
Shark SECC+Frost+Track II SECC (Spinner)
Shark SECC+Frost+Weingarten
Shark SECC+Frost+Weingarten+Sakaue
Shark SECC+Kanno+Alrod
Shark SECC+Kanno+Leung
Shark SECC+Kanno+Track II SECC (Spinner)
Shark SECC+Kanno+Weingarten
Shark SECC+Leung
Shark SECC+Li+Alrod

Appendix B – Exemplary References and Combinations of References

'085 Patent Exemplary Combinations
Shark SECC+Li+Leung
Shark SECC+Li+Track II SECC (Spinner)
Shark SECC+Li+Weingarten
Shark SECC+Otsuka+Alrod
Shark SECC+Otsuka+Leung
Shark SECC+Otsuka+Track II SECC (Spinner)
Shark SECC+Otsuka+Weingarten
Shark SECC+Track II SECC (Spinner)
Shark SECC+Weingarten
SharkSECC+Frost+Leung+Kanno
SharkSECC+Frost+Weingarten+Kanno
Track II SECC (Spinner)+Alrod
Track II SECC (Spinner)+Burger+Alrod
Track II SECC (Spinner)+Burger+Leung
Track II SECC (Spinner)+Burger+Weingarten
Track II SECC (Spinner)+Cideciyan+Alrod
Track II SECC (Spinner)+Cideciyan+Leung
Track II SECC (Spinner)+Cideciyan+Weingarten
Track II SECC (Spinner)+Fillingim+Alrod
Track II SECC (Spinner)+Fillingim+Leung
Track II SECC (Spinner)+Fillingim+Weingarten
Track II SECC (Spinner)+Frost+Alrod
Track II SECC (Spinner)+Frost+Leung
Track II SECC (Spinner)+Frost+Leung+Kanno
Track II SECC (Spinner)+Frost+Leung+Sakaue
Track II SECC (Spinner)+Frost+Weingarten
Track II SECC (Spinner)+Frost+Weingarten+Kanno
Track II SECC (Spinner)+Frost+Weingarten+Sakaue
Track II SECC (Spinner)+Kanno+Alrod
Track II SECC (Spinner)+Kanno+Leung
Track II SECC (Spinner)+Kanno+Weingarten
Track II SECC (Spinner)+Leung
Track II SECC (Spinner)+Li+Alrod
Track II SECC (Spinner)+Li+Leung
Track II SECC (Spinner)+Li+Weingarten

Appendix B – Exemplary References and Combinations of References

'085 Patent Exemplary Combinations
Track II SECC (Spinner)+Otsuka+Alrod
Track II SECC (Spinner)+Otsuka+Leung
Track II SECC (Spinner)+Otsuka+Weingarten
Track II SECC (Spinner)+Weingarten

APPENDIX C

Appendix C – Exemplary References and Combinations of References

'968 Patent Exemplary Combinations
Borchers+Bney-Moshe
Borchers+Foong
Borchers+Gregg
Borchers+Louzoun
Borchers+Marazakis
Borchers+Moriarty
Borchers+NVMe 1.0
Borchers+NVMe 1.0+Bney-Moshe
Borchers+NVMe 1.0+Foong
Borchers+NVMe 1.0+Gregg
Borchers+NVMe 1.0+Louzoun
Borchers+NVMe 1.0+Marazakis
Borchers+NVMe 1.0+Moriarty
Borchers+NVMe 1.0+Onufryk
Borchers+NVMe 1.0+PCI Spec
Borchers+NVMe 1.0+Serebrin
Borchers+NVMe 1.0+Subramanian
Borchers+NVMe 1.0+Tsao
Borchers+Onufryk
Borchers+PCI Spec
Borchers+Rao
Borchers+Rao+Bney-Moshe
Borchers+Rao+Foong
Borchers+Rao+Gregg
Borchers+Rao+Louzoun
Borchers+Rao+Marazakis
Borchers+Rao+Moriarty
Borchers+Rao+Onufryk
Borchers+Rao+PCI Spec
Borchers+Rao+Serebrin
Borchers+Rao+Subramanian
Borchers+Rao+Tsao
Borchers+Serebrin
Borchers+Shah I

Appendix C – Exemplary References and Combinations of References

'968 Patent Exemplary Combinations
Borchers+Shah I+Bney-Moshe
Borchers+Shah I+Foong
Borchers+Shah I+Gregg
Borchers+Shah I+Louzoun
Borchers+Shah I+Marazakis
Borchers+Shah I+Moriarty
Borchers+Shah I+Onufryk
Borchers+Shah I+PCI Spec
Borchers+Shah I+Serebrin
Borchers+Shah I+Subramanian
Borchers+Shah I+Tsao
Borchers+Shah II
Borchers+Shah II+Bney-Moshe
Borchers+Shah II+Foong
Borchers+Shah II+Gregg
Borchers+Shah II+Louzoun
Borchers+Shah II+Marazakis
Borchers+Shah II+Moriarty
Borchers+Shah II+Onufryk
Borchers+Shah II+PCI Spec
Borchers+Shah II+Serebrin
Borchers+Shah II+Subramanian
Borchers+Shah II+Tsao
Borchers+Subramanian
Borchers+Tsao
NVMe 1.0+Bney-Moshe
NVMe 1.0+Borchers
NVMe 1.0+Borchers+Bney-Moshe
NVMe 1.0+Borchers+Foong
NVMe 1.0+Borchers+Gregg
NVMe 1.0+Borchers+Louzoun
NVMe 1.0+Borchers+Marazakis
NVMe 1.0+Borchers+Moriarty
NVMe 1.0+Borchers+Onufryk
NVMe 1.0+Borchers+PCI Spec

Appendix C – Exemplary References and Combinations of References

'968 Patent Exemplary Combinations
NVMe 1.0+Borchers+Serebrin
NVMe 1.0+Borchers+Subramanian
NVMe 1.0+Borchers+Tsao
NVMe 1.0+Foong
NVMe 1.0+Gregg
NVMe 1.0+Louzoun
NVMe 1.0+Marazakis
NVMe 1.0+Moriarty
NVMe 1.0+Onufryk
NVMe 1.0+PCI Spec
NVMe 1.0+Rao
NVMe 1.0+Rao+Bney-Moshe
NVMe 1.0+Rao+Foong
NVMe 1.0+Rao+Gregg
NVMe 1.0+Rao+Louzoun
NVMe 1.0+Rao+Marazakis
NVMe 1.0+Rao+Moriarty
NVMe 1.0+Rao+Onufryk
NVMe 1.0+Rao+PCI Spec
NVMe 1.0+Rao+Serebrin
NVMe 1.0+Rao+Subramanian
NVMe 1.0+Rao+Tsao
NVMe 1.0+Serebrin
NVMe 1.0+Shah I
NVMe 1.0+Shah I+Bney-Moshe
NVMe 1.0+Shah I+Foong
NVMe 1.0+Shah I+Gregg
NVMe 1.0+Shah I+Louzoun
NVMe 1.0+Shah I+Marazakis
NVMe 1.0+Shah I+Moriarty
NVMe 1.0+Shah I+Onufryk
NVMe 1.0+Shah I+PCI Spec
NVMe 1.0+Shah I+Serebrin
NVMe 1.0+Shah I+Subramanian
NVMe 1.0+Shah I+Tsao

Appendix C – Exemplary References and Combinations of References

'968 Patent Exemplary Combinations
NVMe 1.0+Shah II
NVMe 1.0+Shah II+Bney-Moshe
NVMe 1.0+Shah II+Foong
NVMe 1.0+Shah II+Gregg
NVMe 1.0+Shah II+Louzoun
NVMe 1.0+Shah II+Marazakis
NVMe 1.0+Shah II+Moriarty
NVMe 1.0+Shah II+Onufryk
NVMe 1.0+Shah II+PCI Spec
NVMe 1.0+Shah II+Serebrin
NVMe 1.0+Shah II+Subramanian
NVMe 1.0+Shah II+Tsao
NVMe 1.0+Subramanian
NVMe 1.0+Tsao
Rao+Bney-Moshe
Rao+Borchers
Rao+Borchers+Bney-Moshe
Rao+Borchers+Foong
Rao+Borchers+Gregg
Rao+Borchers+Louzoun
Rao+Borchers+Marazakis
Rao+Borchers+Moriarty
Rao+Borchers+Onufryk
Rao+Borchers+PCI Spec
Rao+Borchers+Serebrin
Rao+Borchers+Subramanian
Rao+Borchers+Tsao
Rao+Foong
Rao+Gregg
Rao+Louzoun
Rao+Marazakis
Rao+Moriarty
Rao+NVMe 1.0
Rao+NVMe 1.0+Bney-Moshe
Rao+NVMe 1.0+Foong

Appendix C – Exemplary References and Combinations of References

‘968 Patent Exemplary Combinations
Rao+NVMe 1.0+Gregg
Rao+NVMe 1.0+Louzoun
Rao+NVMe 1.0+Marazakis
Rao+NVMe 1.0+Moriarty
Rao+NVMe 1.0+Onufryk
Rao+NVMe 1.0+PCI Spec
Rao+NVMe 1.0+Serebrin
Rao+NVMe 1.0+Subramanian
Rao+NVMe 1.0+Tsao
Rao+Onufryk
Rao+PCI Spec
Rao+Serebrin
Rao+Shah I
Rao+Shah I+Bney-Moshe
Rao+Shah I+Foong
Rao+Shah I+Gregg
Rao+Shah I+Louzoun
Rao+Shah I+Marazakis
Rao+Shah I+Moriarty
Rao+Shah I+Onufryk
Rao+Shah I+PCI Spec
Rao+Shah I+Serebrin
Rao+Shah I+Subramanian
Rao+Shah I+Tsao
Rao+Shah II
Rao+Shah II+Bney-Moshe
Rao+Shah II+Foong
Rao+Shah II+Gregg
Rao+Shah II+Louzoun
Rao+Shah II+Marazakis
Rao+Shah II+Moriarty
Rao+Shah II+Onufryk
Rao+Shah II+PCI Spec
Rao+Shah II+Serebrin
Rao+Shah II+Subramanian

Appendix C – Exemplary References and Combinations of References

'968 Patent Exemplary Combinations
Rao+Shah II+Tsao
Rao+Subramanian
Rao+Tsao
Shah I+Bney-Moshe
Shah I+Borchers
Shah I+Borchers+Bney-Moshe
Shah I+Borchers+Foong
Shah I+Borchers+Gregg
Shah I+Borchers+Louzoun
Shah I+Borchers+Marazakis
Shah I+Borchers+Moriarty
Shah I+Borchers+Onufryk
Shah I+Borchers+PCI Spec
Shah I+Borchers+Serebrin
Shah I+Borchers+Subramanian
Shah I+Borchers+Tsao
Shah I+Foong
Shah I+Gregg
Shah I+Louzoun
Shah I+Marazakis
Shah I+Moriarty
Shah I+NVMe 1.0
Shah I+NVMe 1.0+Bney-Moshe
Shah I+NVMe 1.0+Foong
Shah I+NVMe 1.0+Gregg
Shah I+NVMe 1.0+Louzoun
Shah I+NVMe 1.0+Marazakis
Shah I+NVMe 1.0+Moriarty
Shah I+NVMe 1.0+Onufryk
Shah I+NVMe 1.0+PCI Spec
Shah I+NVMe 1.0+Serebrin
Shah I+NVMe 1.0+Subramanian
Shah I+NVMe 1.0+Tsao
Shah I+Onufryk
Shah I+PCI Spec

Appendix C – Exemplary References and Combinations of References

'968 Patent Exemplary Combinations
Shah I+Rao
Shah I+Rao+Bney-Moshe
Shah I+Rao+Foong
Shah I+Rao+Gregg
Shah I+Rao+Louzoun
Shah I+Rao+Marazakis
Shah I+Rao+Moriarty
Shah I+Rao+Onufryk
Shah I+Rao+PCI Spec
Shah I+Rao+Serebrin
Shah I+Rao+Subramanian
Shah I+Rao+Tsao
Shah I+Serebrin
Shah I+Shah II
Shah I+Shah II+ Rao
Shah I+Shah II+Bney-Moshe
Shah I+Shah II+Borchers
Shah I+Shah II+Foong
Shah I+Shah II+Gregg
Shah I+Shah II+Louzoun
Shah I+Shah II+Marazakis
Shah I+Shah II+Moriarty
Shah I+Shah II+NVMe 1.0
Shah I+Shah II+Onufryk
Shah I+Shah II+PCI Spec
Shah I+Shah II+Serebrin
Shah I+Shah II+Subramanian
Shah I+Shah II+Tsao
Shah I+Subramanian
Shah I+Tsao
Shah II+Bney-Moshe
Shah II+Borchers
Shah II+Borchers+Bney-Moshe
Shah II+Borchers+Foong
Shah II+Borchers+Gregg

Appendix C – Exemplary References and Combinations of References

'968 Patent Exemplary Combinations
Shah II+Borchers+Louzoun
Shah II+Borchers+Marazakis
Shah II+Borchers+Moriarty
Shah II+Borchers+Onufryk
Shah II+Borchers+PCI Spec
Shah II+Borchers+Serebrin
Shah II+Borchers+Subramanian
Shah II+Borchers+Tsao
Shah II+Foong
Shah II+Gregg
Shah II+Louzoun
Shah II+Marazakis
Shah II+Moriarty
Shah II+NVMe 1.0
Shah II+NVMe 1.0+Bney-Moshe
Shah II+NVMe 1.0+Foong
Shah II+NVMe 1.0+Gregg
Shah II+NVMe 1.0+Louzoun
Shah II+NVMe 1.0+Marazakis
Shah II+NVMe 1.0+Moriarty
Shah II+NVMe 1.0+Onufryk
Shah II+NVMe 1.0+PCI Spec
Shah II+NVMe 1.0+Serebrin
Shah II+NVMe 1.0+Subramanian
Shah II+NVMe 1.0+Tsao
Shah II+Onufryk
Shah II+PCI Spec
Shah II+Rao
Shah II+Rao+Bney-Moshe
Shah II+Rao+Foong
Shah II+Rao+Gregg
Shah II+Rao+Louzoun
Shah II+Rao+Marazakis
Shah II+Rao+Moriarty
Shah II+Rao+Onufryk

Appendix C – Exemplary References and Combinations of References

‘968 Patent Exemplary Combinations
Shah II+Rao+PCI Spec
Shah II+Rao+Serebrin
Shah II+Rao+Subramanian
Shah II+Rao+Tsao
Shah II+Serebrin
Shah II+Shah I
Shah II+Shah I+Bney-Moshe
Shah II+Shah I+Foong
Shah II+Shah I+Gregg
Shah II+Shah I+Louzoun
Shah II+Shah I+Marazakis
Shah II+Shah I+Moriarty
Shah II+Shah I+Onufryk
Shah II+Shah I+PCI Spec
Shah II+Shah I+Serebrin
Shah II+Shah I+Subramanian
Shah II+Shah I+Tsao
Shah II+Subramanian
Shah II+Tsao