

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS,
INC., and MICRON TECHNOLOGY TEXAS LLC,
Petitioners,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2024-00370

Patent 10,268,608

Inventors: Hyun Lee and Jayesh R. Bhakta

Title: MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN
DISTRIBUTED DATA BUFFERS

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 10,268,608**

TABLE OF CONTENTS

I. PETITIONER’S MANDATORY NOTICESxv

A. Real Party-in-Interest (37 C.F.R. § 42.8(b)(1)).....xv

B. Related Matters (37 C.F.R. § 42.8(b)(2)).....xv

C. Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))..... xvi

D. Service Information (37 C.F.R. § 42.8(b)(4)) xvi

II. INTRODUCTION1

III. COMPLIANCE WITH IPR REQUIREMENTS1

A. Grounds for Standing (§42.104(a))1

B. Identification of Challenge (§42.104(b))1

**IV. RELEVANT INFORMATION CONCERNING THE
CONTESTED PATENT1**

A. Effective Filing Date1

B. Person of Ordinary Skill in the Art (“POSITA”)2

C. The ’608 Patent2

 1. Overview2

 2. Prosecution History.....6

D. Construction of Claim Terms7

V. PRIOR ART OVERVIEW8

A. Hiraishi (EX1005)8

B. Tokuhiro (EX1006)10

C. Ellsberry (EX1007)11

D. Butt (EX1029)12

E. Kim (EX1008).....13

VI. PRECISE REASONS FOR RELIEF REQUESTED13

A. Ground 1: Hiraishi + Butt (claims 1-12).....14

1.	<u>Claim 1</u>	14
	a) 1[pre].....	14
	b) 1[a]: module board.....	17
	c) 1[b]: module control device.....	19
	d) 1[c]: memory devices	25
	e) 1[d]: buffer circuits	28
	f) 1[e]: first wherein clause; module control signals.....	31
	g) 1[f]: second wherein clause: tristate buffer and delay circuit configured to delay a signal.....	39
2.	<u>Claim 2</u>	53
	a) 2[a]: first and second memory operations	53
	b) 2[b]: first and second set of command signals	53
	c) 2[c]: first and second set of control signals.....	54
	d) 2[d]: signal associated with the second memory operation	55
3.	<u>Claim 3</u>	56
	a) 3[a]: different ranks	56
	b) 3[b]: module command signals	56
	c) 3[c]: chip select.....	57
4.	<u>Claim 4: x8 buffers and memory devices</u>	58
5.	<u>Claim 5: x8 buffer; x4 memory devices</u>	59
6.	<u>Claim 6: metastability detection circuit</u>	60
7.	<u>Claims 7-8</u>	62
8.	<u>Claim 9:</u>	63
	a) 9[a]: clock regeneration circuit.....	63
	b) 9[b]: output local clock to memory devices	64
9.	<u>Claim 10: claim 9 + sampler</u>	66
10.	<u>Claims 11-12</u>	71
B.	<u>Ground 2: Ground 1 + <u>Tokuhiro</u> (claims 1-12)</u>	72
1.	<u>Motivations to Combine</u>	72

a)	First motivation: <u>Tokuhiro</u> teaches calculating read delays based on delays for write operations, which is more efficient than <u>Hiraishi</u> 's technique of read leveling independent of write delays	73
b)	Second motivation: <u>Tokuhiro</u> provides simple techniques for removing fly-by delays, while <u>Hiraishi</u> does not disclose how its memory controller re-times read data received with fly-by delays	78
c)	Third motivation: <u>Tokuhiro</u> discloses simple solutions for fly-by delays greater than one clock cycle, while <u>Hiraishi</u> does not.....	79
2.	The combination of Ground 1 in further view of <u>Tokuhiro</u> relied upon here.....	81
a)	It would have been obvious to implement <u>Tokuhiro</u> 's delay elements in <u>Hiraishi</u> 's data register buffers	81
b)	It would have been obvious for either <u>Hiraishi</u> 's memory controller or module controller to program <u>Tokuhiro</u> 's delay elements in <u>Hiraishi</u> 's data buffers	90
(1)	First implementation of the combination (system memory controller determines the read delay)	91
(2)	Second implementation of the combination (module controller determines the read delay)	93
3.	Claim 1	97
4.	Claim 2.....	101
a)	2[a]: first and second memory operations	101
b)	2[b]: first and second set of command signals	102
c)	2[c]: first and second set of control signals.....	104
d)	2[d]: signal associated with the second memory operation	106
5.	Claims 3-12	107

C.	Ground 3: Ground 1 or Ground 2 + <u>Ellsberry</u> (claims 5 and 12).....	107
D.	Ground 4: Ground 1 or Ground 2 + <u>Kim</u> (claims 6-8).....	108
E.	Ground 5: Ground 1 or 2 + <u>Kim</u> and <u>Ellsberry</u> (claim 8)	110
VII.	DISCRETIONARY DENIAL IS INAPPROPRIATE	110
A.	35 U.S.C. § 325(d).....	110
B.	35 U.S.C. § 314(a).....	110
1.	<i>Fintiv</i>	110
2.	<i>General Plastic</i>	111
VIII.	CONCLUSION	115

I. PETITIONERS' MANDATORY NOTICES

A. Real Party-in-Interest (37 C.F.R. § 42.8(b)(1))

The real parties in interest of this Petition are the Petitioners Micron Technology, Inc.; Micron Semiconductor Products, Inc., and Micron Technology Texas LLC.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 10,268,608 (“’608 Patent”).

- *Samsung Electronics Co., Ltd. v Netlist, Inc.*, IPR2023-00847 (“Samsung IPR”)
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136 (W.D. Tex. filed Apr. 28, 2021)
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. filed August 1, 2022); *Netlist, Inc. v. Micron Technology, Inc. et al.*, 2:22-cv-00294 (E.D. Tex. filed August 1, 2022)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)

Petitioners represent that it was not aware of the relevant prior art—Butt—when filing its first petition, this further distinguishes the present case from *Apple*.

On balance, these factors weigh against discretionary denial, and any prejudice to Netlist is minimal. Petitioners simply seek to join an already-instituted IPR, using a substantively identical petition, and taking on an “understudy” role. *See also General Plastic*, p.17 (“[The Board’s] intent in formulating these factors was to take undue inequities and prejudices to Patent Owner into account.”).

VIII. CONCLUSION

Petitioners respectfully request that Trial be instituted and claims 1-12 be canceled as unpatentable.

Dated: January 10, 2024

Respectfully submitted,

/ Matthew A. Hopkins /

Matthew A. Hopkins (Reg. No. 76,273)

mhopkins@winston.com

WINSTON & STRAWN LLP

1901 L Street, N.W.

Washington, DC 20036

Telephone: (202) 282-5000

Facsimile: (202) 282-5100

Michael R. Rueckheim (*Pro Hac Vice* to be submitted)

MRueckheim@winston.com

Ryuk Park (*Pro Hac Vice* to be submitted)

RPark@winston.com

WINSTON & STRAWN LLP

255 Shoreline Drive, Suite 520

Redwood City, CA 94065

Petition for *Inter Partes* Review of U.S. Patent No. 10,268,608

Telephone: (650) 858-6500

Facsimile: (650) 858-6559

*Counsel for Petitioners Micron
Technology, Inc.; Micron Semiconductor
Products, Inc.; and Micron Technology
Texas LLC*